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MICROPROCESSOR PRODUCTS

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Your Resource for:

- X86 CMOS Microprocessors
- X86 CMOS Peripherals
- CDP180X Microprocessors
- CDP18XX Peripherals
- Data Communications Support
- CMOS Memory Devices



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   ❑ Data Books ❑ CD-ROM ❑ Internet
   ❑ AnswerFAX ❑ Stand-Alone Data Sheets
4. Would you prefer to have a CD-ROM Data Book, a printed Data Book, or both?
   ❑ CD-ROM Book ❑ Printed Book ❑ Both
5. Which best describes your current design stage (select one):
   ❑ Info Collection ❑ Initial Production
   ❑ Prototyping ❑ Breadboarding
   ❑ Design Concept ❑ Full Production
6. When will your design be finalized?
   Month _____ Year _____
7. Expected Annual Volume at full production (select one):
   ❑ 1 to 999 ❑ 5K to 100K
   ❑ 1K to 4999 ❑ > 100K
8. This location has as its primary function (select one)
   ❑ Manufacturing ❑ Design
   ❑ Both

Which category best describes your primary end market? (Select One) ☐

1100 Video/Imaging
1101 - Desktop Multimedia
1102 - Prof/Broadcast Video
1103 - Medical Imaging
1104 - Cable TV
1105 - Video Conferencing
1199 - Other Video/Imaging

1200 Wireless Communication
1201 - Base Stations
1202 - Wireless LAN/PCS/PB
1203 - Handset/Terminals
1204 - Satellite Communication
1205 - Wireless Local Loop
1299 - Other Wireless Comm.

1300 Government/Military
1301 - Space
1302 - Guidance/Control
1303 - Radar
1304 - Communications
1305 - Avionics
1399 - General Gov't/Military

1400 Telecom
1401 - PBX or CO Line Cards
1402 - Fiber-in-the-Loop
1403 - Wireless Local Loop
1404 - Fiber Optics
1405 - ADSL/HDSL
1406 - Other High Speed Datacomm
1499 - Other Telecom

1500 Computers/Peripherals
1501 - Laptops/Palmtops
1502 - Desktop PCs
1503 - Workstation/File Server
1504 - Disk/Tape Drives
1505 - Printers/Plotter/Scanner
1506 - Datacomm
1599 - General Computer/EDP

1600 Transportation/Consumer
1601 - Power Train
1602 - Vehicle Control
1603 - Safety & Convenience
1604 - Driver Information
1605 - Entertainment
1606 - Electric Vehicles
1607 - Consumer
1699 - Other Transportation

1700 Power Supply/Power Mgmt
1701 - UPS (Uninterruptible Power Supplies)
1702 - AC-DC Power Supplies
1703 - DC-DC Power Supplies
1704 - Transmission Lines
1705 - Utility Substations
1706 - Panel Boxes
1707 - General Protection
1799 - Other Power Supplies/Mgmt

1800 Motor Control
1801 - AC Motors
1802 - 3 Phase Motors
1803 - Brushless
1804 - DC Motors
1805 - Stepper Motors
1899 - Other Motor Control

1900 Industrial Controls & Instrumentation
1901 - Manufacturing System
1902 - High Speed Instrumentation
1903 - Handheld Instruments
1904 - Medical Electronics
1905 - HVAC
1906 - Automatic Test Equipment (ATE)
1999 - General Industrial & Instrumentation

2000 Other Electronics, Not Listed Above

Which best describes your job function? (select one):
❑ Consultant
❑ Corporate/Operating Management
❑ Documentation
❑ Education
❑ Engineering
❑ Manufacturing
❑ Marketing
❑ Purchasing
❑ Quality Assurance
❑ Sales
❑ Systems

What is your primary product interest? (select one):
❑ Analog
❑ Protection Devices
❑ Power Control
❑ Converter
❑ Digital
❑ DSP
❑ Telecom
❑ Rad Hard
❑ Power Discrete
❑ Multimedia
❑ Wireless

Which best describes your job responsibility (select one):
❑ President/Owner
❑ Vice-President/Director
❑ Manager/Section Head
❑ Engineer
❑ Assistant
❑ Independent Contractor

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MICROPROCESSOR PRODUCTS

In the ever-changing IC marketplace, Harris Semiconductor has made a strong business commitment to continue servicing mature CMOS products and technologies. As always, we will supply mature, standard architecture microprocessor families for markets including cellular communications, PABX, networking systems, EDP peripherals, medical and avionics instrumentation.

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When the market demands higher performance and lower-cost solutions, Harris' proven technology is integrated in unique ways for customer applications. The 80C286 is an example of advanced, high-performance technology finding new homes in embedded applications, previously the purview of 4- and 8-bit microcontrollers.

The Harris Semiconductor microprocessor product families include:

- **16-bit microprocessors in the X86 architecture (80C86, 80C88, and 80C286)**
- **8-bit microcomputers (CDP1802, CDP1805, CDP1806)**
- **Broad selection of peripheral support devices (82CXX and CDP18XX)**
- **Data communications (general purpose UARTs, Manchester Encoder/Decoders, ARINC 429 interface)**
- **CMOS RAMs up to 64K bit**
- **4K and 16K CMOS PROMs**
- **Military-grade versions of all devices**

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MICROPROCESSOR PRODUCTS

FOR COMMERCIAL AND MILITARY APPLICATIONS

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Military Grade Product Offerings

Harris High Reliability Products are offered in the following Military grades. All JAN SMD and Harris Class B are processed per MIL-PRF-38535 requirements.

- **JAN (Joint Army Navy)**

Registered trademark of the U.S. Government indicating that a device is fully compliant to MIL-PRF-38535. The Defense Supply Center (DSCC) periodic audits of manufacturers for compliance to the MIL-PRF-38535 requirements. Manufacturers compliant to this specification operate to a Quality Management Plan that is approved by the DSCC organization. Approved manufacturers are listed on a Qualified Manufacturer Listing (QML). JAN products produced by these manufacturers are contained in the QML-38535-5 document. An example specification format for a JAN device is "M38510/29104BJA".

- **SMD (Standard Military Drawing)**

The SMD originally evolved from the DESC drawing program which was viewed as a preliminary specification prior to the approval of the JAN version of a product. SMD's were created to control the proliferation of non-standard Source Control Drawings (SCD's). In 1993, the Government standardized all new military drawings to the SMD format. Harris SMD's are produced in accordance with MIL-PRF-38535 and operate to a DSCC approved Quality Management Plan. Approved SMD manufacturers are listed on a Qualified Manufacturer Listing (QML). The manufacturers SMD product listing is contained in MIL-HDBK-103. An example specification format for a SMD device is "5962-8757701RA".

- **Harris Class B**

These devices are fully compliant to MIL-PRF-38535 and are identified by the /883 or 13A suffix on the Harris part number. The parametric limits for an /883 or 13A data sheet are controlled by the manufacturer rather than a governmental agency, and therefore, there may be differences in the test methodology and actual limits for "similar" devices made by different manufacturers.

- **Harris Class B "Equivalent"**

These devices are processed and tested in a manner equivalent to the MIL-PRF-38535 devices. They may not be classified as compliant since government standards have not been established for processing these types of components (e.g. Ram Modules). The Class B "Equivalent" products can be identified by the -8, /B, or /3 suffix on the Harris part number.

Non-Standard Product Offerings

Harris understands the need for customer generated Source Control Drawings with non-standard parameter and/or screening requirements. A Customer Engineering Department is responsible for efficiently expediting the SCDs through a comprehensive review process. Our Customer Engineering Group compares the SCD to its closest equivalent product grade and works closely with the Product Engineer, Manufacturing Engineer, Design Engineer, or applicable individual to compare Harris' screening ability against the customer's non-standard requirement(s). For products processed to non-standard requirements, a unique part number suffix is assigned.

Harris shares the military's objective to utilize standards wherever possible. We recommend using our SMD data sheets as guidelines for generating new Source Control Drawings. In instances where an available military specification or Harris SMD data sheet is inappropriate, it is Harris' sincerest wish to work closely with the customer in establishing an acceptable procurement document. For this reason, the customer is requested to contact the nearest Harris Sales Office or Representative before finalizing the Source Control Drawing. Harris looks forward to working with the customer prior to implementation of the formal drawing so that both parties may create a mutually acceptable procurement document.

Military Grades Available

PRODUCT	MIL-PRF-38535 JAN	MIL-PRF-38535 SMD/DESC	MIL-PRF-38535	/B,-8,/3
MICROPROCESSORS				
CDP1802A				X
CDP1802AC				X
MG80C286-10		X	X	
MG80C286-12		X	X	
MD80C86		X		X
MR80C86		X		X
MD80C86-2		X		X
MR80C86-2		X		X
MD80C88		X		X
MR80C88		X		X
MD80C88-2				X
MR80C88-2				X
PERIPHERALS				
CDP1852				X
CDP1852C				X
CDP1853				X
CDP1853C				X
CDP1854A				X
CDP1854AC				X
CDP1857				X
CDP1857C				X
MD82C237		X		X
MR82C237		X		X
MD82C237-12		X		X
MR82C237-12		X		X
MD82C284-10			X	
MD82C284-12			X	
MD82C37A		X		X
MR82C37A		X		X
MD82C37A-12		X		X
MR82C37A-12		X		X
MD82C37A-5		X		X
MR82C37A-5		X		X
MD82C50A-5				X
MD82C52		X		X
MR82C52		X		X
MD82C54		X		X
MR82C54		X		X
MD82C54-10				X

PRODUCT	MIL-PRF-38535 JAN	MIL-PRF-38535 SMD/DESC	MIL-PRF-38535	/B,-8,/3
PERIPHERALS (Continued)				
MD82C54-12		X		X
MR82C54-12		X		X
MR82C54-10				X
MD82C55A		X		X
MR82C55A		X		X
MD82C55A-5		X		X
MR82C55A-5		X		X
MD82C59A		X		X
MR82C59A		X		X
MD82C59A-5		X		X
MR82C59A-5		X		X
MD82C59A-12		pending		X
MR82C59A-12		pending		X
MD82C82		X		X
MR82C82		X		X
MD82C83H		X		X
MR82C83H		X		X
MD82C84A		X		X
MR82C84A		X		X
MD82C85				X
MR82C85				X
MD82C86H-5		X		X
MR82C86H-5		X		X
MD82C87H-5		X		X
MR82C87H-5		X		X
MD82C88		X		X
MR82C88		X		X
MD82C89		X		X
MR82C89		X		X
DATA COMMUNICATIONS				
CDP1854A				X
CDP1854AC				X
HD1-15530		X		X
HD4-15530		X		X
HD1-15531		X	X	X
HD1-15531B		X	X	X
HD1-4702		X	X	
HD4-4702				X
HD1-6402R		X	X	
HD1-6402B		X	X	

Military Grades Available (Continued)

PRODUCT	MIL-PRF-38535 JAN	MIL-PRF-38535 SMD/DESC	MIL-PRF-38535	/B,-8,/3
DATA COMMUNICATIONS (Continued)				
HD1-6409		X	X	
HD4-6409		X	X	
HS1-3182		pending		X
HS4-3182		pending		X
HS1-3282		X		X
HS4-3282		X		X
MD82C50A-5				X
MD82C52		X		X
MR82C52		X		X
CMOS RAMs				
CDP1821C				X
CDP1822C				X
CDP1823C				X
CDP1824				X
CDP1824C				X
HM1-6504		X	X	
HM1-6504B		X	X	
HM1-6504S	X	X	X	
HM1-6508			X	
HM1-6508B			X	
HM1-6514		X	X	
HM1-6514B		X	X	
HM1-6514S	X	X	X	
HM1-6516	X	X	X	
HM4-6516	X	X	X	
HM1-6516B		X	X	
HM4-6516B		X	X	
HM1-65162	X	X	X	
HM4-65162	X	X	X	
HM1-65162B	X	X	X	
HM4-65162B	X	X	X	
HM1-65162C		X	X	
HM4-65162C		X	X	
HM1-6518			X	
HM1-6518B			X	
HM1-65262	X	X	X	
HM4-65262	X	X	X	
HM1-65262B	X	X	X	
HM4-65262B	X	X	X	

PRODUCT	MIL-PRF-38535 JAN	MIL-PRF-38535 SMD/DESC	MIL-PRF-38535	/B,-8,/3
CMOS RAMs (Continued)				
HM1-6551			X	
HM1-6551B			X	
HM1-6561			X	
HM1-6561B			X	
HM1-65642			X	
HM4-65642			X	
HM1-65642B	X		X	
HM4-65642B	X		X	
HM1-65642C			X	
HM4-65642C			X	
CMOS PROMs				
HM1-6617		X	X	
HM6-6617		X	X	
HM4-6617		X	X	
HM1-6617B		X	X	
HM6-6617B		X	X	
HM4-6617B		X	X	
HM1-6642		X	X	
HM6-6642		X	X	
HM4-6642		X	X	
HM1-6642B		X	X	
HM6-6642B		X	X	
HM4-6642B		X	X	
CMOS RAM MODULES				
HM5-6564				X
HM5-8808				X
HM5-8808B				X
HM5-8808S				X
HM5-8808A				X
HM5-8808AB				X
HM5-8808AS				X
HM5-8816H				X
HM5-8816HB				X
HM5-8832				X
HM5-8832B				X
HM5-91M2				X
HM5-91M2B				X
HM5-92560				X
HM5-92570				X

Harris MIL-PRF-38535 JAN-SMD-/883
Part Number Listing

HARRIS PART #	JAN PART #	SMD/DESC PART #	/883 PART #
MICROPROCESSOR PRODUCTS			
MG80C286-12		5962-9067802MXC	MG80C286-12/883
MG80C286-10		5962-9067801MXC	MG80C286-10/883
MD80C86		8405201QA	
MR80C86		8405201XA	
MD80C86-2		8405202QA	
MR80C86-2		8405202XA	
MD80C88		5962-8601601QA	
MR80C88		5962-8601601XA	
MD82C237		5962-9054304MQA	
MR82C237		5962-9054304MXA	
MD82C237-12		5962-9054305MQA	
MR82C237-12		5962-9054305MXA	
MD82C284-10			MD82C284-10/883
MD82C284-12			MD82C284-12/883
MD82C37A		5962-9054302MQA	
MR82C37A		5962-9054302MXA	
MD82C37A-12		5962-9054303MQA	
MR82C37A-12		5962-9054303MXA	
MD82C37A-5		5962-9054301MQA	
MR82C37A-5		5962-9054301MXA	
MD82C52		8501501XA	
MR82C52		85015013A	
MD82C54		8406501JA	
MD82C54-12		8406502JA	
MR82C54		84065013A	
MR82C54-12		84065023A	
MD82C55A		8406602QA	
MR82C55A		8406602XA	
MD82C55A-5		8406601QA	
MR82C55A-5		8406601XA	
MD82C59A		5962-8501602YA	
MR82C59A		5962-85016023A	
MD82C59A-5		5962-8501601YA	
MR82C59A-5		5962-85016013A	
MD82C82		8406701RA	
MR82C82		84067012A	
MD82C83H		8406702RA	
MR82C83H		84067022A	
MD82C84A		8406801VA	

Harris JAN-SMD-/883 Part Number Listing (Continued)

HARRIS PART #	JAN PART #	SMD/DESC PART #	/883 PART #
MICROPROCESSOR PRODUCTS (Continued)			
MR82C84A		84068012A	
MD82C86H-5		5962-8757701RA	
MR82C86H-5		5962-87577012A	
MD82C87H-5		5962-8757702RA	
MR82C87H-5		5962-87577022A	
MD82C88		8406901RA	
MR82C88		84069012A	
MD82C89		5962-8552801RA	
MR82C89		5962-85528012A	
DATA COMMUNICATION PRODUCTS			
HD1-15530		7802901JA	
HD4-15530		78029013A	
HD1-15531		5962-9054901MQA	HD1-15531/883
HD1-15531B		5962-9054902MQA	HD1-15531B/883
HD1-4702		5962-9051801MEA	HD1-4702/883
HD1-6402B		5962-9052502MQA	HD1-6402B/883
HD1-6402R		5962-9052501MQA	HD1-6402R/883
HD1-6409		5962-9088801MRA	HD1-6409/883
HD4-6409		5962-9088801M2A	HD4-6409/883
HS1-3182		Pending	
HS4-3182		Pending	
HS1-3282		5962-8688001QA	
HS4-3282		5962-8688001XA	
CMOS MEMORY PRODUCTS			
1K CMOS STATIC RAMs			
HM1-6508			HM1-6508/883
HM1-6508B			HM1-6508B/883
HM1-6518			HM1-6518/883
HM1-6518B			HM1-6518B/883
HM1-6551			HM1-6551/883
HM1-6551B			HM1-6551B/883
HM1-6561			HM1-6561/883
HM1-6561B			HM1-6561B/883
4K CMOS STATIC RAMs			
HM1-6504		8102405VA	HM1-6504/883
HM1-6504B		8102403VA	HM1-6504B/883
HM1-6504S	M38510/24501BVA	8102401VA	HM1-6504S/883
HM1-6514		8102406VA	HM1-6514/883
HM1-6514B		8102404VA	HM1-6514B/883
HM1-6514S	M38510/24502BVA	8102402VA	HM1-6514S/883

Harris JAN-SMD-/883 Part Number Listing (Continued)

HARRIS PART #	JAN PART #	SMD/DESC PART #	/883 PART #
16K CMOS SYNCHRONOUS STATIC RAMs			
HM1-6516	M38510/29102BJA	8403601JA	HM1-6516/883
HM4-6516	M38510/29102BXA	8403601ZA	HM4-6516/883
HM1-6516B		8403607JA	HM1-6516B/883
HM4-6516B		8403607ZA	HM4-6516B/883
16K CMOS ASYNCHRONOUS STATIC RAMs			
HM1-65162	M38510/29104BJA	8403602JA	HM1-65162/883
HM4-65162	M38510/29104BXA	8403602ZA	HM4-65162/883
HM1-65162B	M38510/29110BJA	8403606JA	HM1-65162B/883
HM4-65162B	M38510/29110BXA	8403606ZA	HM4-65162B/883
HM1-65162C		8403603JA	HM1-65162C/883
HM4-65162C		8403603ZA	HM4-65162C/883
HM1-65262	M38510/29103BRA	8413201RA	HM1-65262/883
HM4-65262	M38510/29103BYA	8413201YA	HM4-65262/883
HM1-65262B	M38510/29109BRA	8413203RA	HM1-65262B/883
HM4-65262B	M38510/29109BYA	8413203YA	HM4-65262B/883
64K CMOS STATIC RAMs			
HM1-65642		8552514XA	HM1-65642/883
HM4-65642		8552514YA	HM4-65642/883
HM1-65642B	M38510/29205BXA		HM1-65642B/883
HM4-65642B	M38510/29205BYA		HM4-65642B/883
HM1-65642C			HM1-65642C/883
HM4-65642C			HM4-65642C/883
CMOS FUSE LINK PROMs			
HM1-6617		5962-8954001JA	HM1-6617/883
HM4-6617		5962-8954001XA	HM4-6617/883
HM6-6617		5962-8954001LA	HM6-6617/883
HM1-6617B		5962-8954002JA	HM1-6617B/883
HM4-6617B		5962-8954002XA	HM4-6617B/883
HM6-6617B		5962-8954002LA	HM6-6617B/883
HM1-6642		5962-8869001JA	HM1-6642/883
HM4-6642		5962-88690013A	HM4-6642/883
HM6-6642		5962-8869001LA	HM6-6642/883
HM1-6642B		5962-8869002JA	HM1-6642B/883
HM4-6642B		5962-88690023A	HM4-6642B/883
HM6-6642B		5962-8869002LA	HM6-6642B/883

Programs Served By Harris

Tube-Launched, Optically Tracked, Wire-Guided Missile
Angle Rate Bombing Set
Advanced Medium Range Air-To-Air Missile
Advanced Capability (MK-48 Torpedo)
Position Location and Reporting System
Joint Tactical Information Distribution System
Target Acquisition System (MK-23)
Miniature Vehicle Sensors
Driver's Thermal Viewer
Detecting and Ranging Set
Fighting Vehicle System (Bradley)
Helicopter (or Hughes) Night Vision System
Advanced Optic Adjunct
Advanced Light Weight Torpedo
Ground Launched Cruise Missile
Air Launched Cruise Missile
Medium Range Air-To-Surface Missile
Modular Universal Laser Equipment
Low Altitude Navigation and Targeting Infrared
Anti-Submarine Warfare
Multiple Launch Rocket System
Advanced Self Protection Jammer
Global Positioning System
Distant Early Warning
High Speed Anti-Radar Missile
Rolling Airframe Missile
Medium Depth Mine
Terminal Guidance Small Missile
Time Division Multiple Access
Distributed Time Division Multiple Access
Long Range Search and Track
Glide Bomb Unit
Divisional Air Defense

Field Support Tracked Vehicle
Integrated Solar Sensor Assembly
Continuous Motion Gyro for ISSA
Advanced Warning and Control System
Forward Looking Infrared
Ring Laser Gyro Programs
Tail Warning System
Space Telescope
Mariner Series
MK 46 NEARTIP
AV8B HARRIER
F14/A6E SMS
Bearclaw
CAINS II
TAI/MK6
B1
F-16
Phalanx
Stinger
Locust
Sidearm
Rattler
Pavetack
Viking
Skylab
Shuttle
Intelsat
Spacelab
Voyager
Mark 50
Captor
Maverick
Phoenix

MICROPROCESSOR PRODUCTS 3

CMOS MICROPROCESSORS

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CDP1805AC, CDP1806AC	CMOS 8-Bit Microprocessor with On-Chip RAM† and Counter/Timer	3-38
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Comparison of Harris CMOS CDP1800-Series Microprocessors

FEATURES	CDP1802A CDP1802AC	CDP1802BC	CDP1805AC	CDP1806AC
Memory Addressing (Bytes)	64K	64K	64K	64K
On-Chip RAM (Bytes)	-	-	64K	-
Maximum Clock Frequency (MHz)	3.2	5	5	5
Instruction Time Min./Max. (μs)	5/7.5	3.2/4.8	3.2/16	3.2/16
Timer/Counter Bits	-	-	8	8
Prescalers	-	-	÷ 32	÷ 32
Bus Structure	Multiplexed Address Lines			
Interrupts	Yes	Yes	Yes	Yes
Latched I/O Lines	Off-Chip			
Maximum Operating Temperature Range (^{o}C)	-55°C to +125°C			
Number of Pins, Package	40 D, E 44 Q	40 D, E 44 Q	40 D, E 44 Q	40 D, E 44 Q
Serial Interface	Q-Line			

Industry CMOS Microprocessor Cross Reference

HARRIS	INTEL	NEC	OKI	AMD
8-BIT MICROPROCESSOR				
80C88	80C88	μPD70108D-5	MSM80C88A	-
80C88-2	80C88-2	μPD70108D-8	MSM80C88A-2	-
16-BIT MICROPROCESSOR				
80C86	80C86	μPD70116D-5	MSM80C86A	-
80C86-2	80C86-2	μPD70116D-8	MSM80C86A-2	-
80C286-10	80286-10 80C286-10	-	-	80286-10
80C286-12	80286-12 80C286-12	-	-	80286-12
80C286-16	-	-	-	80286-16

HARRIS SEMICONDUCTOR

CDP1802A, CDP1802AC, CDP1802BC

March 1997

CMOS 8-Bit Microprocessors

Features

- **Maximum Input Clock Maximum Frequency Options At V_{DD} = 5V**
  - **CDP1802A, AC 3.2MHz**
  - **CDP1802BC. 5.0MHz**
- **Maximum Input Clock Maximum Frequency Options At V_{DD} = 10V**
  - **CDP1802A, AC 6.4MHz**
- **Minimum Instruction Fetch-Execute Times At V_{DD} = 5V**
  - **CDP1802A, AC 5.0μs**
  - **CDP1802BC. 3.2μs**
- **Any Combination of Standard RAM and ROM Up to 65,536 Bytes**
- **8-Bit Parallel Organization With Bidirectional Data Bus and Multiplexed Address Bus**
- **16 x 16 Matrix of Registers for Use as Multiple Program Counters, Data Pointers, or Data Registers**
- **On-Chip DMA, Interrupt, and Flag Inputs**
- **Programmable Single-Bit Output Port**
- **91 Easy-to-Use Instructions**

Description

The CDP1802 family of CMOS microprocessors are 8-bit register oriented central processing units (CPUs) designed for use as general purpose computing or control elements in a wide range of stored program systems or products.

The CDP1802 types include all of the circuits required for fetching, interpreting, and executing instructions which have been stored in standard types of memories. Extensive input/output (I/O) control features are also provided to facilitate system design.

The 1800 series architecture is designed with emphasis on the total microcomputer system as an integral entity so that systems having maximum flexibility and minimum cost can be realized. The 1800 series CPU also provides a synchronous interface to memories and external controllers for I/O devices, and minimizes the cost of interface controllers. Further, the I/O interface is capable of supporting devices operating in polled, interrupt driven, or direct memory access modes.

The CDP1802A and CDP1802AC have a maximum input clock frequency of 3.2MHz at V_{DD} = 5V. The CDP1802A and CDP1802AC are functionally identical. They differ in that the CDP1802A has a recommended operating voltage range of 4V to 10.5V, and the CDP1802AC a recommended operating voltage range of 4V to 6.5V.

The CDP1802BC is a higher speed version of the CDP1802AC, having a maximum input clock frequency of 5.0MHz at V_{DD} = 5V, and a recommended operating voltage range of 4V to 6.5V.

Ordering Information

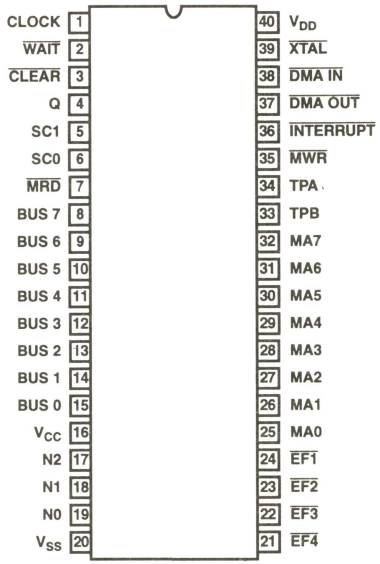
PART NUMBER		TEMPERATURE RANGE	PACKAGE	PKG. NO.
5V - 3.2MHz	5V - 5MHz			
CDP1802ACE	CDP1802BCE	-40°C to +85°C	PDIP	E40.6
CDP1802ACEX	CDP1802BCEX		Burn-In	E40.6
CDP1802ACQ	CDP1802BCQ	-40°C to +85°C	PLCC	N44.65
CDP1802ACD	-	-40°C to +85°C	SBDIP	D40.6
CDP1802ACDX	CDP1802BCDX		Burn-In	D40.6

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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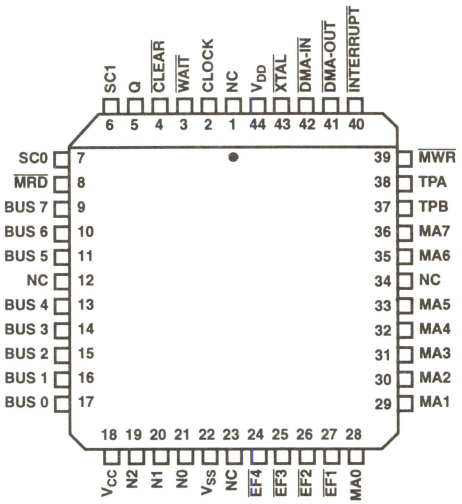
File Number **1305.2**

Pinouts

40 LEAD PDIP (PACKAGE SUFFIX E)
40 LEAD SBDIP (PACKAGE SUFFIX D)
TOP VIEW



44 LEAD PLCC
(PACKAGE TYPE Q)
TOP VIEW



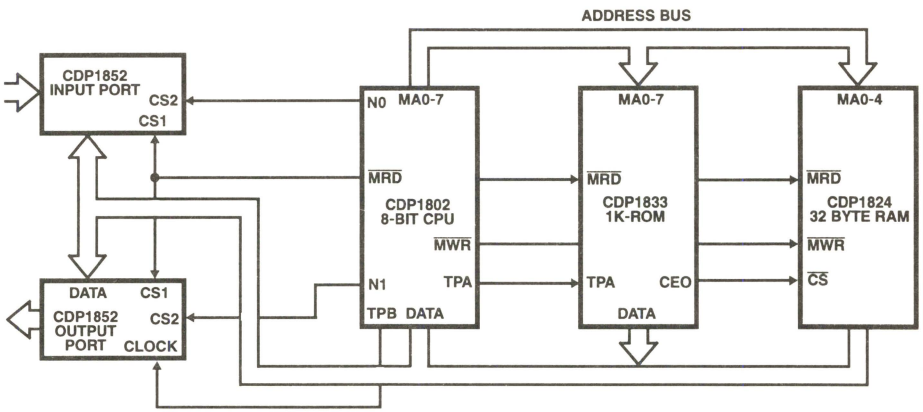


FIGURE 1. TYPICAL CDP1802 SMALL MICROPROCESSOR SYSTEM

Block Diagram

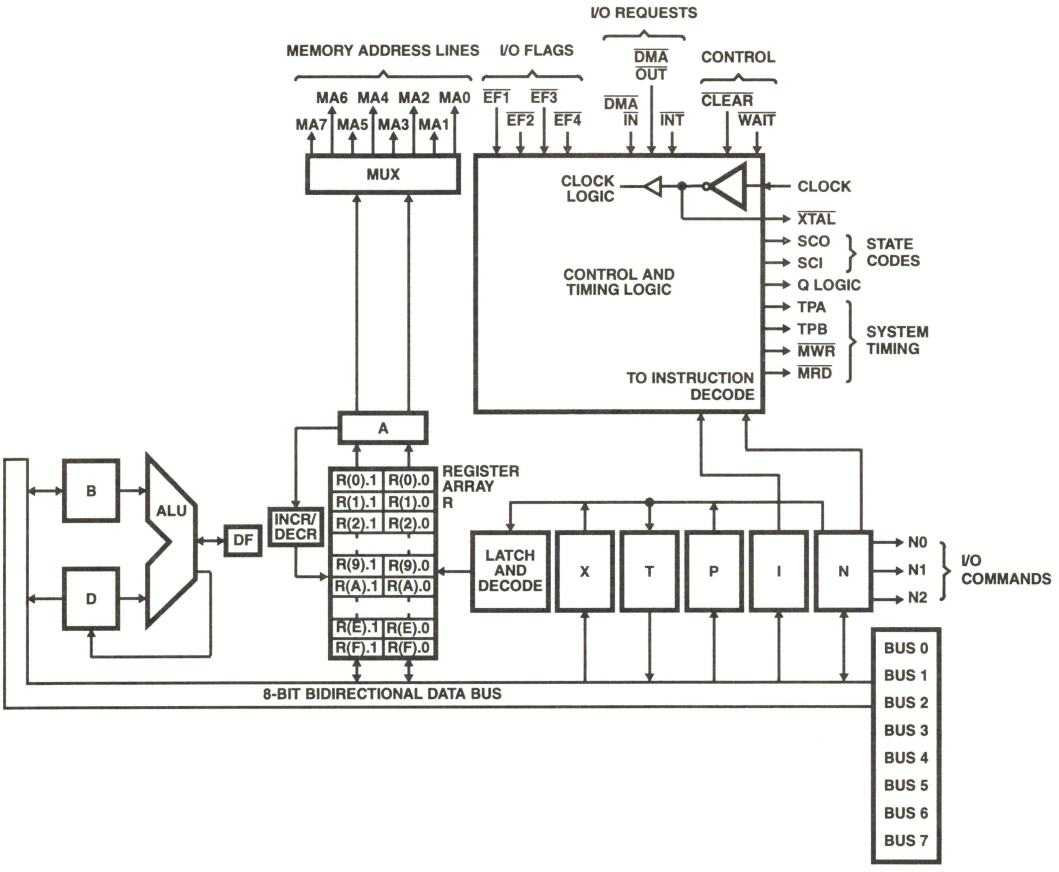


FIGURE 2.

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1802A. . . . . -0.5V to +11V
CDP1802AC, CDP1802BC. . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, any One Input. . . . . ±10mA

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP	50	N/A
PLCC	46	N/A
SBDIP	55	15

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range 100mW
Operating Temperature Range (T_A)
Package Type D . . . . . -55°C to +125°C
Package Type E and Q. . . . . -40°C to +85°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ±1/32 In. (1.59 ± 0.79mm)
from case for 10s max. . . . . +265°C
Lead Tips Only . . . . . +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

T_A = -40°C to +85°C. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	TEST CONDITIONS (NOTE 2) V_{CC} (V)	TEST CONDITIONS V_{DD} (V)	CDP1802A MIN	CDP1802A MAX	CDP1802AC MIN	CDP1802AC MAX	CDP1802BC MIN	CDP1802BC MAX	UNITS
DC Operating Voltage Range	-	-	4	10.5	4	6.5	4	6.5	V
Input Voltage Range	-	-	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Maximum Clock Input Rise or Fall Time	4 to 6.5	4 to 6.5	-	-	-	1	-	1	µs
	4 to 10.5	4 to 10.5	-	1	-	-	-	-	µs
Minimum Instruction Time (Note 3)	5	5	5	-	5	-	3.2	-	µs
	5	10	4	-	-	-	-	-	µs
	10	10	2.5	-	-	-	-	-	µs
Maximum DMA Transfer Rate	5	5	-	400	-	400	-	667	KBytes/s
	5	10	-	500	-	-	-	-	
	10	10	-	800	-	-	-	-	
Maximum Clock Input Frequency, f_{CL}, Load Capacitance (C_L) = 50pF	5	5	DC	3.2	DC	3.2	DC	5	MHz
	5	10	DC	4	-	-	-	-	MHz
	10	10	DC	6.4	-	-	-	-	MHz

NOTES:

1. Printed circuit board mount: 57mm x 57mm minimum area x 1.6mm thick G10 epoxy glass, or equivalent.
2. V_{CC} must never exceed V_{DD}.
3. Equals 2 machine cycles - one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles - one Fetch and two Execute operations.
4. θ_{JA} is measured with component mounted on an evaluation board in free air.

Static Electrical Specifications at T_A = -40°C to +85°C, Except as Noted

PARAMETER	SYMBOL	TEST CONDITIONS			CDP1802A			CDP1802AC, CDP1802BC			UNITS
		V_{OUT} (V)	V_{IN} (V)	V_{CC}, V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	-	5	-	0.1	50	-	1	200	µA
		-	-	10	-	1	200	-	-	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.1	2.2	-	1.1	2.2	-	mA
(Except $\overline{XTAL}$)		0.5	0, 10	10	2.2	4.4	-	-	-	-	mA
$\overline{XTAL}$		0.4	5	5	170	350	-	170	350	-	µA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-0.27	-0.55	-	-0.27	-0.55	-	mA
(Except $\overline{XTAL}$)		9.5	0, 10	10	-0.55	-1.1	-	-	-	-	mA
$\overline{XTAL}$		4.6	0	5	-125	-250	-	-125	-250	-	µA
Output Voltage		-	0, 5	5	-	0	0.1	-	0	0.1	V
Low Level	V_{OL}	-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage		-	0, 5	5	4.9	5	-	4.9	5	-	V
High Level	V_{OH}	-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 4.5	-	5, 10	-	-	1	-	-	-	V
		1, 9	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 4.5	-	5, 10	4	-	-	-	-	-	V
		1, 9	-	10	7	-	-	-	-	-	V
$\overline{CLEAR}$ Input Voltage	V_H	-	-	5	0.4	0.5	-	0.4	0.5	-	V
Schmitt Hysteresis		-	-	5, 10	0.3	0.4	-	-	-	-	V
		-	-	10	1.5	2	-	-	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	$\pm10^{-4}$	±1	-	$\pm10^{-4}$	±1	µA
			0, 10	10	-	$\pm10^{-4}$	±1	-	-	-	µA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	$\pm10^{-4}$	±1	-	$\pm10^{-4}$	±1	µA
		0, 10	0, 10	10	-	$\pm10^{-4}$	±1	-	-	-	µA
Operating Current CDP1802A, AC at f = 3.2MHz	I_{DDI} (Note 2)	-	-	5	-	2	4	-	2	4	mA
CDP1802BC at f = 5.0MHz		-	-	5	-	-	-	-	3	6	mA
Minimum Data Retention Voltage	V_{DR}	$V_{DD} = V_{DR}$			-	2	2.4	-	2	2.4	V
Data Retention Current	I_{DR}	V_{DD} = 2.4V			-	0.05	-	-	0.5	-	µA

Static Electrical Specifications at T_A = -40°C to +85°C, Except as Noted (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS			CDP1802A			CDP1802AC, CDP1802BC			UNITS
		V_{OUT} (V)	V_{IN} (V)	V_{CC}, V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Input Capacitance	C_{IN}				-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}				-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = +25°C and nominal V_{DD}.
2. Idle "00" at M(0000), C_L = 50pF.

Dynamic Electrical Specifications T_A = -40°C to +85°C, C_L = 50pF, V_{DD} ±5%, Except as Noted

PARAMETER	SYMBOL	TEST CONDITIONS		CDP1802A, CDP1802AC		CDP1802BC		UNITS
		V_{CC} (V)	V_{DD} (V)	(NOTE 1) TYP	MAX	(NOTE 1) TYP	MAX	
PROPAGATION DELAY TIMES								
Clock to TPA, TPB	t_{PLH}, t_{PHL}	5	5	200	300	200	300	ns
		5	10	150	250	-	-	ns
		10	10	100	150	-	-	ns
Clock-to-Memory High-Address Byte	t_{PLH}, t_{PHL}	5	5	600	850	475	525	ns
		5	10	400	600	-	-	ns
		10	10	300	400	-	-	ns
Clock-to-Memory Low-Address Byte Valid	t_{PLH}, t_{PHL}	5	5	250	350	175	250	ns
		5	10	150	250	-	-	ns
		10	10	100	150	-	-	ns
Clock to $\overline{MRD}$	t_{PHL}	5	5	200	300	175	275	ns
		5	10	150	250	-	-	ns
		10	10	100	150	-	-	ns
Clock to $\overline{MRD}$	t_{PLH}	5	5	200	350	175	275	ns
		5	10	150	290	-	-	ns
		10	10	100	175	-	-	ns
Clock to $\overline{MWR}$	t_{PLH}, t_{PHL}	5	5	200	300	175	225	ns
		5	10	150	250	-	-	ns
		10	10	100	150	-	-	ns
Clock to (CPU DATA to BUS) Valid	t_{PLH}, t_{PHL}	5	5	300	450	250	375	ns
		5	10	250	350	-	-	ns
		10	10	100	200	-	-	ns

Dynamic Electrical Specifications T_A = -40°C to +85°C, C_L = 50pF, V_{DD} ±5%, Except as Noted **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		CDP1802A, CDP1802AC		CDP1802BC		UNITS
		V_{CC} (V)	V_{DD} (V)	(NOTE 1) TYP	MAX	(NOTE 1) TYP	MAX	
Clock to State Code	t_{PLH}, t_{PHL}	5	5	300	450	250	400	ns
		5	10	250	350	-	-	ns
		10	10	150	250	-	-	ns
Clock to Q	t_{PLH}, t_{PHL}	5	5	250	400	200	300	ns
		5	10	150	250	-	-	ns
		10	10	100	150	-	-	ns
Clock to N (0 - 2)	t_{PLH}, t_{PHL}	5	5	300	550	275	350	ns
		5	10	200	350	-	-	ns
		10	10	150	250	-	-	ns
MINIMUM SET UP AND HOLD TIMES								
Data Bus Input Set Up	t_{SU}	5	5	-20	25	-20	0	ns
		5	10	0	50	-	-	ns
		10	10	-10	40	-	-	ns
Data Bus Input Hold	t_H (Note 2)	5	5	150	200	125	150	ns
		5	10	100	125	-	-	ns
		10	10	75	100	-	-	ns
$\overline{DMA}$ Set Up	t_{SU}	5	5	0	30	0	30	ns
		5	10	0	20	-	-	ns
		10	10	0	10	-	-	ns
$\overline{DMA}$ Hold	t_H (Note 2)	5	5	150	250	100	150	ns
		5	10	100	200	-	-	ns
		10	10	75	125	-	-	ns
Interrupt Set Up	t_{SU}	5	5	-75	0	-75	0	ns
		5	10	-50	0	-	-	ns
		10	10	-25	0	-	-	ns
Interrupt Hold	t_H (Note 2)	5	5	100	150	75	125	ns
		5	10	75	100	-	-	ns
		10	10	50	75	-	-	ns
$\overline{WAIT}$ Set Up	t_{SU}	5	5	10	50	20	40	ns
		5	10	-10	15	-	-	ns
		10	10	0	25	-	-	ns

Dynamic Electrical Specifications T_A = -40°C to +85°C, C_L = 50pF, V_{DD} ±5%, Except as Noted (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		CDP1802A, CDP1802AC		CDP1802BC		UNITS
		V_{CC} (V)	V_{DD} (V)	(NOTE 1) TYP	MAX	(NOTE 1) TYP	MAX	
$\overline{EF1-4}$ Set Up	t_{SU}	5	5	-30	20	-30	0	ns
		5	10	-20	30	-	-	ns
		10	10	-10	40	-	-	ns
EF1-4 Hold	t_H (Note 2)	5	5	150	200	100	150	ns
		5	10	100	150	-	-	ns
		10	10	75	100	-	-	ns
Minimum Pulse Width Times								
$\overline{CLEAR}$ Pulse Width	t_{WL} (Note 2)	5	5	150	300	100	150	ns
		5	10	100	200	-	-	ns
		10	10	75	150	-	-	ns
$\overline{CLOCK}$ Pulse Width	t_{WL}	5	5	125	150	90	100	ns
		5	10	100	125	-	-	ns
		10	10	60	75	-	-	ns

NOTES:

1. Typical values are for T_A = +25°C and nominal V_{DD}.
2. Maximum limits of minimum characteristics are the values above which all devices function.

Timing Specifications as a function of T($T = 1/f_{CLOCK}$) at T_A = -40 to +85°C, Except as Noted

PARAMETERS	SYMBOL	TEST CONDITIONS		CDP1802A, CDP1802AC		CDP1802BC		UNITS
		V_{CC} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MIN	(NOTE 1) TYP	
High-Order Memory-Address Byte Set Up to TPA ↘ Time	t_{SU}	5	5	2T-550	2T-400	2T-325	2T-275	ns
		5	10	2T-350	2T250	-	-	ns
		10	10	2T-250	2T-200	-	-	ns
High-Order Memory-Address Byte Hold After TPA Time	t_H	5	5	t/2-25	T/2-15	T/2-25	T/2-15	ns
		5	10	T/2-35	T/2-25	-	-	ns
		10	10	T/2-10	T/2-+0	-	-	ns
Low-Order Memory-Address Byte Hold After WR Time	t_H	5	5	T-30	T+0	T-30	T+0	ns
		5	10	T-20	T+0	-	-	ns
		10	10	T-10	T+0	-	-	ns
CPU Data to Bus Hold After WR Time	t_H	5	5	T-200	T-150	T-175	T-125	ns
		5	10	T-150	T-100	-	-	ns
		10	10	T-100	T-50	-	-	ns

Timing Specifications as a function of T(T = $1/f_{CLOCK}$) at T_A = -40 to +85°C, Except as Noted

PARAMETERS	SYMBOL	TEST CONDITIONS		CDP1802A, CDP1802AC		CDP1802BC		UNITS
		V_{CC} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MIN	(NOTE 1) TYP	
Required Memory Access Time Address to Data	t_{ACC}	5	5	5T-375	5T-250	5T-225	5T-175	ns
		5	10	5T-250	5T-150	-	-	ns
		10	10	5T-190	5T-100	-	-	ns
$\overline{MRD}$ to TPA ↘	t_{SU}	5	5	T/2-25	T/2-18	T/2-20	T/2-15	ns
		5	10	T/2-20	T/2-15	-	-	ns
		10	10	T/2-15	T/2-10	-	-	ns

NOTE:

1. Typical values are for T_A = +25°C and nominal V_{DD}.

Timing Waveforms

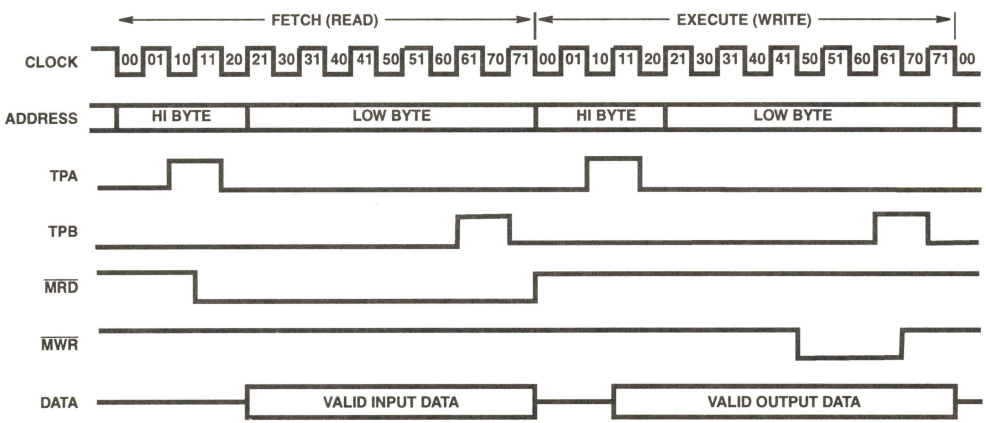
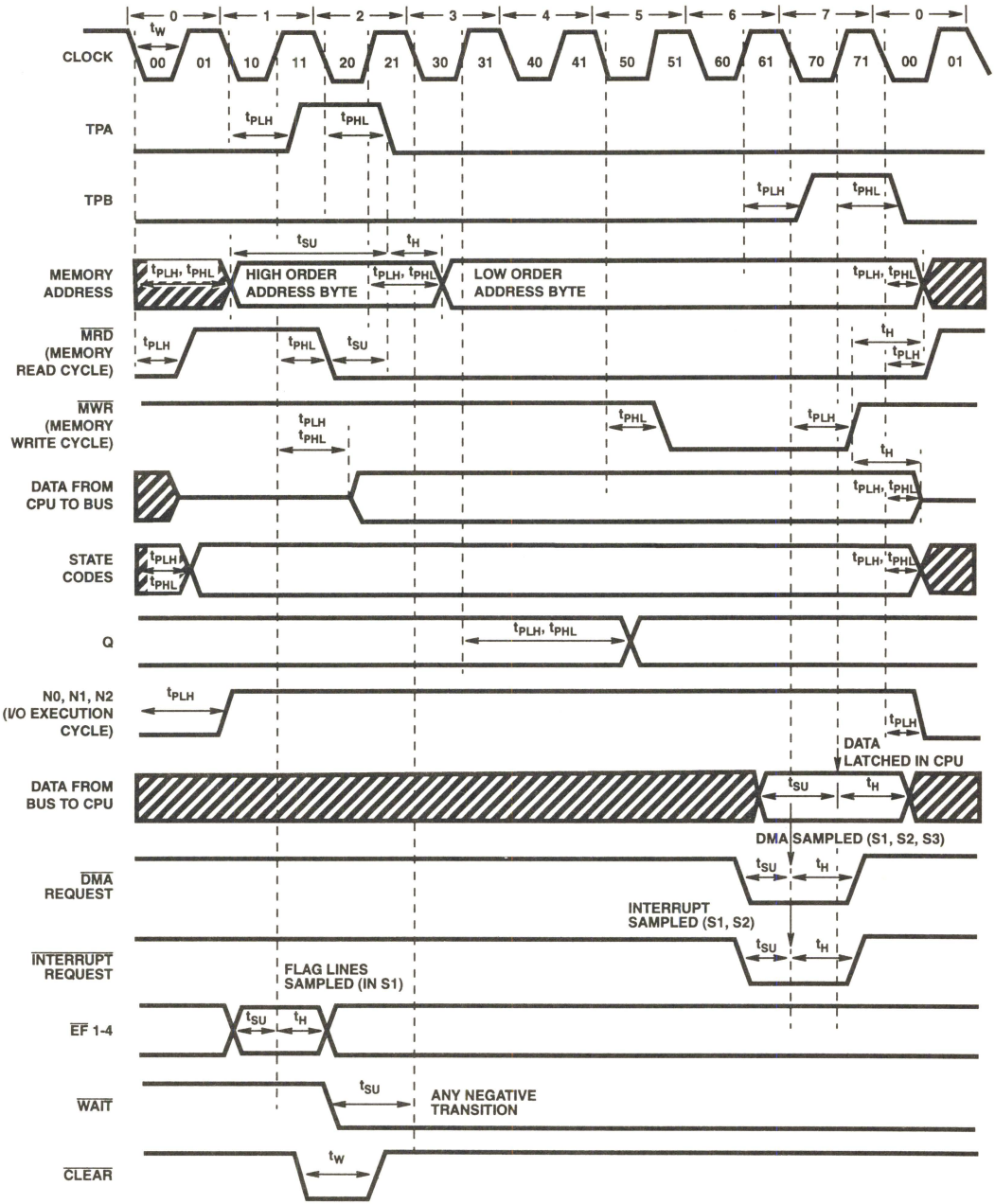


FIGURE 3. BASIC DC TIMING WAVEFORM, ONE INSTRUCTION CYCLE

Timing Waveforms (Continued)



NOTES:

1. This timing diagram is used to show signal relationships only and does not represent any specific machine cycle.
2. All measurements are referenced to 50% point of the waveforms.
3. Shaded areas indicate "Don't Care" or undefined state. Multiple transitions may occur during this period.

FIGURE 4. TIMING WAVEFORM

Machine Cycle Timing Waveforms (Propagation Delays Not Shown)

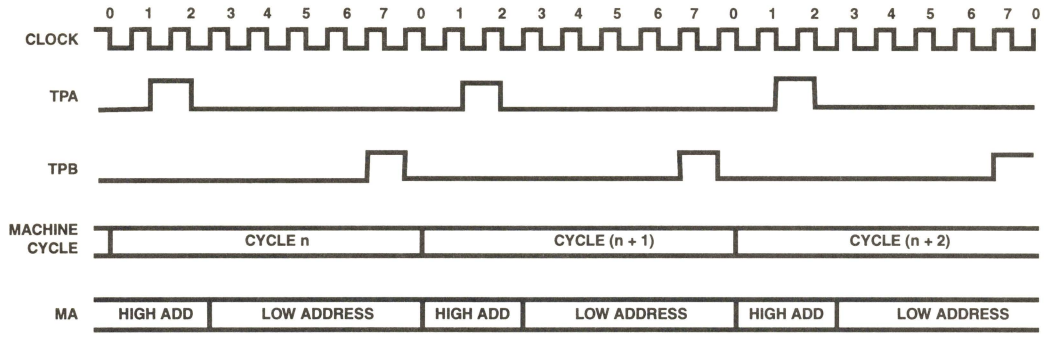


FIGURE 5. GENERAL TIMING WAVEFORMS

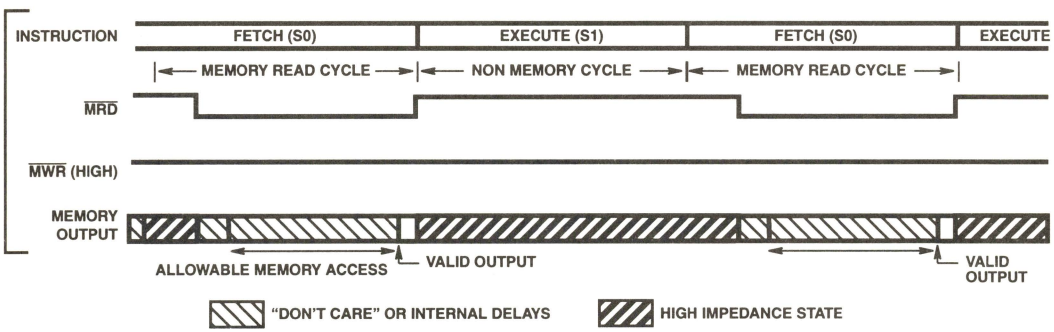


FIGURE 6. NON-MEMORY CYCLE TIMING WAVEFORMS

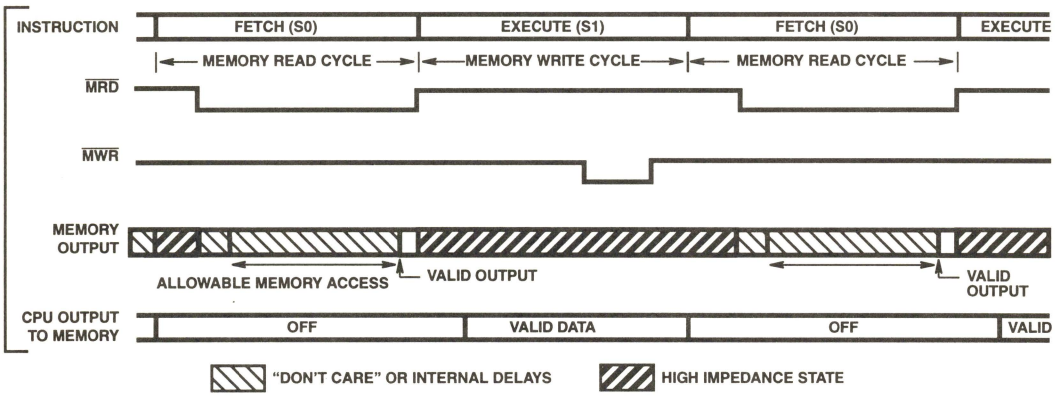


FIGURE 7. MEMORY WRITE CYCLE TIMING WAVEFORMS

Machine Cycle Timing Waveforms (Propagation Delays Not Shown) (Continued)

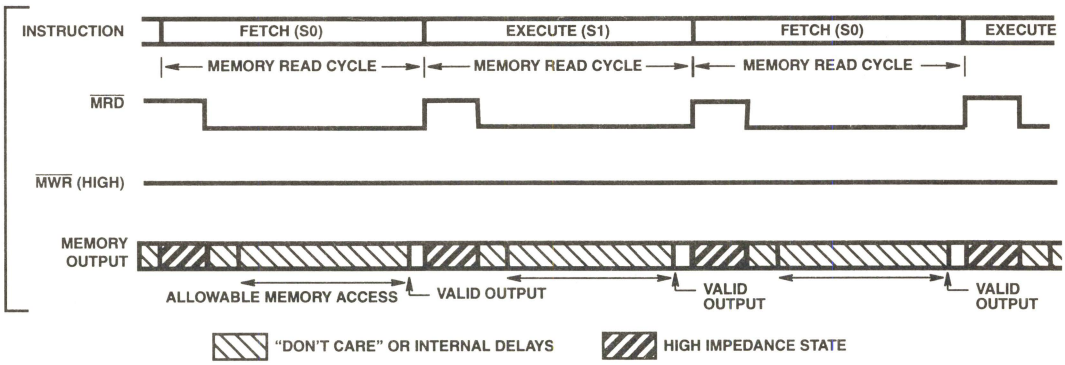


FIGURE 8. MEMORY READ CYCLE TIMING WAVEFORMS

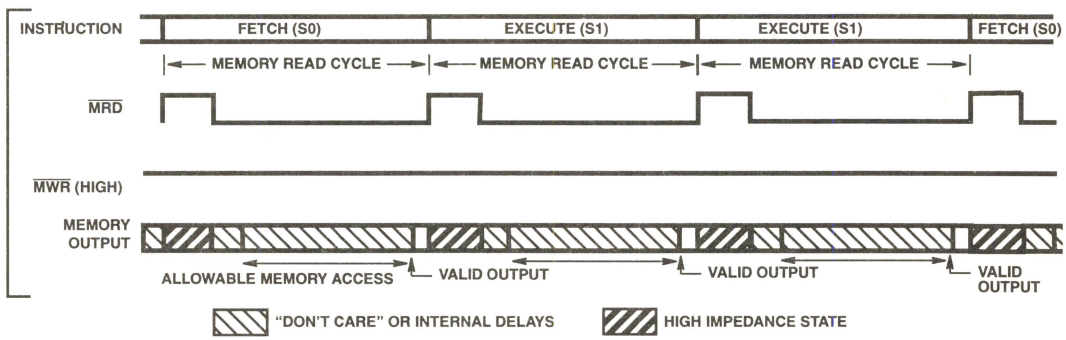


FIGURE 9. LONG BRANCH OR LONG SKIP CYCLE TIMING WAVEFORMS

Machine Cycle Timing Waveforms (Propagation Delays Not Shown) (Continued)

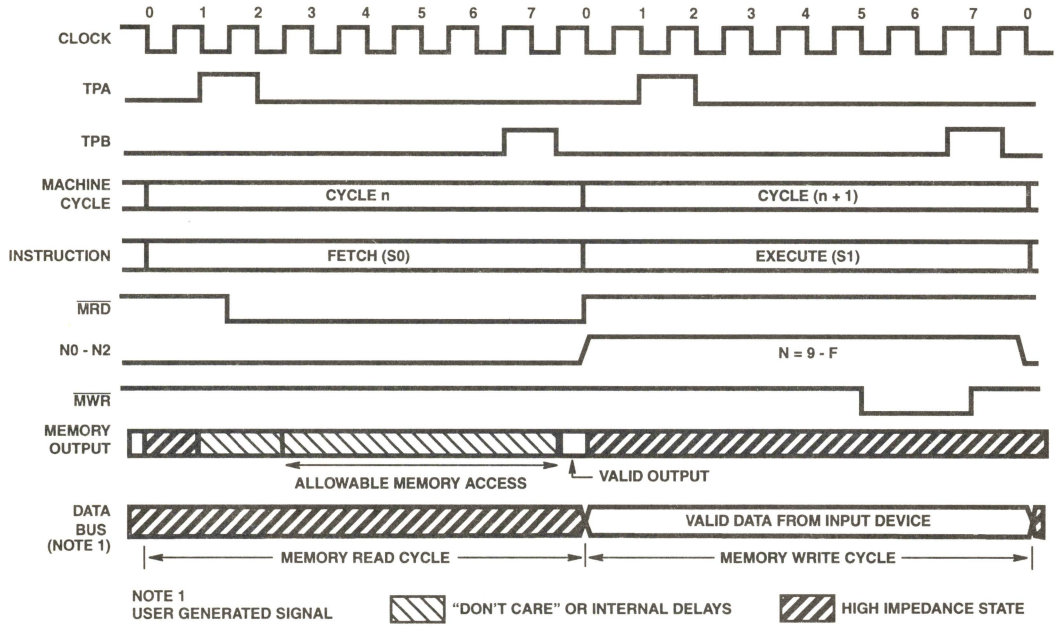


FIGURE 10. INPUT CYCLE TIMING WAVEFORMS

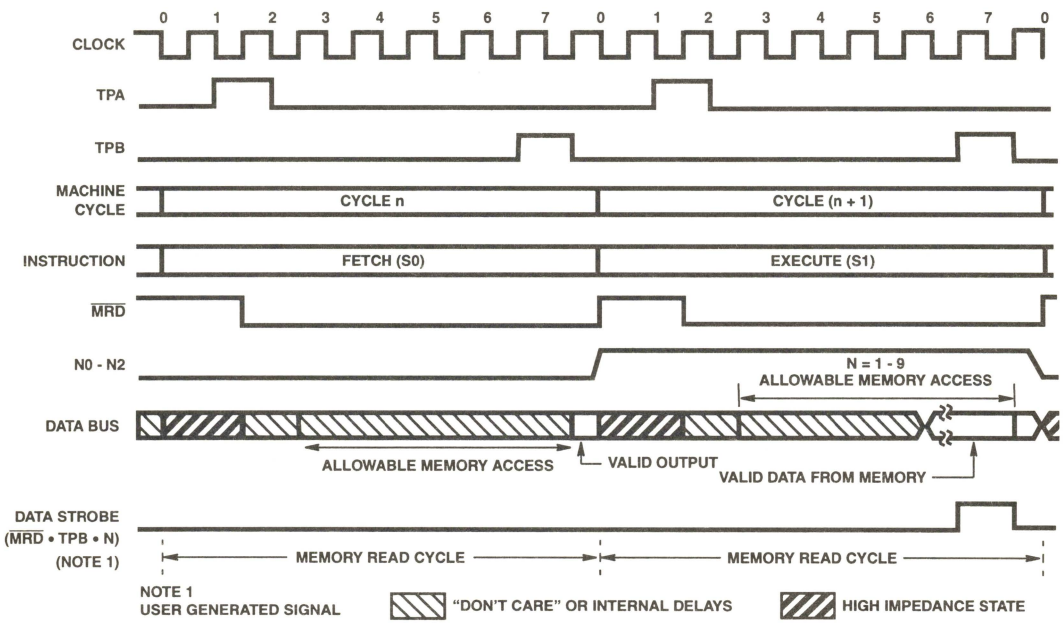


FIGURE 11. OUTPUT CYCLE TIMING WAVEFORMS

Machine Cycle Timing Waveforms (Propagation Delays Not Shown) (Continued)

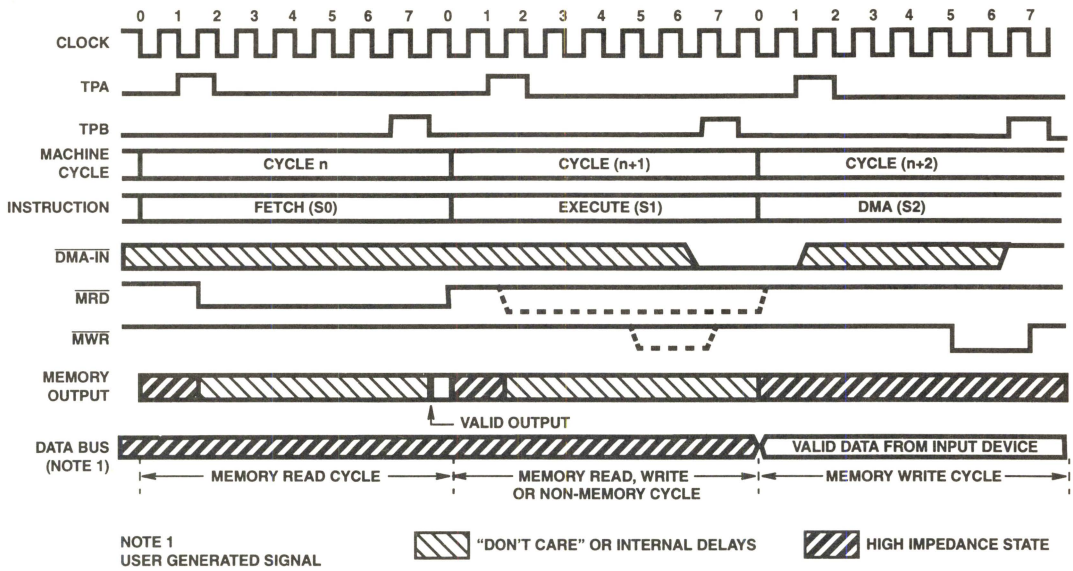


FIGURE 12. $\overline{\text{DMA IN}}$ CYCLE TIMING WAVEFORMS

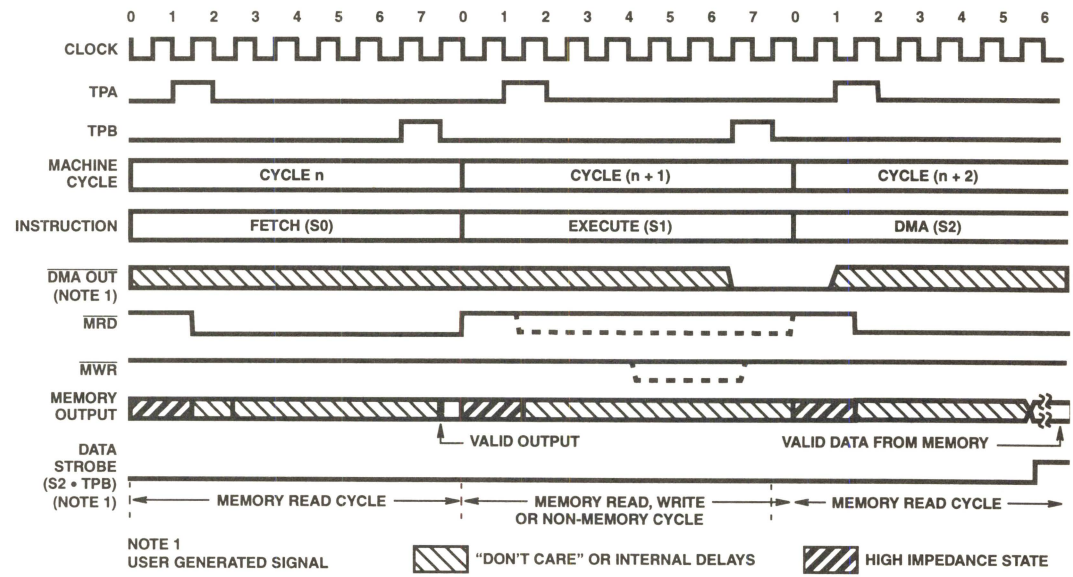


FIGURE 13. $\overline{\text{DMA OUT}}$ CYCLE TIMING WAVEFORMS

Machine Cycle Timing Waveforms (Propagation Delays Not Shown) (Continued)

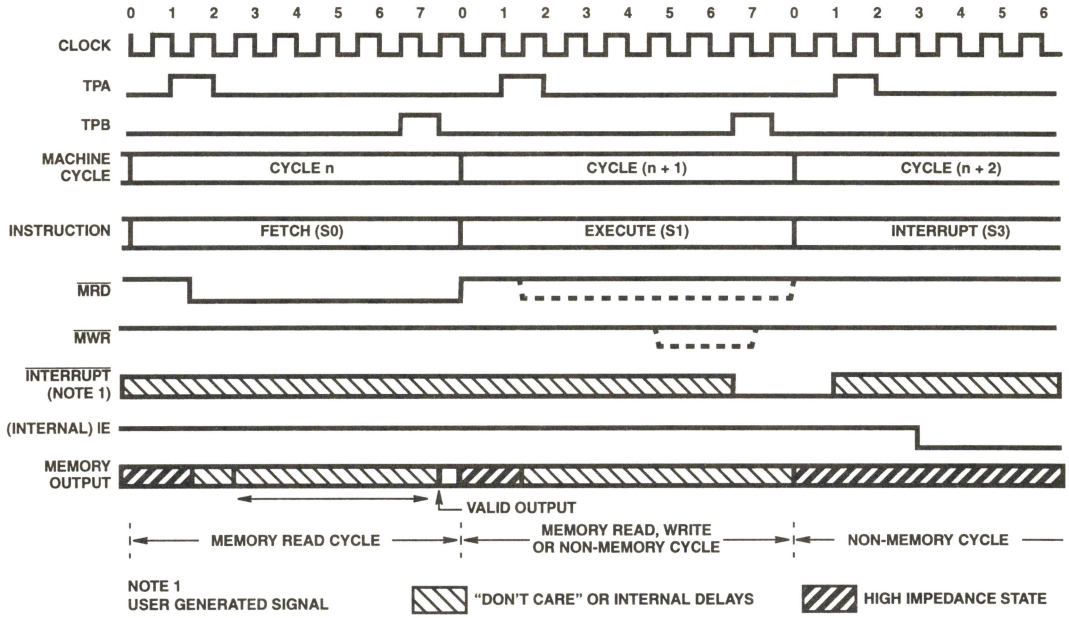


FIGURE 14. INTERRUPT CYCLE TIMING WAVEFORMS

Performance Curves

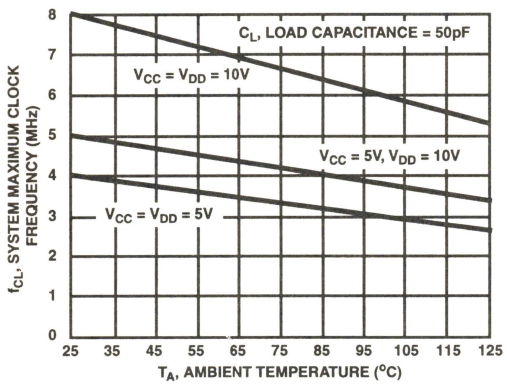


FIGURE 15. CDP1802A, AC TYPICAL MAXIMUM CLOCK FREQUENCY AS A FUNCTION OF TEMPERATURE

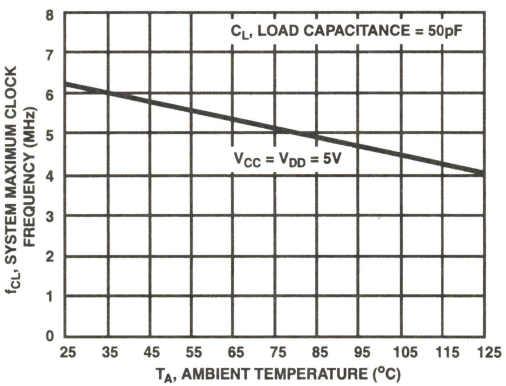


FIGURE 16. CDP1802BC TYPICAL MAXIMUM CLOCK FREQUENCY AS A FUNCTION OF TEMPERATURE

Performance Curves (Continued)

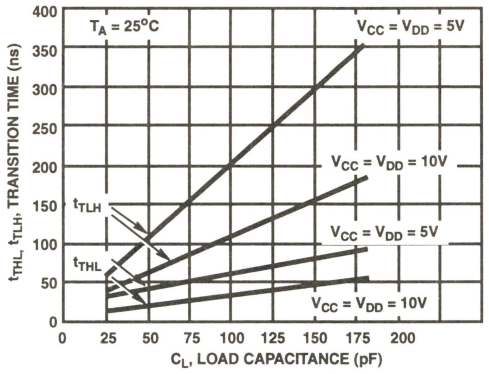


FIGURE 17. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE FOR ALL TYPES

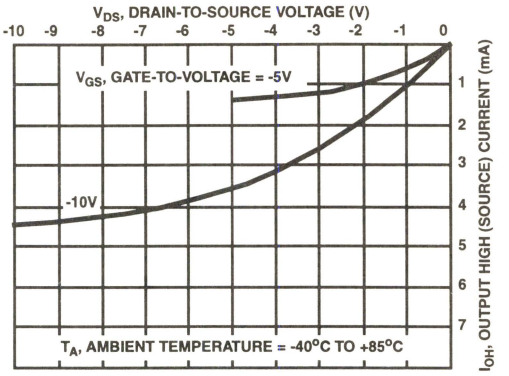


FIGURE 18. CDP1802A, AC MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

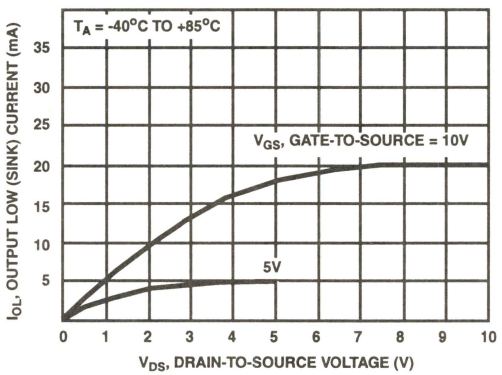


FIGURE 19. CDP1802A, AC MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

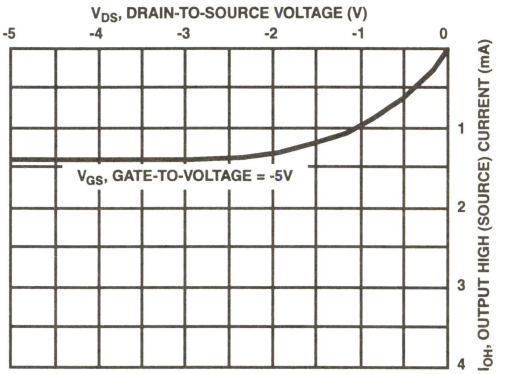


FIGURE 20. CDP1802BC MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

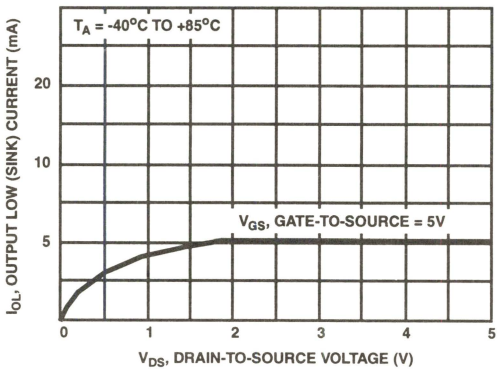
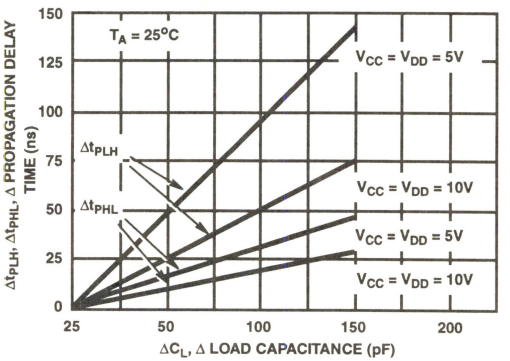


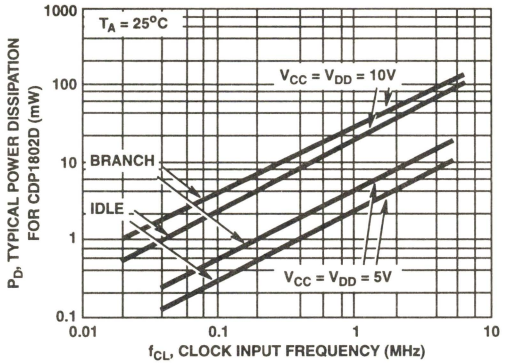
FIGURE 21. CDP1802BC MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS



NOTE: ANY OUTPUT EXCEPT $\overline{XTAL}$

FIGURE 22. TYPICAL CHANGE IN PROPAGATION DELAY AS A FUNCTION OF A CHANGE IN LOAD CAPACITANCE FOR ALL TYPES

Performance Curves (Continued)



NOTE: IDLE = "00" AT M(0000), BRANCH = "3707" AT M(8107), CL = 50pF

FIGURE 23. TYPICAL POWER DISSIPATION AS A FUNCTION OF CLOCK FREQUENCY FOR BRANCH INSTRUCTION AND IDLE INSTRUCTION FOR ALL TYPES

Signal Descriptions

Bus 0 to Bus 7 (Data Bus)

8-bit bidirectional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O Control Lines)

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the MRD signal.

$\overline{MRD}$ = V_{CC}: Data from I/O to CPU and Memory

$\overline{MRD}$ = V_{SS}: Data from Memory to I/O

$\overline{EF1}$ to $\overline{EF4}$ (4 Flags)

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "call the attention" of the processor, in which case the program must routinely test the status of these flag(s). The flag(s) are sampled at the beginning of every S1 cycle.

$\overline{INTERRUPT}$, $\overline{DMA\text{-}IN}$, $\overline{DMA\text{-}OUT}$ (3 I/O Requests)

These inputs are sampled by the CPU during the interval between the leading edge of TPB and the leading edge of TPA.

Interrupt Action - X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action - Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

NOTE: In the event of concurrent DMA and Interrupt requests, DMA-IN has priority followed by DMA-OUT and then Interrupt.

SC0, SC1, (2 State Code Lines)

These outputs indicate that the CPU is: 1) fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA. H = V_{CC}, L = V_{SS}.

STATE TYPE	STATE CODE LINES	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB (2 Timing Pulses)

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode.

MA0 to MA7 (8 Memory Address Lines)

In each cycle, the higher-order byte of a 16-bit CPU memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 64K bytes.

$\overline{\text{MWR}}$ (Write Pulse)

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

$\overline{\text{MRD}}$ (Read Level)

A low level on MRD indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory does not have a three-state high-impedance output, MRD is useful for driving memory/bus separator gates. It is also used to indicate the direction of data transfer during an I/O instruction. For additional information see Table 1.

Q

Single bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

CLOCK

Input for externally generated single-phase clock. The clock is counted down internally to 8 clock pulses per machine cycle.

$\overline{\text{XTAL}}$

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and $\overline{\text{XTAL}}$) in parallel with a resistance (10MΩ typ). Frequency trimming capacitors may be required at terminals 1 and 39. For additional information, see Application Note AN6565.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$ (2 Control Lines)

Provide four control modes as listed in the following truth table:

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	LOAD
L	H	RESET
H	L	PAUSE
H	H	RUN

V_{DD}, V_{SS}, V_{CC} (Power Levels)

The internal voltage supply V_{DD} is isolated from the Input/Output voltage supply V_{CC} so that the processor may operate at maximum speed while interfacing with peripheral devices operating at lower voltage. V_{CC} must be less than or equal to V_{DD}. All outputs swing from V_{SS} to V_{CC}. The recommended input voltage swing is V_{SS} to V_{CC}.

Architecture

The CPU block diagram is shown in Figure 2. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P and X. The contents of any register can be directed to any one of the following three paths:

1. The external memory (multiplexed, higher-order byte first, on to 8 memory address lines).
2. The D register (either of the two bytes can be gated to D).
3. The increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

With two exceptions, CPU instruction consists of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second - and third if necessary - are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher order 4 bits of the instruction byte are loaded into the register and the lower order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. Designate one of the 16 registers in R to be acted upon during register operations.
2. Indicate to the I/O devices a command code or device selection code for peripherals.
3. Indicate the specific operation to be executed during the ALU instructions, types of test to be performed during the Branch instruction, or the specific operation required in a class of miscellaneous instructions (70 - 73 and 78 - 7B).
4. Indicate the value to be loaded into P to designate a new register to be used as the program counter R(P).
5. Indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other reg-

isters in R can be used as subroutine program counters. By single instruction the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R(0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table 1).

1. ALU operations F1 - F5, F7, 74, 75, 77
2. Output instructions 61 through 67
3. Input instructions 69 through 6F
4. Certain miscellaneous instructions - 70 - 73, 78, 60, F0

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8 - FD, FF, 7C, 7D, 7F. During these instruction executions, the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the 1800-series architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

Data Registers

When registers in R are used to store bytes of data, four instructions are provided which allow D to receive from or write into either the higher-order or lower-order byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

The Q Flip-Flop

An internal flip-flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. The output of Q is also available as a microprocessor output.

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initiated. When an interrupt request occurs and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction), the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Interrupt Enable is automatically deactivated to inhibit further interrupts. The user's interrupt routine is now in control; the contents of T may be saved by means of a single instruction (78) in the memory location pointed to by R(X). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with a single instruction (70 or 71). The Interrupt Enable flip-flop can be activated to permit further interrupts or can be disabled to prevent them.

CPU Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1-Bit	Data Flag (ALU Carry)
B	8 Bits	Auxiliary Holding Register
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which register is Program Counter
X	4 Bits	Designates which register is Data Pointer
N	4 Bits	Holds Low-Order Instruction Digit
I	4 Bits	Holds High-Order Instruction Digit
T	8 Bits	Holds old X, P after Interrupt (X is high nibble)
IE	1-Bit	Interrupt Enable
Q	1-Bit	Output Flip-Flop

CDP1802 Control Modes

The $\overline{\text{WAIT}}$ and $\overline{\text{CLEAR}}$ lines provide four control modes as listed in the following truth table:

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	LOAD
L	H	RESET
H	L	PAUSE
H	H	RUN

The function of the modes are defined as follows:

Load

Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that DMA-IN operation does not force execution of the next instruction.

Reset

Registers I, N, Q are reset, IE is set and 0's (VSS) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1 and register X, P, and R(0) are reset. Interrupt and DMA servicing are

suppressed during the initialization cycle. The next cycle is an S0, S1, or an S2 but never an S3. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE, so as to preclude interrupts until ready for them. Power-up reset can be realized by connecting an RC network directly to the CLEAR pin, since it has a Schmitt triggered input, see Figure 24.

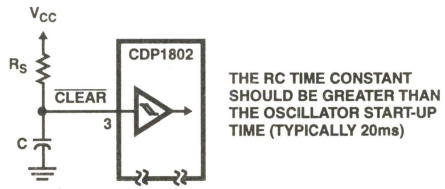


FIGURE 24. RESET DIAGRAM

Pause

Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation on the first negative high-to-low transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

Run-Mode State Transitions

The CPU state transitions when in the RUN and RESET modes are shown in Figure 25. Each machine cycle requires the same period of time, 8 clock pulses, except the initialization cycle, which requires 9 clock pulses. The execution of an instruction requires either two or three machine cycles, S0 followed by a single S1 cycle or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt response. Table 2 shows the conditions on Data Bus and Memory Address lines during all machine states.

Instruction Set

The CPU instruction summary is given in Table 1. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where

W = N or X, or P

R(W).0: Lower order byte of R(W)

R(W).1: Higher order byte of R(W)

Operation Notation

$M(R(N)) \rightarrow D; R(N) + 1 \rightarrow R(N)$

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

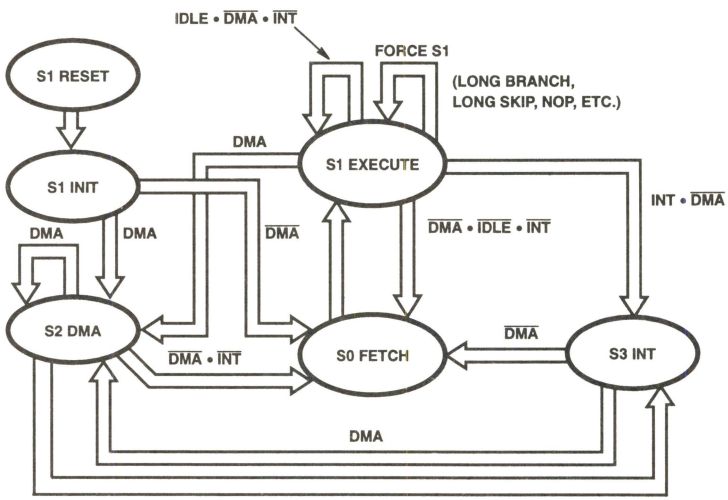


FIGURE 25. STATE TRANSITION DIAGRAM

TABLE 1. INSTRUCTION SUMMARY (SEE NOTES)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	M(R(N)) → D; FOR N not 0
LOAD ADVANCE	LDA	4N	M(R(N)) → D; R(N) + 1 → R(N)
LOAD VIA X	LDX	F0	M(R(X)) → D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X)) → D; R(X) + 1 → R(X)
LOAD IMMEDIATE	LDI	F8	M(R(P)) → D; R(P) + 1 → R(P)
STORE VIA N	STR	5N	D → M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D → M(R(X)); R(X) - 1 → R(X)
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	R(N) + 1 → R(N)
DECREMENT REG N	DEC	2N	R(N) - 1 → R(N)
INCREMENT REG X	IRX	60	R(X) + 1 → R(X)
GET LOW REG N	GLO	8N	R(N).0 → D
PUT LOW REG N	PLO	AN	D → R(N).0
GET HIGH REG N	GHI	9N	R(N).1 → D
PUT HIGH REG N	PHI	BN	D → R(N).1
LOGIC OPERATIONS (Note 1)			
OR	OR	F1	M(R(X)) OR D → D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D → D; R(P) + 1 → R(P)
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D → D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D → D; R(P) + 1 → R(P)
AND	AND	F2	M(R(X)) AND D → D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D → D; R(P) + 1 → R(P)
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D) → DF, 0 → MSB(D)
SHIFT RIGHT WITH CARRY	SHRC	76 (Note 2)	SHIFT D RIGHT, LSB(D) → DF, DF → MSB(D)
RING SHIFT RIGHT	RSHR	76 (Note 2)	SHIFT D RIGHT, LSB(D) → DF, DF → MSB(D)
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D) → DF, 0 → LSB(D)
SHIFT LEFT WITH CARRY	SHLC	7E (Note 2)	SHIFT D LEFT, MSB(D) → DF, DF → LSB(D)
RING SHIFT LEFT	RSHL	7E (Note 2)	SHIFT D LEFT, MSB(D) → DF, DF → LSB(D)
ARITHMETIC OPERATIONS (Note 1)			
ADD	ADD	F4	M(R(X)) + D → DF, D
ADD IMMEDIATE	ADI	FC	M(R(P)) + D → DF, D; R(P) + 1 → R(P)
ADD WITH CARRY	ADC	74	M(R(X)) + D + DF → DF, D
ADD WITH CARRY, IMMEDIATE	ADCI	7C	M(R(P)) + D + DF → DF, D; R(P) + 1 → R(P)
SUBTRACT D	SD	F5	M(R(X)) - D → DF, D
SUBTRACT D IMMEDIATE	SDI	FD	M(R(P)) - D → DF, D; R(P) + 1 → R(P)
SUBTRACT D WITH BORROW	SDB	75	M(R(X)) - D - (NOT DF) → DF, D

TABLE 1. INSTRUCTION SUMMARY (SEE NOTES) **(Continued)**

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	M(R(P)) - D - (Not DF) → DF, D; R(P) + 1 → R(P)
SUBTRACT MEMORY	SM	F7	D-M(R(X)) → DF, D
SUBTRACT MEMORY IMMEDIATE	SMI	FF	D-M(R(P)) → DF, D; R(P) + 1 → R(P)
SUBTRACT MEMORY WITH BORROW	SMB	77	D-M(R(X))-(NOT DF) → DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	D-M(R(P))-(NOT DF) → DF, D; R(P) + 1 → R(P)
BRANCH INSTRUCTIONS - SHORT BRANCH			
SHORT BRANCH	BR	30	M(R(P)) → R(P).0
NO SHORT BRANCH (See SKP)	NBR	38 (Note 2)	R(P) + 1 → R(P)
SHORT BRANCH IF D = 0	BZ	32	IF D = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF DF = 1	BDF	33 (Note 2)	IF DF = 1, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF = 0	BNF	3B (Note 2)	IF DF = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q = 1	BQ	31	IF Q = 1, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF Q = 0	BNQ	39	IF Q = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF1 = 1 ($\overline{EF1} = V_{SS}$)	B1	34	IF EF1 =1, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF1 = 0 ($\overline{EF1} = V_{CC}$)	BN1	3C	IF EF1 = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF2 = 1 ($\overline{EF2} = V_{SS}$)	B2	35	IF EF2 = 1, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF2 = 0 ($\overline{EF2} = V_{CC}$)	BN2	3D	IF EF2 = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF3 = 1 ($\overline{EF3} = V_{SS}$)	B3	36	IF EF3 = 1, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF3 = 0 ($\overline{EF3} = V_{CC}$)	BN3	3E	IF EF3 = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF4 = 1 ($\overline{EF4} = V_{SS}$)	B4	37	IF EF4 = 1, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF4 = 0 ($\overline{EF4} = V_{CC}$)	BN4	3F	IF EF4 = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
BRANCH INSTRUCTIONS - LONG BRANCH			
LONG BRANCH	LBR	C0	M(R(P)) → R(P). 1, M(R(P) + 1) → R(P).0
NO LONG BRANCH (See LSKP)	NLBR	C8 (Note 2)	R(P) = 2 → R(P)
LONG BRANCH IF D = 0	LBZ	C2	IF D = 0, M(R(P)) → R(P).1, M(R(P) +1) → R(P).0, ELSE R(P) + 2 → R(P)
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D Not 0, M(R(P)) → R(P).1, M(R(P) + 1) → R(P).0, ELSE R(P) + 2 → R(P)
LONG BRANCH IF DF = 1	LBDF	C3	IF DF = 1, M(R(P)) → R(P).1, M(R(P) + 1) → R(P).0, ELSE R(P) + 2 → R(P)
LONG BRANCH IF DF = 0	LBNF	CB	IF DF = 0, M(R(P)) → R(P).1, M(R(P) + 1) → R(P).0, ELSE R(P) + 2 → R(P)
LONG BRANCH IF Q = 1	LBQ	C1	IF Q = 1, M(R(P)) → R(P).1, M(R(P) + 1) → R(P).0, ELSE R(P) + 2 → R(P)

TABLE 1. INSTRUCTION SUMMARY (SEE NOTES) **(Continued)**

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
LONG BRANCH IF Q = 0	LBNQ	C9	IF Q = 0, M(R(P)) → R(P).1, M(R(P) + 1) → R(P).0 EISE R(P) + 2 → R(P)
SKIP INSTRUCTIONS			
SHORT SKIP (See NBR)	SKP	38 (Note 2)	R(P) + 1 → R(P)
LONG SKIP (See NLBR)	LSKP	C8 (Note 2)	R(P) + 2 → R(P)
LONG SKIP IF D = 0	LSZ	CE	IF D = 0, R(P) + 2 → R(P), ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D Not 0, R(P) + 2 → R(P), ELSE CONTINUE
LONG SKIP IF DF = 1	LSDF	CF	IF DF = 1, R(P) + 2 → R(P), ELSE CONTINUE
LONG SKIP IF DF = 0	LSNF	C7	IF DF = 0, R(P) + 2 → R(P), ELSE CONTINUE
LONG SKIP IF Q = 1	LSQ	CD	IF Q = 1, R(P) + 2 → R(P), ELSE CONTINUE
LONG SKIP IF Q = 0	LSNQ	C5	IF Q = 0, R(P) + 2 → R(P), ELSE CONTINUE
LONG SKIP IF IE = 1	LSIE	CC	IF IE = 1, R(P) + 2 → R(P), ELSE CONTINUE
CONTROL INSTRUCTIONS			
IDLE	IDL	00 (Note 3)	WAIT FOR DMA OR INTERRUPT; M(R(0)) → BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N → P
SET X	SEX	EN	N → X
SET Q	SEQ	7B	1 → Q
RESET Q	REQ	7A	0 → Q
SAVE	SAV	78	T → M(R(X))
PUSH X, P TO STACK	MARK	79	(X, P) → T; (X, P) → M(R(2)), THEN P → X; R(2) - 1 → R(2)
RETURN	RET	70	M(R(X)) → (X, P); R(X) + 1 → R(X), 1 → IE
DISABLE	DIS	71	M(R(X)) → (X, P); R(X) + 1 → R(X), 0 → IE
INPUT - OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X)) → BUS; R(X) + 1 → R(X); N LINES = 1
OUTPUT 2	OUT 2	62	M(R(X)) → BUS; R(X) + 1 → R(X); N LINES = 2
OUTPUT 3	OUT 3	63	M(R(X)) → BUS; R(X) + 1 → R(X); N LINES = 3
OUTPUT 4	OUT 4	64	M(R(X)) → BUS; R(X) + 1 → R(X); N LINES = 4
OUTPUT 5	OUT 5	65	M(R(X)) → BUS; R(X) + 1 → R(X); N LINES = 5
OUTPUT 6	OUT 6	66	M(R(X)) → BUS; R(X) + 1 → R(X); N LINES = 6
OUTPUT 7	OUT 7	67	M(R(X)) → BUS; R(X) + 1 → R(X); N LINES = 7
INPUT 1	INP 1	69	BUS → M(R(X)); BUS → D; N LINES = 1
INPUT 2	INP 2	6A	BUS → M(R(X)); BUS → D; N LINES = 2
INPUT 3	INP 3	6B	BUS → M(R(X)); BUS → D; N LINES = 3
INPUT 4	INP 4	6C	BUS → M(R(X)); BUS → D; N LINES = 4
INPUT 5	INP 5	6D	BUS → M(R(X)); BUS → D; N LINES = 5
INPUT 6	INP 6	6E	BUS → M(R(X)); BUS → D; N LINES = 6
INPUT 7	INP 7	6F	BUS → M(R(X)); BUS → D; N LINES = 7

TABLE 1. INSTRUCTION SUMMARY (SEE NOTES) **(Continued)**

INSTRUCTION	MNEMONIC	OP CODE	OPERATION

NOTES: (For Table 1)

1. The arithmetic operations and the shift instructions are the only instructions that can alter the DF.

   After an add instruction:
   DF = 1 denotes a carry has occurred
   DF = 0 Denotes a carry has not occurred
   After a subtract instruction:
   DF = 1 denotes no borrow. D is a true positive number
   DF = 0 denotes a borrow. D is two's complement
   The syntax "-(not DF)" denotes the subtraction of the borrow.

2. This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

3. An idle instruction initiates a repeating S1 cycle. The processor will continue to idle until an I/O request ($\overline{\text{INTERRUPT}}$, $\overline{\text{DMA-IN}}$, or $\overline{\text{DMA- OUT}}$) is activated. When the request is acknowledged, the idle cycle is terminated and the I/O request is serviced, and then normal operation is resumed.

4. Long-Branch, Long-Skip and No Op instructions require three cycles to complete (1 fetch + 2 execute).

   Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

   The long-branch instructions can:
   a. Branch unconditionally
   b. Test for D = 0 or D ≠ 0
   c. Test for DF = 0 or DF = 1
   d. Test for Q = 0 or Q = 1
   e. Effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

   If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

5. The short-branch instructions are two bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address.

   The short branch instruction can:
   a. Branch unconditionally
   b. Test for D = 0 or D ≠ 0
   c. Test for DF = 0 or DF = 1
   d. Test for Q = 0 or Q = 1
   e. Test the status (1 or 0) of the four EF flags
   f. Effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch within the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR).

6. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

   The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.
   The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

   They can:
   a. Skip unconditionally
   b. Test for D = 0 or D ≠ 0
   c. Test for DF = 0 or DF = 1
   d. Test for Q = 0 or Q = 1
   e. Test for IE = 1

   If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over, and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

TABLE 2. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	SYMBOL	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES	NOTES
S1	RESET			0 → I, N, Q, X, P; 1 → IE	00	XXXX	1	1	0	1
	Initialize, Not Programmer Accessible			0000 → R	00	XXXX	1	1	0	2
S0		FETCH		MRP → I, N; RP + 1 → RP	MRP	RP	0	1	0	3
S1	0	0	IDL	IDLE	MR0	RO	0	1	0	4, Fig. 8
	0	1 - F	LDN	MRN → D	MRN	RN	0	1	0	Fig. 8
	1	0 - F	INC	RN + 1 → RN	Float	RN	1	1	0	Fig. 6
	2	0 - F	DEC	RN - 1 → RN	Float	RN	1	1	0	Fig. 6
	3	0 - F	Short Branch	Taken: MRP → RP.0 Not Taken; RP + 1 → RP	MRP	RP	0	1	0	Fig. 8
	4	0 - F	LDA	MRN → D; RN + 1 → RN	MRN	RN	0	1	0	Fig. 8
	5	0 - F	STR	D → MRN	D	RN	1	0	0	Fig. 7
	6	0	IRX	RX + 1 → RX	MRX	RX	0	1	0	Fig. 7
	6	1	OUT 1	MRX → BUS; RX + 1 → RX	MRX	RX	0	1	1	Fig. 11
		2	OUT 2						2	Fig. 11
		3	OUT 3						3	Fig. 11
		4	OUT 4						4	Fig. 11
		5	OUT 5						5	Fig. 11
		6	OUT 6						6	Fig. 11
		7	OUT 7						7	Fig. 11
		9	INP 1	BUS → MRX, D	Data from I/O Device	RX	1	0	1	Fig. 10
		A	INP 2						2	Fig. 10
		B	INP 3						3	Fig. 10
		C	INP 4						4	Fig. 10
		D	INP5						5	Fig. 10
		E	INP6						6	Fig. 10
		F	INP7						7	Fig. 10
	7	0	RET	MRX → (X, P); RX + 1 → RX; 1 → IE	MRX	RX	0	1	0	Fig. 8
		1	DIS	MRX → (X, P); RX + 1 → RX; 0 → IE	MRX	RX	0	1	0	Fig. 8
		2	LDXA	MRX → D; RX + 1 → RX	MRX	RX	0	1	0	Fig. 8
		3	STXD	D → MRX; RX - 1 → RX	D	RX	1	0	0	Fig. 7
		4	ADC	MRX + D + DF → DF, D	MRX	RX	0	1	0	Fig. 8
		5	SDB	MRX - D - DFN → DF, D	MRX	RX	0	1	0	Fig. 8
		6	SHRC	LSB(D) → DF; DF → MSB(D)	Float	RX	1	1	0	Fig. 6
		7	SMB	D - MRX - DFN → DF, D	MRX	RX	0	1	0	Fig. 8
		8	SAV	T → MRX	T	RX	1	0	0	Fig. 7

TABLE 2. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Continued)

STATE	I	N	SYMBOL	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES	NOTES
S1	7	9	MARK	(X, P) → T, MR2; P → X; R2 - 1 → R2	T	R2	1	0	0	Fig. 7
		A	REQ	0 → Q	Float	RP	1	1	0	Fig. 6
		B	SEQ	1 → Q	Float	RP	1	1	0	Fig. 6
		C	ADCI	MRP + D + DF → DF, D; RP + 1	MRP	RP	0	1	0	Fig. 8
		D	SDBI	MRP - D - DFN → DF, D; RP + 1	MRP	RP	0	1	0	Fig. 8
		E	SHLC	MSB(D) → DF; DF → LSB(D)	Float	RP	1	1	0	Fig. 6
		F	SMBI	D - MRP - DFN → DF, D; RP + 1	MRP	RP	0	1	0	Fig. 8
	8	0 - F	GLO	RN.0 → D	RN.0	RN	1	1	0	Fig. 6
	9	0 - F	GHI	RN.1 → D	RN.1	RN	1	1	0	Fig. 6
	A	0 - F	PLO	D → RN.0	D	RN	1	1	0	Fig. 6
	B	0 - F	PHI	D → RN.1	D	RN	1	1	0	Fig. 6
S1#1	C	0 - 3, 8 - B	Long Branch	Taken: MRP → B; RP + 1 → RP	MRP	RP	0	1	0	Fig. 9
#2				Taken: B → RP.1; MRP → RP.0	M(RP + 1)	RP + 1	0	1	0	Fig. 9
S1#1				Not Taken: RP + 1 → RP	MRP	RP	0	1	0	Fig. 9
#2				Not Taken: RP + 1 → RP	M(RP + 1)	RP + 1	0	1	0	Fig. 9
S1#1		5 6 7 C D E F	Long Skip	Taken: RP + 1 → RP	MRP	RP	0	1	0	Fig. 9
#2				Taken: RP + 1 → RP	M(RP + 1)	RP + 1	0	1	0	Fig. 9
S1#1				Not Taken: No Operation	MRP	RP	0	1	0	Fig. 9
#2				Not Taken: No Operation	MRP	RP	0	1	0	Fig. 9
S1#1		4	NOP	No Operation	MRP	RP	0	1	0	Fig. 9
#2				No Operation	MRP	RP	0	1	0	Fig. 9
S1	D	0 - F	SEP	N → P	NN	RN	1	1	0	Fig. 6
	E	0 - F	SEX	N → X	NN	RN	1	1	0	Fig. 6
S1	F	0	LDX	MRX → D	MRX	RX	0	1	0	Fig. 8
		1 2 3 4 5 7	OR AND XOR ADD SD SM	MRX OR D → D MRX AND D → D MRX XOR D → D MRX + D → DF, D MRX - D → DF, D D - MRX → DF, D	MRX	RX	0	1	0	Fig. 8
		6	SHR	LSB(D) → DF; 0 → MSB(D)	Float	RX	1	1	0	Fig. 6

TABLE 2. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Continued)

STATE	I	N	SYMBOL	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES	NOTES
S1	F	8	LDI	MRP → D; RP + 1 → RP	MRP	RP	0	1	0	Fig. 8
		9	ORI	MRP OR D → D; RP + 1 → RP						
		A	ANI	MRP AND D → D; RP + 1 → RP						
		B	XRI	MRP XOR D → D; RP + 1 → RP						
		C	ADI	MRP + D → DF, D; RP + 1 → RP						
		D	SDI	MRP - D → DF, D; RP + 1 → RP						
		F	SMI	D - MRP → DF, D; RP +1 → RP						
		E	SHL	MSB(D) → DF; 0 → LSB(D)	Float	RP	1	1	0	Fig. 6
S2	DMA IN			BUS → MR0; R0 + 1 → R0	Data from I/O Device	R0	1	0	0	6, Fig. 12
	DMAOUT			MR0 → BUS; R0 + 1 → R0	MR0	R0	0	1	0	6, Fig. 13
S3	INTERRUPT			X, P → T; 0 → IE, 1 → P; 2 → X	Float	RN	1	1	0	Fig. 14
S1	LOAD			IDLE ($\overline{CLEAR}$, $\overline{WAIT}$ = 0)	M(R0 - 1)	R0 - 1	0	1	0	5, Fig. 8

NOTES:

1. IE = 1, TPA, TPB suppressed, state = S1.
2. BUS = 0 for entire cycle.
3. Next state always S1.
4. Wait for DMA or INTERRUPT.
5. Suppress TPA, wait for DMA.
6. IN REQUEST has priority over OUT REQUEST.
7. See Timing Waveforms, Figure 5 through Figure 14 for machine cycles.

Operating and Handling Considerations

Handling

All inputs and outputs of Harris CMOS devices have a network for electrostatic protection during handling.

Operating

Operating Voltage - During operation near the maximum supply voltage limit care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD} - V_{SS} to exceed the absolute maximum rating.

Input Signals - To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10mA even when the power supply is off.

Unused Inputs - A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits - Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

HARRIS SEMICONDUCTOR

CDP1802AC/3

March 1997

High-Reliability CMOS 8-Bit Microprocessor

Features

- For Use In Aerospace, Military, and Critical Industrial Equipment
- Minimum Instruction Fetch-Execute Time of 4.5μs (Maximum Clock Frequency of 3.6MHz) at V_{DD} = 5V, T_A = +25°C
- Operation Over the Full Military Temperature Range . . . . . -55°C to +125°C
- Any Combination of Standard RAM and ROM Up to 65,536 Bytes
- 8–Bit Parallel Organization With Bidirectional Data Bus and Multiplexed Address Bus
- 16 x 16 Matrix of Registers for Use as Multiple Program Counters, Data Pointers, or Data Registers
- On-Chip DMA, Interrupt, and Flag Inputs
- High Noise Immunity . . . . . 30% of V_{DD}

Ordering Information

PACKAGE	TEMP. RANGE (°C)	5V - 3.2MHz	PKG NO.
SBDIP	-55 to 125	CDP1802ACD3	D40.6

Description

The CDP1802A/3 High-Reliability LSI CMOS 8-bit register oriented Central-Processing Unit (CPU) is designed for use as a general purpose computing or control element in a wide range of stored-program systems or products.

The CDP1802A/3 includes all of the circuits required for fetching, interpreting, and executing instructions which have been stored in standard types of memories. Extensive input/output (I/O) control features are also provided to facilitate system design.

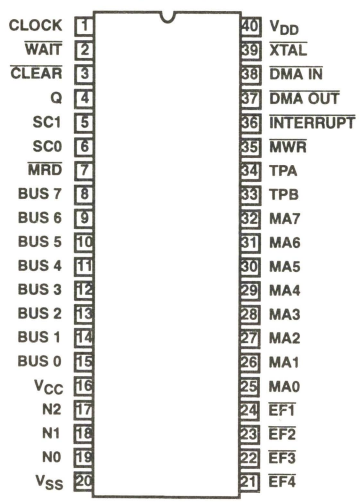
The 1800 Series Architecture is designed with emphasis on the total microcomputer system as an integral entity so that systems having maximum flexibility and minimum cost can be realized. The 1800 Series CPU also provides a synchronous interface to memories and external controllers for I/O devices, and minimizes the cost of interface controllers. Further, the I/O interface is capable of supporting devices operating in polled, interrupt-driven, or direct memory-access modes.

The CDP1802AC/3 is functionally identical to its predecessor, the CDP1802. The "A" version includes some performance enhancements and can be used as a direct replacement in systems using the CDP1802.

This type is supplied in 40 lead dual-in-line sidebrazed ceramic packages (D suffix).

Pinout

CDP1802AC/3 (SBDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1441.2**

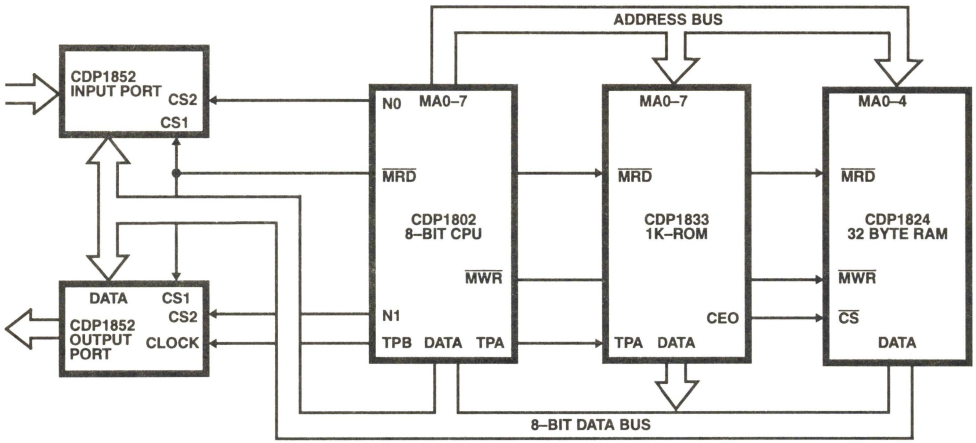


FIGURE 1. TYPICAL CDP1802A/3 SMALL MICROPROCESSOR SYSTEM

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1802AC/3 . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, any One Input . . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	55	15

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range 100mW
Operating Temperature Range (T_A)
Package Type D . . . . . -55°C to +125°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ±1/32 In. (1.59 ±0.79mm)
from case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges

PARAMETER	MIN	MAX	UNITS
DC Operating Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V
Maximum Clock Input Rise or Fall Time	-	1	µs

Performance Specifications

PARAMETER	V_{DD} (V)	-55°C TO +25°C	+125°C	UNITS
Minimum Instruction Time (Note 1)	5	4.5	5.9	µs
Maximum DMA Transfer Rate	5	450	340	Kbytes/s
Maximum Clock Input Frequency, Load Capacitance (C_L) = 50pF, f_{CL}	5	DC-3.6	DC-2.7	MHz

NOTE:

1. Equals 2 machine cycles - one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles - one Fetch and two Execute operations.

Static Electrical Specifications

All Limits are 100% Tested

PARAMETER	CONDITIONS			-55°C, +25°C		+125°C		UNITS
	V_{OUT} (V)	V_{IN}, (V)	V_{CC}, V_{DD} (V)	MIN	MAX	MIN	MAX	
Quiescent Device Current, I_{DD}	-	-	5	-	100	-	250	µA
Output Low Drive (Sink) Current (Except $\overline{XTAL}$), I_{OL}	0.4	0, 5	5	1.20	-	0.90	-	mA
$\overline{XTAL}$	0.4	5	5	185	-	140	-	µA
Output High Drive (Source) Current (Except $\overline{XTAL}$), I_{OH}	4.6	0, 5	5	-	-0.30	-	-0.20	mA
$\overline{XTAL}$	4.6	0	5	-	-135	-	-100	µA
Output Voltage Low-Level, V_{OL}	-	0, 5	5	-	0.1	-	0.2	V
Output Voltage High-Level, V_{OH}	-	0, 5	5	4.9	-	4.8	-	V

Static Electrical Specifications All Limits are 100% Tested (Continued)

PARAMETER	CONDITIONS			-55°C, +25°C		+125°C		UNITS
	V_{OUT} (V)	V_{IN}, (V)	V_{CC}, V_{DD} (V)	MIN	MAX	MIN	MAX	
Input Low Voltage, V_{IL}	0.5, 4.5	-	5	-	1.5	-	1.5	V
Input High Voltage, V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	V
Input Leakage Current, I_{IN}	Any Input	0, 5	5	-	±1	-	±5	µA
Three-State Output Leakage Current, I_{OUT}	0, 5	0, 5	5	-	±1	-	±5	µA

NOTE:

2. 5V level characteristics apply to Part No. CDP1802AC/3, and 5V and 10V level characteristics apply to part No. CDP1802A/3.

Timing Specifications As a Function of T (T = 1/fCLOCK), C_L = 50 pF

PARAMETER	V_{DD} (V)	LIMITS (NOTE 3)		UNITS
		-55°C, +25°C	+125°C	
High-Order Memory-Address Byte Setup to TPA ↘ Time, t_{SU}	5	2T-450	2T-580	ns
High-Order Memory-Address Byte Hold After TPA Time, t_H	5	T/2 +0	T/2 +0	ns
Low-Order Memory-Address Byte Hold After WR Time, t_H	5	T-30	T-40	ns
CPU Data to Bus Hold After WR Time, t_H	5	T-170	T-250	ns
Required Memory Access Time Address to Data, t_{ACC}	5	5T-300	5T-400	ns

NOTE:

3. These limits are not directly tested.

Implicit Specifications (Note 4) T_A = -55°C to +25°C

PARAMETER		SYMBOL	V_{DD} (V)	TYPICAL VALUES	UNITS
Typical Total Power Dissipation Idle "00" at M(0000), C_L = 50pF	f = 2MHz	-	5	4	mW
Effective Input Capacitance any Input	-	C_{IN}	-	5	pF
Effective Three-State Terminal Capacitance Data Bus	-		-	7.5	pF
Minimum Data Retention Voltage	-	V_{DR}	-	2.4	V
Data Retention Current	-	I_{DR}	2.4	10	µA

NOTE:

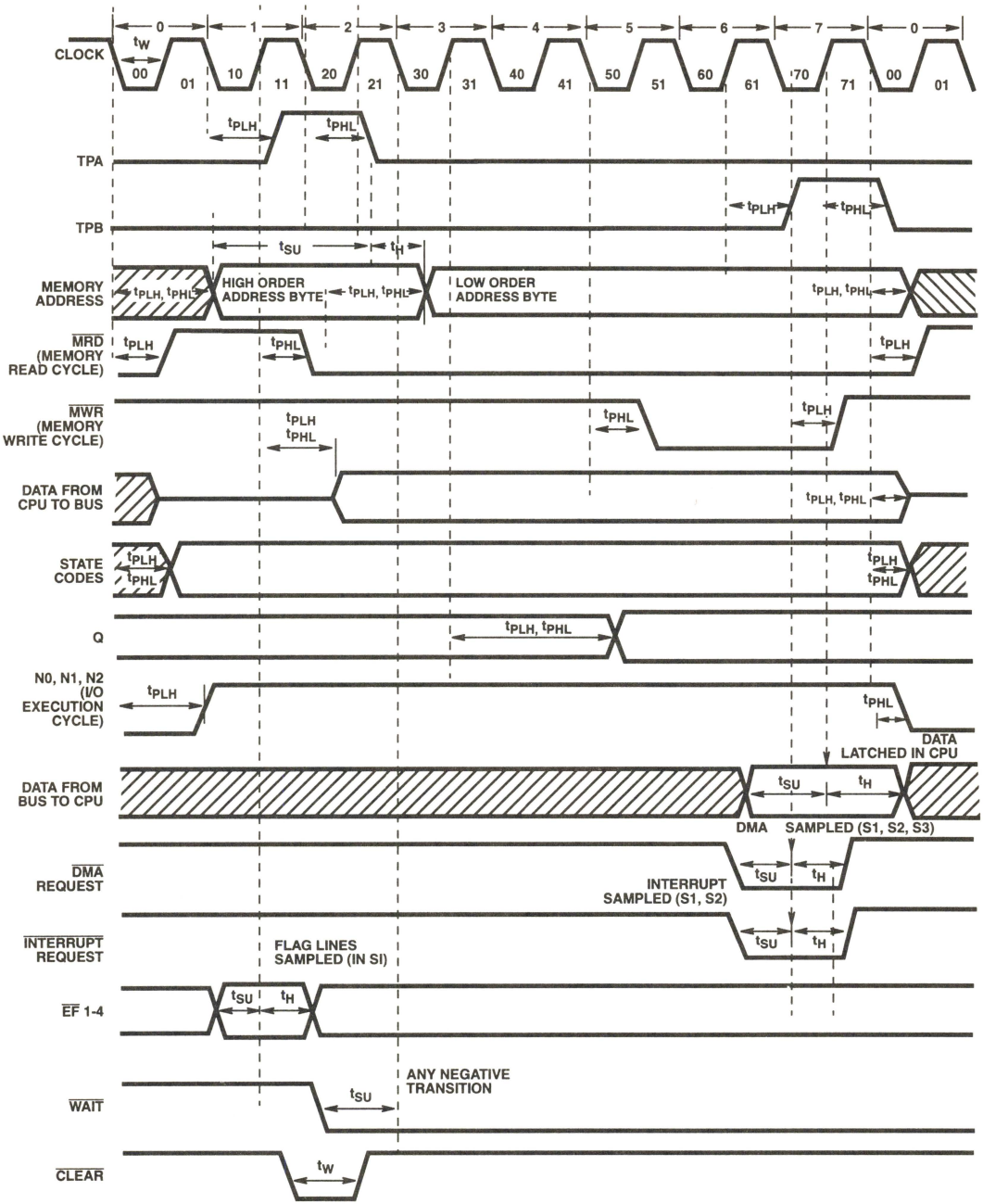
4. These specifications are not tested. Typical values are provided for guidance only.

Dynamic Electrical Specifications C_L = 50pF, Timing Measurement at 0.5 V_{DD} Point

PARAMETERS	V_{DD} (V)	-55°C TO +25°C		+125°C		UNITS
		MIN	MAX	MIN	MAX	
Progagation Delay Times, t_{PLH}, t_{PHL}						
Clock to TPA, TPB	5	-	275	-	370	ns
Clock-to-Memory High Address Byte, t_{PLH}, t_{PHL}	5	-	725	-	950	ns
Clock-to-Memory Low Address Byte Valid, t_{PLH}, t_{PHL}	5	-	340	-	425	ns
Clock to $\overline{MRD}$, t_{PLH}, t_{PHL}	5	-	340	-	425	ns
Clock to $\overline{MWR}$, t_{PLH}, t_{PHL}	5	-	275	-	370	ns
Clock to (CPU DATA to BUS) Valid, t_{PLH}, t_{PHL}	5	-	430	-	550	ns
Clock to State Code, t_{PLH}, t_{PHL}	5	-	440	-	550	ns
Clock to Q, t_{PLH}, t_{PHL}	5	-	375	-	475	ns
Clock to N (0 - 2), t_{PLH}, t_{PHL}	5	-	400	-	525	ns
Interface Timing Requirements (Note 5)						
Data Bus Input Setup, t_{SU}	5	10	-	10	-	ns
Data Bus Input Hold, t_H	5	175	-	230	-	ns
$\overline{DMA}$ Setup, t_{SU}	5	10	-	10	-	ns
$\overline{DMA}$ Hold, t_H	5	200	-	270	-	ns
Interrupt Setup, t_{SU}	5	10	-	10	-	ns
Interrupt Hold, t_H	5	175	-	230	-	ns
$\overline{WAIT}$ Setup, t_{SU}	5	30	-	30	-	ns
$\overline{EF1\text{-}4}$ Setup, t_{SU}	5	20	-	20	-	ns
$\overline{EF1\text{-}4}$ Hold, t_H	5	100	-	135	-	ns
Required Pulse Width Times						
$\overline{CLEAR}$ Pulse Width, t_{WL}	5	150	-	200	-	ns
$\overline{CLOCK}$ Pulse Width, t_{WL}	5	140	-	185	-	ns

NOTE:

5. Minimum input setup and hold times required by Part CDP1802AC/3.



NOTES:

6. This timing diagram is used to show signal relationships only, and does not represent any specific machine cycle.
7. All measurements are referenced to 50% point of the waveforms.
8. Shaded areas indicate "don't care" or undefined state. Multiple transitions may occur during this period.

FIGURE 2. TIMING WAVEFORMS

Performance Curves

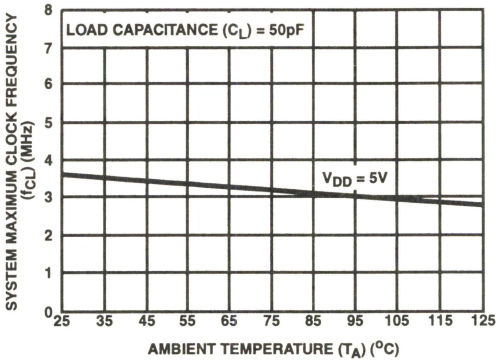


FIGURE 3. TYPICAL MAXIMUM CLOCK FREQUENCY AS A FUNCTION OF TEMPERATURE

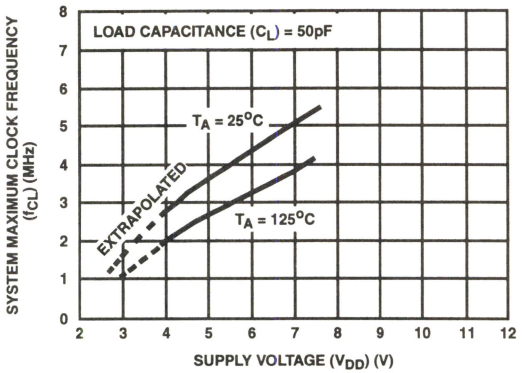


FIGURE 4. TYPICAL MAXIMUM CLOCK FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

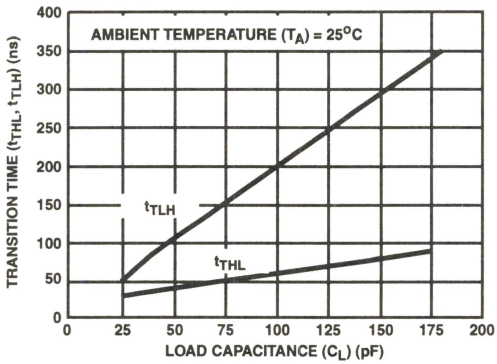


FIGURE 5. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

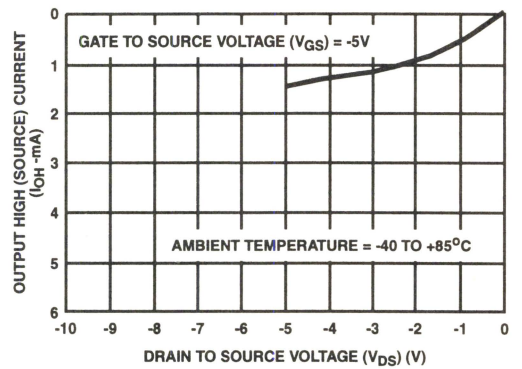


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

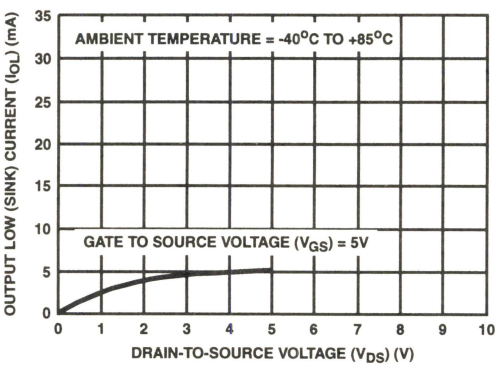
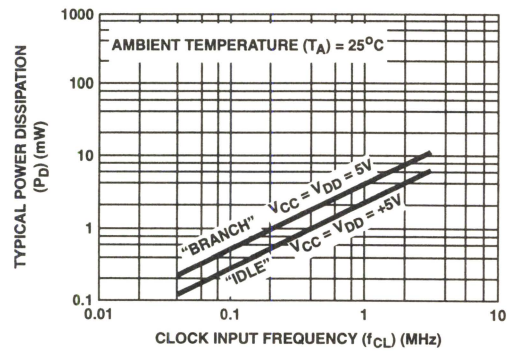


FIGURE 7. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

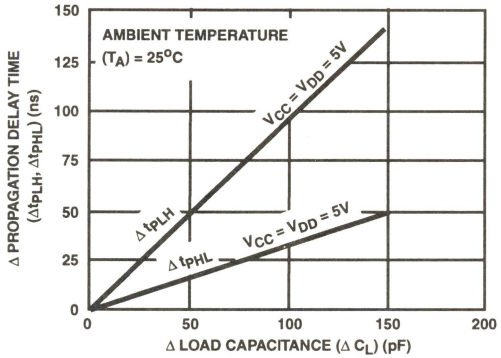


NOTES:

9. Idle = "00" at M (0000)
10. Branch = "3707" at M (8107)

FIGURE 8. TYPICAL POWER DISSIPATION AS A FUNCTION OF CLOCK FREQUENCY FOR BRANCH INSTRUCTION AND IDLE INSTRUCTION

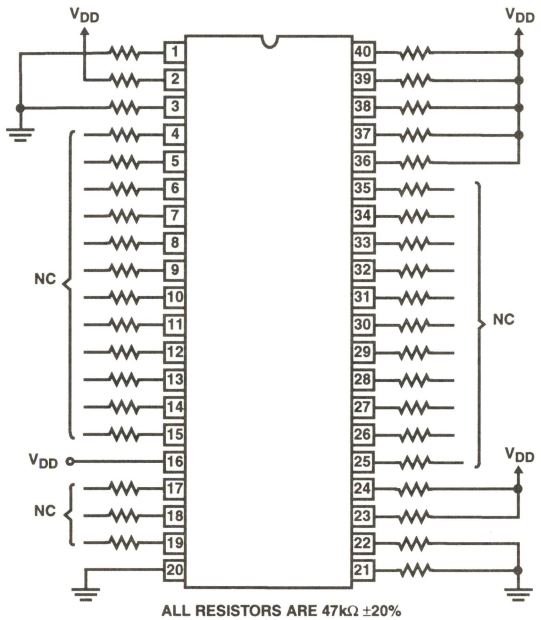
Performance Curves (Continued)



NOTE: Any output except $\overline{XTAL}$.

FIGURE 9. TYPICAL CHANGE IN PROPAGATION DELAY AS A FUNCTION OF A CHANGE IN LOAD CAPACITANCE

Burn-In Circuit



ALL RESISTORS ARE 47kΩ ±20%

TYPE	V_{DD}	TEMPERATURE	TIME
CDP1802AC	7V	+125°C	160 Hours

FIGURE 10. BIAS/STATIC BURN-IN CIRCUIT

HARRIS SEMICONDUCTOR

CDP1805AC, CDP1806AC

CMOS 8-Bit Microprocessor with On-Chip RAM† and Counter/Timer

March 1997

Features

- Instruction Time of 3.2μs, -40°C to +85°C
- 123 Instructions - Upwards Software Compatible With CDP1802
- BCD Arithmetic Instructions
- Low-Power IDLE Mode
- Pin Compatible With CDP1802 Except for Terminal 16
- 64K-Byte Memory Address Capability
- 64 Bytes of On-Chip RAM†
- 16 x 16 Matrix of On-Board Registers
- On-Chip Crystal or RC Controlled Oscillator
- 8-Bit Counter/Timer

Description

The CDP1805AC and CDP1806AC are functional and performance enhancements of the CDP1802 CMOS 8-bit register-oriented microprocessor series and are designed for use in general-purpose applications.

The CDP1805AC hardware enhancements include a 64-byte RAM and an 8-bit presettable down counter. The Counter/Timer which generates an internal interrupt request, can be programmed for use in timebase, event-counting, and pulse-duration measurement applications. The Counter/Timer underflow output can also be directed to the Q output terminal. The CDP1806AC hardware enhancements are identical to the CDP1805AC, except the CDP1806AC contains no on-chip RAM.

The CDP1805AC and CDP1806AC software enhancements include 32 more instructions than the CDP1802. The 32 new software instructions add subroutine call and return capability, enhanced data transfer manipulation, Counter/Timer control, improved interrupt handling, single-instruction loop counting, and BCD arithmetic.

Upwards software and hardware compatibility is maintained when substituting a CDP1805AC or CDP1806AC for other CDP1800-series microprocessors. Pinout is identical except for the replacement of V_{CC} with $\overline{ME}$ on the CDP1805AC and the replacement of V_{CC} with V_{DD} on the CDP1806AC.

Ordering Information

CDP1805AC	CDP1806AC	TEMPERATURE RANGE	PACKAGE	PKG. NO.
CDP1805ACE	CDP1806ACE	-40°C to +85°C	Plastic DIP	E40.6
-	CDP1806ACEX		Burn-In	
CDP1805ACQ	CDP1806ACQ	-40°C to +85°C	PLCC	N44.65
CDP1805ACD	CDP1806ACD	-40°C to +85°C	SBDIP	D40.6
CDP1805ACDX	-		Burn-In	

† CDP1805AC Only

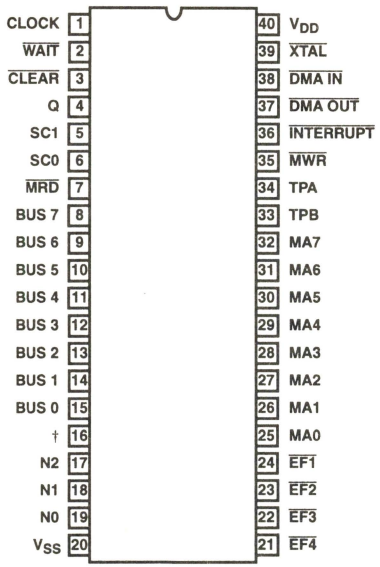
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Copyright © Harris Corporation 1997

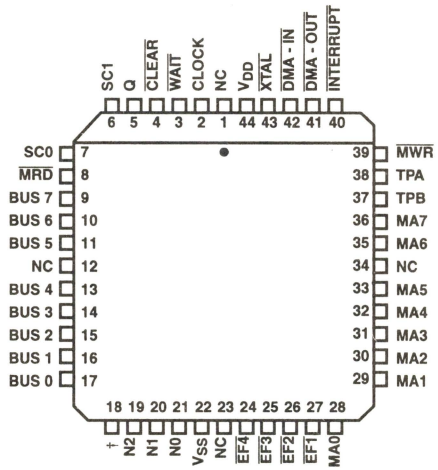
File Number **1370.2**

Pinouts

CDP1805AC, CDP1806AC
(PDIP, SBDIP)
TOP VIEW



CDP1805AC, CDP1806AC
(PLCC, PACKAGE TYPE Q)
TOP VIEW



† $\overline{ME}$ for CDP1805AC
V_{DD} for CDP1806AC

Schematic

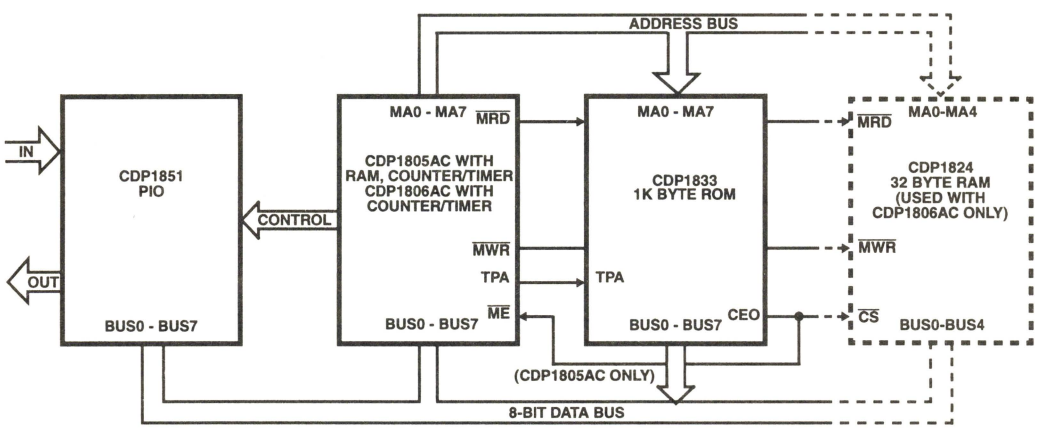


FIGURE 1. TYPICAL CDP1805AC, CDP1806AC SMALL MICROPROCESSOR SYSTEM

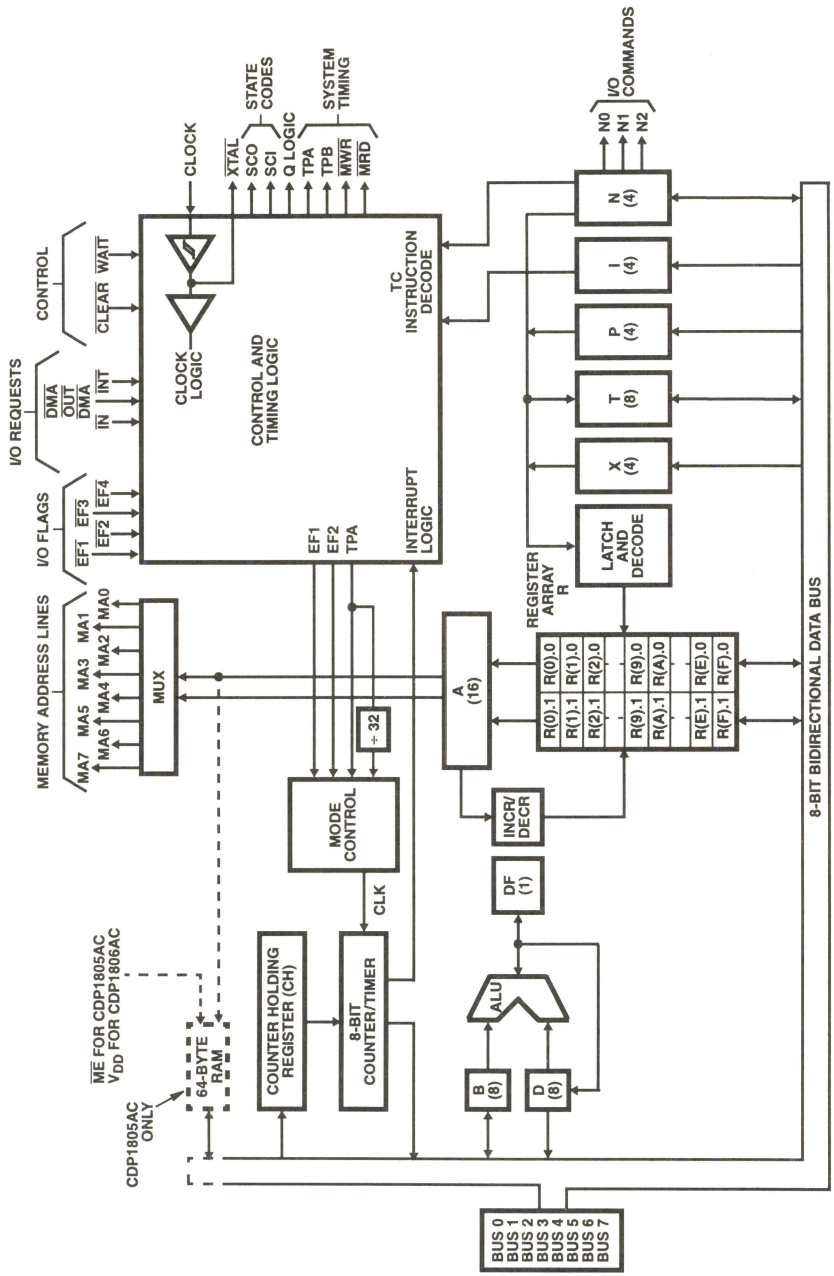


FIGURE 2. BLOCK DIAGRAM FOR CDP1805AC AND CDP1806AC

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal) . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, any One Input . . . . . ±10mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	50	N/A
PLCC Package	46	N/A
SBDIP Package	55	15

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range 100mW
Operating Temperature Range (T_A)
Package Type D . . . . . -55°C to +125°C
Package Type E and Q . . . . . -40°C to +85°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At Distance 1/16 ±1/32in (1.59 ± 0.79mm) from case for 10s Max . . . . . +265°C
Printed Circuit Board Mount: 57mm x 57mm Minimum Area x 1.6mm Thick G10 Epoxy Glass, or Equivalent.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

T_A = Full-Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges.

PARAMETER	TEST CONDITIONS V_{DD} (V)	CDP1805ACD, CDP1805ACE CDP1806ACD, CDP1806ACE		UNITS
		MIN	MAX	
DC Operating Voltage Range	-	4	6.5	V
Input Voltage Range	-	V_{SS}	V_{DD}	V
Minimum Instruction Time (Note 1) (f_{CL} = 5MHz)	5	3.2	-	µs
Maximum DMA Transfer Rate	5	-	0.625	Mbyte/s
Maximum Clock Input Frequency, Load Capacitance (C_L) = 50pF	5	DC	5	MHz
Maximum External Counter/Timer Clock Input Frequency to $\overline{EF1}$, $\overline{EF2}$	5	DC	2	MHz

NOTES:

1. Equals 2 machine cycles - one Fetch and one Execute operation for all instructions except Long Branch, Long Skip, NOP, and "68" family instructions, which are more than two cycles.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Static Electrical Specifications

at T_A = -40°C to +85°C, V_{DD} ±5%, Except as Noted

PARAMETER	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1805ACD, CDP1805ACE CDP1806ACD, CDP1806ACE			UNITS
				MIN	(NOTE 3) TYP	MAX	
Quiescent Device Current, I_{DD}	-	0, 5	5	-	50	200	µA
Output Low Drive (Sink) Current, (Except $\overline{XTAL}$), I_{OL}	0.4	0, 5	5	1.6	4	-	mA
$\overline{XTAL}$ Output, I_{OL}	0.4	5	5	0.2	0.4	-	mA
Output High Drive (Source) Current (Except $\overline{XTAL}$, I_{OH}	4.6	0, 5	5	-1.6	-4	-	mA
$\overline{XTAL}$, I_{OH}	4.6	0	5	-0.1	-0.2	-	mA
Output Voltage Low Level, V_{OL}	-	0, 5	5	-	0	0.1	V
Output Voltage High Level, V_{OH}	-	0, 5	5	4.9	5	-	V

Static Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ±5%, Except as Noted **(Continued)**

PARAMETER	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1805ACD, CDP1805ACE CDP1806ACD, CDP1806ACE MIN	(NOTE 3) TYP	MAX	UNITS
Output Voltage High Level, V_{OH}	-	0, 5	5	4.9	5	-	V
Input Low Voltage (BUS0 - BUS7, $\overline{ME}$), V_{IL}	0.5, 4.5	-	5	-	-	1.5	V
Input High Voltage (BUS0 - BUS7, $\overline{ME}$), V_{IH}	0.5, 4.5	-	5	3.5	-	-	V
Schmitt Trigger Input Voltage (Except BUS0 - BUS7, $\overline{ME}$)							
Positive Trigger Threshold, V_P	0.5, 4.5	-	5	2.2	2.9	3.6	V
Negative Trigger Threshold, V_N	0.5, 4.5	-	5	0.9	1.9	2.8	V
Hysteresis, V_H	0.5, 4.5	-	5	0.3	0.9	1.6	V
Input Leakage Current, I_{IN}	-	0, 5	5	-	±0.1	±5	µA
Three-State Output Leakage Current, I_{OUT}	0, 5	0, 5	5	-	±0.2	±5	µA
Input Capacitance, C_{IN}	-	-	-	-	5	7.5	pF
Output Capacitance, C_{OUT}	-	-	-	-	10	15	pF
Total Power Dissipation (Note 4)							
Run	-	-	5	-	35	50	mW
Idle "00" at M (0000)	-	-	5	-	12	18	mW
Minimum Data Retention Voltage, V_{DR}	$V_{DD} = V_{DR}$			-	2	2.4	V
Data Retention Current, I_{DR}	V_{DD} = 2.4			-	25	100	µA

NOTES:

3. Typical values are for T_A = +25°C and nominal V_{DD}.
4. External clock: f = 5MHz, t_R, t_F = 10ns; C_L = 50pF.

Dynamic Electrical Specifications at T_A = -40° to +85°C; C_L = 50pF; Input t_R, t_F = 10ns; Input Pulse Levels = 0.1V to V_{DD} -0.1V; V_{DD} = 5V, ±5%.

PARAMETER	CDP1805AC CDP1806AC (NOTE 5) TYP	MAX	UNITS
Propagation Delay Times			
Clock to TPA, TPB, t_{PLH}, t_{PHL}	150	275	ns
Clock-to-Memory High-Address Byte, t_{PLH}, t_{PHL}	325	550	ns
Clock-to-Memory Low-Address Byte, t_{PLH}, t_{PHL}	275	450	ns
Clock to $\overline{MRD}$, t_{PLH}, t_{PHL}	200	325	ns
Clock to $\overline{MWR}$, t_{PLH}, t_{PHL} (See Note 5)	150	275	ns
Clock to (CPU DATA to BUS), t_{PLH}, t_{PHL}	375	625	ns
Clock to State Code, t_{PLH}, t_{PHL}	225	400	ns
Clock to Q, t_{PLH}, t_{PHL}	250	425	ns
Clock to N, t_{PLH}, t_{PHL}	250	425	ns
Clock to Internal RAM Data to BUS, t_{PLH}, t_{PHL}	420	650	ns

Dynamic Electrical Specifications at $T_A = -40^o$ to $+85^oC$; $C_L = 50pF$; Input t_R, $t_F = 10ns$; Input Pulse Levels = 0.1V to V_{DD} -0.1V; $V_{DD} = 5V, \pm 5\%$. **(Continued)**

PARAMETER	CDP1805AC CDP1806AC (NOTE 5) TYP	CDP1805AC CDP1806AC MAX	UNITS
Minimum Set-Up And Hold Times (Note 2)			
Data Bus Input Set-Up, t_{SU}	-100	0	ns
Data Bus Input Hold, t_H	125	225	ns
$\overline{DMA}$ Set-Up, t_{SU}	-75	0	ns
$\overline{DMA}$ Hold, t_H	100	175	ns
$\overline{ME}$ Set-Up, t_{SU}	125	320	ns
$\overline{ME}$ Hold, t_H	0	50	ns
Interrupt Set-Up, t_{SU}	-100	0	ns
Interrupt Hold, t_H	100	175	ns
$\overline{WAIT}$ Set-Up, t_{SU}	20	50	ns
$\overline{EF1\text{-}4}$ Set-Up, t_{SU}	-125	0	ns
$\overline{EF1\text{ -}4}$ Hold, t_H	175	300	ns
Minimum Pulse Width Times (Note 6)			
$\overline{CLEAR}$ Pulse Width, t_{WL}	100	175	ns
$\overline{CLOCK}$ Pulse Width, t_W	75	100	ns

NOTES:

5. Typical values are for $T_A = 25^o$ C and nominal V_{DD}.
6. Maximum limits of minimum characteristics are the values above which all devices function.

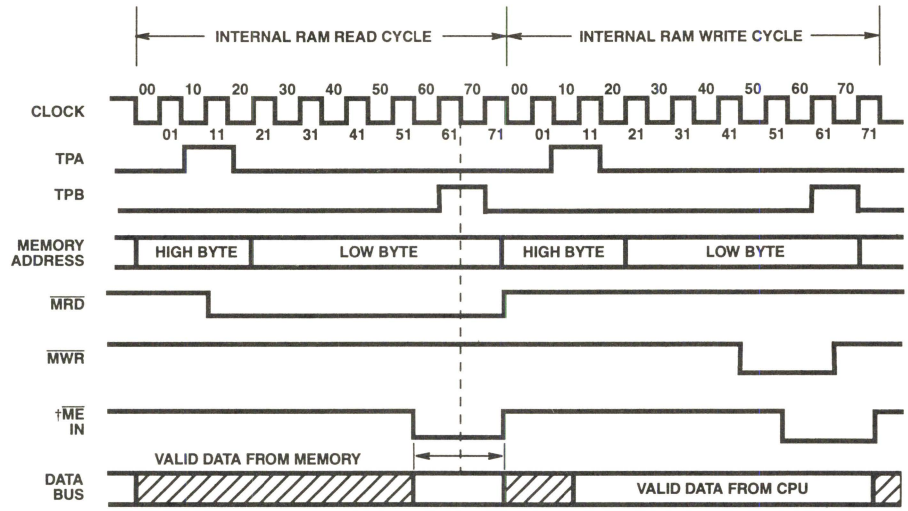
Timing Specifications as a function of T ($T = {}^1/f_{CLOCK}$) at $T_A = -40$ to $+85^oC$, $V_{DD} = 5V, \pm 15\%$

PARAMETER	CDP1805AC, CDP1806AC TYP	CDP1805AC, CDP1806AC (NOTE 7) MAX	UNITS
High-Order Memory-Address Byte Set-Up to TPA ↘ Time, t_{SU}	2T-275	2T -175	ns
$\overline{MRD}$ to TPA ↘ Time, t_{SU}	T/2 -100	T/2 -75	ns
High-Order Memory-Address Byte Hold after TPA Time, t_H	T/2 +75	T/2 +100	ns
Low-Order Memory-Address Byte Hold after WR Time, t_H	T +180	T +240	ns
CPU Data to Bus Hold after WR Time, t_H	T +110	T +150	ns
Required Memory Access Time, t_{ACC} Address to Data	4.5T -440	4.5T -330	ns

NOTE:

7. Typical values are for $T_A = +25^oC$ and nominal V_{DD}.

Timing Waveforms For Possible Operating Modes

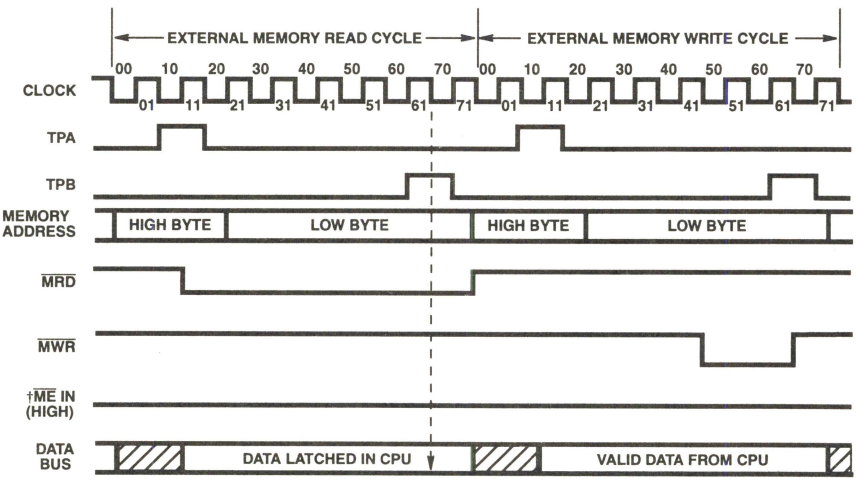


NOTE:

8. $\overline{ME}$ has a minimum setup and hold time with respect to the beginning of clock 70. For a memory read operation, RAM data will appear on the data bus during the time $\overline{ME}$ is active after clock 31. The time shown can be longer, if for instance, a DMA out operation is performed on internal RAM data, to allow data enough time to be latched into an external device. The internal RAM is automatically deselected at the end of clock 71 independent of $\overline{ME}$.

† For CDP1805AC only.

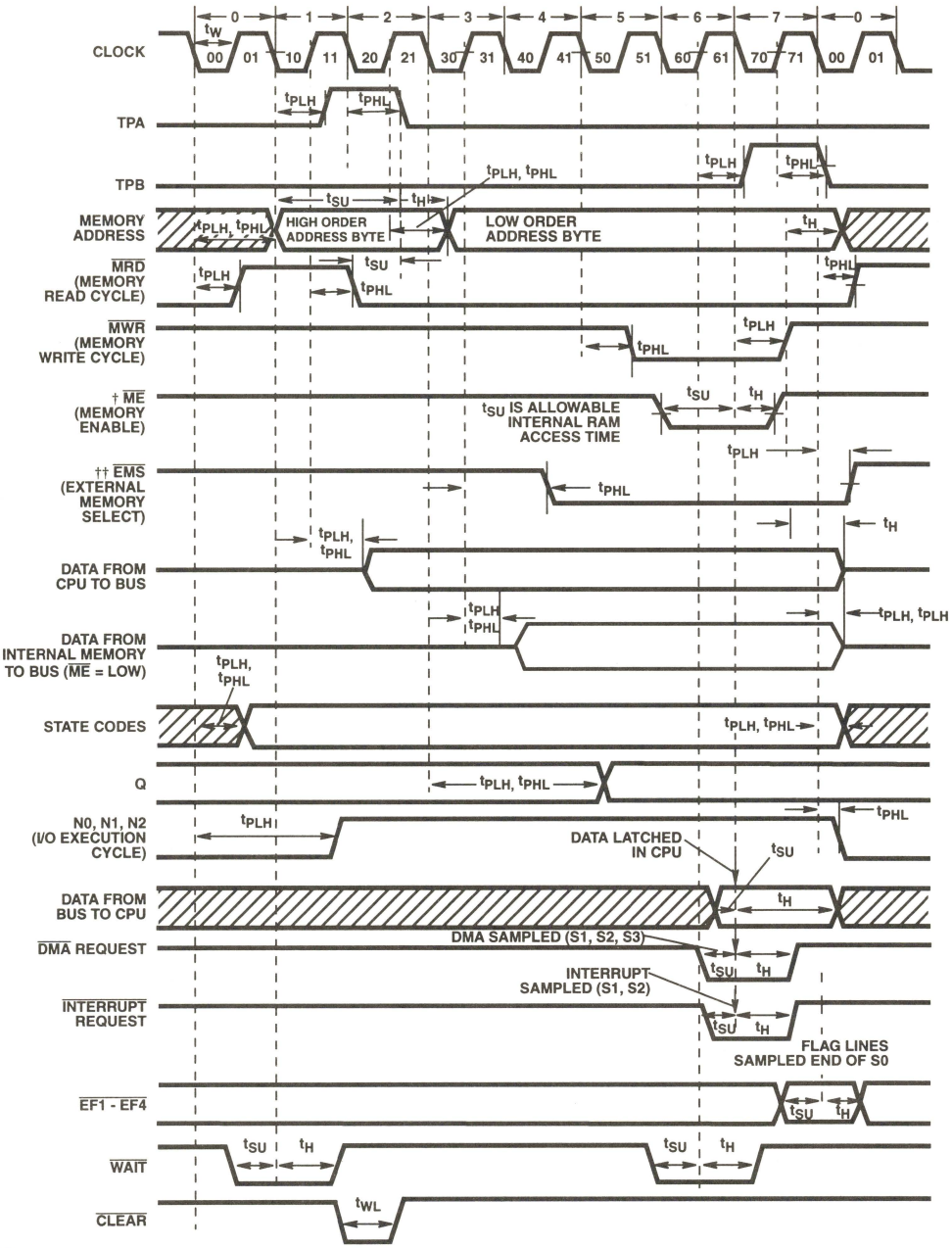
FIGURE 3. INTERNAL MEMORY OPERATION TIMING WAVEFORMS



NOTE:

† For CDP1805AC only.

FIGURE 4. EXTERNAL MEMORY OPERATION TIMING WAVEFORMS



NOTES:

† This Timing Diagram is used to show signal relationships only, and does not represent any specific machine cycle.
† All measurements are referenced to 50% point of the wave forms.
† Shaded areas indicate "don't care" or undefined state. Multiple transitions may occur during this period.
† For the run (RAM only) mode only.
†† For the run (RAM/ROM) mode only.

FIGURE 5. TIMING WAVEFORMS

Enhanced CDP1805AC and CDP1806AC Operation

Timing

Timing for the CDP1805AC and CDP1806AC is the same as the CDP1802 microprocessor series, with the following exceptions:

- 4.5 Clock Cycles Are Provided for Memory Access Instead of 5.
- Q Changes 1/2 Clock Cycle Earlier During the SEQ and REQ Instructions.
- Flag Lines ($\overline{EF1}$-$\overline{EF4}$) Are Sampled at the End of the S0 Cycle Instead of at the Beginning of the S1 Cycle.
- Pause Can Only Occur on the Low-To-High Transition of Either TPA or TPB, Instead of any Negative Clock Transition.

Special Features

Schmitt triggers are provided on all inputs, except $\overline{ME}$ and BUS 0-BUS 7, for maximum immunity from noise and slow signal transitions. A Schmitt Trigger in the oscillator section allows operation with an RC or crystal.

The CDP1802 Series LOAD mode is not retained. This mode ($\overline{WAIT}$, $\overline{CLEAR}$ = 0) is not allowed on the CDP1805AC and CDP1806AC.

A low power mode is provided, which is initiated via the IDLE instruction. In this mode all external signals, except the oscillator, are stopped on the low-to-high transition of TPB. All outputs remain in their previous states, $\overline{MRD}$ is set to a logic "1", and the data bus floats. The IDLE mode is exited by a DMA or INT condition. The INT includes both external interrupts and interrupts generated by the Counter/Timer. The only restrictions are that the Timer mode, which uses the TPA ÷ 32 clock source, and the underflow condition of the Pulse Width Measurement modes are not available to exit the IDLE mode.

Signal Descriptions

Bus 0 to Bus 7 (Data Bus)

8-Bit bidirectional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O) Lines

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices. The N-bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N Register. The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the $\overline{MRD}$ Signal:

$\overline{MRD}$ = V_{DD}: Input data from I/O to CPU and memory.

$\overline{MRD}$ = V_{SS}: Output data from Memory to I/O.

$\overline{EF1}$ to $\overline{EF4}$ (4 Flags)

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. The flag(s) are sampled at the end of every S0 cycle. $\overline{EF1}$ and $\overline{EF2}$ are also used for event counting and pulse width measurement in conjunction with the Counter/Timer.

$\overline{INTERRUPT}$, $\overline{DMA\text{-}IN}$, $\overline{DMA\text{-}OUT}$ (3 I/O Requests)

$\overline{DMA\text{-}IN}$ and $\overline{DMA\text{-}OUT}$ are sampled during TPB every S1, S2, and S3 cycle. $\overline{INTERRUPT}$ is sampled during TPB every S1 and S2 cycle.

Interrupt Action - X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable (MIE) is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action - Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and R(0) is incremented.

NOTE: In the event of concurrent DMA and INTERRUPT requests, DMA-IN has priority followed by DMA-OUT and then INTERRUPT. (The interrupt request is not internally latched and must be held true after DMA).

SC0, SC1, (2 State Code Lines)

These outputs indicate that the CPU is: 1) fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA.

STATE TYPE	STATE CODE LINES	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

NOTE: H = V_{DD}, L = V_{SS}.

TPA, TPB (2 Timing Pulses)

Positive pulses that occurrence in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the high-order byte of the multiplexed 16-bit memory address.

MA0 to MA7 (8 Memory Address Lines)

In each cycle, the higher-order byte of a 16-bit memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines 1/2 clock after the termination of TPA.

$\overline{MWR}$ (Write Pulse)

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

$\overline{MRD}$ (Read Level)

A low level on $\overline{MRD}$ indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory and to indicate the direction of data transfer during an I/O instruction.

Q

Single bit output from the CPU which can be set or reset, under program control. During SEQ and REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB. The Q line can also be controlled by the Counter/Timer underflow via the Enable Toggle Q instruction.

The Enable Toggle Q command connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q line changes state. This command is cleared by a LOAD COUNTER (LDC) instruction with the Counter/Timer stopped, a CPU reset, or a BRANCH COUNTER INTERRUPT (BCI) instruction with the counter interrupt flip-flop set.

Clock

Input for externally generated single-phase clock. The maximum clock frequency is 5MHz at V_{DD} = 5V. The clock is counted down internally to 8 clock pulses per machine cycle.

$\overline{XTAL}$

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized.

$\overline{WAIT}$, $\overline{CLEAR}$ (2 Control Lines)

Provide four control modes as listed in the following truth table:

$\overline{CLEAR}$	$\overline{WAIT}$	MODE
L	L	Not Allowed
L	H	Reset
H	L	Pause
H	H	Run

$\overline{ME}$ (Memory Enable CDP1805AC Only)

This active low input is used to select or deselect the internal RAM. It must be active prior to clock 70 for an internal RAM access to take place. Internal RAM data will appear on the data bus during the time that $\overline{ME}$ is active (after clock 31). Thus, if this data is to be latched into an external device (i.e., during an OUTPUT instruction or DMA OUT cycle), $\overline{ME}$ should be wide enough to provide enough time for valid data to be latched. The internal RAM is automatically deselected after clock 71. $\overline{ME}$ is ineffective when $\overline{MRD} \bullet \overline{MWR} = 1$.

The internal RAM is not internally mask-decoded. Decoding of the starting address is performed externally, and may reside in any 64-byte block of memory.

V_{DD} (CDP1806AC Only)

This input replaces the $\overline{ME}$ signal of the CDP1805AC and must be connected to the positive power supply.

V_{DD}, V_{SS}, (Power Levels)

V_{SS} is the most negative supply voltage terminal and is normally connected to ground. V_{DD} is the positive supply voltage terminal. All outputs swing from V_{SS} to V_{DD}. The recommended input voltage swing is from V_{SS} to V_{DD}.

Architecture

Figure 2 shows a block diagram of the CDP1805AC and CDP1806AC. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following paths:

1. The external memory (multiplexed, higher-order byte first on to 8 memory address lines).
2. The D register (either of the two bytes can be gated to D).
3. The increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.
4. To any other 16-bit scratch pad register in the array.

The four paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

Most instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second, and more if necessary, are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher order 4 bits of the instruction byte are loaded into the register and the lower order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. Designate one of the 16 registers in R to be acted upon during register operations.
2. Indicate to the I/O devices a command code or device-selection code for peripherals.
3. Indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions.
4. Indicate the value to be loaded into P to designate a new register to be used as the program counter R(P).
5. Indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R(0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table 1):

1. ALU operations.
2. Output instructions.
3. Input instructions.
4. Register to memory transfer.
5. Memory to register transfer.
6. Interrupt and subroutine handling.

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions ON and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F, and the RLDI instruction 68CN. During these instruction executions, the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the CDP1805AC and CDP1806AC architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

Data Registers

When registers in R are used to store bytes of data, instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters. The new RLDI, RLXA, RSXD, and RNX instructions also allow loading, storing, and exchanging the full 16-Bit contents of the R registers without affecting the D register. The new DBNZ instruction allows decrementing and branching-on-not-zero of any 16-Bit R register also without affecting the D register.

The Q Flip-Flop

An internal flip-flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. It can also be driven by the underflow output of the counter/timer The output of Q is also available as a microprocessor output.

REGISTER SUMMARY

D	8 Bits	Data Register (Accumulator)
DF	1-Bit	Data Flag (ALU Carry)
B	8 Bits	Auxiliary Holding Register
R	16 Bits	1 of 16 Scratch and Registers
P	4 Bits	Designates which Register is Program Counter
X	4 Bits	Designates which Register is Data Pointer
N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high nibble)
Q	1-Bit	Output Flip-Flop
CNTR	8-Bits	Counter/Timer
CH	8 Bits	Holds Counter Jam Value
MIE	1-Bit	Master Interrupt Enable
CIE	1-Bit	Counter Interrupt Enable
XIE	1-Bit	External Interrupt Enable
CIL	1-Bit	Counter Interrupt Latch

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initialized. When an interrupt request occurs and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction), the contents of the X and P registers are stored in the temporary Register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Master Interrupt Enable is automatically deactivated to inhibit further interrupts. The user's interrupt routine is now in control; the contents of T may be saved by means of a single SAV instruction (78) in the memory location pointed to by R(X) or the contents of T, D, and DF may be saved using a single DSAV instruction (6876). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with either a RET instruction (70) which permits further interrupts, or a DIS instruction (71), which disables further interrupts.

Interrupt Generation and Arbitration (See Figure 6)

Interrupt requests can be generated from the following sources:

1. Externally through the interrupt input (request not latched).
2. Internally due to Counter/Timer response (request is latched).
   a. On the transition from count $(01)_{16}$ to its next value (counter underflow).
   b. On the $\downarrow$ transition of $\overline{EF1}$ in pulse measurement mode 1.
   c. On the $\downarrow$ transition of $\overline{EF2}$ in pulse measurement mode 2.

For an interrupt to be serviced by the CPU, the appropriate Interrupt Enable flip-flops must be set. Thus, the External Interrupt Enable flip-flop must be set to service an external interrupt request, and the Counter Interrupt Enable flip-flop must be set to service an internal Counter/Timer interrupt request. In addition, the Master interrupt Enable flip-flop (as used in the CDP1802) must be set to service either type of request. All 3 flip-flops are initially enabled with the application of a hardware reset, and, can be selectively enabled or disabled with software: CIE, CID instructions for the CIE flip-flop; XIE, XID instructions for the XIE flip-flop; RET, DIS instructions for the MIE flip flop.

Short branch instructions on Counter Interrupt (BCI) and External Interrupt (BXI) can be placed in the user's interrupt service routine to provide a means of identifying and prioritizing the interrupt source. Note, however, that since the External Interrupt request is not latched, it must remain active until the short branch is executed if this priority arbitration scheme is used.

Interrupt requests can also be polled if automatic interrupt service is not desired (MIE = 0). With the Counter Interrupt and External Interrupt short branch instructions, the branch will be taken if an interrupt request is pending, regardless of the state of any of the 3 Interrupt Enable flip-flops. The latched counter interrupt request signal will be reset when the branch is taken, when the CPU is reset, or with a LDC instruction with the Counter stopped. Note, that exiting a counter-initiated interrupt routine without resetting the counter-interrupt latch will result in immediately reentering the interrupt routine.

Counter/Timer and Controls (See Figure 7)

This logic consists of a presettable 8-Bit down-counter (Modulo N type), and a conditional divide-by-32 prescaler. After counting down to $(01)_{16}$the counter returns to its initial value at the next count and sets the Counter Interrupt Latch. It will continue decrementing on subsequent counts. If the counter is preset to $(00)_{16}$ full 256 counts will occur.

During a Load Counter instruction (LDC) if the counter was stopped with a STPC Instruction, the counter and its holding register (CH) are loaded with the value in the D Register and any previous counter interrupt is cleared. If the LDC is executed when the counter is running, the contents of the D Register are loaded into the holding register (CH) only and any previous counter interrupt is not cleared. (LDC RESETS the Counter Interrupt Latch only when the Counter is stopped). After counting down to $(01)_{16}$ the next count will load the new initial value into the counter, set the Counter Interrupt Latch, and operation will continue.

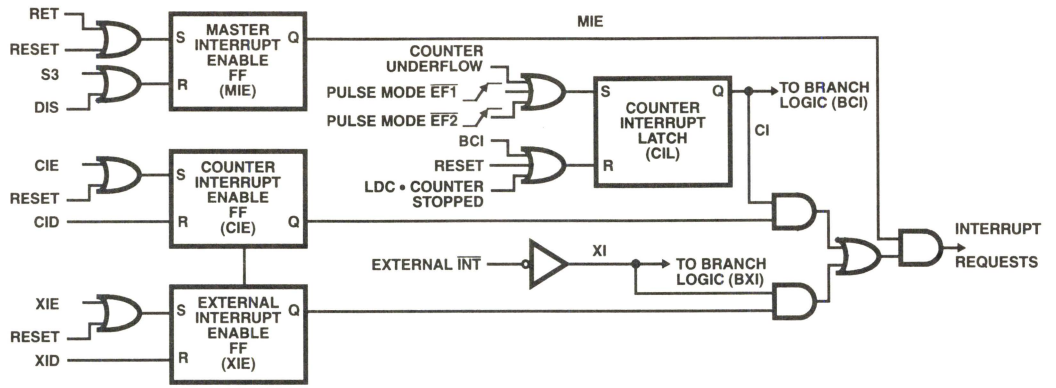


FIGURE 6. INTERRUPT LOGIC CONTROL DIAGRAM

The Counter/Timer has the following five programmable modes:

1. Event Counter 1: Input to counter is connected to the $\overline{EF1}$ terminal. The high-to-low transition decrements the counter.
2. Event Counter 2: Input to counter is connected to the $\overline{EF2}$ terminal. The high-to-low transition decrements the counter.
3. Timer: Input to counter is from the divide by 32 prescaler clocked by TPA. The prescaler is decremented on the low-to-high transition of TPA. The divide by 32 prescaler is reset when the counter is in a mode other than the Timer mode, system RESET, or stopped by a STPC.
4. Pulse Duration Measurement 1: Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{EF1}$ terminal (gate input) is low. On the transition of $\overline{EF1}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but counting will continue.
5. Pulse Duration Measurement 2: Operation is identical to Pulse Duration Measurement 1, except $\overline{EF2}$ is used as the gate input.

The modes can be changed without affecting the stored count.

Those modes which use $\overline{EF1}$ and $\overline{EF2}$ terminals as inputs do not exclude testing these flags for branch instructions.

The Stop Counter (STPC) instruction clears the counter mode and stops counting. The STPC instruction should be executed prior to a GEC instruction, if the counter is in the Event Counter Mode 1 or 2.

In addition to the five programmable modes, the Decrement Counter instruction (DTC) enables the user to count in software. In order to avoid conflict with counting done in the other modes, the instruction should be used only after the mode has been cleared by a Stop Counter instruction.

The Enable Toggle Q instruction (ETQ) connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q output changes state. This action is independent of the counter mode and the Interrupt Enable flip-flops. The Enable Toggle Q condition is cleared by an LDC with the Counter/Timer stopped, system Reset, or a BCI with CI = 1.

NOTE: SEQ and REQ instructions are independent of ETQ, they can SET or RESET Q while the Counter is running.

On-Board Clock (See Figure 8, Figure 9 and Figure 10)

Clock circuits may use either an external crystal or an RC network.

A typical crystal oscillator circuit is shown in Figure 8. The crystal is connected between terminals 1 and 39 (CLOCK and $\overline{XTAL}$) in parallel with a resistance, RF (1mΩ typ). Frequency trimming capacitors, C_{IN} and C_{OUT}, may be required at terminals 1 and 39. For additional information on crystal oscillators, see ICAN-6565.

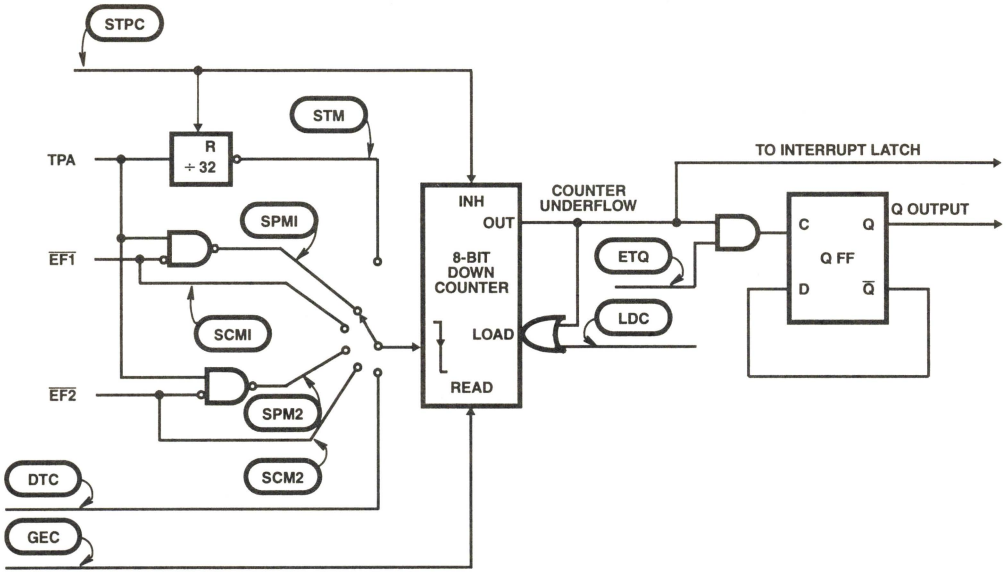
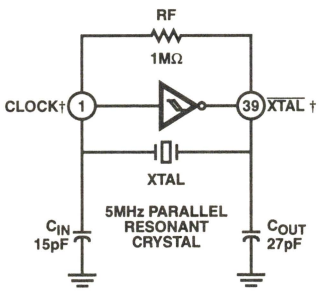


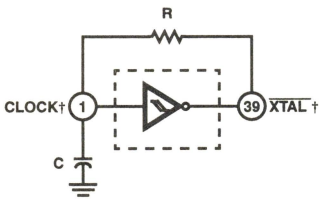
FIGURE 7. TIMER/COUNTER DIAGRAM

Because of the Schmitt Trigger input, an RC oscillator can be used as shown in Figure 9. The frequency is approximately 1/RC (see Figure 10).



†Pin numbers refer to 40 pin DIP.

FIGURE 8. TYPICAL 5MHz CRYSTAL OSCILLATOR



†Pin numbers refer to 40 pin DIP.

FIGURE 9. RC NETWORK FOR OSCILLATOR

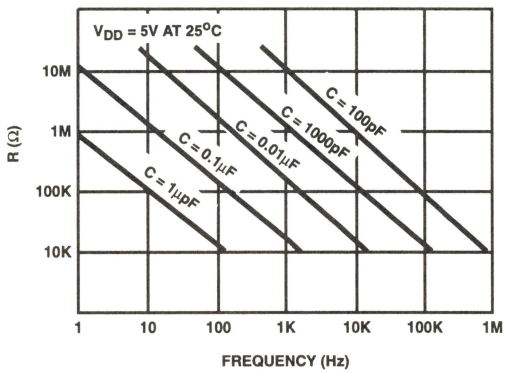


FIGURE 10. NOMINAL COMPONENT VALUES AS A FUNCTION OF FREQUENCY FOR THE RC OSCILLATOR

CONTROL MODES

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	Not Allowed
L	H	Reset
H	L	Pause
H	H	Run

The function of the modes are defined as follows:

Reset

The levels on the CDP1805A and CDP1806A external signal lines will asynchronously be forced by RESET to the following states:

Q = 0	SC1, SC0 = 0,1	BUS 0-7 = 0
MRD = 1	(EXECUTE)	MA0-7 = RO.1
TPB = 0	N0, N1, N2 = 0, 0, 0	TPA = 0
	$\overline{MWR}$ = 1	

Internal Changes Caused By RESET are:

I, N Instruction Register is cleared to 00. XIE and CIE are set to allow interrupts following initialize. CIL is cleared (any pending counter interrupt is cleared), counter is stopped, the counter mode is cleared, and ETQ is disabled.

Initialization Cycle

The first machine cycle following termination of RESET is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1 and the following additional changes occur:

1 → MIE

X, P → T (The old value of X, P will be put into T. This only has meaning following an orderly Reset with power applied).

X, P, RO ← 0 (X, P, and RO are cleared).

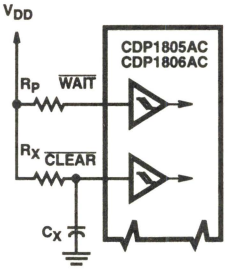
Interrupt and DMA servicing is suppressed during the initialization cycle. The next cycle is an S0 or an S2 but never an S1 or S3.The use of a 71 instruction followed by 00 at memory locations 0000 and 0001, may be used to reset MIE so as to preclude interrupts until ready for them.

Reset and Initialize Do Not Affect:

D (Accumulator)
DF
R1, R2, R3, R4, R5, R6, R7, R8, R9, FA, RB, RC, RD, RE, RF
CH (Counter Holding Register)
Counter (the counter is stopped but the value is unaffected)

Power-up Reset/Run Circuit

Power-up Reset/Run can be realized with the circuit shown in Figure 11.



THE RC TIME CONSTANT SHOULD BE GREATER THAN THE OSCILLATOR START-UP TIME (TYPICALLY 20ms)

FIGURE 11. RESET/RUN DIAGRAM

Pause

Pause is a low power mode which stops the internal CPU timing generator and freezes the state of the processor. The CPU may be held in the Pause mode indefinitely. Hardware pause can occur at two points in a machine cycle, on the low-to-high transition of either TPA or TPB. A TPB pause can also be initiated by software with the execution of an IDLE instruction. In the pause mode, the oscillator continues to run but subsequent clock transitions are ignored. TPA and TPB remain at their previous state (see Figure 12).

Pause is entered from RUN by dropping WAIT low. Appropriate Setup and Hold times must be met.

If Pause is entered while in the event counter mode, the appropriate Flag transition will continue to decrement the counter.

Hardware-initiated pause is exited to RUN by raising the Wait line high. Pause entered with an IDLE instruction requires DMA, INTERRUPT or RESET to resume execution.

Run

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation at the point it left off. If paused at TPA, it will resume on the next high-to-low clock transition, while if paused at TPB, it will resume on the next low-to-high clock transition (see Figure 12). When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

Schmitt Trigger Inputs

All inputs except BUS 0-BUS 7 and ME contain a Schmitt Trigger circuit, which is especially useful on the CLEAR input as a power-up RESET (see Figure 11) and the CLOCK input (see Figure 8 and Figure 9).

State Transitions

The CDP1805A and CDP1806A state transitions are shown in Figure 13. Each machine cycle requires the same period of time, 8 clock pulses, except the initialization cycle (INIT) which requires 9 clock pulses. Reset is asynchronous and can be forced at any time.

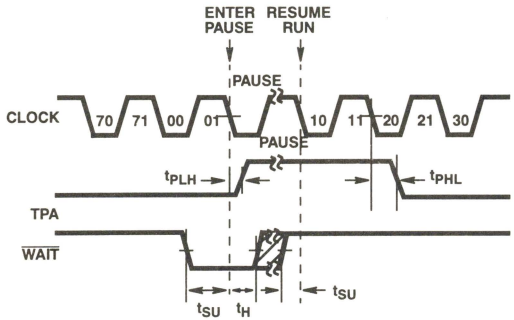
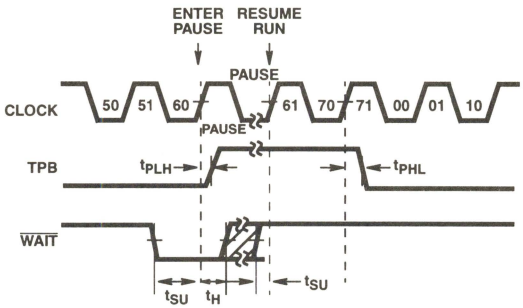


FIGURE 12A. TPA PAUSE TIMING



NOTE:

9. Pause (in clock waveform) while represented here as one clock cycle in duration, could be infinitely long.

FIGURE 12B. TPB PAUSE TIMING

FIGURE 12. PAUSE MODE TIMING WAVEFORMS

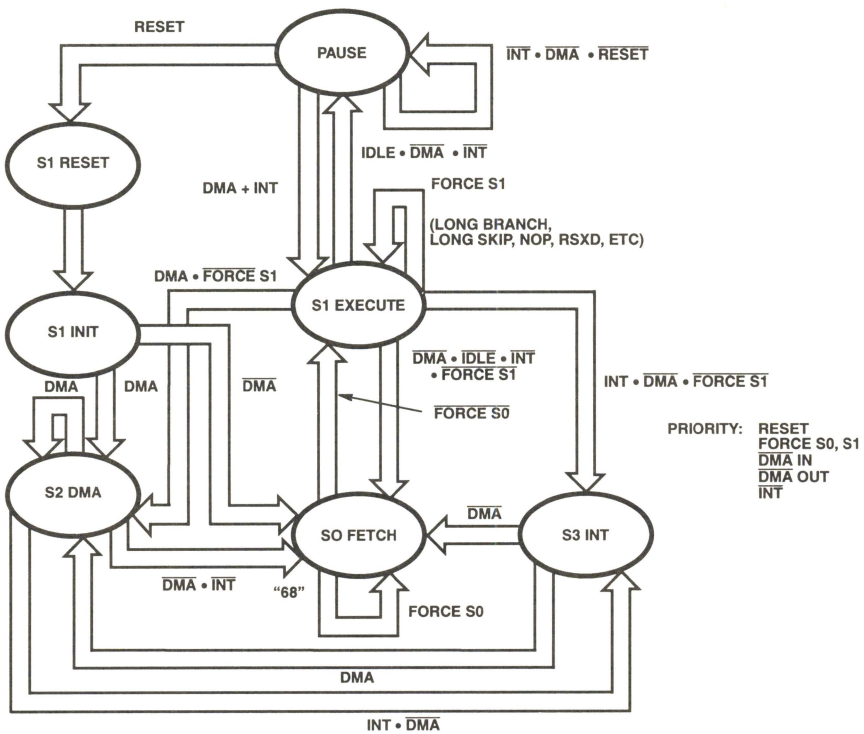


FIGURE 13. STATE TRANSITION DIAGRAM

Instruction Set

The CDP1805AC and CDP1806AC instruction summary is given in Table 1. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers, bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where

W = N or X, or P

R(W).0: Lower-order byte of R(W)

R(W).1: Higher-order byte of R(W)

Operation Notation

M (R(N)) → D; R(N) + 1 → R(N)

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

TABLE 1. INSTRUCTION SUMMARY (SEE NOTES)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE				
LOAD IMMEDIATE	2	LDI	F8	M(R(P)) → D; R(P) + 1 → R(P)
REGISTER LOAD IMMEDIATE	5	RLDI	68CN (Note 10)	M(R(P)) → R(N).1; M(R(P)) + 1 → R(N).0; R(P) + 2 → R(P)
LOAD VIA N	2	LDN	0N	M(R(N)) → D; FOR N NOT 0
LOAD ADVANCE	2	LDA	4N	M(R(N)) → D; R(N) + 1 → R(N)
LOAD VIA X	2	LDX	F0	M(R(X)) → D
LOAD VIA X AND ADVANCE	2	LDXA	72	M(R(X)) → D; R(X) + 1 → R(X)
REGISTER LOAD VIA X AND ADVANCE	5	RLXA	686N (Note 10)	M(R(X)) → R(N).1; M(R(X) + 1) → R(N).0; R(X)) + 2 → R(X)
STORE VIA N	2	STR	5N	D → M(RN))
STORE VIA X AND DECREMENT	2	STXD	73	D → M(R(X)); R(X) - 1 → R(X)
REGISTER STORE VIA X AND DECREMENT	5	RSXD	68AN (Note 10)	R(N).0 → M(R(X)); R(N).1 → M(R)(X) - 1); R(X) - 2 → R (X)
REGISTER OPERATIONS				
INCREMENT REG N	2	INC	1N	R(N) + 1 → R(N)
DECREMENT REG N	2	DEC	2N	R(N) - 1 → R(N)
DECREMENT REG N AND LONG BRANCH IF NOT EQUAL 0	5	DBNZ	682N	R(N) - 1 → R(N); IF R(N) NOT 0, M(R(P)) → R(P).1, M(R(P) + 1) → R(P).0, ELSE R(P) + 2 → R(P)
INCREMENT REG X	2	IRX	60	R(X) + 1 → R(X)
GET LOW REG N	2	GLO	8N	R(N).0 → D
PUT LOW REG N	2	PLO	AN	D → R(N).0
GET HIGH REG N	2	GHI	9N	R(N).1 → D
PUT HIGH REG N	2	PHI	BN	D → R(N).1
REGISTER N TO REGISTER X COPY	4	RNX	68BN (Note 10)	R(N) → R(X)
LOGIC OPERATIONS (Note 19)				
OR	2	OR	F1	M(R(X)) OR D → D
OR IMMEDIATE	2	ORI	F9	M(R(P)) OR D → D; R(P) + 1 → R(P)
EXCLUSIVE OR	2	XOR	F3	M(R(X)) XOR D → D
EXCLUSIVE OR IMMEDIATE	2	XRI	FB	M(R(P)) XOR D → D; R(P) + 1 → R(P)
AND	2	AND	F2	M(R(X)) AND D → D

TABLE 1. INSTRUCTION SUMMARY (SEE NOTES) **(Continued)**

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
AND IMMEDIATE	2	ANI	FA	M(R(P)) AND D → D; R(P) + 1 → R(P)
SHIFT RIGHT	2	SHR	F6	Shift D Right, LSB(D) → DF, 0 → MSB(D)
SHIFT RIGHT WITH CARRY	2	SHRC	76 (Note 11)	Shift D Right, LSB(D) → DF, DF → MSB(D)
RING SHIFT RIGHT	2	RSHR	76 (Note 11)	SHIFT D RIGHT, LSB(D) → DF, DF → MSB(D)
SHIFT LEFT	2	SHL	FE	SHIFT D LEFT, MSB(D) → DF, 0 → LSB(D)
SHIFT LEFT WITH CARRY	2	SHLC	7E (Note 11)	SHIFT D LEFT, MSB(D) → DF, DF → LSB(D)
RING SHIFT LEFT	2	RSHL	7E (Note 11)	SHIFT D LEFT, MSB(D) → DF, DF → LSB(D)
ARITHMETIC OPERATIONS (Note 3)				
ADD	2	ADD	F4	M(R(X)) + D → DF, D
DECIMAL ADD	4	DADD	68F4	M(R(X)) + D → DF, D DECIMAL ADJUST → DF, D
ADD IMMEDIATE	2	ADI	FC	M(R(P)) + D → DF, D; R(P) + 1 → R(P)
DECIMAL ADD IMMEDIATE	4	DADI	68FC	M(R(P)) + D → DF, D; R(P) + 1 → R(P) DECIMAL ADJUST → DF, D
ADD WITH CARRY	2	ADC	74	M(R(X)) + D + DF → DF, D
DECIMAL ADD WITH CARRY	4	DADC	6874	M(R(X)) + D + DF → DF, D DECIMAL ADJUST → DF, D
ADD WITH CARRY, IMMEDIATE	2	ADCI	7C	M(R(P)) + D + DF → DF, D; R(P) + 1 → R(P)
DECIMAL ADD WITH CARRY, IMMEDIATE	4	DACI	687C	M(R(P)) + D + DF → DF, D; R(P) + 1 → R(P), DECIMAL ADJUST → DF, D
SUBTRACT D	2	SD	F5	M(R(X)) - D → DF, D
SUBTRACT D IMMEDIATE	2	SDI	FD	M(R(P)) - D → DF, D; R(P) + 1 → R(P)
SUBTRACT D WITH BORROW	2	SDB	75	M(R(X)) - D - (NOT DF) → DF, D
SUBTRACT D WITH BORROW, IMMEDIATE	2	SDBI	7D	M(R(P)) - D - (NOT DF) → DF, D; R(P) + 1 → R(P)
SUBTRACT MEMORY	2	SM	F7	D - M(R(X)) → DF, D
DECIMAL SUBTRACT MEMORY	4	DSM	68F7	D - M(R(X)) → DF, D; DECIMAL ADJUST → DF, D
SUBTRACT MEMORY IMMEDIATE	2	SMI	FF	D - M(R(P)) → DF, D; R(P) + 1 → R(P)
DECIMAL SUBTRACT MEMORY, IMMEDIATE	4	DSMI	68FF	D - M(R(P)) → DF, D; R(P) + 1 → R(P), DECIMAL ADJUST → DF, D
SUBTRACT MEMORY WITH BORROW	2	SMB	77	D - M(R(X)) - (NOT DF) → DF, D
DECIMAL SUBTRACT MEMORY WITH BORROW	4	DSMB	6877	D - M(R(X)) - (NOT DF) → DF, D; DECIMAL ADJUST → DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	2	SMBI	7F	D - M(R(P)) - (NOT DF) → DF, D; R(P) + 1 → R(P)

TABLE 1. INSTRUCTION SUMMARY (SEE NOTES) **(Continued)**

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
DECIMAL SUBTRACT MEMORY WITH BORROW, IMMEDIATE	4	DSBI	687F	D - M(R(P)) - (NOT DF) → DF, D R(P) + 1 → R(P) DECIMAL ADJUST → DF, D
BRANCH INSTRUCTIONS - SHORT BRANCH				
SHORT BRANCH	2	BR	30	M(R(P)) → R(P).0
NO SHORT BRANCH (See SKP)	2	NBR	38 (Note 11)	R(P) + 1 → R(P)
SHORT BRANCH IF D = 0	2	BZ	32	IF D = 0, M(R(P)) → R(P).0 ELSE R(P) + 1 → R(P)
SHORT BRANCH IF D NOT 0	2	BNZ	3A	IF D NOT 0, M(R(P)) → R(P).0 ELSE R(P) + 1 → R(P)
SHORT BRANCH IF DF = 1	2	BDF	33 (Note 11)	IF DF = 1, M(R(P)) → R(P).0 ELSE R(P) + 1 → R(P)
SHORT BRANCH IF POS OR ZERO	2	BPZ	33 (Note 11)	IF DF = 1, M(R(P)) → R(P).0 ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EQUAL OR GREATER	2	BGE	33 (Note 11)	IF DF = 1, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF DF = 0	2	BNF	3B (Note 11)	IF D = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF MINUS	2	BM	3B (Note 11)	IF D = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF LESS	2	BL	3B (Note 11)	IF D = 0, M(R(P)) → R(P).0, ELSE R(P) + 1 → R(P)
SHORT BRANCH IF Q = 1	2	BQ	31	IF Q = 1, M(R(P)) → R(P).0 ELSE R(P) + 1 → R(P)
SHORT BRANCH IF Q = 0	2	BNQ	39	IF Q = 0, M(R(P)) → R(P).0 ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF1 = 1 ($\overline{EF1} = V_{SS}$)	2	B1	34	IF EF1 = 1, M(R(P)) → R(P).0 ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF1 = 0 ($\overline{EF1} = V_{DD}$)	2	BN1	3C	IF EF1 = 0, M(R(P)) → R(P).0 ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF2 = 1 ($\overline{EF2} = V_{SS}$)	2	B2	35	IF EF2 = 1, M(R(P)) → R(P).0 ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF2 = 0 ($\overline{EF2} = V_{DD}$)	2	BN2	3D	IF EF2 = 0, M(R(P)) → R(P).0 ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF3 = 1 ($\overline{EF3} = V_{SS}$)	2	B3	36	IF EF3 = 1, M(R(P)) → R(P).0 ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF3 = 0 ($\overline{EF3} = V_{DD}$)	2	BN3	3E	IF EF3 = 0, M(R(P)) → R(P).0 ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF4 = 1 ($\overline{EF4} = V_{SS}$)	2	B4	37	IF EF4 = 1, M(R(P)) → R(P).0 ELSE R(P) + 1 → R(P)
SHORT BRANCH IF EF4 = 0 ($\overline{EF4} = V_{DD}$)	2	BN4	3F	IF EF4 = 0, M(R(P)) → R(P).0 ELSE R(P) + 1 → R(P)
SHORT BRANCH ON COUNTER INTERRUPT	3	BCI	683E (Note 12)	IF CI = 1, M(R(P)) → R(P).0; 0 → CI ELSE R(P) + 1 → R(P)
SHORT BRANCH ON EXTERNAL INTERRUPT	3	BXI	683F	IF XI = 1, M(R(P)) → R(P).0 ELSE R(P) + 1 → R(P)

TABLE 1. INSTRUCTION SUMMARY (SEE NOTES) **(Continued)**

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS - LONG BRANCH				
LONG BRANCH	3	LBR	C0	M(R(P)) → R(P).1, M(R(P) + 1) → R(P).0
NO LONG BRANCH (See LSKP)	3	NLBR	C8 (Note 11)	R(P) + 2 → R(P)
LONG BRANCH IF D = 0	3	LBZ	C2	IF D = 0, M(R(P)) → R(P).1 M(R(P) + 1) → R(P).0 ELSE R(P) + 2 → R(P)
LONG BRANCH IF D NOT 0	3	LBNZ	CA	IF D NOT 0, M(R(P)) → R(P).1 M(R(P) + 1) → R(P).0 ELSE R(P) + 2 → R(P)
LONG BRANCH IF DF = 1	3	LBDF	C3	IF DF = 1, M(R(P)) → R(P).1 M(R(P) + 1) → R(P).0 ELSE R(P) + 2 → R(P)
LONG BRANCH IF DF = 0	3	LBNF	CB	IF DF = 0, M(R(P)) → R(P).1 M(R(P) + 1) → R(P).0 ELSE R(P) + 2 → R(P)
LONG BRANCH IF Q = 1	3	LBQ	C1	IF Q = 1, M(R(P)) → R(P).1 M(R(P) + 1) → R(P).0 ELSE R(P) + 2 → R(P)
LONG BRANCH IF Q = 0	3	LBNQ	C9	IF Q = 0, M(R(P)) → R(P).1 M(R(P) + 1) → R(P).0 ELSE R(P) + 2 → R(P)
SKIP INSTRUCTIONS				
SHORT SKIP (See NBR)	2	SKP	38 (Note 11)	R(P) + 1 → R(P)
LONG SKIP (See NLBR)	3	LSKP	C8 (Note 11)	R(P) + 2 → R(P)
LONG SKIP IF D = 0	3	LSZ	CE	IF D = 0, R(P) + 2 → R(P) ELSE CONTINUE
LONG SKIP IF D NOT 0	3	LSNZ	C6	IF D NOT 0, R(P) + 2 → R(P) ELSE CONTINUE
LONG SKIP IF DF = 1	3	LSDF	CF	IF DF = 1, R(P) + 2 → R(P) ELSE CONTINUE
LONG SKIP IF DF = 0	3	LSNF	C7	IF DF = 0, R(P) + 2 → R(P) ELSE CONTINUE
LONG SKIP IF Q = 1	3	LSQ	CD	IF Q = 1, R(P) + 2 → R(P) ELSE CONTINUE
LONG SKIP IF Q = 0	3	LSNQ	C5	IF Q = 0, R(P) + 2 → R(P) ELSE CONTINUE
LONG SKIP IF MIE = 1	3	LSIE	CC	IF MIE = 1, R(P) + 2 → R(P) ELSE CONTINUE
CONTROL INSTRUCTIONS				
IDLE	2	IDL	00 (Note 14)	STOP ON TPB; WAIT FOR DMA OR INTERRUPT; BUS FLOATS
NO OPERATION	3	NOP	C4	CONTINUE
SET P	2	SEP	DN	N → P
SET X	2	SEX	EN	N → X

TABLE 1. INSTRUCTION SUMMARY (SEE NOTES) **(Continued)**

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
SET Q	2	SEQ	7B	1 → Q
RESET Q	2	REQ	7A	0 → Q
PUSH X, P TO STACK	2	MARK	79	(X, P) → T; (X, P) → M(R(2)), THEN P → X; R(2) → 1→ R(2)
TIMER/COUNTER INSTRUCTIONS				
LOAD COUNTER	3	LDC	6806 (Note 15)	CNTR STOPPED: D → CH, CNTR; 0 → CI. CNTR RUNNING; D → CH
GET COUNTER	3	GEC	6808	CNTR → D
STOP COUNTER	3	STPC	6800	STOP CNTR CLOCK; 0 → ÷ 32 PRESCALER
DECREMENT TIMER/COUNTER	3	DTC	6801	CNTR - 1 → CNTR
SET TIMER MODE AND START	3	STM	6807	TPA ÷ 32 → CNTR
SET COUNTER MODE 1 AND START	3	SCM1	6805	$\overline{EF1}$ → CNTR CLOCK
SET COUNTER MODE 2 AND START	3	SCM2	6803	$\overline{EF2}$ → CNTR CLOCK
SET PULSE WIDTH MODE 1 AND START	3	SPM1	6804	TPA.$\overline{EF1}$ → CNTR CLOCK; $\overline{EF1}$ ↓ STOPS COUNT
SET PULSE WIDTH MODE 2 AND START	3	SPM2	6802	TPA.EF2 → CNTR CLOCK; $\overline{EF2}$ ↓ STOPS COUNT
ENABLE TOGGLE Q	3	ETQ	6809 (Note 15)	IF CNTR = 01 • NEXT CNTR CLOCK ↓ ; $\overline{Q}$ → Q
INTERRUPT CONTROL				
EXTERNAL INTERRUPT ENABLE	3	XIE	680A	1 → XIE
EXTERNAL INTERRUPT DISABLE	3	XID	680B	0 → XIE
COUNTER INTERRUPT ENABLE	3	CIE	680C	I → CIE
COUNTER INTERRUPT DISABLE	3	CID	680D	0 → CIE
RETURN	2	RET	70	M(R(X)) → X, P; R(X) + 1 → R(X); 1 → MIE
DISABLE	2	DIS	71	M(R(X) → X, P; R(X) + 1 → R(X); 0 → MIE
SAVE	2	SAV	78	T → M(R(X))
SAVE T, D, DF	6	DSAV	6876 (Note 10)	R(X) - 1 → R(X), T → M(R(X)), R(X) - 1 → R(X), D → M (R(X)), R(X) - 1 → R(X), SHIFT D RIGHT WITH CARRY, D → M(R(X))
INPUT-OUTPUT BYTE TRANSFER				
OUTPUT 1	2	OUT 1	61	M(R(X)) → BUS; R(X) + 1 → R(X) N LINES = 1
OUTPUT 2	2	OUT 2	62	M(R(X)) → BUS; R(X) + 1 → R(X) N LINES = 2
OUTPUT 3	2	OUT 3	63	M(R(X)) → BUS; R(X) + 1 → R(X) N LINES = 3
OUTPUT 4	2	OUT 4	64	M(R(X)) → BUS; R(X) + 1 → R(X) N LINES = 4
OUTPUT 5	2	OUT 5	65	M(R(X)) → BUS; R(X) + 1 → R(X) N LINES = 5

TABLE 1. INSTRUCTION SUMMARY (SEE NOTES) **(Continued)**

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
OUTPUT 6	2	OUT 6	66	M(R(X)) → BUS; R(X) + 1 → R(X) N LINES = 6
OUTPUT 7	2	OUT 7	67	M(R(X)) → BUS; R(X) + 1 → R(X) N LINES = 7
INPUT 1	2	INP 1	69	BUS → M(R(X)); BUS → D N LINES = 1
INPUT 2	2	INP 2	6A	BUS → M(R(X)); BUS → D N LINES = 2
INPUT 3	2	INP 3	6B	BUS → M(R(X)); BUS → D N LINES = 3
INPUT 4	2	INP 4	6C	BUS → M(R(X)); BUS → D N LINES = 4
INPUT 5	2	INP 5	6D	BUS → M(R(X)); BUS → D N LINES = 5
INPUT 6	2	INP 6	6E	BUS → M(R(X)); BUS → D N LINES = 6
INPUT 7	2	INP 7	6F	BUS → M(R(X)); BUS → D N LINES = 7
CALL AND RETURN				
STANDARD CALL	10	SCAL	688N (Note 10)	R(N).0 → M(R(X)); R(N).1 → M(R(X) - 1); R(X) - 2 → R(X); R(P) → R(N); THEN M(R(N)) → R(P).1; M(R(N) + 1) → R(P).0; R(N) + 2 → R(N)
STANDARD RETURN	8	SRET	689N (Note 10)	R(N) → R(P); M(R(X) + 1) → R(N).1; M(R(X) + 2) → R(N).0; R(X) + 2 → R(X)

NOTES:

10. Previous contents of T register are destroyed during instruction execution.
11. This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.
12. ETQ cleared by LDC with the Counter/Timer stopped, reset of CPU, or BCI • (CI = 1).
13. CI = Counter Interrupt, XI = External Interrupt.
14. An IDLE instruction initiates an S1 cycle. All external signals, except the oscillator, are stopped on the low-to-high transition of TPB. All outputs remain in their previous states, $\overline{MRD}$, $\overline{MWR}$, are set to a logic '1' and the data bus floats. The processor will continue to IDLE until an I/O request (INTERRUPT, DMA-IN, or DMA-OUT) is activated. When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and the normal operation is resumed. (To respond to an INTERRUPT during an IDLE, MIE and either CIE or XIE must be enabled).
15. Long-Branch, Long-Skip and No Op instructions require three cycles to complete (1 fetch + 2 execute).

    Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

    The long branch instruction can:

    a. Branch unconditionally
    b. Test for D = 0 or D ≠ 0
    c. Test for DF = 0 or DF = 1
    d. Test for Q = 0 or Q = 1
    e. Effect an unconditional no branch

    If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

    If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

16. The short-branch instructions are two or three bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address, except for the branches on interrupt. For those, the first two bytes specify the condition to be tested and the third byte specifies the branching address.

    The short branch instruction can:

    a. Branch unconditionally
    b. Test for D = 0 or D ≠ 0
    c. Test for DF = 0 or DF = 1
    d. Test for Q = 0 or Q = 1
    e. Test the status (1 or 0) of the four EF flags
    f. Effect an unconditional no branch
    g. Test for counter or external interrupts (BCI, BXI)

    If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch within the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR).

17. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

    The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional No-Branch Instruction (NBR) except that the skipped-over byte is not considered part of the program.

    The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

    They can:

    a. Skip unconditionally
    b. Test for D = 0 or D ≠ 0
    c. Test for DF = 0 or DF = 1
    d. Test for Q = 0 or Q = 1
    e. Test for MIE = 1

    If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus, two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

18. Instruction 6800 through 68FF take a minimum of 3 machine cycles and up to a maximum of 10 machine cycles. In all cases, the first two cycles are fetches and subsequent cycles are executes. The first byte (68) of these two-byte op codes is used to generate the second fetch, the second byte is then interpreted differently than the same code without the 68 prefix. DMA and INT requests are not serviced until the end of the last execute cycle.

19. Arithmetic Operations:

    The arithmetic and shift operations are the only instructions that can alter the content of DF. The syntax '(NOT DF)' denotes the subtraction of the borrow.

    Binary Operations:

    After an ADD instruction

    DF = 1 denotes a carry has occurred. Result is greater than FF_{16}.

    DF = 0 denotes a carry has not occurred.

    After a SUBTRACT instruction

    DF = 1 denotes no borrow. D is a true positive number.

    DF = 0 denotes a borrow. D is in two's complement form.

    Binary Coded Decimal Operations:

    After a BCD ADD instruction

    DF = 1 denotes a carry has occurred. Result is greater than 99_{10}.

    DF = 0 denotes a carry has not occurred.

    After a BCD SUBTRACT instruction

    DF = 1 denotes no borrow. D is a true positive decimal number.

    Example

    ```
    99      D
    -88     M(R(X))
    11      D          DF = 1
    ```

    DF = 0 denotes a borrow. D is in ten's complement form.

    Example

    ```
    88      D
    -99     M(R(X))
    89      D          DF = 0
    ```

    89 is the ten's complement of 11, which is the correct answer (with a minus value denoted by DF = 0).

TABLE 2. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES
S1	RESET			0 → Q, I, N, COUNTER, PRESCALER, CIL; 1 → CIE, XIE	00	UNDE-FINED	1	1	0
S1	INITIALIZE, NOT PROGRAMMER ACCESSIBLE			X, P → T THEN 0 → X, P; 1 → MIE, 0000 → R0	00 (Note 20)	UNDE-FINED	1	1	0
S0	FETCH			MRP → I, N; RP + 1 → RP	MRP	RP	0	1	0
S1	0	0	IDL	STOP AT TPB WAIT FOR DMA OR INT	HIGH Z	RO	1	1	0
S1	0	1-F	LDN	MRN → D	MRN	RN	0	1	0
S1	1	0-F	INC	RN + 1 → RN	HIGH Z	RN	1	1	0
S1	2	0-F	DEC	RN - 1 → RN	HIGH Z	RN	1	1	0
S1	3	0-F	SHORT BRANCH	TAKEN: MRP → RP.0 NOT TAKEN: RP + 1 → RP	MRP	RP	0	1	0
S1	4	0-F	LDA	MRN → D; RN + 1 → RN	MRN	RN	0	1	0
S1	5	0-F	STR	D → MRN	D	RN	1	0	0
S1	6	0	IRX	RX + 1 → RX	MRX	RX	1	1	0
S1	6	1	OUT 1	MRX → BUS; RX + 1 → RX	MRX	RX	0	1	1
S1	6	2	OUT 2	MRX → BUS; RX + 1 → RX	MRX	RX	0	1	2
S1	6	3	OUT 3	MRX → BUS; RX + 1 → RX	MRX	RX	0	1	3
S1	6	4	OUT 4	MRX → BUS; RX + 1 → RX	MRX	RX	0	1	4
S1	6	5	OUT 5	MRX → BUS; RX + 1 → RX	MRX	RX	0	1	5
S1	6	6	OUT 6	MRX → BUS; RX + 1 → RX	MRX	RX	0	1	6
S1	6	7	OUT 7	MRX → BUS; RX + 1 → RX	MRX	RX	0	1	7
S1	6	9	INP 1	BUS → MRX, D	DATA FROM I/O DEVICE	RX	1	0	1
S1	6	A	INP 2	BUS → MRX, D	DATA FROM I/O DEVICE	RX	1	0	2
S1	6	B	INP 3	BUS → MRX, D	DATA FROM I/O DEVICE	RX	1	0	3
S1	6	C	INP 4	BUS → MRX, D	DATA FROM I/O DEVICE	RX	1	0	4
S1	6	D	INP 5	BUS → MRX, D	DATA FROM I/O DEVICE	RX	1	0	5

TABLE 2. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Continued)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES
S1	6	E	INP 6	BUS → MRX, D	DATA FROM I/O DEVICE	RX	1	0	6
S1	6	F	INP 7	BUS → MRX, D	DATA FROM I/O DEVICE	RX	1	0	7
S1	7	0	RET	MRX → X, P; RX + 1 → RX 1 → MIE	MRX	RX	0	1	0
S1	7	1	DIS	MRX → X, P; RX + 1 → RX 0 → MIE	MRX	RX	0	1	0
S1	7	2	LDXA	MRX → D; RX + 1 → RX	MRX	RX	0	1	0
S1	7	3	STXD	D → MRX; RX - 1 → RX	D	RX	1	0	0
S1	7	4	ADC	MRX + D + DF → DF, D	MRX	RX	0	1	0
S1	7	5	SDB	MRX - D - DFN → DF, D	MRX	RX	0	1	0
S1	7	6	SHRC	LSB(D) → DF; DF → MSB(D)	HIGH Z	RX	1	1	0
S1	7	7	SMB	D - MRX - DFN → DF, D	MRX	RX	0	1	0
S1	7	8	SAV	T → MRX	T	RX	1	0	0
S1	7	9	MARK	X, P → T, MR2; P → X R2 - 1 → R2	T	R2	1	0	0
S1	7	A	REQ	0 → Q	HIGH Z	RP	1	1	0
S1	7	B	SEQ	1 → Q	HIGH Z	RP	1	1	0
S1	7	C	ADCI	MRP + D + DF → DF, D; RP + 1	MRP	RP	0	1	0
S1	7	D	SDBI	MRP - D - DFN → DF, D; RP + 1	MRP	RP	0	1	0
S1	7	E	SHLC	MSB(D) → DF; DF → LSB D	HIGH Z	RP	1	1	0
S1	7	F	SMBI	D - MRP - DFN → DF, D; RP + 1	MRP	RP	0	1	0
S1	8	0-F	GLO	RN.0 → D	RN.0	RN	1	1	0
S1	9	0-F	GHI	RN.1 → D	RN.1	RN	1	1	0
S1	A	0-F	PLO	D → RN.0	D	RN	1	1	0
S1	B	0-F	PHI	D → RN.1	D	RN	1	1	0
S1#1	C	0-3, 8-B	LONG BRANCH	TAKEN: MRP → B; RP + 1 → RP	MRP	RP	0	1	0
#2	C	0-3, 8-B	LONG BRANCH	TAKEN: B → RP.1; MRP → RP.0	M(RP + 1)	RP + 1	0	1	0
S1#1	C	0-3, 8-B	LONG BRANCH	NOT TAKEN RP + 1 → RP	MRP	RP	0	1	0
#2	C	0-3, 8-B	LONG BRANCH	NOT TAKEN RP + 1 → RP	M(RP + 1)	RP + 1	0	1	0
S1#1	C	5	LONG SKIP	TAKEN: RP + 1 → RP	MRP	RP	0	1	0
#2	C	6	LONG SKIP	TAKEN: RP + 1 → RP	M(RP + 1)	RP + 1	0	1	0

TABLE 2. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Continued)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES
#2	C	7	LONG SKIP	TAKEN: RP + 1 → RP	M(RP + 1)	RP + 1	0	1	0
S1#1	C	C	LONG SKIP	NOT TAKEN: NO OPERATION	MRP	RP	0	1	0
S1#1	C	D	LONG SKIP	NOT TAKEN: NO OPERATION	MRP	RP	0	1	0
#2	C	E	LONG SKIP	NOT TAKEN: NO OPERATION	M(RP + 1)	RP + 1	0	1	0
S1#1	C	F	LONG SKIP	NOT TAKEN: NO OPERATION	M(RP + 1)	RP + 1	0	1	0
S1#1	C	4	NOP	NO OPERATION	MRP	RP	0	1	0
#2	C	4	NOP	NO OPERATION	M(RP + 1)	RP + 1	0	1	0
S1	D	0-F	SEP	N → P	NN	RN	1	1	0
S1	E	0-F	SEX	N → X	NN	RN	1	1	0
S1	F	0	LDX	MRX → D	MRX	RX	0	1	0
S1	F	1	OR	MRX OR D → D	MRX	RX	0	1	0
S1	F	2	AND	MRX AND D → D	MRX	RX	0	1	0
S1	F	3	XOR	MRX XOR D → D	MRX	RX	0	1	0
S1	F	4	ADD	MRX + D → DF, D	MRX	RX	0	1	0
S1	F	5	SD	MRX - D → DF, D	MRX	RX	0	1	0
S1	F	7	SM	D - MRX → DF; D	MRX	RX	0	1	0
S1	F	6	SHR	LSB(D) → DF; 0 → MSB(D)	HIGH Z	RX	1	1	0
S1	F	8	LDI	MRP → D; RP + 1 → RP	MRP	RP	0	1	0
S1	F	9	ORI	MRP OR D → D; RP + 1 → RP	MRP	RP	0	1	0
S1	F	A	ANI	MRP AND D → D; RP + 1 → RP	MRP	RP	0	1	0
S1	F	B	XRI	MRP XOR D → D; RP + 1 → RP	MRP	RP	0	1	0
S1	F	C	ADI	MRP + D → DF, D; RP + 1 → RP	MRP	RP	0	1	0
S1	F	D	SDI	MRP - D → DF, D; RP + 1 → RP	MRP	RP	0	1	0
S1	F	F	SMI	D - MRP → DF, D; RP + 1 → RP	MRP	RP	0	1	0
S1	F	E	SHL	MSB(D) → DF; 0 → LSB(D)	HIGH Z	RP	1	1	0
S2	DMA IN	DMA IN	DMA IN	BUS → MR0; R0 + 1 → R0	DATA FROM I/O DEVICE	R0	1	0	0
S2	DMA OUT	DMA OUT	DMA OUT	MRO → BUS; R0 + 1 → R0	MR0	R0	0	1	0
S3	INTER-RUPT	INTER-RUPT	INTERRUPT	X, P → T; 0 → MIE 1 → P; 2 → X	HIGH Z	RN	1	1	0
THE FOLLOWING ARE ALL LINKED INSTRUCTIONS "68" PRECEEDS ALL OP CODES, SO THERE IS A DUPLICATE FETCH									
S1	0	0	STPC	STOP COUNTER CLOCK; 0 → ÷ 32 PRESCALER	HIGH Z	R0	1	1	0
S1	0	1	DTC	CNTR - 1 → CNTR	HIGH Z	R1	1	1	0

TABLE 2. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Continued)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES
S1	0	2	SPM2	CNTR - 1 ON EF2 AND TPA	HIGH Z	R2	1	1	0
S1	0	3	SCM2	CNTR - 1 ON EF2 0 TO 1	HIGH Z	R3	1	1	0
S1	0	4	SPM1	CNTR - 1 ON EF1 AND TPA	HIGH Z	R4	1	1	0
S1	0	5	SCM1	CNTR - 1 ON EF1 0 TO 1	HIGH Z	R5	1	1	0
S1	0	6	LDC	CNTR STOPPED: D → CH, CNTR; 0 → CI CNTR RUNNING: D → CH	D	R6	1	1	0
S1	0	7	STM	CNTR - 1 ON TPA ÷ 32	HIGH Z	R7	1	1	0
S1	0	8	GEC	CNTR → D	CNTR	R8	1	1	0
S1	0	9	ETQ	IF CNTR THRU 0: $\overline{Q}$ → Q	HIGH Z	R9	1	1	0
S1	0	A	XIE	1 → XIE	HIGH Z	RA	1	1	0
S1	0	B	XID	0 → XIE	HIGH Z	RB	1	1	0
S1	0	C	CIE	1 → CIE	HIGH Z	RC	1	1	0
S1	0	D	CID	0 → CIE	HIGH Z	RD	1	1	0
S1#1	2	0-F	DBNZ	RN - 1 → RN	HIGH Z	RN	1	1	0
#2	2	0-F	DBNZ	MRP → B; RP + 1 → RP	MRP	RP	0	1	0
#3	2	0-F	DBNZ	TAKEN: B → RP.1, MRP → RP.0 NOT TAKEN: RP + 1 → RP	M(RP + 1)	RP + 1	0	1	0
S1	3	E	BCI	TAKEN: MRP → RP.0; 0 → CI NOT TAKEN: RP + 1 → RP	MRP	RP	0	1	0
S1	3	F	BXI	TAKEN: MRP → RP.0 NOT TAKEN: RP + 1 → RP	MRP	RP	0	1	0
S1#1	6	0-F	RLXA	MRX → B, RX + 1 → RX	MRX	RX	0	1	0
#2	6	0-F	RLXA	B → T; MRX → B; RX + 1 → RX	M(RX + 1)	RX + 1	0	1	0
#3	6	0-F	RLXA	B, T → RN.0, RN.1	HIGH Z	RN	1	1	0
S1#1	7	4	DADC	MRX + D + DF → DF, D	MRX	RX	0	1	0
#2	7	4	DADC	DECIMAL ADJUST → DF, D	HIGH Z	RD	1	1	1
S1#1	7	6	DSAV	RX - 1 → RX	HIGH Z	RP	1	1	0
#2	7	6	DSAV	T → MRX; RX - 1 → RX	T	RX - 1	1	0	0
#3	7	6	DSAV	D → MRX; RX - 1 → RX SHIFT D RIGHT WITH CARRY	D	RX - 2	1	0	0
#4	7	6	DSAV	D → MRX	D	RX - 3	1	0	0
S1#1	7	7	DSMB	D - MRX - (NOT DF) → DF, D	MRX	RX	0	1	0
#2	7	7	DSMB	DECIMAL ADJUST → DF, D	HIGH Z	RP	1	1	0
S1#1	7	C	DACI	MRP + D + DF → DF, D; RP + 1 → RP	MRP	RP	0	1	0
#2	7	C	DACI	DECIMAL ADJUST → DF, D	HIGH Z	RP + 1	1	1	0
S1#1	7	F	DSBI	D - MRP - (NOT DF) → DF, D; RP + 1 → RP	MRP	RP	0	1	0

TABLE 2. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Continued)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES
#2	7	F	DSBI	DECIMAL ADJUST → DF, D	HIGH Z	RP + 1	1	1	0
S1#1	8	0-F	SCAL	RN.0, RN.1 → T, B	HIGH Z	RN	1	1	0
#2	8	0-F	SCAL	T→ MRX RX - 1 → RX	RN.0	RX	1	0	0
#3	8	0-F	SCAL	B → MRX RX - 1 → RX	RN.1	RX - 1	1	0	0
#4	8	0-F	SCAL	RP.0, RP.1 → T, B	HIGH Z	RP	1	1	0
#5	8	0-F	SCAL	B, T → RN.1, RN.0	HIGH Z	RN	1	1	0
#6	8	0-F	SCAL	MRN → B; RN + 1 → RN	MRP	RP	0	1	0
#7	8	0-F	SCAL	B → T; MRN → B; RN + 1 → RN	M(RP + 1)	RP + 1	0	1	0
#8	8	0-F	SCAL	B, T → RP.0, RP.1	HIGH Z	RP	1	1	0
S1#1	9	0-F	SRET	RN.0, RN.1 → T, B	HIGH Z	RN	1	1	0
#2	9	0-F	SRET	RX + 1 → RX	HIGH Z	RX	1	1	0
#3	9	0-F	SRET	B, T → RP.1, RP.0	HIGH Z	RP	1	1	0
#4	9	0-F	SRET	MRX → B; RX + 1 → RX	M(RX + 1)	RX + 1	0	1	0
#5	9	0-F	SRET	B → T; MRX → B	M(RX + 1	RX + 2	0	1	0
#6	9	0-F	SRET	B, T → RN.0, RN.1	HIGH Z	RN	1	1	0
S1#1	A	0-F	RSXD	RN.0, RN.1 → T, B	HIGH Z	RN	1	1	0
#2	A	0-F	RSXD	T → MRX; RX - 1 → RX	RN.0	RX	1	0	0
#3	A	0-F	RSXD	B → MRX; RX - 1 → RX	RN.1	RX - 1	1	0	0
S1#1	B	0-F	RNX	RN.0, RN.1 → T, B	HIGH Z	RN	1	1	0
#2	B	0-F	RNX	B, T → RX.1, RX.0	HIGH Z	RX	1	1	0
S1#1	C	0-F	RLDI	MRP → B; RP + 1 → RP	MRP	RP	0	1	0
#2	C	0-F	RLDI	B → T; MRP → B; RP + 1 → RP	M(RP + 1)	RP + 1	0	1	0
#3	C	0-F	RLDI	B, T → RN.0, RN.1;` RP + 1 → RP	HIGH Z	RN	1	1	0
S1#1	F	4	DADD	MRX + D → DF; D	MRX	RX	0	1	0
#2	F	4	DADD	DECIMAL ADJUST → DF, D	HIGH Z	RP	1	1	0
S1#1	F	7	DSM	D - MRX → DF, D	MRX	RX	0	1	0
#2	F	7	DSM	DECIMAL ADJUST → DF, D	HIGH Z	RP	1	1	0
S1#1	F	C	DADI	MRP + D → DF, D; RP + 1 → RP	MRP	RP	0	1	0
#2	F	C	DADI	DECIMAL ADJUST → DF, D	HIGH Z	RP + 1	1	1	0
S1#1	F	F	DSMI	D - MRP → DF, D RP + 1 → RP	MRP	RP	0	1	0
#2	F	F	DSMI	DECIMAL ADJUST → DF, D	HIGH Z	RP + 1	1	1	0

NOTE:

20. Data bus floats for first 2-1/2 clocks of the nine clock initialization cycle; all zeros for remainder of cycle.

INSTRUCTION SUMMARY

	N															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	IDL	LDN														
1	INC															
2	DEC															
3	BR	BQ	BZ	BDF	B1	B2	B3	B4	SKP	BNQ	BNZ	BNF	BN1	BN2	BN3	BN4
4	LDA															
5	STR															
6	IRX	OUT							†	INP						
7	RET	DIS	LDXA	STXD	ADC	SDB	SHRC	SMB	SAV	MARK	REQ	SEQ	ADCI	SDBI	SHLC	SMBI
8	GLO															
9	GHI															
A	PLO															
B	PHI															
C	LBR	LBQ	LBZ	LBDF	NOP	LSNQ	LSNZ	LSNF	LSKP	LBNQ	LBNZ	LBNF	LSIE	LSQ	LSZ	LSDF
D	SEP															
E	SEX															
F	LDX	OR	AND	XOR	ADD	SD	SHR	SM	LDI	ORI	ANI	XRI	ADI	SDI	SHL	SMI
'68' LINKED OPCODES (DOUBLE FETCH)																
0	STPC	DTC	SPM2	SCM2	SPM1	SCM1	LDC	STM	GEC	ETQ	XIE	XID	CIE	CID	-	-
2	DBNZ															
3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	BCI	BXI
6	RLXA															
7	-	-	-	-	DADC	-	DSAV	DSMB	-	-	-	-	DACI	-	-	DSBI
8	SCAL															
9	SRET															
A	RSXD															
B	RNX															
C	RLDI															
F	-	-	-	-	DADD	-	-	DSM	-	-	-	-	DADI	-	-	DSMI

†'68' is used as a linking OPCODE for the double fetch instructions.

Operating and Handling Considerations

Handling

All inputs and outputs of Harris CMOS devices have a network for electrostatic protection during handling.

Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD} - V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

HARRIS SEMICONDUCTOR

80C286

High Performance Microprocessor with Memory Management and Protection

March 1997

Features

- Compatible with NMOS 80286
- Wide Range of Clock Rates
  - DC to 25MHz (80C286-25)
  - DC to 20MHz (80C286-20)
  - DC to 16MHz (80C286-16)
  - DC to 12.5MHz (80C286-12)
  - DC to 10MHz (80C286-10)
- Static CMOS Design for Low Power Operation
  - ICCSB = 5mA Maximum
  - ICCOP = 185mA Maximum (80C286-10)
    220mA Maximum (80C286-12)
    260mA Maximum (80C286-16)
    310mA Maximum (80C286-20)
    410mA Maximum (80C286-25)
- High Performance Processor (Up to 19 Times the 8086 Throughput)
- Large Address Space
- 16 Megabytes Physical/1 Gigabyte Virtual per Task
- Integrated Memory Management, Four-Level Memory Protection and Support for Virtual Memory and Operating Systems
- Two 80C86 Upward Compatible Operating Modes
  - 80C286 Real Address Mode
  - PVAM
- Compatible with 80287 Numeric Data Co-Processor
- High Bandwidth Bus Interface (25 Megabyte/Sec)
- Available In
  - 68 Pin PGA (Commercial, Industrial, and Military)
  - 68 Pin PLCC (Commercial and Industrial)

Description

The Harris 80C286 is a static CMOS version of the NMOS 80286 microprocessor. The 80C286 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. The 80C286 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. A 25MHz 80C286 provides up to nineteen times the throughput of a standard 5MHz 8086. The 80C286 includes memory management capabilities that map 2^{30} (one gigabyte) of virtual address space per task into 2^{24} bytes (16 megabytes) of physical memory.

The 80C286 is upwardly compatible with 80C86 and 80C88 software (the 80C286 instruction set is a superset of the 80C86/80C88 instruction set). Using the 80C286 real address mode, the 80C286 is object code compatible with existing 80C86 and 80C88 software. In protected virtual address mode, the 80C286 is source code compatible with 80C86 and 80C88 software but may require upgrading to use virtual address as supported by the 80C286's integrated memory management and protection mechanism. Both modes operate at full 80C286 performance and execute a superset of the 80C86 and 80C88 instructions.

The 80C286 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The 80C286 also supports virtual memory systems by providing a segment-not-present exception and restartable instructions.

Ordering Information

PACKAGE	TEMP. RANGE	10MHz	12.5MHz	16MHz	20MHz	25MHz	PKG. NO.
PGA	0°C to +70°C	-	CG80C286-12	CG80C286-16	CG80C286-20	-	G68.B
	-40°C to +85°C	IG80C286-10	IG80C286-12	-	-	-	G68.B
	-55°C to +125°C	5962-9067801MXC	5962-9067802MXC	-	-	-	G68.B
PLCC	0°C to +70°C	-	CS80C286-12	CS80C286-16	CS80C286-20	CS80C286-25	N68.95
	-40°C to +85°C	IS80C286-10	IS80C286-12	IS80C286-16	IS80C286-20	-	N68.95

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

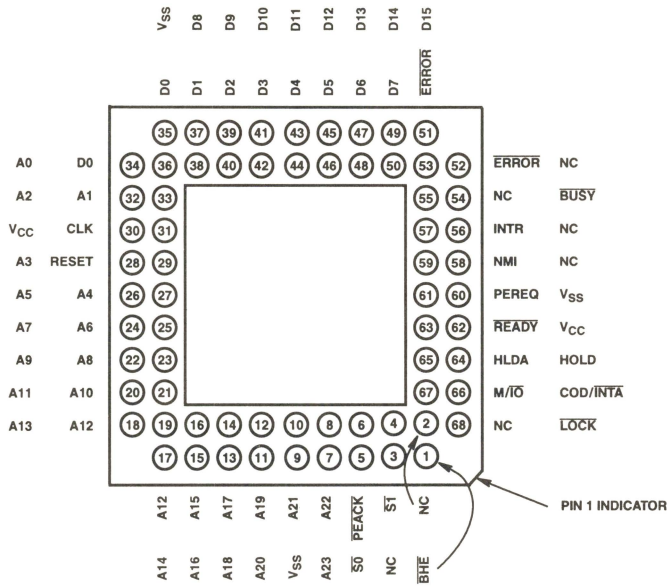
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File Number **2947.2**

Pinouts

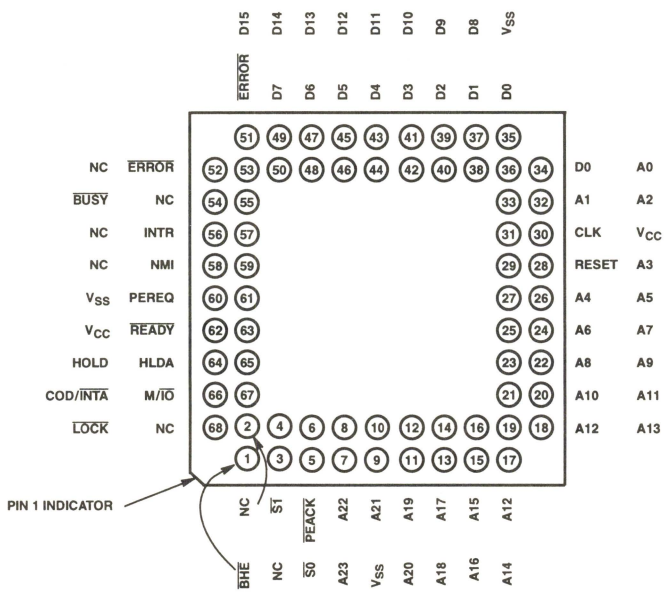
68 LEAD PGA

Component Pad View - As viewed from underside of the component when mounted on the board.



68 LEAD PGA

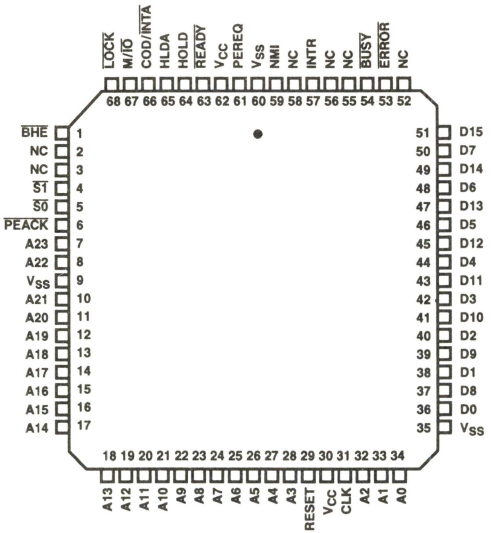
P.C. Board View - As viewed from the component side of the P.C. board.



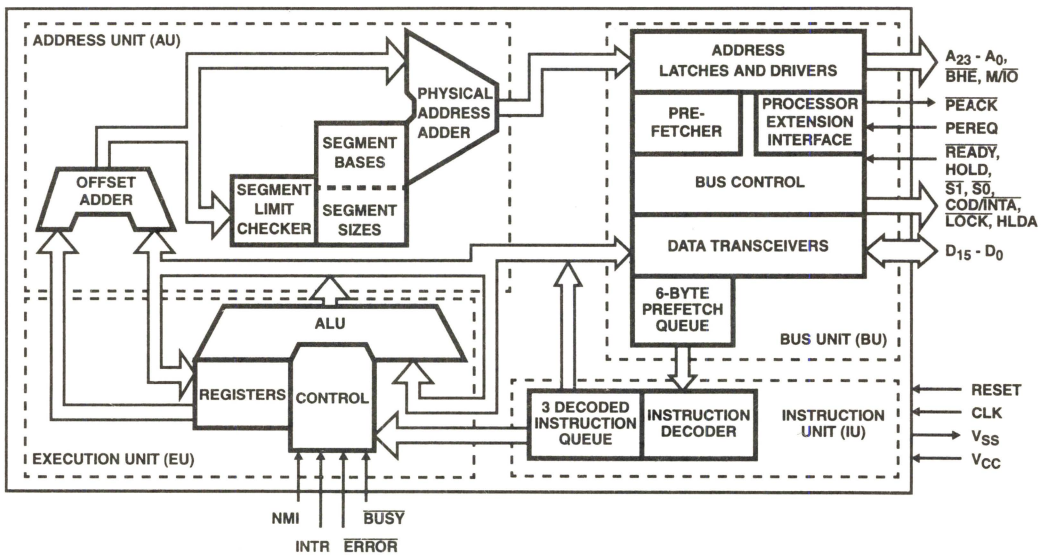
Pinouts (Continued)

68 LEAD PLCC

P.C. Board View - As viewed from the component side of the P.C. board.



Functional Diagram



Pin Descriptions

The following pin function descriptions are for the 80C286 microprocessor.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
CLK	31	I	SYSTEM CLOCK: provides the fundamental timing for the 80C286 system. It is divided by two inside the 80C286 to generate the processor clock. The internal divide-by-two circuitry can be synchronized to an external clock generator by a LOW to HIGH transition on the RESET input.
D_{15} - D_0	36 - 51	I/O	DATA BUS: inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles. The data bus is active HIGH and is held at high impedance to the last valid logic level during bus hold acknowledge.
A_{23} - A_0	7 - 8 10 - 28 32 - 43	O	ADDRESS BUS: outputs physical memory and I/O port addresses. A_{23} - A_{16} are LOW during I/O transfers. A_0 is LOW when data is to be transferred on pins D_7 - D_0 (see table below). The address bus is active High and floats to three-state off during bus hold acknowledge.
$\overline{BHE}$	1	O	BUS HIGH ENABLE: indicates transfer of data on the upper byte of the data bus, D_{15} - D_8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use BHE to condition chip select functions. BHE is active LOW and floats to three-state OFF during bus hold acknowledge.
$\overline{S1}$, $\overline{S0}$	4, 5	O	BUS CYCLE STATUS: indicates initiation of a bus cycle and along with M/$\overline{IO}$ and COD/$\overline{INTA}$, defines the type of bus cycle. The bus is in a T_S state whenever one or both are LOW. $\overline{S1}$ and $\overline{S0}$ are active LOW and are held at a high impedance logic one during bus hold acknowledge.

$\overline{BHE}$ AND A_0 ENCODINGS

$\overline{BHE}$ VALUE	A_0 VALUE	FUNCTION
0	0	Word transfer
0	1	Byte transfer on upper half of data bus (D_{15} - D_8)
1	0	Byte transfer on lower half of data bus (D_7 - D_0)
1	1	Reserved

80C286 BUS CYCLE STATUS DEFINITION

COD/$\overline{INTA}$	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	BUS CYCLE INITIATED
0(LOW)	0	0	0	Interrupt acknowledge
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	None; not a status cycle
0	1	0	0	If A_1 = 1 then halt; else shutdown
0	1	0	1	Memory data read
0	1	1	0	Memory data write
0	1	1	1	None; not a status cycle
1(HIGH)	0	0	0	Reserved
1	0	0	1	I/O read
1	0	1	0	I/O write
1	0	1	1	None; not a status cycle
1	1	0	0	Reserved
1	1	0	1	Memory instruction read
1	1	1	0	Reserved
1	1	1	1	None; not a status cycle

Pin Descriptions The following pin function descriptions are for the 80C286 microprocessor. (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
M/$\overline{IO}$	67	O	MEMORY I/O SELECT: distinguishes memory access from I/O access. If HIGH during T_S, a memory cycle or a halt/shutdown cycle is in progress. If LOW, an I/O cycle or an interrupt acknowledge cycle is in progress. M/$\overline{IO}$ is held at high impedance to the last valid logic state during bus hold acknowledge.
COD/$\overline{INTA}$	66	O	CODE/INTERRUPT ACKNOWLEDGE: distinguishes instruction fetch cycles from memory data read cycles. Also distinguishes interrupt acknowledge cycles from I/O cycles. COD/$\overline{INTA}$ is held at high impedance to the last valid logic state during bus hold acknowledge. Its timing is the same as M/$\overline{IO}$.
$\overline{LOCK}$	68	O	BUS LOCK: indicates that other system bus masters are not to gain control of the system bus for the current and following bus cycles. The $\overline{LOCK}$ signal may be activated explicitly by the "LOCK" instruction prefix or automatically by 80C286 hardware during memory XCHG instructions, interrupt acknowledge, or descriptor table access. $\overline{LOCK}$ is active LOW and is held at a high impedance logic one during bus hold acknowledge.
$\overline{READY}$	63	I	BUS READY: terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{READY}$ LOW. $\overline{READY}$ is an active LOW synchronous input requiring setup and hold times relative to the system clock be met for correct operation. $\overline{READY}$ is ignored during bus hold acknowledge. (See Note 1)
HOLD HLDA	64 65	I O	BUS HOLD REQUEST AND HOLD ACKNOWLEDGE: control ownership of the 80C286 local bus. The HOLD input allows another local bus master to request control of the local bus. When control is granted, the 80C286 will float its bus drivers and then activate HLDA, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until HOLD becomes inactive which results in the 80C286 deactivating HLDA and regaining control of the local bus. This terminates the bus hold acknowledge condition. HOLD may be asynchronous to the system clock. These signals are active HIGH. Note that HLDA never floats.
INTR	57	I	INTERRUPT REQUEST: requires the 80C286 to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the 80C286 responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt. To ensure program interruption, INTR must remain active until an interrupt acknowledge bus cycle is initiated. INTR is sampled at the beginning of each processor cycle and must be active HIGH at least two processor cycles before the current instruction ends in order to interrupt before the next instruction. INTR is level sensitive, active HIGH, and may be asynchronous to the system clock.
NMI	59	I	NON-MASKABLE INTERRUPT REQUEST: interrupts the 80C286 with an internally supplied vector value of two. No interrupt acknowledge cycles are performed. The interrupt enable bit in the 80C286 flag word does not affect this input. The NMI input is active HIGH, may be asynchronous to the system clock, and is edge triggered after internal synchronization. For proper recognition, the input must have been previously LOW for at least four system clock cycles and remain HIGH for at least four system clock cycles.
PEREQ $\overline{PEACK}$	61 6	I O	PROCESSOR EXTENSION OPERAND REQUEST AND ACKNOWLEDGE: extend the memory management and protection capabilities of the 80C286 to processor extensions. The PEREQ input requests the 80C286 to perform a data operand transfer for a processor extension. The $\overline{PEACK}$ output signals the processor extension when the requested operand is being transferred. PEREQ is active HIGH. $\overline{PEACK}$ is active LOW and is held at a high impedance logic one during bus hold acknowledge. PEREQ may be asynchronous to the system clock.
$\overline{BUSY}$ $\overline{ERROR}$	54 53	I I	PROCESSOR EXTENSION BUSY AND ERROR: indicates the operating condition of a processor extension to the 80C286. An active $\overline{BUSY}$ input stops 80C286 program execution on WAIT and some ESC instructions until $\overline{BUSY}$ becomes inactive (HIGH). The 80C286 may be interrupted while waiting for $\overline{BUSY}$ to become inactive. An active $\overline{ERROR}$ input causes the 80C286 to perform a processor extension interrupt when executing WAIT or some ESC instructions. These inputs are active LOW and may be asynchronous to the system clock.

Pin Descriptions

The following pin function descriptions are for the 80C286 microprocessor. **(Continued)**

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
RESET	29	I	SYSTEM RESET: clears the internal logic of the 80C286 and is active HIGH. The 80C286 may be reinitialize at any time with a LOW to HIGH transition on RESET which remains active for more than 16 system clock cycles. During RESET active, the output pins of the 80C286 enter the state shown below. **80C286 PIN STATE DURING RESET** PIN VALUE: 1 (HIGH) — PIN NAMES: $\overline{S0}$, $\overline{S1}$, $\overline{PEACK}$, A_{23} - A_0, $\overline{BHE}$, $\overline{LOCK}$ PIN VALUE: 0 (LOW) — PIN NAMES: M/$\overline{IO}$, COD/$\overline{INTA}$, HLDA (Note 2) PIN VALUE: HIGH IMPEDANCE — PIN NAMES: D15 - D0 Operation of the 80C286 begins after a HIGH to LOW transition on RESET. The HIGH to LOW transition of RESET must be synchronous to the system clock. Approximately 50 system clock cycles are required by the 80C286 for internal initializations before the first bus cycle to fetch code from the power-on execution address is performed. A LOW to HIGH transition of RESET synchronous to the system clock will end a processor cycle at the second HIGH to LOW transition of the system clock. The LOW to HIGH transition of RESET may be asynchronous to the system clock; however, in this case it cannot be predetermined which phase of the processor clock will occur during the next system clock period. Synchronous LOW to HIGH transitions of RESET are required only for systems where the processor clock must be phase synchronous to another clock.
V_{SS}	9, 35, 60	I	SYSTEM GROUND: are the ground pins (all must be connected to system ground).
V_{CC}	30, 62	I	SYSTEM POWER: +5V power supply pins. A 0.1µF capacitor between pins 60 and 62 is recommended.

NOTES:

1. READY is an open-collector signal and should be pulled inactive with an appropriate resistor (620Ω at 10MHz and 12.5MHz, 470Ω at 16MHz, 390Ω at 20MHz, 270Ω at 25MHz).
2. HLDA is only Low if HOLD is inactive (Low).
3. All unused inputs should be pulled to their inactive state with pull up/down resistors.

Functional Description

Introduction

The Harris 80C286 microprocessor is a static CMOS version of the NMOS 80286 microprocessor. The 80C286 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. Depending on the application, the 80C286's performance is up to nineteen times faster than the standard 5MHz 8086's, while providing complete upward software compatibility with Harris 80C86 and 80C88 CPU family.

The 80C286 operates in two modes: 80C286 real address mode and protected virtual address mode. Both modes execute a superset of the 80C86 and 80C88 instruction set.

In 80C286 real address mode programs use real addresses with up to one megabyte of address space. Programs use virtual addresses in protected virtual address mode, also called protected mode. In protected mode, the 80C286 CPU automatically maps 1 gigabyte of virtual addresses per task into a 16 megabyte real address space. This mode also provides memory protection to isolate the operating system and ensure privacy of each tasks' programs and data. Both modes provide the same base instruction set, registers and addressing modes.

The Functional Description describes the following: Static operation, the base 80C286 architecture common to both modes, 80C286 real address mode, and finally, protected mode.

Static Operation

The 80C286 is comprised of completely static circuitry. Internal registers, counters, and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction typically placed on microprocessors. The CMOS 80C286 can operate from DC to the specified upper frequency limit. The clock to the processor may be stopped at any point (either phase one or phase two of the processor clock cycle) and held there indefinitely. There is, however, a significant decrease in power requirement if the clock is stopped in phase two of the processor clock cycle. Details on the clock relationships will be discussed in the Bus Operation section. The ability to stop the clock to the processor is especially useful for system debug or power critical applications.

The 80C286 can be single-stepped using only the CPU clock. This state can be maintained as long as necessary. Single step clock information allows simple interface circuitry to provide critical information for system debug.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide low power operation since 80C286 power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, with the clock stopped in phase two of the processor clock cycle, the 80C286 power requirement is the standby current (5mA maximum).

80C286 Base Architecture

The 80C86, 80C88, and 80C286 CPU family all contain the same basic set of registers, instructions, and addressing modes. The 80C286 processor is upwardly compatible with the 80C86 and 80C88 CPU's.

Register Set

The 80C286 base architecture has fifteen registers as shown in Figure 1. These registers are grouped into the following four categories.

GENERAL REGISTERS: Eight 16-bit general purpose registers used to contain arithmetic and logical operands. Four of these (AX, BX, CX and DX) can be used either in their entirety as 16-bit words or split into pairs of separate 8-bit registers.

SEGMENT REGISTERS: Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack and data. (For usage, refer to Memory Organization.)

BASE AND INDEX REGISTERS: Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode determines the specific registers used for operand address calculations.

STATUS AND CONTROL REGISTERS: Three 16-bit special purpose registers record or control certain aspects of the 80C286 processor state. These include the Flags register and Machine Status Word register shown in Figure 2, and the Instruction Pointer, which contains the offset address of the next sequential instruction to be executed.

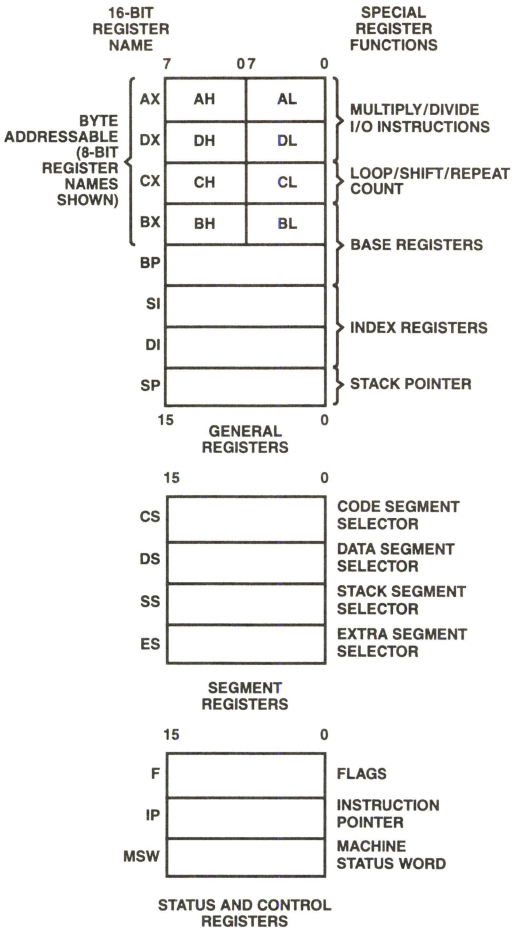


FIGURE 1. REGISTER SET

Flags Word Description

The Flags word (Flags) records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 6, 7 and 11) and controls the operation of the 80C286 within a given operating mode (bits 8 and 9). Flags is a 16-bit register. The function of the flag bits is given in Table 1.

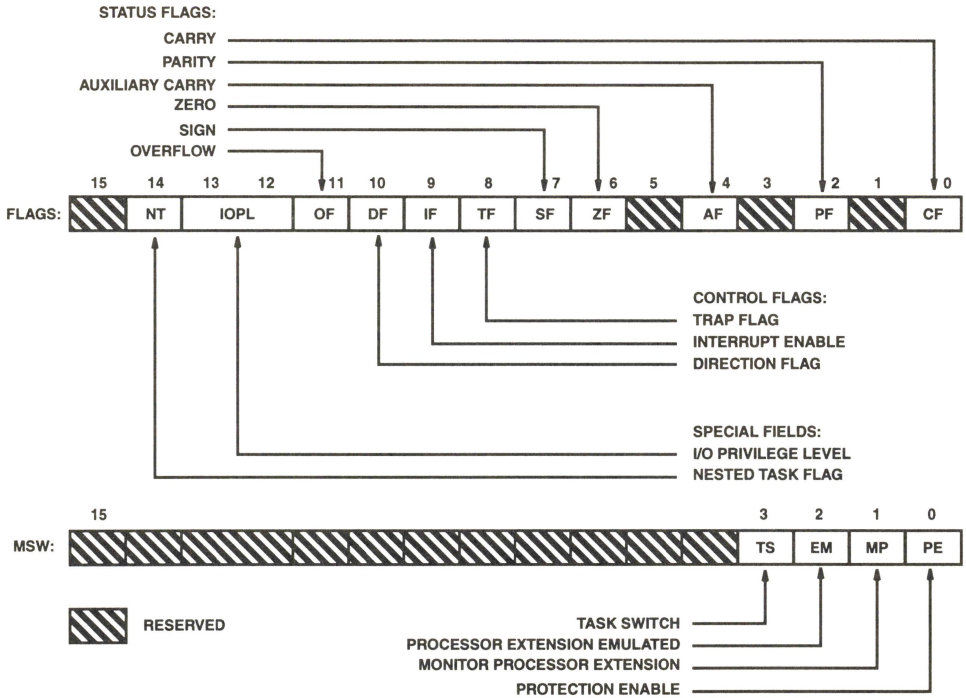


FIGURE 2. STATUS AND CONTROL REGISTER BIT FUNCTIONS

TABLE 1. FLAGS WORD BIT FUNCTIONS

BIT POSITION	NAME	FUNCTION
0	CF	Carry Flag - Set on high-order bit carry or borrow; cleared otherwise.
2	PF	Parity Flag - Set if low-order 8 bits of result contain an even number of 1 bits; cleared otherwise.
4	AF	Set on carry from or borrow to the low order four bits of AL; cleared otherwise.
6	ZF	Zero Flag - Set if result is zero; cleared otherwise.
7	SF	Sign Flag - Set equal to high-order bit of result (0 if positive, 1 if negative).
11	OF	Overflow Flag - Set if result is a too-large positive number or a too-small negative number (excluding sign-bit) to fit in destination operand; cleared otherwise.
8	TF	Single Step Flag - Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	Interrupt-Enable Flag - When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location.
10	DF	Direction Flag - Causes string instructions to auto decrement the appropriate index registers when set. Clearing DF causes auto increment.

Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, string manipulation, shift/rotate/logical, high level, processor control and control transfer instructions. These categories are summarized in Table 2.

An 80C286 instruction can reference zero, one, or two operands; where an operand may reside in a register, in the instruction itself, or in memory. Zero-operand instructions (e.g. NOP and HLT) are usually one byte long. One-operand instructions (e.g. INC and DEC) are usually two bytes long but some are encoded in only one byte. One-operand instructions may reference a register or memory location. Two-operand instructions permit the following six types of instruction operations:

- Register to Register
- Memory to Register
- Immediate to Register
- Memory to Memory
- Register to Memory
- Immediate to Memory

Two-operand instructions (e.g. MOV and ADD) are usually three to six bytes long. Memory to memory operations are provided by a special class of string instructions requiring one to three bytes. For detailed instruction formats and encodings refer to the instruction set summary at the end of this document.

TABLE 2A. DATA TRANSFER INSTRUCTIONS

GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack

TABLE 2B. ARITHMETIC INSTRUCTIONS

ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte or word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiply byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

TABLE 2C. STRING INSTRUCTIONS

MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMPS	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/REPZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal/not zero

TABLE 2D. SHIFT/ROTATE LOGICAL INSTRUCTIONS

LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"Test" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word

TABLE 2E. HIGH LEVEL INSTRUCTIONS

ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure exit
BOUND	Detects values outside prescribed range

TABLE 2F. PROCESSOR CONTROL INSTRUCTIONS

FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for $\overline{\text{TEST}}$ pin active
ESC	Escape to extension processor
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation
EXECUTION ENVIRONMENT CONTROL	
LMSW	Load machine status word
SMSW	Store machine status word

TABLE 2G. PROGRAM TRANSFER INSTRUCTIONS

CONDITIONAL TRANSFERS		UNCONDITIONAL TRANSFERS	
JA/JNBE	Jump if above/not below nor equal	CALL	Call procedure
JAE/JNB	Jump if above or equal/not below	RET	Return from procedure
JB/JNAE	Jump if below/not above nor equal	JMP	Jump
JBE/JNA	Jump if below or equal/not above		
JC	Jump if carry	ITERATION CONTROLS	
JE/JZ	Jump if equal/zero	LOOP	Loop
JG/JNLE	Jump if greater/not less nor equal		
JGE/JNL	Jump if greater or equal/not less	LOOPE/LOOPZ	Loop if equal/zero
JL/JNGE	Jump if less/not greater nor equal	LOOPNE/LOOPNZ	Loop if not equal/not zero
JLE/JNG	Jump if less or equal/not greater	JCXZ	Jump if register CX = 0
JNC	Jump if not carry		
JNE/JNZ	Jump if not equal/not zero	INTERRUPTS	
JNO	Jump if not overflow	INT	Interrupt
JNP/JPO	Jump if not parity/parity odd		
JNS	Jump if not sign	INTO	Interrupt if overflow
JO	Jump if overflow	IRET	Interrupt return
JP/JPE	Jump if parity/parity even		
JS	Jump if sign		

Memory Organization

Memory is organized as sets of variable-length segments. Each segment is a linear contiguous sequence of up to 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit segment selector and a 16-bit offset. The segment selector indicates the desired segment in memory. The offset component indicates the desired byte address within the segment. (See Figure 3).

All instructions that address operands in memory must specify the segment and the offset. For speed and compact instruction encoding, segment selectors are usually stored in the high speed segment registers. An instruction need specify only the desired segment register and offset in order to address a memory operand.

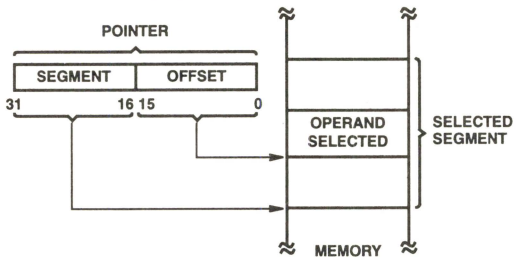


FIGURE 3. TWO COMPONENT ADDRESS

Most instructions need not explicitly specify which segment register is used. The correct segment register is automatically chosen according to the rules of Table 3. These rules follow the way programs are written (see Figure 4) as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data and extra segments may coincide for simple programs. To access operands not residing in one of the four immediately available segments, a full 32-bit pointer or a new segment selector must be loaded.

TABLE 3. SEGMENT REGISTER SELECTION RULES

MEMORY REFERENCE NEEDED	SEGMENT REGISTER USED	IMPLICIT SEGMENT SELECTION RULE
Instructions	Code (CS)	Automatic with instruction prefetch
Stack	Stack (SS)	All stack pushes and pops. Any memory reference which uses BP as a base register.
Local Data	Data (DS)	All data references except when relative to stack or string destination
External (Global) Data	Extra (ES)	Alternate data segment and destination of string operation

Addressing Modes

The 80C286 provides a total of eight addressing modes for instructions to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

REGISTER OPERAND MODE: The operand is located in one of the 8 or 16-bit general registers.

IMMEDIATE OPERAND MODE: The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: segment selector and offset. The segment selector is supplied by a segment register either implicitly chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset is calculated by summing any combination of the following three address elements:

the **displacement** (an 8 or 16-bit immediate value contained in the instruction)

the **base** (contents of either the BX or BP base registers)

the **index** (contents of either the SI or DI index registers)

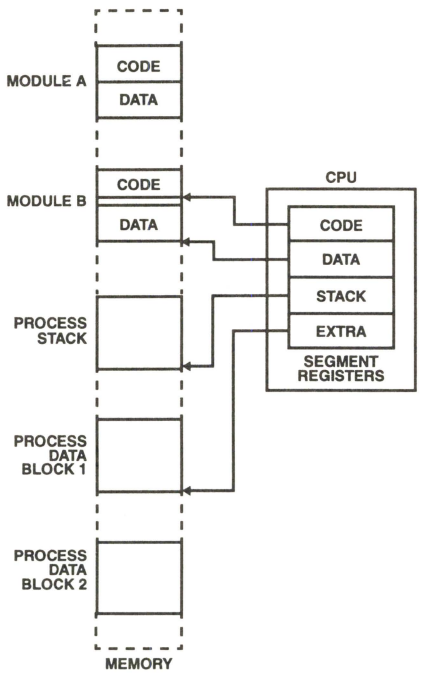


FIGURE 4. SEGMENTED MEMORY HELPS STRUCTURE SOFTWARE

Any carry out from the 16-bit addition is ignored. Eight-bit displacements are sign extended to 16-bit values.

Combinations of these three address elements define the six memory addressing modes, described below.

DIRECT MODE: The operand's offset is contained in the instruction as an 8 or 16-bit displacement element.

REGISTER INDIRECT MODE: The operand's offset is in one of the registers SI, DI, BX or BP.

BASED MODE: The operand's offset is the sum of an 8 or 16-bit displacement and the contents of a base register (BX or BP).

INDEXED MODE: The operand's offset is the sum of an 8 or 16-bit displacement and the contents of an index register (SI or DI).

BASED INDEXED MODE: The operand's offset is the sum of the contents of a base register and an index register.

BASED INDEXED MODE WITH DISPLACEMENT: The operand's offset is the sum of a base register's contents, an index register's contents, and an 8 or 16-bit displacement.

Data Types

The 80C286 directly supports the following data types:

Integer: A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32 and 64-bit integers are supported using the 80287 Numeric Data Processor.

Ordinal: An unsigned binary numeric value contained in an 8-bit byte or 16-bit word.

Pointer: A 32-bit quantity, composed of a segment selector component and an offset component. Each component is a 16-bit word.

String: A contiguous sequence of bytes or words. A string may contain from 1 byte to 64K bytes.

ASCII: A byte representation of alphanumeric and control characters using the ASCII standard of character representation.

BCD: A byte (unpacked) representation of the decimal digits 0-9.

Packed BCD: A byte (packed) representation of two decimal digits 0-9 storing one digit in each nibble of the byte.

Floating Point: A signed 32, 64 or 80-bit real number representation. (Floating point operands are supported using the 80287 Numeric Processor extension).

Figure 5 graphically represents the data types supported by the 80C286.

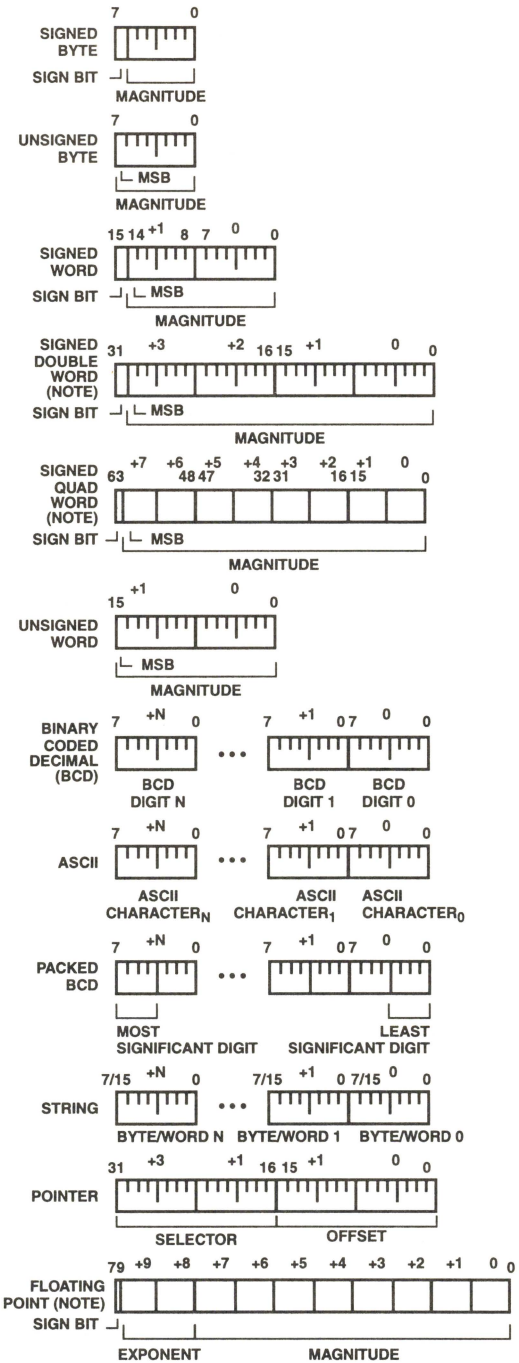


FIGURE 5. 80C286 SUPPORTED DATA TYPES

NOTE: Supported by 80C286/80C287 Numeric Data Processor Configuration

TABLE 4. INTERRUPT VECTOR ASSIGNMENTS

FUNCTION	INTERRUPT NUMBER	RELATED INSTRUCTIONS	DOES RETURN ADDRESS POINT TO INSTRUCTION CAUSING EXCEPTION?
Divide Error Exception	0	DIV, IDIV	Yes
Single Step Interrupt	1	All	
NMI Interrupt	2	INT 2 or NMI Pin	
Breakpoint Interrupt	3	INT 3	
INTO Detected Overflow Exception	4	INTO	No
BOUND Range Exceeded Exception	s	BOUND	Yes
Invalid Opcode Exception	6	Any Undefined Opcode	Yes
Processor Extension Not Available Exception	7	ESC or WAIT	Yes
Reserved - Do Not Use	8 - 15		
Processor Extension Error Interrupt	16	ESC or WAIT	
Reserved	17 - 31		
User Defined	32 - 255		

I/O Space

The I/O space consists of 64K 8-bit ports, 32K 16-bit ports, or a combination of the two. I/O instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero extended such that A_{15}-A_8 are LOW. I/O port addresses 00F8(H) through 00FF(H) are reserved.

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (Flags) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware initiated interrupts occur in response to an external input and are classified as non-maskable or maskable. Programs may cause an interrupt with an INT instruction. Instruction exceptions occur when an unusual condition which prevents further instruction processing is detected while attempting to execute an instruction. The return address from an exception will always point to the instruction causing the exception and include any leading instruction prefixes.

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0-31, some of which are used for instruction exceptions, are reserved. For each interrupt, an 8-bit vector must be supplied to the 80C286 which identifies the appropriate table entry. Exceptions supply the interrupt vector internally. INT instructions contain or imply the vector and allow access to all 256 interrupts. Maskable hardware initiated interrupts supply the 8-bit vector to the CPU during an interrupt acknowledge bus sequence. Nonmaskable hardware interrupts use a predefined internally supplied vector.

Maskable Interrupt (INTR)

The 80C286 provides a maskable hardware interrupt request pin, INTR. Software enables this input by setting the interrupt flag bit (IF) in the flag word. All 224 user-defined interrupt sources can share this input, yet they can retain separate interrupt handlers. An 8-bit vector read by the CPU during the interrupt acknowledge sequence (discussed in System Interface section) identifies the source of the interrupt.

The processor automatically disables further maskable interrupts internally by resetting the IF as part of the response to an interrupt or exception. The saved flag word will reflect the enable status of the processor prior to the interrupt. Until the flag word is restored to the flag register, the interrupt flag will be zero unless specifically set. The interrupt return instruction includes restoring the flag word, thereby restoring the original status of IF.

Non-Maskable Interrupt Request (NMI)

A non-maskable interrupt input (NMI) is also provided. NMI has higher priority than INTR. A typical use of NMI would be to activate a power failure routine. The activation of this input causes an interrupt with an internally supplied vector value of 2. No external interrupt acknowledge sequence is performed.

While executing the NMI servicing procedure, the 80C286 will service neither further NMI requests, INTR requests, nor the processor extension segment overrun interrupt until an interrupt return (IRET) instruction is executed or the CPU is reset. If NMI occurs while currently servicing an NMI, its presence will be saved for servicing after executing the first IRET instruction. IF is cleared at the beginning of an NMI interrupt to inhibit INTR interrupts.

Single Step Interrupt

The 80C286 has an internal interrupt that allows programs to execute one instruction at a time. It is called the single step interrupt and is controlled by the single step flag bit (TF) in the flag word. Once this bit is set, an internal single step interrupt will occur after the next instruction has been executed. The interrupt clears the TF bit and uses an internally supplied vector of 1. The IRET instruction is used to set the TF bit and transfer control to the next instruction to be single stepped.

Interrupt Priorities

When simultaneous interrupt requests occur, they are processed in a fixed order as shown in Table 5. Interrupt processing involves saving the flags, return address, and setting CS:IP to point at the first instruction of the interrupt handler. If another enabled interrupt should occur, it is processed before the next instruction of the current interrupt handler is executed. The last interrupt processed is therefore the first one serviced.

TABLE 5. INTERRUPT PROCESSING ORDER

ORDER	INTERRUPT
1	Instruction Exception
2	Single Step
3	NMI
4	Processor Extension Segment Overrun
5	INTR
6	INT Instruction

Initialization and Processor Reset

Processor initialization or start up is accomplished by driving the RESET input pin HIGH. RESET forces the 80C286 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as RESET is active. After RESET becomes inactive, and an internal processing interval elapses, the 80C286 begins execution in real address mode with the instruction at physical location FFFFF0(H). RESET also sets some registers to predefined values as shown in Table 6.

TABLE 6. 80C286 INITIAL REGISTER STATE AFTER RESET

Flag Word	0002(H)
Machine Status Word	FFF0(H)
Instruction Pointer	FFF0(H)
Code Segment	F000(H)
Data Segment	0000(H)
Extra Segment	0000(H)
Stack Segment	0000(H)

HOLD must not be active during the time from the leading edge of the initial RESET to 34 CLKs after the trailing edge of the initial RESET of an 80C286 system.

Machine Status Word Description

The machine status word (MSW) records when a task switch takes place and controls the operating mode of the 80C286. It is a 16-bit register of which the lower four bits are used. One bit places the CPU into protected mode, while the other three bits, as shown in Table 7, control the processor extension interface. After RESET, this register contains FFF0(H) which places the 80C286 in 80C286 real address mode.

TABLE 7. MSW BIT FUNCTIONS

BIT POSITION	NAME	FUNCTION
0	PE	Protected mode enable places the 80C286 into protected mode and cannot be cleared except by RESET.
1	MP	Monitor processor extension allows WAIT instructions to cause a processor extension not present exception (number 7).
2	EM	Emulate processor extension causes a processor extension not present exception (number 7) on ESC instructions to allow emulating a processor extension.
3	TS	Task switched indicates the next instruction using a processor extension will cause exception 7, allowing software to test whether the current processor extension context belongs to the current task.

The LMSW and SMSW instructions can load and store the MSW in real address mode. The recommended use of TS, EM, and MP is shown in Table 8.

Halt

The HLT instruction stops program execution and prevents the CPU from using the local bus until restarted. Either NMI, INTR with IF = 1, or RESET will force the 80C286 out of halt. If interrupted, the saved CS:IP will point to the next instruction after the HLT.

TABLE 8. RECOMMENDED MSW ENCODINGS FOR PROCESSOR EXTENSION CONTROL

TS	MP	EM	RECOMMENDED USE	INSTRUCTION CAUSING EXCEPTION 7
0	0	0	Initial encoding after RESET. 80C286 operation is identical to 80C86/88.	None
0	0	1	No processor extension is available. Software will emulate its function.	ESC
1	0	1	No processor extension is available. Software will emulate its function. The current processor extension context may belong to another task.	ESC
0	1	0	A processor extension exists.	None
1	1	0	A processor extension exists. The current processor extension context may belong to another task. The exception 7 on WAIT allows software to test for an error pending from a previous processor extension operation.	ESC or WAIT

TABLE 9. REAL ADDRESS MODE ADDRESSING INTERRUPTS

FUNCTION	INTERRUPT NUMBER	RELATED INSTRUCTIONS	RETURN ADDRESS BEFORE INSTRUCTION
Interrupt table limit too small exception	8	INT vector is not within table limit	Yes
Processor extension segment overrun interrupt	9	ESC with memory operand extending beyond offset FFFF(H)	No
Segment overrun exception	13	Word memory reference with offset = FFFF(H) or an attempt to execute past the end of a segment	Yes

80C286 Real Address Mode

The 80C286 executes a fully upward-compatible superset of the 80C86 instruction set in real address mode. In real address mode the 80C286 is object code compatible with 80C86 and 80C88 software. The real address mode architecture (registers and addressing modes) is exactly as described in the 80C286 Base Architecture section of this Functional Description.

Memory Size

Physical memory is a contiguous array of up to 1,048,576 bytes (one megabyte) addressed by pins A_0 through A_{19} and $\overline{BHE}$. A_{20} through A_{23} should be ignored.

Memory Addressing

In real address mode physical memory is a contiguous array of up to 1,048,576 bytes (one megabyte) addressed by pin A_0 through A_{19} and $\overline{BHE}$. Address bits A_{20}-A_{23} may not always be zero in real mode. A_{20}-A_{23} should not be used by the system while the 80C286 is operating in Real Mode.

The selector portion of a pointer is interpreted as the upper 16-bits of a 20-bit segment address. The lower four bits of the 20-bit segment address are always zero. Segment addresses, therefore, begin on multiples of 16 bytes. See Figure 6 for a graphic representation of address information.

All segments in real address mode are 64K bytes in size and may be read, written, or executed. An exception or interrupt can occur if data operands or instructions attempt to wrap around the end of a segment (e.g. a word with its low order byte at offset FFFF(H) and its high order byte at offset 0000(H)). If, in real address mode, the information contained in a segment does not use the full 64K bytes, the unused end of the segment may be overlaid by another segment to reduce physical memory requirements.

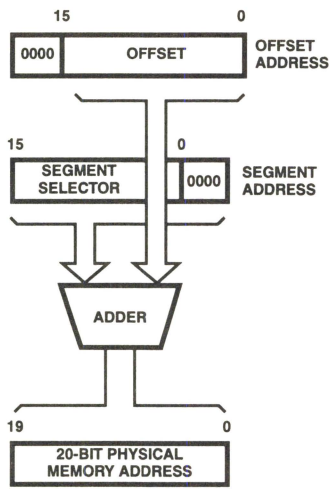
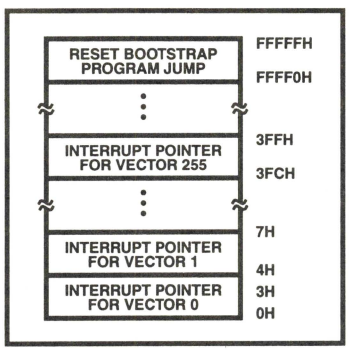


FIGURE 6. 80C286 REAL ADDRESS MODE ADDRESS CALCULATION

Reserved Memory Locations

The 80C286 reserves two fixed areas of memory in real address mode (see Figure 7); system initialization area and interrupt table area. Locations from addresses FFFF0(H) through FFFFF(H) are reserved for system initialization. Initial execution begins at location FFFF0(H). Locations 00000(H) through 003FF(H) are reserved for interrupt vectors.



INITIAL CS:IP VALUE IS F000:FFF0

FIGURE 7. 80C286 REAL ADDRESS MODE INITIALLY RESERVED MEMORY LOCATIONS

Interrupts

Table 9 shows the interrupt vectors reserved for exceptions and interrupts which indicate an addressing error. The exceptions leave the CPU in the state existing before attempting to execute the failing instruction (except for PUSH, POP, PUSHA, or POPA). Refer to the next section on protected mode initialization for a discussion on exception 8.

Protected Mode Initialization

To prepare the 80C286 for protected mode, the LIDT instruction is used to load the 24-bit interrupt table base and 16-bit limit for the protected mode interrupt table. This instruction can also set a base and limit for the interrupt vector table in real address mode. After reset, the interrupt table base is initialized to 000000(H) and its size set to 03FF(H). These values are compatible with 80C86 and 80C88 software. LIDT should only be executed in preparation for protected mode.

Shutdown

Shutdown occurs when a severe error is detected that prevents further instruction processing by the CPU. Shutdown and halt are externally signalled via a halt bus operation. They can be distinguished by A_1 HIGH for halt and A_1 LOW for shutdown. In real address mode, shutdown can occur under two conditions:

- Exceptions 8 or 13 happen and the IDT limit does not include the interrupt vector.
- A CALL INT or PUSH instruction attempts to wrap around the stack segment when SP is not even.

An NMI input can bring the CPU out of shutdown if the IDT limit is at least 000F(H) and SP is greater than 0005(H), otherwise shutdown can only be exited via the RESET input.

Protected Virtual Address Mode

The 80C286 executes a fully upward-compatible superset of the 80C86 instruction set in protected virtual address mode (protected mode). Protected mode also provides memory management and protection mechanisms and associated instructions.

The 80C286 enters protected virtual address mode from real address mode by setting the PE (Protection Enable) bit of the machine status word with the Load Machine Status Word (LMSW) instruction. Protected mode offers extended physical and virtual memory address space, memory protection mechanisms, and new operations to support operating systems and virtual memory.

All registers, instructions, and addressing modes described in the 80C286 Base Architecture section of this Functional Description remain the same. Programs for the 80C86, 80C88, and real address mode 80C286 can be run in protected mode; however, embedded constants for segment selectors are different.

Memory Size

The protected mode 80C286 provides a 1 gigabyte virtual address space per task mapped into a 16 megabyte physical address space defined by the address pins A_{23}-A_0 and $\overline{BHE}$. The virtual address space may be larger than the physical address space since any use of an address that does not map to a physical memory location will cause a restartable exception.

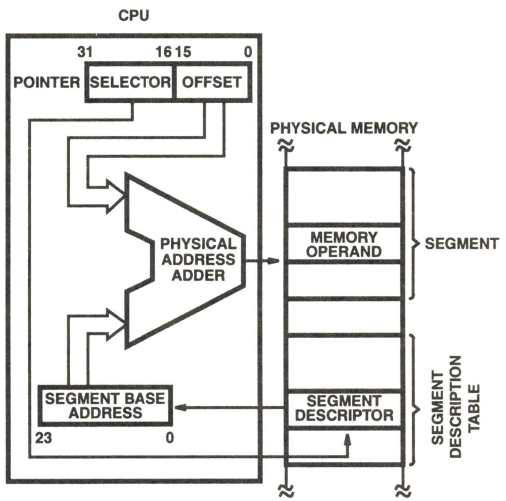


FIGURE 8. PROTECTED MODE MEMORY ADDRESSING

Memory Addressing

As in real address mode, protected mode uses 32-bit pointers, consisting of 16-bit selector and offset components. The selector, however, specifies an index into a memory resident table rather than the upper 16-bits of a real memory address. The 24-bit base address of the desired segment is obtained

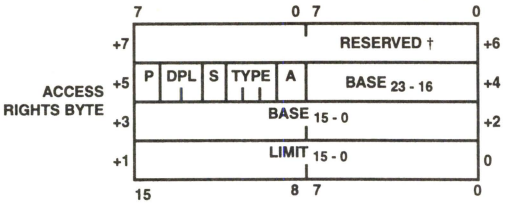
from the tables in memory. The 16-bit offset is added to the segment base address to form the physical address as shown in Figure 8. The tables are automatically referenced by the CPU whenever a segment register is loaded with a selector. All 80C286 instructions which load a segment register will reference the memory based tables without additional software. The memory based tables contain 8 byte values called descriptors.

Descriptors

Descriptors define the use of memory. Special types of descriptors also define new functions for transfer of control and task switching. The 80C286 has segment descriptors for code, stack and data segments, and system control descriptors for special system data segments and control transfer operations. Descriptor accesses are performed as locked bus operations to assure descriptor integrity in multi-processor systems.

Code and Data Segment Descriptors (S = 1)

Besides segment base addresses, code and data descriptors contain other segment attributes including segment size (1 to 64K bytes), access rights (read only, read/write, execute only, and execute/read), and presence in memory (for virtual memory systems) (See Table 10). Any segment usage violating a segment attribute indicated by the segment descriptor will prevent the memory cycle and cause an exception or interrupt.



† MUST BE SET TO 0 FOR COMPATIBILITY WITH FUTURE UPGRADES

FIGURE 9. CODE OR DATA SEGMENT DESCRIPTOR

Code and data (including stack data) are stored in two types of segments: code segments and data segments. Both types are identified and defined by segment descriptors (S = 1). Code segments are identified by the executable (E) bit set to 1 in the descriptor access rights byte. The access rights byte of both code and data segment descriptor types have three fields in common: present (P) bit, Descriptor Privilege Level (DPL), and accessed (A) bit. If P = 0, any attempted use of this segment will cause a not-present exception. DPL specifies the privilege level of the segment descriptor. DPL controls when the descriptor may be used by a task (refer to privilege discussion below). The A bit shows whether the segment has been previously accessed for usage profiling, a necessity for virtual memory systems. The CPU will always set this bit when accessing the descriptor.

TABLE 10. CODE AND DATA SEGMENT DESCRIPTOR FORMATS - ACCESS RIGHTS BYTE DEFINITION

	BIT POSITION	NAME	FUNCTION		
	7	Present (P)	P = 1	Segment is mapped into physical memory.	
			P = 0	No mapping to physical memory exits, base and limit are not used.	
	6 - 5	Descriptor Privilege Level (DPL)		Segment privilege attribute used in privilege tests.	
	4	Segment Descriptor (S)	S = 1	Code or Data (includes stacks) segment descriptor	
			S = 0	System Segment Descriptor or Gate Descriptor	
Type Field Definition	3	Executable (E)	E = 0	Data segment descriptor type is:	If Data Segment (S = 1, E = 0)
	2	Expansion Direction (ED)	ED = 0	Expand up segment, offsets must be ≤ limit.	
			ED = 1	Expand down segment, offsets must be > limit.	
	1	Writable (W)	W = 0	Data segment may not be written into.	
			W = 1	Data segment may be written into.	
	3	Executable (E)	E = 1	Code Segment Descriptor type is:	If Code Segment (S = 1, E = 1)
	2	Conforming (C)	C = 1	Code segment may only be executed when CPL ≥ DPL and CPL remains unchanged.	
	1	Readable (R)	R = 0	Code segment may not be read.	
			R = 1	Code segment may be read.	
	0	Accessed (A)	A = 0	Segment has not been accessed.	
			A = 1	Segment selector has been loaded into segment register or used by selector test instructions.	

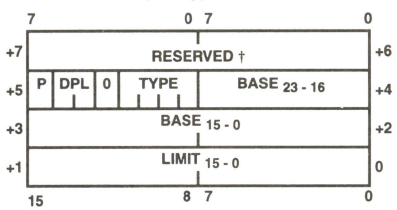
Data segments (S = 1, E = 0) may be either read-only or read-write as controlled by the W bit of the access rights byte. Read-only (W = 0) data segments may not be written into. Data segments may grow in two directions, as determined by the Expansion Direction (ED) bit: upwards (ED = 0) for data segments, and downwards (ED = 1) for a segment containing a stack. The limit field for a data segment descriptor is interpreted differently depending on the ED bit (see Table 10).

A code segment (S = 1, E = 1) may be execute-only or execute/read as determined by the Readable (R) bit. Code segments may never be written into and execute-only code segments (R = 0) may not be read. A code segment may also have an attribute called conforming (C). A conforming code segment may be shared by programs that execute at different privilege levels. The DPL of a conforming code segment defines the range of privilege levels at which the segment may be executed (refer to privilege discussion below). The limit field identifies the last byte of a code segment.

System Segment Descriptors (S = 0, Type = 1-3)

In addition to code and data segment descriptors, the protected mode 80C286 defines System Segment Descriptors. These descriptors define special system data segments which contain a table of descriptors (Local Descriptor Table Descriptor) or segments which contain the execution state of a task (Task State Segment Descriptor).

Table 11 gives the formats for the special system data segment descriptors. The descriptors contain a 24-bit base address of the segment and a 16-bit limit. The access byte defines the type of descriptor, its state and privilege level. The descriptor contents are valid and the segment is in physical memory if P = 1. If P = 0, the segment is not valid. The DPL field is only used in Task State Segment descriptors and indicates the privilege level at which the descriptor may be used (see Privilege). Since the Local Descriptor Table descriptor may only be used by a special privileged instruction, the DPL field is not used. Bit 4 of the access byte is 0 to indicate that it is a system control descriptor. The type field specifies the descriptor type as indicated in Table 11.



† MUST BE SET TO 0 FOR COMPATIBILITY WITH FUTURE UPGRADES

FIGURE 10. SYSTEM SEGMENT DESCRIPTOR

TABLE 11. SYSTEM SEGMENT DESCRIPTOR FORMAT FIELDS

NAME	VALUE	DESCRIPTION
TYPE	1	Available Task State Segment (TSS)
	2	Local Descriptor Table
	3	Busy Task State Segment (TSS)
P	0	Descriptor contents are not valid
	1	Descriptor contents are valid
DPL	0-3	Descriptor Privilege Level
BASE	24-Bit Number	Base Address of special system data segment in real memory
LIMIT	16-Bit Number	Offset of last byte in segment

Gate Descriptors (S = 0, Type = 4-7)

Gates are used to control access to entry points within the target code segment. The gate descriptors are call gates, task gates, interrupt gates and trap gates. Gates provide a level of indirection between the source and destination of the control transfer. This indirection allows the CPU to automatically perform protection checks and control entry point of the destination. Call gates are used to change privilege levels (see Privilege), task gates are used to perform a task switch, and interrupt and trap gates are used to specify interrupt service routines. The interrupt gate disables interrupts (resets IF) while the trap gate does not.

Table 12 shows the format of the gate descriptors. The descriptor contains a destination pointer that points to the descriptor of the target segment and the entry point offset. The destination selector in an interrupt gate, trap gate, and call gate must refer to a code segment descriptor. These gate descriptors contain the entry point to prevent a program from constructing and using an illegal entry point. Task gates may only refer to a task state segment. Since task gates invoke a task switch, the destination offset is not used in the task gate.

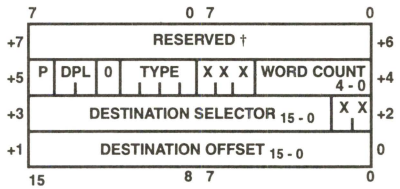
Exception 13 is generated when the gate is used if a destination selector does not refer to the correct descriptor type. The word count field is used in the call gate descriptor to indicate the number of parameters (0-31 words) to be automatically copied from the caller's stack to the stack of the called routine when a control transfer changes privilege levels. The word count field is not used by any other gate descriptor.

The access byte format is the same for all descriptors. P = 1 indicates that the gate contents are valid. P = 0 indicates the contents are not valid and causes exception 11 if referenced. DPL is the descriptor privilege level and specifies when this descriptor may be used by a task (refer to privilege discussion below). Bit 4 must equal 0 to indicate a system control descriptor. The type field specifies the descriptor type as indicated in Table 12.

Segment Descriptor Cache Registers

A segment descriptor cache register is assigned to each of the four segment registers (CS, SS, DS, ES). Segment descriptors are automatically loaded (cached) into a segment descriptor cache register (Figure 12) whenever the associated segment register is loaded with a selector.

Only segment descriptors may be loaded into segment descriptor cache registers. Once loaded, all references to that segment of memory use the cached descriptor information instead of reaccessing the descriptor. The descriptor cache registers are not visible to programs. No instructions exist to store their contents. They only change when a segment register is loaded.



† MUST BE SET TO 0 FOR COMPATIBILITY WITH FUTURE UPGRADES

FIGURE 11. GATE DESCRIPTOR

TABLE 12. GATE DESCRIPTOR FORMAT FIELD

NAME	VALUE	DESCRIPTION
TYPE	4	Call Gate
	5	Task Gate
	6	Interrupt Gate
	7	Trap Gate
P	0	Descriptor Contents are not valid
	1	Descriptor Contents are valid
DPL	0 - 3	Descriptor Privilege Level
WORD COUNT	0 - 31	Number of words to copy from callers stack to called procedures stack. Only used with call gate.
DESTINATION SELECTOR	16-Bit Selector	Selector to the target code segment (call, interrupt or selector Trap Gate). Selector to the target task state segment (Task Gate).
DESTINATION OFFSET	16-Bit Offset	Entry point within the target code segment

Selector Fields

A protected mode selector has three fields: descriptor entry index, local or global descriptor table indicator (T_I), and selector privilege (RPL) as shown in Figure 13. These fields select one of two memory based tables of descriptors, select the appropriate table entry and allow high-speed testing of the selector's privilege attribute (refer to privilege discussion below).

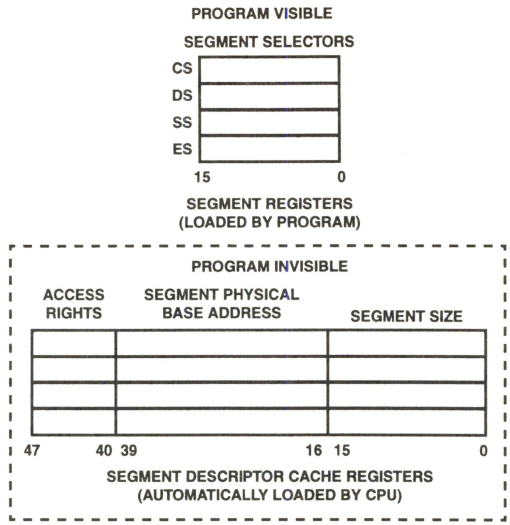
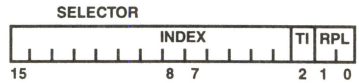


FIGURE 12. DESCRIPTOR CACHE REGISTERS



BITS	NAME	FUNCTION
1 - 0	Requested Privilege Level (RPL)	Indicates Selector Privilege Level Desired
2	Table Indicator (TI)	TI = 0 Use Global Descriptor Table (GDT) TI = 1 Use Local Descriptor Table (LDT)
15 - 3	Index	Select Descriptor Entry In Table

FIGURE 13. SELECTOR FIELDS

Local and Global Descriptor Tables

Two tables of descriptors, called descriptor tables, contain all descriptors accessible by a task at any given time. A descriptor table is a linear array of up to 8192 descriptors. The upper 13 bits of the selector value are an index into a descriptor table. Each table has a 24-bit base register to locate the descriptor table in physical memory and a 16-bit limit register that confine descriptor access to the defined limits of the table as shown in Figure 14. A restartable exception (13) will occur if an attempt is made to reference a descriptor outside the table limits.

One table, called the Global Descriptor table (GDT), contains descriptors available to all tasks. The other table, called the Local Descriptor Table (LDT), contains descriptors that can be private to a task. Each task may have its own private LDT. The GDT may contain all descriptor types except interrupt and trap descriptors. The LDT may contain only segment, task gate, and call gate descriptors. A segment cannot be accessed by a task if its segment descriptor does not exist in either descriptor table at the time of access.

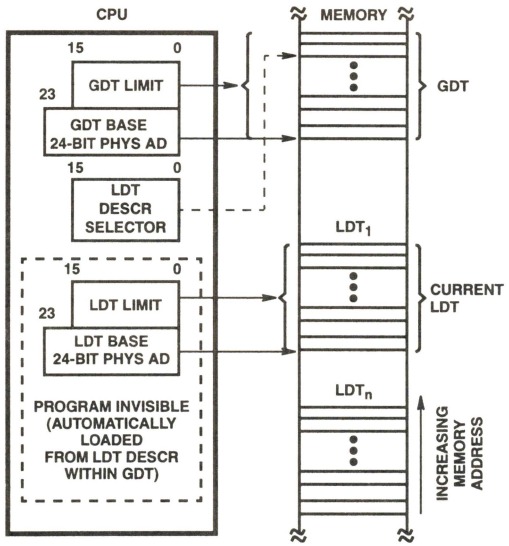
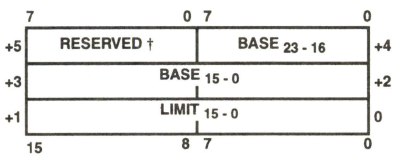


FIGURE 14. LOCAL AND GLOBAL DESCRIPTOR TABLE DEFINITION

The LGDT and LLDT instructions load the base and limit of the global and local descriptor tables. LGDT and LLDT are privileged, i.e. they may only be executed by trusted programs operating at level 0. The LGDT instruction loads a six byte field containing the 16-bit table limit and 24-bit physical base address of the Global Descriptor Table as shown in Figure 15. The LDT instruction loads a selector which refers to a Local Descriptor Table descriptor containing the base address and limit for an LDT, as shown in Table 11.



† MUST BE SET TO 0 FOR COMPATIBILITY WITH FUTURE UPGRADES

FIGURE 15. GLOBAL DESCRIPTOR TABLE AND INTERRUPT DESCRIPTOR TABLE DATA TYPE

Interrupt Descriptor Table

The protected mode 80C286 has a third descriptor table, called the Interrupt Descriptor Table (IDT) (see Figure 16), used to define up to 256 interrupts. It may contain only task gates, interrupt gates and trap gates. The IDT (Interrupt Descriptor Table) has a 24-bit physical base and 16-bit limit register in the CPU. The privileged LIDT instruction loads these registers with a six byte value of identical form to that of the LGDT instruction (see Figure 16 and Protected Mode Initialization).

References to IDT entries are made via INT instructions, external interrupt vectors, or exceptions. The IDT must be at least 256 bytes in size to allocate space for all reserved interrupts.

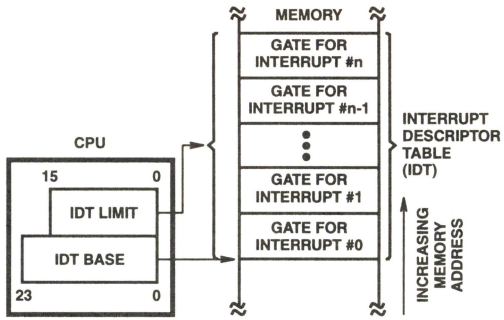
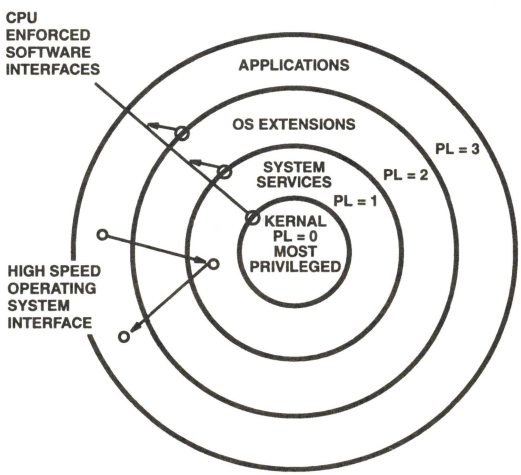


FIGURE 16. INTERRUPT DESCRIPTOR TABLE DEFINITION

Privilege

The 80C286 has a four-level hierarchical privilege system which controls the use of privileged instructions and access to descriptors (and their associated segments) within a task. Four-level privilege, as shown in Figure 17, is an extension of the users/supervisor mode commonly found in minicomputers. The privilege levels are numbered 0 through 3. Level 0 is the most privileged level. Privilege levels provide protection within a task. (Tasks are isolated by providing private LDT's for each task.) Operating system routines, interrupt handlers, and other system software can be included and protected within the virtual address space of each task using the four levels of privilege. Each task in the system has a separate stack for each of its privilege levels.

Tasks, descriptors, and selectors have a privilege level attribute that determines whether the descriptor may be used. Task privilege affects the use of instructions and descriptors. Descriptor and selector privilege only affect access to the descriptor.



NOTE: PL becomes numerically lower as privilege level increases.

FIGURE 17. HIERARCHICAL PRIVILEGE LEVELS

Task Privilege

A task always executes at one of the four privilege levels. The task privilege level at any specific instant is called the Current Privilege Level (CPL) and is defined by the lower two bits of the CS register. CPL cannot change during execution in a single code segment. A task's CPL may only be changed by control transfers through gate descriptors to a new code segment (See Control Transfer). Tasks begin executing at the CPL value specified by the code segment selector within TSS when the task is initiated via a task switch operation (See Figure 18). A task executing at Level 0 can access all data segments defined in the GDT and the task's LDT and is considered the most trusted level. A task executing a Level 3 has the most restricted access to data and is considered the least trusted level.

Descriptor Privilege

Descriptor privilege is specified by the Descriptor Privilege Level (DPL) field of the descriptor access byte. DPL specifies the least trusted task privilege level (CPL) at which a task may access the descriptor. Descriptors with DPL = 0 are the most protected. Only tasks executing at privilege level 0 (CPL = 0) may access them. Descriptors with DPL = 3 are the least protected (i.e. have the least restricted access) since tasks can access them when CPL = 0, 1, 2, or 3). This rule applies to all descriptors, except LDT descriptors.

Selector Privilege

Selector privilege is specified by the Requested Privilege Level (RPL) field in the least significant two bits of a selector. Selector RPL may establish a less trusted privilege level than the current privilege level for the use of a selector. This level is called the task's effective privilege level (EPL). RPL can only reduce the scope of a task's access to data with this selector. A task's effective privilege is the numeric maximum of RPL and CPL. A selector with RPL = 0 imposes no additional restriction on its use while a selector with RPL = 3 can only refer to segments at privilege Level 3 regardless of the task's CPL. RPL is generally used to verify that pointer parameters passed to a more trusted procedure are not allowed to use data at a more privileged level than the caller (refer to pointer testing instructions).

Descriptor Access and Privilege Validation

Determining the ability of a task to access a segment involves the type of segment to be accessed, the instruction used, the type of descriptor used and CPL, RPL, and DPL. The two basic types of segment accesses are control transfer (selectors loaded into CS) and data (selectors loaded into DS, ES or SS).

Data Segment Access

Instructions that load selectors into DS and ES must refer to a data segment descriptor or readable code segment descriptor. The CPL of the task and the RPL of the selector must be the same as or more privileged (numerically equal to or lower than) than the descriptor DPL. In general, a task can only access data segments at the same or less privileged levels than the CPL or RPL (whichever is numerically higher) to prevent a program from accessing data it cannot be trusted to use.

An exception to the rule is a readable conforming code segment. This type of code segment can be read from any privilege level.

If the privilege checks fail (e.g. DPL is numerically less than the maximum of CPL and RPL) or an incorrect type of descriptor is referenced (e.g. gate descriptor or execute only code segment) exception 13 occurs. If the segment is not present, exception 11 is generated.

Instructions that load selectors into SS must refer to data segment descriptors for writable data segments. The descriptor privilege (DPL) and RPL must equal CPL. All other descriptor types or a privilege level violation will cause exception 13. A not present fault causes exception 12.

TABLE 13. DESCRIPTOR TYPES USED FOR CONTROL TRANSFER

CONTROL TRANSFER TYPES	OPERATION TYPES	DESCRIPTOR REFERENCED	DESCRIPTOR TABLE
Intersegment within the same privilege levels	JMP, CALL, RET, IRET (Note 4)	Code Segment	GDT/LDT
Intersegment to the same or higher privilege level interrupt within task may change CPL	CALL	Call Gate	GDT/LDT
	Interrupt Instruction, Exception External Interrupt	Trap or Interrupt Gate	IDT
Intersegment to a lower privilege level (changes task CPL)	RET, IRET (Note 4)	Code Segment	GDT/LDT
Task Switch	CALL, JMP	Task State Segment	GDT
	CALL, JMP	Task Gate	GDT/LDT
	IRET (Note 5) Interrupt Instruction, Exception External Interrupt	Task Gate	IDT

NOTES:

4. NT (Nested Task bit of flag word) = 0
5. NT (Nested Task bit of flag word) = 1

Control Transfer

Four types of control transfer can occur when a selector is loaded into CS by a control transfer operation (see Table 13). Each transfer type can only occur if the operation which loaded the selector references the correct descriptor type. Any violation of these descriptor usage rules (e.g. JMP through a call gate or RET to a Task State Segment) will cause exception 13.

The ability to reference a descriptor for control transfer is also subject to rules of privilege. A CALL or JUMP instruction may only reference a code segment descriptor with DPL equal to the task CPL or a conforming segment with DPL of equal or greater privilege than CPL. The RPL of the selector used to reference the code descriptor must have as much privilege as CPL.

RET and IRET instructions may only reference code segment descriptors with descriptor privilege equal to or less privileged than the task CPL. The selector loaded into CS is the return address from the stack. After the return, the selector RPL is the task's new CPL. If CPL changes, the old stack pointer is popped after the return address.

When a JMP or CALL references a Task State Segment descriptor, the descriptor DPL must be the same or less privileged than the task's CPL. Reference to a valid Task State Segment descriptor causes a task switch (see Task Switch Operation). Reference to a Task State Segment descriptor at a more privileged level than the task's CPL generates exception 13.

When an instruction or interrupt references a gate descriptor, the gate DPL must have the same or less privilege than the task CPL. If DPL is at a more privileged level than CPL, exception 13 occurs. If the destination selector contained in the gate references a code segment descriptor, the code segment descriptor DPL must be the same or more privileged than the task CPL. If not, Exception 13 is issued. After the control transfer, the code segment descriptors DPL is the task's new CPL. If the destination selector in the gate references a task state segment, a task switch is automatically performed (see Task Switch Operation).

The privilege rules on control transfer require:

- JMP or CALL direct to a code segment (code segment descriptor) can only be a conforming segment with DPL of equal or greater privilege than CPL or a non-conforming segment at the same privilege level.
- Interrupts within the task, or calls that may change privilege levels, can only transfer control through a gate at the same or a less privileged level than CPL to a code segment at the same or more privileged level than CPL.
- Return instructions that don't switch tasks can only return control to a code segment at the same or less privileged level.
- Task switch can be performed by a call, jump or interrupt which references either a task gate or task state segment at the same or less privileged level.

Privilege Level Changes

Any control transfer that changes CPL within the task, causes a change of stacks as part of the operation. Initial values of SS:SP for privilege levels 0, 1, and 2 are kept in the task state segment (refer to Task Switch Operation). During a JMP or CALL control transfer, the new stack pointer is loaded into the SS and SP registers and the previous stack pointer is pushed onto the new stack.

When returning to the original privilege level, its stack is restored as part of the RET or IRET instruction operation. For subroutine calls that pass parameters on the stack and cross privilege levels, a fixed number of words, as specified in the gate, are copied from the previous stack to the current stack. The inter-segment RET instruction with a stack adjustment value will correctly restore the previous stack pointer upon return.

Protection

The 80C286 includes mechanisms to protect critical instructions that effect the CPU execution state (e.g. HLT) and code or data segments from improper usage. These protection mechanisms are grouped into three forms:

- Restricted usage of segments (e.g. no write allowed to read-only data segments). The only segments available for use are defined by descriptors in the Local Descriptor Table (LDT) and Global Descriptor Table (GDT).
- Restricted access to segments via the rules of privilege and descriptor usage.
- Privileged instructions or operations that may only be executed at certain privilege levels as determined by the CPL and I/O Privilege Level (IOPL). The IOPL is defined by bits 14 and 13 of the flag word.

These checks are performed for all instructions and can be split into three categories: segment load checks (Table 14), operand reference checks (Table 15), and privileged instruction checks (Table 16). Any violation of the rules shown will result in an exception. A not-present exception related to the stack segment causes exception 12.

TABLE 14. SEGMENT REGISTER LOAD CHECKS

ERROR DESCRIPTION	EXCEPTION NUMBER
Descriptor table limit exceeded	13
Segment descriptor not-present	11 or 12
Privilege rules violated	13
Invalid descriptor/segment type segment register load: - Read only data segment load to SS - Special control descriptor load to DS, ES, SS - Execute only Segment load to DS, ES, SS - Data segment load to CS - Read/Execute code segment load SS	13

TABLE 15. OPERAND REFERENCE CHECKS

ERROR DESCRIPTION	EXCEPTION NUMBER
Write into code segment	13
Read from execute-only code segment	13
Write to read-only data segment	13
Segment limit exceeded (See Note)	12 or 13

NOTE: Carry out in offset calculations is ignored.

TABLE 16. PRIVILEGED INSTRUCTION CHECKS

ERROR DESCRIPTION	EXCEPTION NUMBER
CPL ≠ 0 when executing the following instructions: LIDT, LLDT, LGDT, LTR, LMSW, CTS, HLT	13
CPT > IOPL when executing the following instructions: INS, IN, OUTS, OUT, STI, CLI, LOCK	13

The IRET and POPF instructions do not perform some of their defined functions if CPL is not of sufficient privilege (numerically small enough). Precisely these are:

- The IF bit is not changed if CPL is greater than IOPL.
- The IOPL field of the flag word is not changed if CPL is greater than 0.

No exceptions or other indication are given when these conditions occur.

Exceptions

The 80C286 detects several types of exceptions and interrupts in protected mode (see Table 17). Most are restartable after the exceptional condition is removed. Interrupt handlers for most exceptions can read an error code, pushed on the stack after the return address, that identifies the selector involved (0 if none). The return address normally points to the failing instruction including all leading prefixes. For a processor extension segment overrun exception, the return address will not point at the ESC instruction that caused the exception; however, the processor extension registers may contain the address of the failing instruction.

These exceptions indicate a violation to privilege rules or usage rules has occurred. Restart is generally not attempted under those conditions.

All these checks are performed for all instructions and can be split into three categories: segment load checks (Table 14), operand reference checks (Table 15), and privileged instruction checks (Table 16). Any violation of the rules shown will result in an exception. A not-present exception causes exception 11 or 12 and is restartable.

SPECIAL OPERATIONS

Task Switch Operation

The 80C286 provides a built-in task switch operation which saves the entire 80C286 execution state (registers, address space, and a link to the previous task), loads a new execution state, and commences execution in the new task. Like gates, the task switch operation is invoked by executing an inter-segment JMP or CALL instruction which refers to a Task State Segment (TSS) or task gate descriptor in the GDT or LDT. An INT instruction, exception, or external interrupt may also invoke the task switch operation by selecting a task gate descriptor in the associated IDT descriptor entry.

The TSS descriptor points at a segment (see Figure 18) containing the entire 80C286 execution state while a task gate descriptor contains a TSS selector. The limit field of the descriptor must be greater than 002B(H).

Each task must have a TSS associated with it. The current TSS is identified by a special register in the 80C286 called the Task Register (TR). This register contains a selector referring to the task state segment descriptor that defines the current TSS. A hidden base and limit register associated with TR are loaded whenever TR is loaded with a new selector. The IRET instruction is used to return control to the task that called the current task or was interrupted. Bit 14 in the flag register is called the Nested Task (NT) bit. It controls the

TABLE 17. PROTECTED MODE EXCEPTIONS

INTERRUPT VECTOR	FUNCTION	RETURN ADDRESS AT FALLING INSTRUCTION?	ALWAYS RESTARTABLE?	ERROR CODE ON STACK?
8	Double exception detected	Yes	No (Note 7)	Yes
9	Processor extension segment overrun	No	No (Note 7)	No
10	Invalid task state segment	Yes	Yes	Yes
11	Segment not present	Yes	Yes	Yes
12	Stack segment overrun or stack segment not present	Yes	Yes (Note 6)	Yes
13	General protection	Yes	No (Note 7)	Yes

NOTES:

6. When a PUSHA or POPA instruction attempts to wrap around the stack segment, the machine state after the exception will not be restartable because stack segment wrap around is not permitted. This condition is identified by the value of the saved SP being either 0000(H), 0001(H), FFFE(H), or FFFF(H).
7. These exceptions indicate a violation to privilege rules or usage rules has occurred. Restart is generally not attempted under those conditions.

function of the IRET instruction. If NT = 0, the IRET instruction performs the regular current task by popping values off the stack; when NT = 1, IRET performs a task switch operation back to the previous task.

When a CALL, JMP, or INT instruction initiates a task switch, the old (except for case of JMP) and new TSS will be marked busy and the back link field of the new TSS set to the old TSS selector. The NT bit of the new task is set by CALL or INT initiated task switches. An interrupt that does not cause a task switch will clear NT. NT may also be set or cleared by POPF or IRET instructions.

The task state segment is marked busy by changing the descriptor type field from Type 1 to Type 3. Use of a selector that references a busy task state segment causes Exception 13.

Processor Extension Context Switching

The context of a processor extension is not changed by the task switch operation. A processor extension context need only be changed when a different task attempts to use the processor extension (which still contains the context of a previous task). The 80C286 detects the first use of a processor extension after a task switch by causing the processor extension not present exception (7). The interrupt handler may then decide whether a context change is necessary.

Whenever the 80C286 switches tasks, it sets the Task Switched (TS) bit of the MSW. TS indicates that a processor extension context may belong to a different task than the current one. The processor extension not present exception (7) will occur when attempting to execute an ESC or WAIT instruction if TS = 1 and a processor extension is present (MP = 1 in MSW).

Pointer Testing Instructions

The 80C286 provides several instructions to speed pointer testing and consistency checks for maintaining system integrity (see Table 18). These instructions use the memory management hardware to verify that a selector value refers to an appropriate segment without risking an exception. A condition flag (ZF) indicates whether use of the selector or segment will cause an exception.

Double Fault and Shutdown

If two separate exceptions are detected during a single instruction execution, the 80C286 performs the double fault exception (8). If an exception occurs during processing of the double fault exception, the 80C286 will enter shutdown. During shutdown no further instructions or exceptions are processed. Either NMI (CPU remains in protected mode) or RESET (CPU exits protected mode) can force the 80C286 out of shutdown. Shutdown is externally signalled via a HALT bus operation with A_1 LOW.

Protected Mode Initialization

The 80C286 initially executes in real address mode after RESET. To allow initialization code to be placed at the top of physical memory. A_{23-20} will be HIGH when the 80C286 performs memory references relative to the CS register until CS is changed. A_{23-20} will be zero for references to the DS, ES, or SS segments. Changing CS in real address mode will force A_{23-20} LOW whenever CS is used again. The initial CS:IP value of F000:FFF0 provides 64K bytes of code space for initialization code without changing CS.

Protected mode operation requires several registers to be initialized. The GDT and IDT base registers must refer to a valid GDT and IDT. After executing the LMSW instruction to set PE, the 80C286 must immediately execute an intrasegment JMP instruction to clear the instruction queue of instructions decoded in real address mode.

To force the 80C286 CPU registers to match the initial protected mode state assumed by software, execute a JMP instruction with a selector referring to the initial TSS used in the system. This will load the task register, local descriptor table register, segment registers and initial general register state. The TR should point at a valid TSS since any task switch operation involves saving the current task state.

TABLE 18. 80C286 POINTER TEST INSTRUCTIONS

INSTRUCTION	OPERANDS	FUNCTION
ARPL	Selector, Register	Adjust Requested Privilege Level: adjusts the RPL of the selector to the numeric maximum of current selector RPL value and the RPL value in the register. Set zero flag if selector RPL was changed by ARPL.
VERR	Selector	VERify for Read: sets the zero flag if the segment referred to by the selector can be read.
VERW	Selector	VERify for Write: sets the zero flag if the segment referred to by the selector can be written.
LSL	Register, Selector	Load Segment Limit: reads the segment limit into the register if privilege rules and descriptor type allow. Set zero flag if successful.
LAR	Register, Selector	Load Access Rights: reads the descriptor access rights byte into the register if privilege rules allow. Set zero flag if successful.

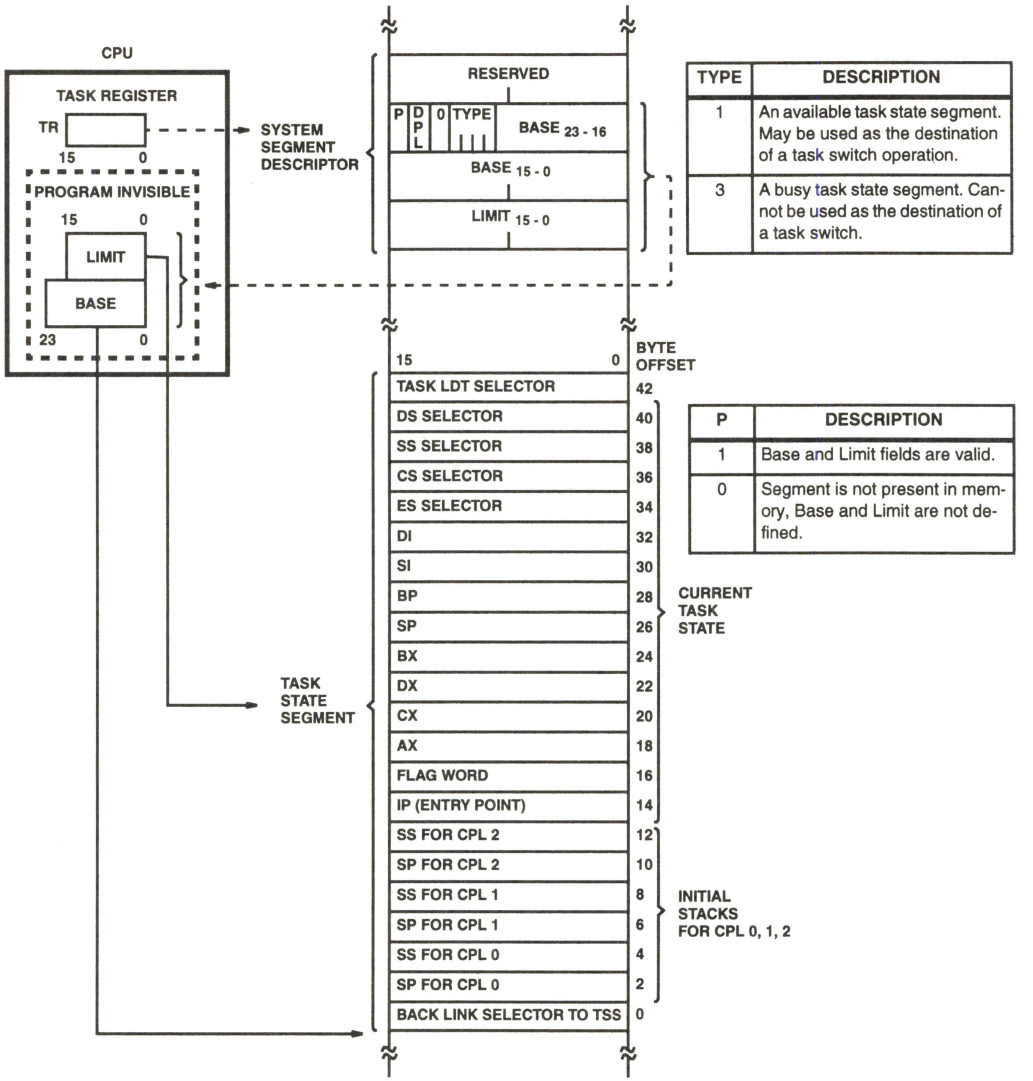


FIGURE 18. TASK STATE SEGMENT AND TSS REGISTERS

System Interface

The 80C286 system interface appears in two forms: a local bus and a system bus. The local bus consists of address, data, status, and control signals at the pins of the CPU. A system bus is any buffered version of the local bus. A system bus may also differ from the local bus in terms of coding of status and control lines and/or timing and loading of signals.

Bus Interface Signals and Timing

The 80C286 microsystems local bus interfaces the 80C286 to local memory and I/O components. The interface has 24 address lines, 16 data lines, and 8 status and control signals.

The 80C286 CPU, 82C284 clock generator, 82C288 bus controller, 82289 bus arbiter, 82C86H/87H transceivers, and 82C82/83H latches provide a buffered and decoded system bus interface. The 82C284 generates the system clock and

synchronizes $\overline{\text{READY}}$ and RESET. The 82C288 converts bus operation status encoded by the 80C286 into command and bus control signals. The 82289 bus arbiter generates Multibus™ bus arbitration signals. These components can provide the critical timing required for most system bus interfaces including the Multibus.

Bus Hold Circuitry

To avoid high current conditions caused by floating inputs to CMOS devices, and to eliminate the need for pull-up/down resistors, "bus-hold" circuitry has been used on the 80C286 pins 4-6, 36-51 and 66-68 (See Figure 19A and 19B). The circuit shown in Figure 19A will maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source which goes to a high impedance state). The circuit shown in Figure 19B will maintain a high impedance logic one state if no driving source is present. To overdrive the "bus-hold" circuits, an external driver must be capable of sinking or sourcing approximately 400 microamps at valid input voltage levels. Since this "bus-hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible, and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

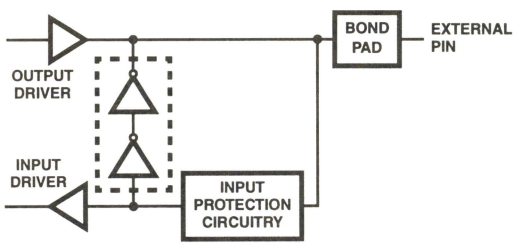


FIGURE 19A. BUS HOLD CIRCUITRY, PINS 36-51, 66, 67

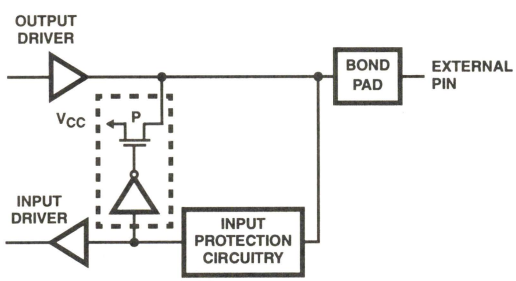


FIGURE 19B. BUS HOLD CIRCUITRY, PINS 4-6, 68

Physical Memory and I/O Interface

A maximum of 16 megabytes of physical memory can be addressed in protected mode. One megabyte can be addressed in real address mode. Memory is accessible as bytes or words. Words consist of any two consecutive bytes addressed with the least significant byte stored in the lowest address. Byte transfers occur on either half of the 16-bit local data bus. Even bytes are accessed over D_{7-0} while odd bytes are transferred over D_{15-8}. Even addressed words are transferred over D_{15-0} in one bus cycle, while odd addressed word require two bus operations. The first transfers data on D_{15-8}, and the second transfers data on D_{7-0}. Both byte data transfers occur automatically, transparent to software.

Two bus signals, A_0 and $\overline{\text{BHE}}$, control transfers over the lower and upper halves of the data bus. Even address byte transfers are indicated by A_0 LOW and $\overline{\text{BHE}}$ HIGH. Odd address byte transfers are indicated by A_0 HIGH and $\overline{\text{BHE}}$ LOW. Both A_0 and $\overline{\text{BHE}}$ are LOW for even address word transfers.

The I/O address space contains 64K addresses in both modes. The I/O space is accessible as either bytes or words, as is memory. Byte wide peripheral devices may be attached to either the upper or lower byte of the data bus. Byte-wide I/O devices attached to the upper data byte (D_{15-8}) are accessed with odd I/O addresses. Devices on the lower data byte are accessed with even I/O addresses. An interrupt controller such as Harris's 82C59A must be connected to the lower data byte (D_{7-0}) for proper return of the interrupt vector.

Bus Operation

The 80C286 uses a double frequency system clock (CLK input) to control bus timing. All signals on the local bus are measured relative to the system CLK input. The CPU divides the system clock by 2 to produce the internal processor clock, which determines bus state. Each processor clock is composed of two system clock cycles named phase 1 and phase 2. The 82C284 clock generator output (PCLK) identifies the next phase of the processor clock. (See Figure 20.)

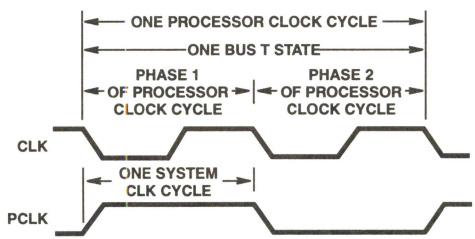


FIGURE 20. SYSTEM AND PROCESSOR CLOCK RELATIONSHIPS

Six types of bus operations are supported; memory read, memory write, I/O read, I/O write, interrupt acknowledge, and halt/shutdown. Data can be transferred at a maximum rate of one word per two processor clock cycles.

The 80C286 bus has three basic states: idle (T_I), send status (T_S), and perform command (T_C). The 80C286 CPU also has a fourth local bus state called hold (T_H). T_H indicates that the 80C286 has surrendered control of the local bus to another bus master in response to a HOLD request.

Each bus state is one processor clock long. Figure 21 shows the four 80C286 local bus states and allowed transitions.

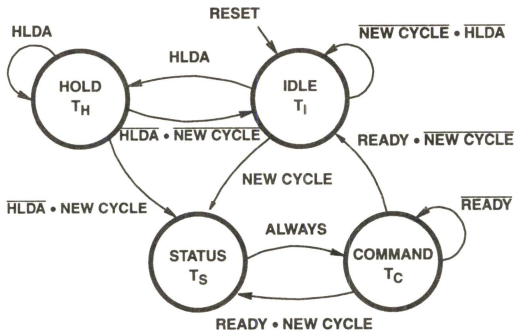


FIGURE 21. 80C286 BUS STATES

Bus States

The idle (T_I) state indicates that no data transfers are in progress or requested. The first active state T_S is signaled by status line $\overline{S1}$ or $\overline{S0}$ going LOW and identifying phase 1 of the processor clock. During T_S, the command encoding, the address, and data (for a write operation) are available on the 80C286 output pins. The 82C288 bus controller decodes the status signals and generates Multibus compatible read/write command and local transceiver control signals.

After T_S, the perform command (T_C) state is entered. Memory or I/O devices respond to the bus operation during T_C, either transferring read data to the CPU or accepting write data. T_C states may be repeated as often as necessary to ensure sufficient time for the memory or I/O device to respond. The $\overline{READY}$ signal determines whether T_C is repeated. A repeated T_C state is called a wait state.

During hold (T_H), the 80C286 will float all address, data, and status output drivers enabling another bus master to use the local bus. The 80C286 HOLD input signal is used to place the 80C286 into the T_H state. The 80C286 HLDA output signal indicates that the CPU has entered T_H.

Pipelined Addressing

The 80C286 uses a local bus interface with pipelined timing to allow as much time as possible for data access. Pipelined timing allows a new bus operation to be initiated every two processor cycles, while allowing each individual bus operation to last for three processor cycles.

The timing of the address outputs is pipelined such that the address of the next bus operation becomes available during the current bus operation. Or, in other words, the first clock of the next bus operation is overlapped with the last clock of the current bus operation. Therefore, address decode and routing logic can operate in advance of the next bus operation.

External address latches may hold the address stable for the entire bus operation, and provide additional AC and DC buffering.

The 80C286 does not maintain the address of the current bus operation during all T_C states. Instead, the address for the next bus operation may be emitted during phase 2 of any T_C. The address remains valid during phase 1 of the first T_C to guarantee hold time, relative to ALE, for the address latch inputs.

Bus Control Signals

The 82C288 bus controller provides control signals; address latch enable (ALE), Read/Write commands, data transmit/receive (DT/$\overline{R}$), and data enable (DEN) that control the address latches, data transceivers, write enable, and output enable for memory and I/O systems.

The Address Latch Enable (ALE) output determines when the address may be latched. ALE provides at least one system CLK period of address hold time from the end of the previous bus operation until the address for the next bus operation appears at the latch outputs. This address hold time is required to support Multibus and common memory systems.

The data bus transceivers are controlled by 82C288 outputs Data Enable (DEN) and Data Transmit/Receive (DT/$\overline{R}$). DEN enables the data transceivers; while DT/$\overline{R}$ controls transceiver direction. DEN and DT/$\overline{R}$ are timed to prevent bus contention between the bus master, data bus transceivers, and system data bus transceivers.

Command Timing Controls

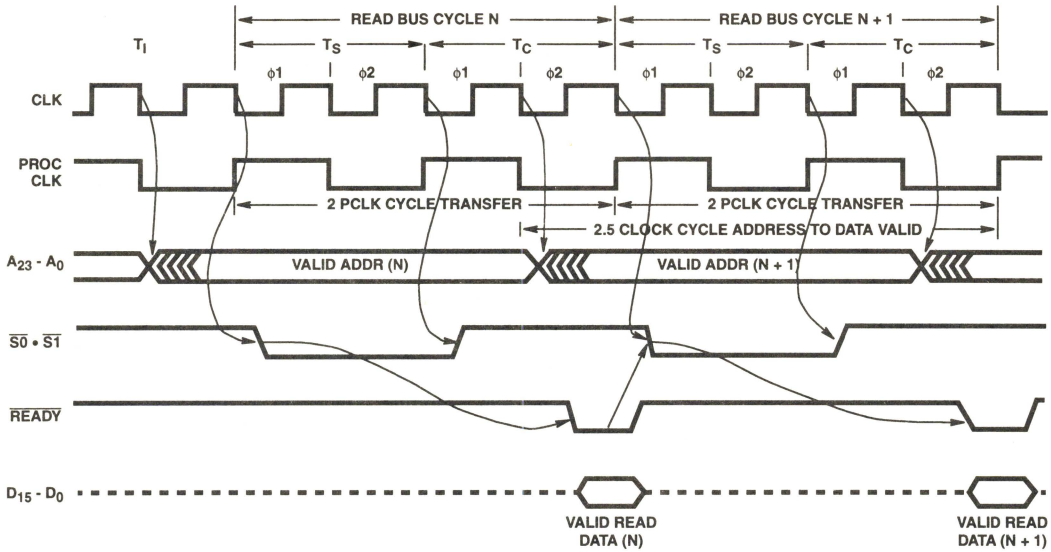
Two system timing customization options, command extension and command delay, are provided on the 80C286 local bus.

Command extension allows additional time for external devices to respond to a command and is analogous to inserting wait states on the 80C86. External logic can control the duration of any bus operation such that the operation is only as long as necessary. The $\overline{READY}$ input signal can extend any bus operation for as long as necessary.

Command delay allows an increase of address or write data setup time to system bus command active for any bus operation by delaying when the system bus command becomes active. Command delay is controlled by the 82C288 CMDLY input. After T_S, the bus controller samples CMDLY at each failing edge of CLK. If CMDLY is HIGH, the 82C288 will not activate the command signal. When CMDLY is LOW, the 82C288 will activate the command signal. After the command becomes active, the CMDLY input is not sampled.

When a command is delayed, the available response time from command active to return read data or accept write data is less. To customize system bus timing, an address decoder can determine which bus operations require delaying the command. The CMDLY input does not affect the timing of ALE, DEN or DT/$\overline{R}$.

Figure 23 illustrates four uses of CMDLY. Example 1 shows delaying the read command two system CLKs for cycle N-1 and no delay for cycle N, and example 2 shows delaying the read command one system CLK for cycle N-1 and one system CLK delay for cycle N.



PIPELINING: VALID ADDRESS (N + 1) AVAILABLE IN LAST PHASE OF BUS CYCLE (N).

FIGURE 22. BASIC BUS CYCLE

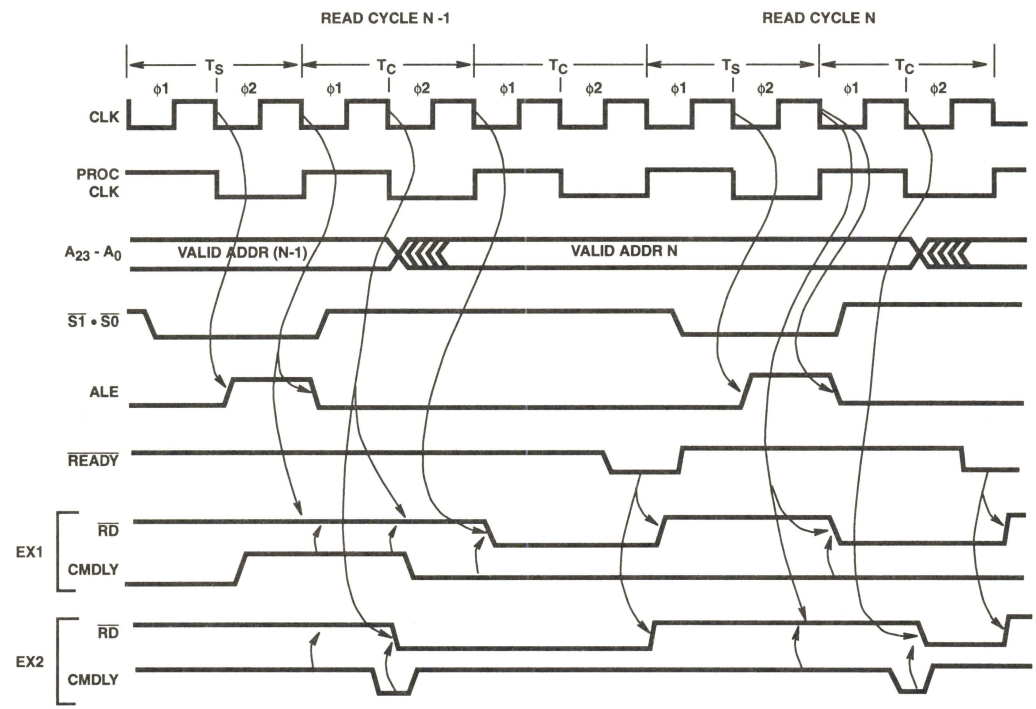


FIGURE 23. CMDLY CONTROLS THE LEADING EDGE OF COMMAND SIGNAL

Bus Cycle Termination

At maximum transfer rates, the 80C286 bus alternates between the status and command states. The bus status signals become inactive after T_S so that they may correctly signal the start of the next bus operation after the completion of the current cycle. No external indication of T_C exists on the 80C286 local bus. The bus master and bus controller enter T_C directly after T_S and continue executing T_C cycles until terminated by the assertion of $\overline{READY}$.

$\overline{READY}$ Operation

The current bus master and 82C288 bus controller terminate each bus operation simultaneously to achieve maximum bus operation bandwidth. Both are informed in advance by $\overline{READY}$ active (open-collector output from 82C284) which identifies the last T_C cycle of the current bus operation. The bus master and bus controller must see the same sense of the $\overline{READY}$ signal, thereby requiring $\overline{READY}$ to be synchronous to the system clock.

Synchronous Ready

The 82C284 clock generator provides $\overline{READY}$ synchronization from both synchronous and asynchronous sources (see Figure 24). The synchronous ready input ($\overline{SRDY}$) of the clock generator is sampled with the falling edge of CLK at the end of phase 1 of each T_C. The state of $\overline{SRDY}$ is then broadcast to the bus master and bus controller via the $\overline{READY}$ output line.

Asynchronous Ready

Many systems have devices or subsystems that are asynchronous to the system clock. As a result, their ready outputs cannot be guaranteed to meet the 82C284 $\overline{SRDY}$ setup and hold time requirements. But the 82C284 asynchronous ready input ($\overline{ARDY}$) is designed to accept such signals. The $\overline{ARDY}$ input is sampled at the beginning of each T_C cycle by 82C284 synchronization logic. This provides one system CLK cycle time to resolve its value before broadcasting it to the bus master and bus controller.

$\overline{ARDY}$ or $\overline{ARDYEN}$ must be HIGH at the end of T_S. $\overline{ARDY}$ cannot be used to terminate the bus cycle with no wait states.

Each ready input of the 82C284 has an enable pin ($\overline{SRDYEN}$ and $\overline{ARDYEN}$) to select whether the current bus operation will be terminated by the synchronous or asynchronous ready. Either of the ready inputs may terminate a bus operation. These enable inputs are active low and have the same timing as their respective ready inputs. Address decode logic usually selects whether the current bus operation should be terminated by $\overline{ARDY}$ or $\overline{SRDY}$.

Data Bus Control

Figures 25, 26, and 27 show how the DT/$\overline{R}$, DEN, data bus, and address signals operate for different combinations of read, write, and idle bus operations. DT/$\overline{R}$ goes active (LOW) for a read operation. DT/$\overline{R}$ remains HIGH before, during, and between write operations.

The data bus is driven with write data during the second phase of T_S. The delay in write data timing allows the read data drivers, from a previous read cycle, sufficient time to enter three-state OFF before the 80C286 CPU begins driving the local data bus for write operations. Write data will always remain valid for one system clock past the last T_C to provide sufficient hold time for Multibus or other similar memory or I/O systems. During write-read or write-idle sequences the data bus enters a high impedance state during the second phase of the processor cycle after the last T_C. In a write-write sequence the data bus does not enter a high impedance state between T_C and T_S.

Bus Usage

The 80C286 local bus may be used for several functions: instruction data transfers, data transfers by other bus masters, instruction fetching, processor extension data transfers, interrupt acknowledge, and halt/shutdown. This section describes local bus activities which have special signals or requirements. Note that I/O transfers take place in exactly the same manner as memory transfers (i.e. to the 80C286 the timing, etc. of an I/O transfer is identical to a memory transfer).

HOLD and HLDA

HOLD and HLDA allow another bus master to gain control of the local bus by placing the 80C286 bus into the T_H state. The sequence of events required to pass control between the 80C286 and another local bus master are shown in Figure 28.

In this example, the 80C286 is initially in the T_H state as signaled by HLDA being active. Upon leaving T_H, as signaled by HLDA going inactive, a write operation is started. During the write operation another local bus master requests the local bus from the 80C286 as shown by the HOLD signal. After completing the write operation, the 80C286 performs one T_I bus cycle, to guarantee write data hold time, then enters T_H as signaled by HLDA going active.

The CMDLY signal and $\overline{ARDY}$ ready are used to start and stop the write bus command, respectively. Note that $\overline{SRDY}$ must be inactive or disabled by $\overline{SRDYEN}$ to guarantee $\overline{ARDY}$ will terminate the cycle.

HOLD must not be active during the time from the leading edge of RESET until 34 CLKs following the trailing edge of RESET unless the 80C286 is in the Halt condition. To ensure that the 80C286 remains in the Halt condition until the processor Reset operation is complete, no interrupts should occur after the execution of HLT until 34 CLKs after the trailing edge of the RESET pulse.

LOCK

The CPU asserts an active lock signal during Interrupt-Acknowledge cycles, the XCHG instruction, and during some descriptor accesses. Lock is also asserted when the LOCK prefix is used. The LOCK prefix may be used with the following ASM-286 assembly instructions; MOVS, INS and OUTS. For bus cycles other than Interrupt-Acknowledge cycles, Lock will be active for the first and subsequent

cycles of a series of cycles to be locked. Lock will not be shown active during the last cycle to be locked. For the next-to-last cycle, Lock will become inactive at the end of the first T_C regardless of the number of wait states inserted. For Interrupt-Acknowledge cycles, Lock will be active for each cycle, and will become inactive at the end of the first T_C for each cycle regardless of the number of wait-states inserted.

Instruction Fetching

The 80C286 Bus Unit (BU) will fetch instructions ahead of the current instruction being executed. This activity is called prefetching. It occurs when the local bus would otherwise be idle and obeys the following rules:

A prefetch bus operation starts when at least two bytes of the 6-byte prefetch queue are empty.

The prefetcher normally performs word prefetches independent of the byte alignment of the code segment base in physical memory.

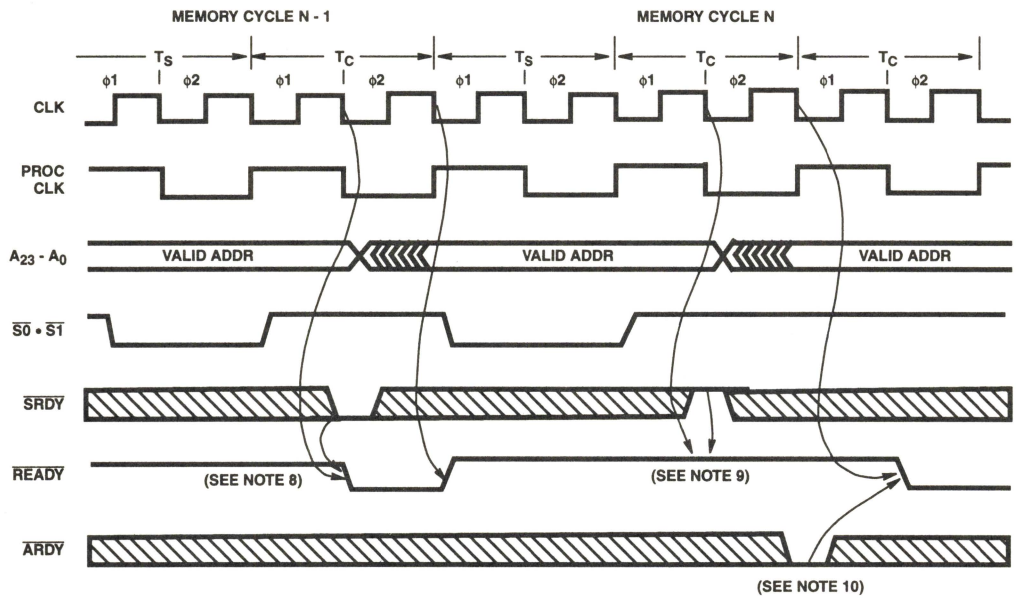
The prefetcher will perform only a byte code fetch operation for control transfers to an instruction beginning on a numerically odd physical address.

Prefetching stops whenever a control transfer or HLT instruction is decoded by the IU and placed into the instruction queue.

In real address mode, the prefetcher may fetch up to 6 bytes beyond the last control transfer or HLT instruction in a code segment.

In protected mode, the prefetcher will never cause a segment overrun exception. The prefetcher stops at the last physical memory word of the code segment. Exception 13 will occur if the program attempts to execute beyond the last full instruction in the code segment.

If the last byte of a code segment appears on an even physical memory address, the prefetcher will read the next physical byte of memory (perform a word code fetch). The value of this byte is ignored and any attempt to execute it causes exception 13.



NOTES:

8. SRDYEN is active low.
9. If SRDYEN is high, the state of SRDY will not effect READY.
10. ARDYEN is active low.

FIGURE 24. SYNCHRONOUS AND ASYNCHRONOUS READY

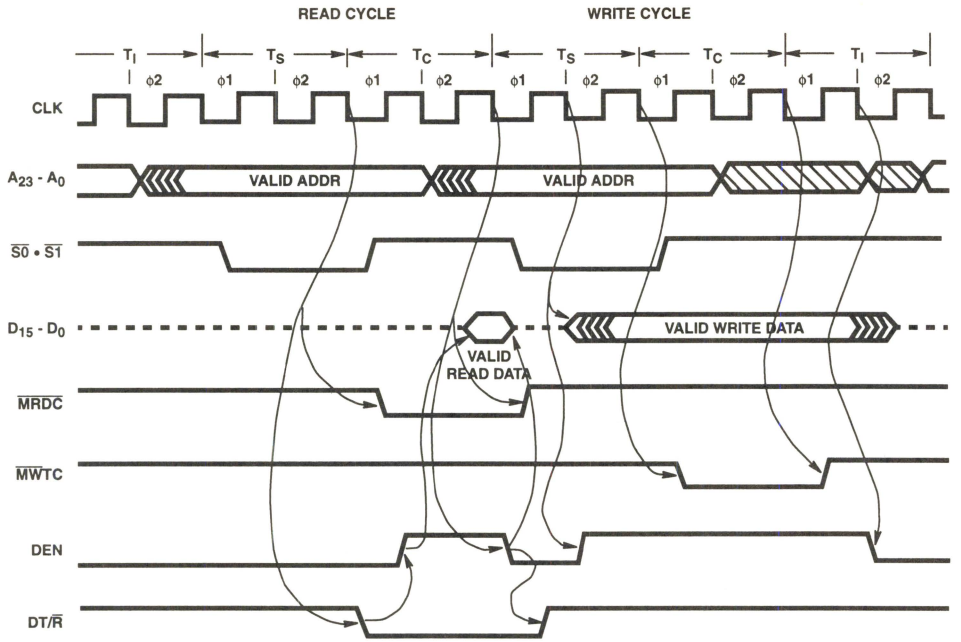


FIGURE 25. BACK TO BACK READ-WRITE CYCLE

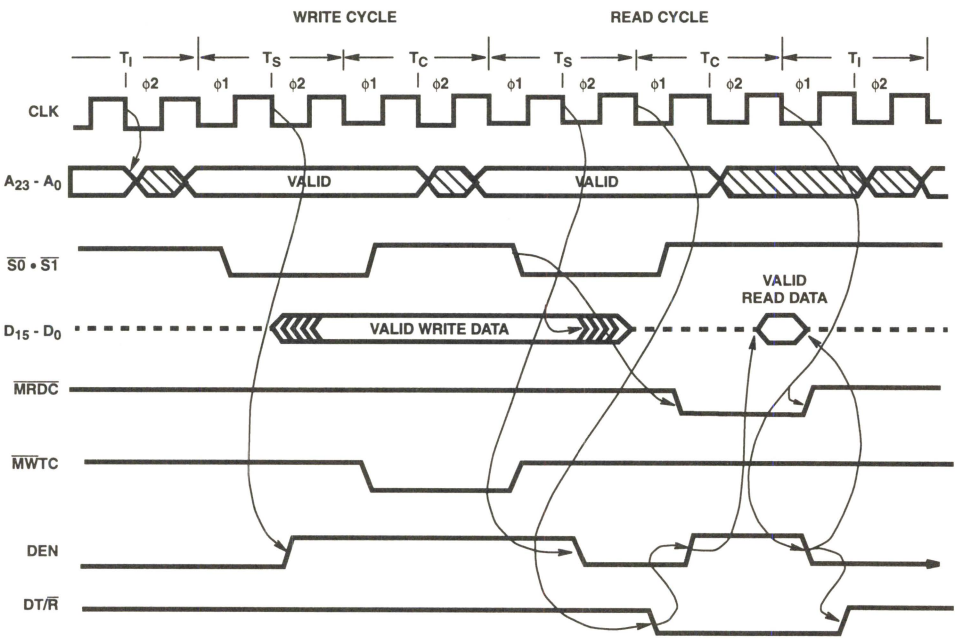


FIGURE 26. BACK TO BACK WRITE-READ CYCLE

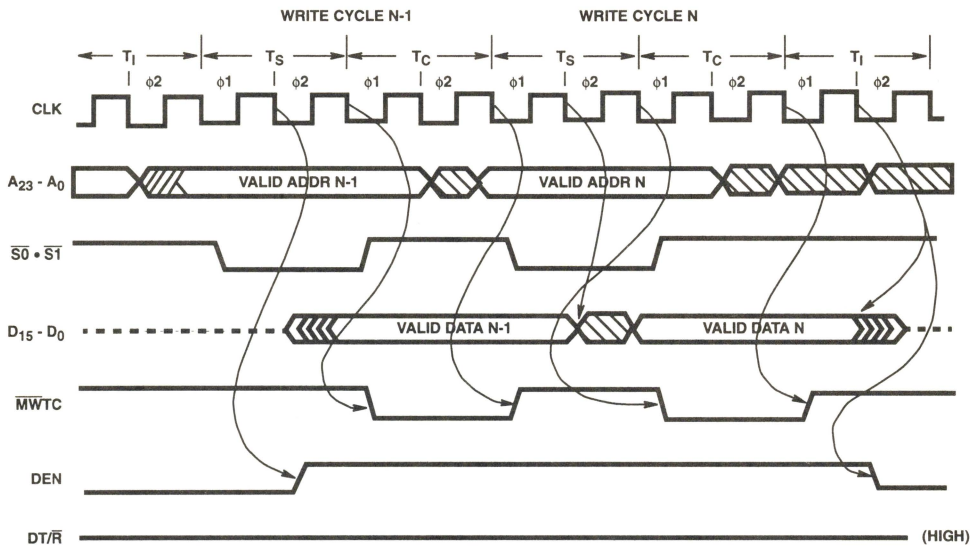


FIGURE 27. BACK TO BACK WRITE-WRITE CYCLE

Processor Extension Transfers

The processor extension interface uses I/O port addresses 00F8(H), and 00FC(H) which are part of the I/O port address range reserved by Harris. An ESC instruction with Machine Status Word bits EM = 0 and T_S = 0 will perform I/O bus operations to one or more of these I/O port addresses independent of the value of IOPL and CPL.

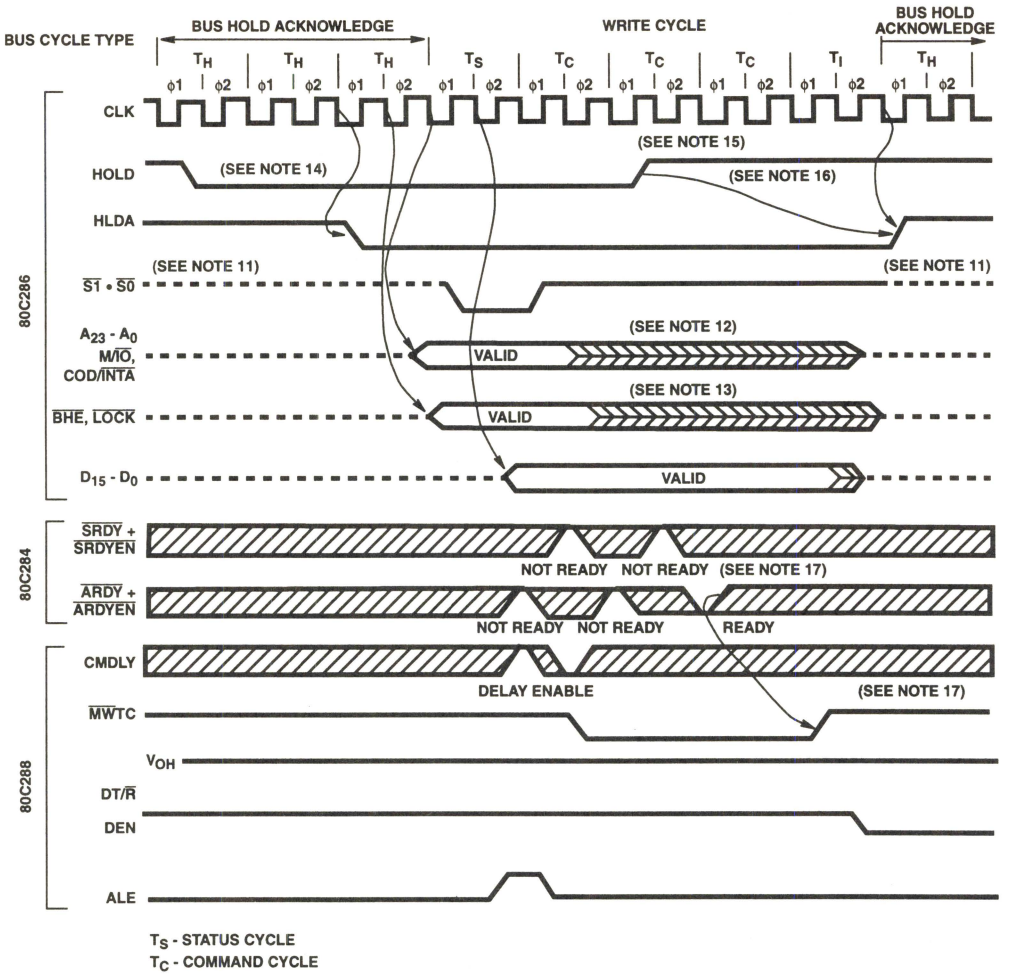
ESC instructions with memory references enable the CPU to accept PEREQ inputs for processor extension operand transfers. The CPU will determine the operand starting address and read/write status of the instruction. For each operand transfer, two or three bus operations are performed, one word transfer with I/O port address 00FA(H) and one or two bus operations with memory. Three bus operations are required for each word operand aligned on an odd byte address.

Interrupt Acknowledge Sequence

Figure 29 illustrates an interrupt acknowledge sequence performed by the 80C286 in response to an INTR input. An interrupt acknowledge sequence consists of two INTA bus operations. The first allows a master 82C59A Programmable Interrupt Controller (PIC) to determine which if any of its slaves should return the interrupt vector. An eight bit vector is read on D_0-D_7 of the 80C286 during the second INTA bus operation to select an interrupt handler routine from the interrupt table.

The Master Cascade Enable (MCE) signal of the 82C288 is used to enable the cascade address drivers during INTA bus operations (See Figure 29) onto the local address bus for distribution to slave interrupt controllers via the system address bus. The 80C286 emits the $\overline{LOCK}$ signal (active LOW) during T_S of the first INTA bus operation. A local bus "hold" request will not be honored until the end of the second INTA bus operation.

Three idle processor clocks are provided by the 80C286 between INTA bus operations to allow for the minimum INTA to INTA time and CAS (cascade address) out delay of the 82C59A. The second INTA bus operation must always have at least one extra T_C state added via logic controlling $\overline{READY}$. A_{23}-A_0 are in three-state OFF until after the first T_C state of the second INTA bus operation. This prevents bus contention between the cascade address drivers and CPU address drivers. The extra T_C state allows time for the 80C286 to resume driving the address lines for subsequent bus operations.



NOTES:

11. Status lines are held at a high impedance logic one by the 80C286 during a HOLD state.
12. Address, M/$\overline{IO}$ and COD/$\overline{INTA}$ may start floating during any T_C depending on when internal 80C286 bus arbiter decides to release bus to external HOLD. The float starts in $\phi 2$ of T_C.
13. $\overline{BHE}$ and $\overline{LOCK}$ may start floating after the end of any T_C depending on when internal 80C286 bus arbiter decides to release bus to external HOLD. The float starts in $\phi 1$ of T_C.
14. The minimum HOLD to HLDA time is shown. Maximum is one T_H longer.
15. The earliest HOLD time is shown. It will always allow a subsequent memory cycle if pending is shown.
16. The minimum HOLD to HLDA time is shown. Maximum is a function of the instruction, type of bus cycle and other machine state (i.e., Interrupts, Waits, Lock, etc.).
17. Asynchronous ready allows termination of the cycle. Synchronous ready does not signal ready in this example. Synchronous ready state is ignored after ready is signaled via the asynchronous input.

FIGURE 28. MULTIBUS WRITE TERMINATED BY ASYNCHRONOUS READY WITH BUS HOLD

Local Bus Usage Priorities

The 80C286 local bus is shared among several internal units and external HOLD requests. In case of simultaneous requests, their relative priorities are:

(Highest) Any transfers which assert $\overline{LOCK}$ either explicitly (via the LOCK instruction prefix) or implicitly (i.e. some segment descriptor accesses, an interrupt acknowledge sequence, or an XCHG with memory).

The second of the two byte bus operations required for an odd aligned word operand.

The second or third cycle of a processor extension data transfer.

Local bus request via HOLD input.

Processor extension data operand transfer via PEREQ input.

Data transfer performed by EU as part of an instruction.

(Lowest) An instruction prefetch request from BU. The EU will inhibit prefetching two processor clocks in advance of any data transfers to minimize waiting by the EU for a prefetch to finish.

Halt or Shutdown Cycles

The 80C286 externally indicates halt or shutdown conditions as a bus operation. These conditions occur due to a HLT instruction or multiple protection exceptions while attempting to execute one instruction. A halt or shutdown bus operation is signalled when $\overline{S_1}$, $\overline{S_0}$ and COD/$\overline{INTA}$ are LOW and M/$\overline{IO}$ is HIGH. A_1 HIGH indicates halt, and A_1 LOW indicates shutdown. The 82C288 bus controller does not issue ALE, nor is $\overline{READY}$ required to terminate a halt or shutdown bus operation.

During halt or shutdown, the 80C286 may service PEREQ or HOLD requests. A processor extension segment overrun during shutdown will inhibit further service of PEREQ. Either NMI or RESET will force the 80C286 out of either halt or shutdown. An INTR, if interrupts are enabled, or a processor extension segment overrun exception will also force the 80C286 out of halt.

System Configurations

The versatile bus structure of the 80C286 micro-system, with a full complement of support chips, allows flexible configuration of a wide range of systems. The basic configuration, shown in Figure 30, is similar to an 80C86 maximum mode system. It includes the CPU plus an 82C59A interrupt controller, 82C284 clock generator, and the 82C288 Bus Controller. The 80C86 latches (82C82 and 82C83H) and transceivers (82C86H and 82C87H) may be used in an 80C286 microsystem.

As indicated by the dashed lines in Figure 30, the ability to add processor extensions is an integral feature of 80C286 based microsystems. The processor extension interface allows external hardware to perform special functions and transfer data concurrent with CPU execution of other instructions. Full system integrity is maintained because the 80C286 supervises all data transfers and instruction execution for the processor extension.

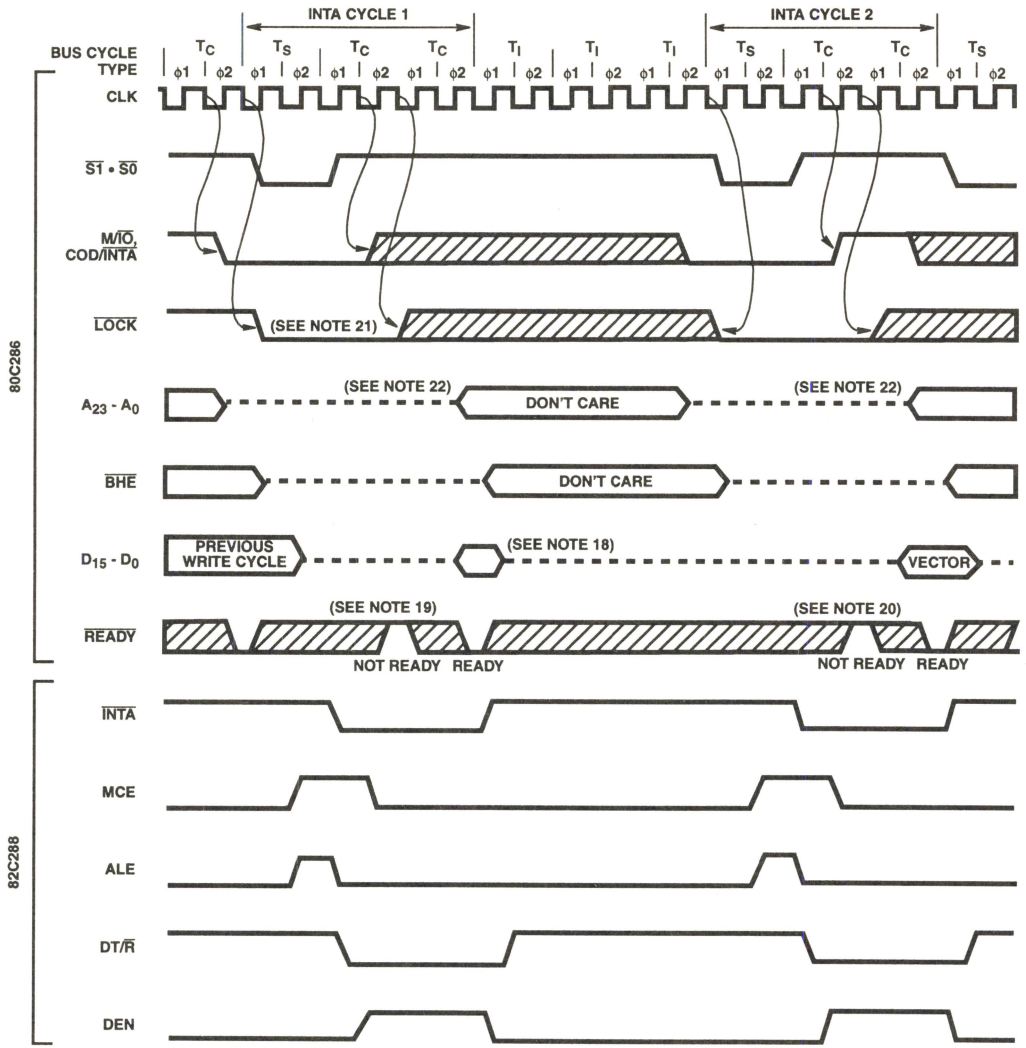
An 80C286 system which includes the 80287 numeric processor extension (NPX) uses this interface. The 80C286/80287 system has all the instructions and data types of an 80C86 or 80C88 with 8087 numeric processor extension. The 80287 NPX can perform numeric calculations and data transfers concurrently with CPU program execution. Numerics code and data have the same integrity as all other information protected by the 80C286 protection mechanism.

The 80C286 can overlap chip select decoding and address propagation during the data transfer for the previous bus operation. This information is latched into the 82C82/83H's by ALE during the middle of a T_S cycle. The latched chip select and address information remains stable during the bus operation while the next cycle's address is being decoded and propagated into the system. Decode logic can be implemented with a high speed PROM or PAL.

The optional decode logic shown in Figure 30 takes advantage of the overlap between address and data of the 80C286 bus cycle to generate advanced memory and I/O select signals. This minimizes system performance degradation caused by address propagation and decode delays. In addition to selecting memory and I/O, the advanced selects may be used with configurations supporting local and system buses to enable the appropriate bus interface for each bus cycle. The COD/$\overline{INTA}$ and M/$\overline{IO}$ signals are applied to the decode logic to distinguish between interrupt, I/O, code, and data bus cycles.

By adding the 82289 bus arbiter chip the 80C286 provides a Multibus system bus interface as shown in Figure 31. The ALE output of the 82C288 for the Multibus bus is connected to its CMDLY input to delay the start of commands one system CLK as required to meet Multibus address and write data setup times. This arrangement will add at least one extra T_C state to each bus operation which uses the Multibus.

A second 82C288 bus controller and additional latches and transceivers could be added to the local bus of Figure 31. This configuration allows the 80C286 to support an on-board bus for local memory and peripherals, and the Multibus for system bus interfacing.



NOTES:

18. Data is ignored.
19. First INTA cycle should have at least one wait state inserted to meet 82C59A minimum INTA pulse width.
20. Second INTA cycle must have at least one wait state inserted since the CPA will not drive A_{23}-A_0, $\overline{BHE}$, and $\overline{LOCK}$ until after the first T_C state. The CPU imposed one/clock delay prevents has contention between cascade address buffer being disabled by MCE ↓ and address outputs.
21. Without the wait state, the 80C286 address will not be valid for a memory cycle started immediately after the second INTA cycle. The 82C59A also requires one wait state for minimum INTA pulse width.
22. $\overline{LOCK}$ is active for the first INTA cycle to prevent the 82289 from releasing the bus between INTA cycles in a multi-master system. $\overline{LOCK}$ is also active for the second INTA cycle.
23. A_{23}-A_0 exits three-state OFF during φ2 of the second T_C in the INTA cycle.

FIGURE 29. INTERRUPT ACKNOWLEDGE SEQUENCE

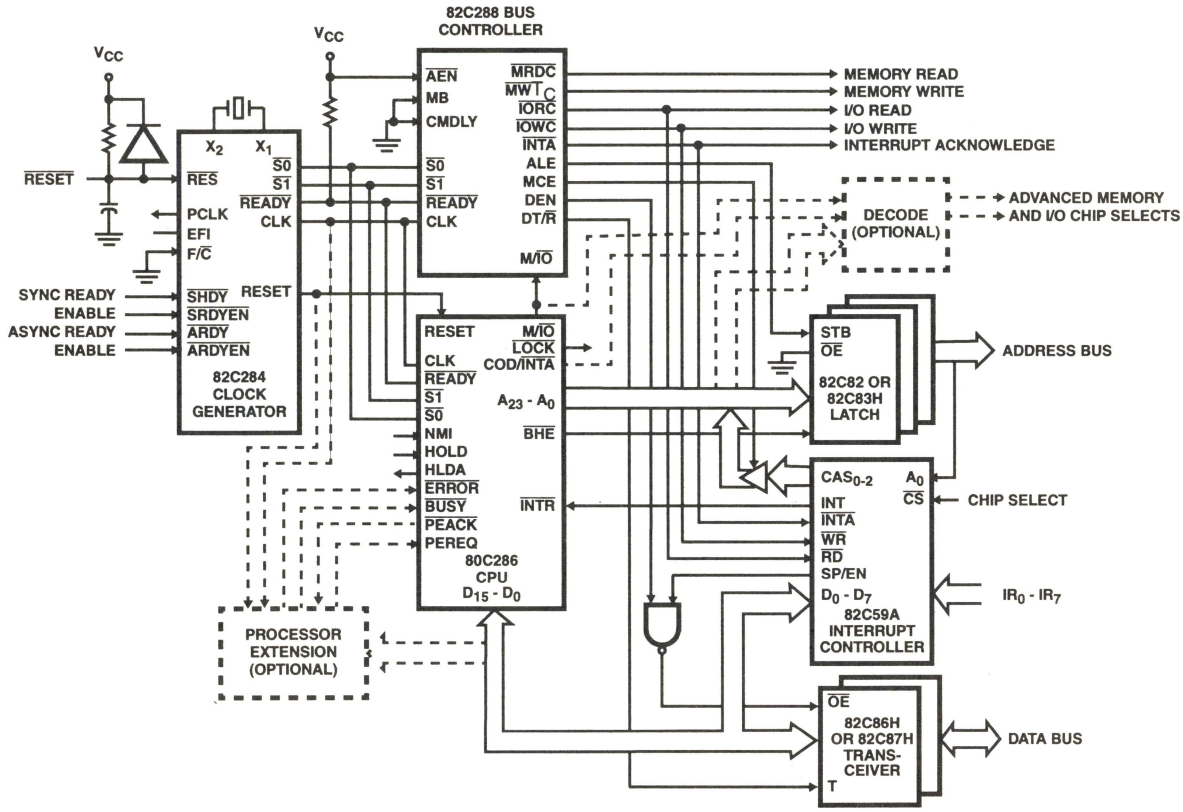


FIGURE 30. BASIC 80C286 SYSTEM CONFIGURATION

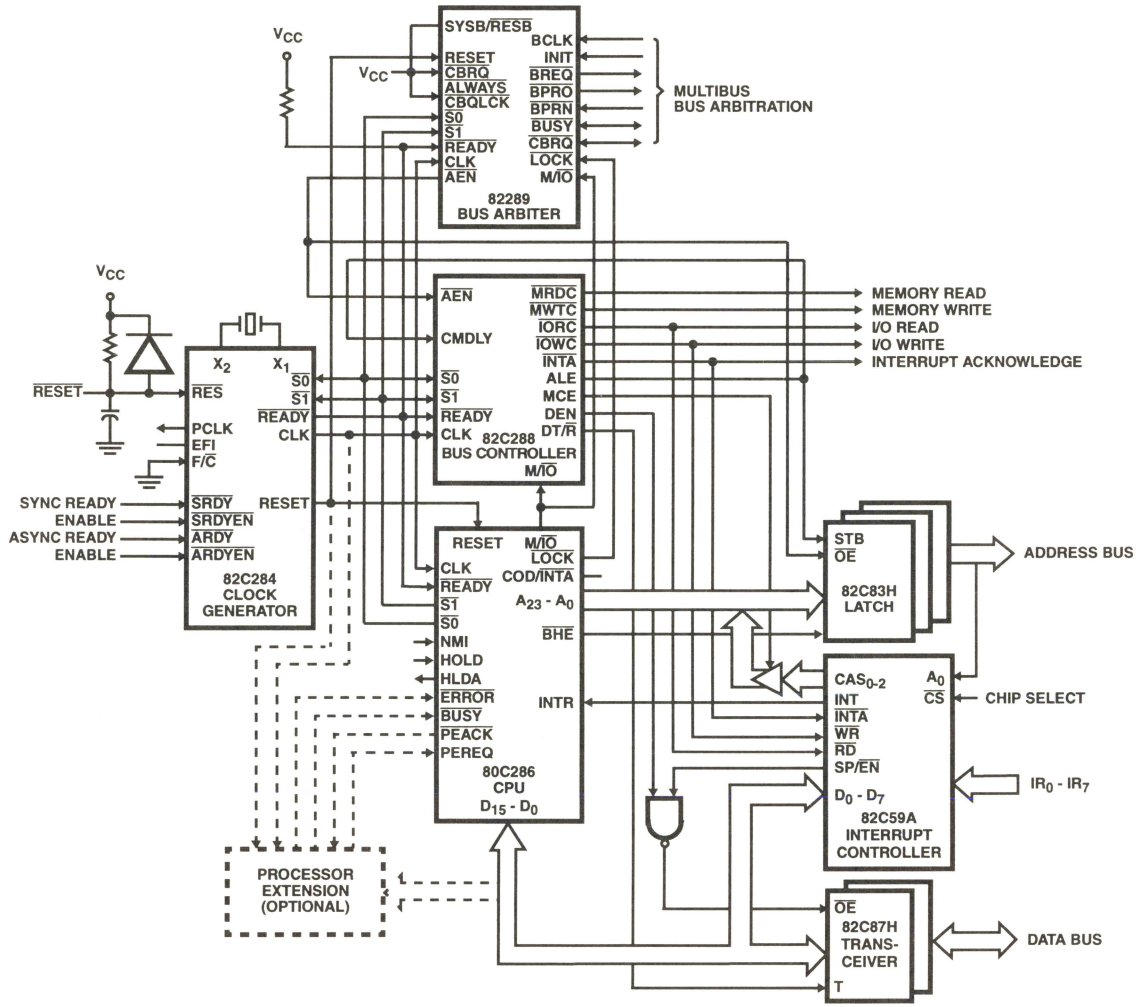


FIGURE 31. MULTIBUS SYSTEM BUS INTERFACE

Absolute Maximum Ratings

Supply Voltage ..... ±8.0V
Input, Output or I/O Voltage Applied..... GND -1.0V to V_{CC} +1.0V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature, PGA ..... +175°C
PLCC ..... +150°C
Lead Temperature (Soldering, 10s) ..... +300°C
(PLCC - Lead Tips Only)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	35	6
CERDIP Package	33	9

Maximum Package Power Dissipation
PGA Package 1.22W
PLCC Package 2.2W
Gate Count 22,500

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range
80C286-10, -12 ..... +4.5V to +5.5V
80C286-16, -20, -25 ..... +4.75V to +5.25V

Operating Temperature Range
I80C286-10, -12, -16, -20 ..... -40°C to +85°C
C80C286-12, -16, -20, -25..... 0°C to +70°C

DC Electrical Specifications

V_{CC} = +5V ± 10%, T_A = 0°C to +70°C (C80C286-12), V_{CC} = +5V ± 5%, T_A = 0°C to +70°C (C80C286-16, -20, -25), V_{CC} = +5V ± 10%, T_A = -40°C to +85°C (I80C286-10, -12), V_{CC} = +5V ± 5%, T_A = -40°C to +85°C (I80C286-16, -20)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input LOW Voltage	-0.5	0.8	V	
V_{IH}	Input HIGH Voltage	2.0	V_{CC} +0.5	V	
V_{ILC}	CLK Input LOW Voltage	-0.5	1.0	V	
V_{IHC}	CLK Input HIGH Voltage	3.6	V_{CC} +0.5	V	
V_{OL}	Output LOW Voltage	-	0.4	V	I_{OL} = 2.0mA
V_{OH}	Output HIGH Voltage	3.0 V_{CC} -0.4	- -	V	I_{OH} = -2.0mA, I_{OH} = -100µA
I_I	Input Leakage Current	-10	10	µA	V_{IN} = GND or V_{CC} Pins 29, 31, 57, 59, 61, 63-64
I_{SH}	Input Sustaining Current on $\overline{BUSY}$ and $\overline{ERROR}$ Pins	-30	-500	µA	V_{IN} = GND (See Note 28)
I_{BHL}	Input Sustaining Current LOW	38	200	µA	V_{IN} = 1.0V (See Note 24)
I_{BHH}	Input Sustaining Current HIGH	-50	-400	µA	V_{IN} = 3.0V (See Note 25)
I_O	Output Leakage Current	-10	10	µA	V_O = GND or V_{CC} Pins 1, 7-8, 10-28, 32-34
I_{CCOP}	Active Power Supply Current	-	185	mA	80C286-10 (See Note 27)
		-	220	mA	80C286-12 (See Note 27)
		-	260	mA	80C286-16 (See Note 27)
		-	310	mA	80C286-20 (See Note 27)
		-	410	mA	80C286-25 (See Note 27)
I_{CCSB}	Standby Power Supply Current	-	5	mA	(See Note 26)

Capacitance

T_A = +25°C, All Measurements Referenced to Device GND

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
C_{CLK}	CLK Input Capacitance	10	pF	FREQ = 1MHz
C_{IN}	Other Input Capacitance	10	pF	
$C_{I/O}$	I/O Capacitance	10	pF	

NOTES:

24. I_{BHL} should be measured after lowering V_{IN} to GND and then raising to 1.0V on the following pins: 36-51, 66, 67.
25. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering to 3.0V on the following pins: 4-6, 36-51, 66-68.
26. I_{CCSB} tested with the clock stopped in phase two of the processor clock cycle. V_{IN} = V_{CC} or GND, V_{CC} = V_{CC} (Max), outputs unloaded.
27. I_{CCOP} measured at 10MHz for the 80C286-10, 12.5MHz for the 80C286-12, 16MHz for the 80C286-16, 20MHz for the 80C286-20, and 25MHz for the 80C286-25. V_{IN} = 2.4V or 0.4V, V_{CC} = V_{CC} (Max), outputs unloaded.
28. I_{SH} should be measured after raising V_{IN} to V_{CC} and then lowering to GND on pins 53 and 54.

AC Electrical Specifications

V_{CC} = +5V ±10%, T_A = 0°C to +70°C (C80C286-12), T_A = -40°C to +85°C (I80C286-10, -12)
V_{CC} = +5V ±5%, T_A = 0°C to +70°C (C80C286-16), T_A = -40°C to +85°C (I80C286-16) AC Timings are Referenced to 0.8V and 2.0V Points of the Signals as Illustrated in Data Sheet Waveforms, Unless Otherwise Specified

SYMBOL	PARAMETER	10MHz		12.5MHz		16MHz		UNIT	TEST CONDITION
		MIN	MAX	MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS									
1	System Clock (CLK) Period	50	-	40	-	31	-	ns	
2	System Clock (CLK) LOW Time	12	-	11	-	7	-	ns	At 1.0V
3	System Clock (CLK) HIGH Time	16	-	13	-	11	-	ns	At 3.6V
17	System Clock (CLK) RISE Time	-	8	-	8	-	5	ns	1.0V to 3.6V
18	System Clock (CLK) FALL Time	-	8	-	8	-	5	ns	3.6V to 1.0V
4	Asynchronous Inputs SETUP Time	20	-	15	-	5	-	ns	(Note 29)
5	Asynchronous Inputs HOLD Time	20	-	15	-	5	-	ns	(Note 29)
6	RESET SETUP Time	19	-	10	-	10	-	ns	
7	RESET HOLD Time	0	-	0	-	0	-	ns	
8	Read Data SETUP Time	8	-	5	-	5	-	ns	
9	Read Data HOLD Time	4	-	4	-	3	-	ns	
10	$\overline{\text{READY}}$ SETUP Time	26	-	20	-	12	-	ns	
11	$\overline{\text{READY}}$ HOLD Time	25	-	20	-	5	-	ns	
20	Input RISE/FALL Times	-	10	-	8	-	6	ns	0.8V to 2.0V
TIMING RESPONSES									
12A	Status/$\overline{\text{PEACK}}$ Active Delay	1	22	1	21	1	18	ns	1, (Notes 31, 35)
12B	Status/$\overline{\text{PEACK}}$ Inactive Delay	1	30	1	24	1	20	ns	1, (Notes 31, 34)
13	Address Valid Delay	1	35	1	32	1	27	ns	1, (Notes 30, 31)
14	Write Data Valid Delay	0	40	0	31	0	28	ns	1, (Notes 30, 31)
15	Address/Status/Data Float Delay	0	47	0	32	0	29	ns	2, (Note 33)
16	HLDA Valid Delay	0	47	0	25	0	25	ns	1, (Notes 31, 36)
19	Address Valid to Status SETUP Time	27	-	22	-	16	-	ns	1, (Notes 31, 32)

NOTES:

29. Asynchronous inputs are INTR, NMI, HOLD, PEREQ, ERROR, and BUSY. This specification is given only for testing purposes, to assure recognition at a specific CLK edge.
30. Delay from 1.0V on the CLK to 0.8V or 2.0V.
31. Output load: C_L = 100pF.
32. Delay measured from address either reaching 0.8V or 2.0V (valid) to status going active reaching 0.8V or status going inactive reaching 2.0V.
33. Delay from 1.0V on the CLK to Float (no current drive) condition.
34. Delay from 1.0V on the CLK to 0.8V for min. (HOLD time) and to 2.0V for max. (inactive delay).
35. Delay from 1.0V on the CLK to 2.0V for min. (HOLD time) and to 0.8V for max. (active delay).
36. Delay from 1.0V on the CLK to 2.0V.

AC Test Conditions

TEST CONDITION	I_L (CONSTANT CURRENT SOURCE)	C_L
1	|2.0mA|	100pF
2	-6mA (V_{OH} to Float) 8mA (V_{OL} to Float)	100pF

AC Electrical Specifications

V_{CC} = +5V ±5%, T_A = 0°C to +70°C (C80C286-20, -25), T_A = -40°C to +85°C (I80C286-20)
AC Timings are Referenced to the 1.5V Point of the Signals as Illustrated in Data Sheet Waveforms, Unless Otherwise Specified

SYMBOL	PARAMETER	20MHz		25MHz		UNIT	TEST CONDITION
		MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS							
1	System Clock (CLK) Period	25	-	20	-	ns	
2	System Clock (CLK) LOW Time	6	-	5	-	ns	At 1.0V
3	System Clock (CLK) HIGH Time	9	-	7	-	ns	At 3.6V
17	System Clock (CLK) RISE Time	-	4	-	4	ns	1.0V to 3.6V
18	System Clock (CLK) FALL Time	-	4	-	4	ns	3.6V to 1.0V
4	Asynchronous Inputs SETUP Time	4	-	4	-	ns	(Note 37)
5	Asynchronous Inputs HOLD Time	4	-	4	-	ns	(Note 37)
6	RESET SETUP Time	10	-	10	-	ns	
7	RESET HOLD Time	0	-	0	-	ns	
8	Read Data SETUP Time	3	-	3	-	ns	
9	Read Data HOLD Time	2	-	2	-	ns	
10	$\overline{\text{READY}}$ SETUP Time	10	-	9	-	ns	
11	$\overline{\text{READY}}$ HOLD Time	3	-	3	-	ns	
20	Input RISE/FALL Times	-	6	-	6	ns	0.8V to 2.0V
TIMING RESPONSES							
12A	Status/$\overline{\text{PEACK}}$ Active Delay	1	15	1	12	ns	1, (Notes 39, 42)
12B	Status/$\overline{\text{PEACK}}$ Inactive Delay	1	16	1	13	ns	1, (Notes 39, 42)
13	Address Valid Delay	1	23	1	20	ns	1, (Notes 38, 39)
14	Write Data Valid Delay	0	27	0	24	ns	1, (Notes 38, 39)
15	Address/Status/Data Float Delay	0	25	0	24	ns	2, (Note 41)
16	HLDA Valid Delay	0	20	0	19	ns	1, (Notes 38, 39)
19	Address Valid to Status SETUP Time	9	-	12	-	ns	1, (Notes 39, 40)

NOTES:

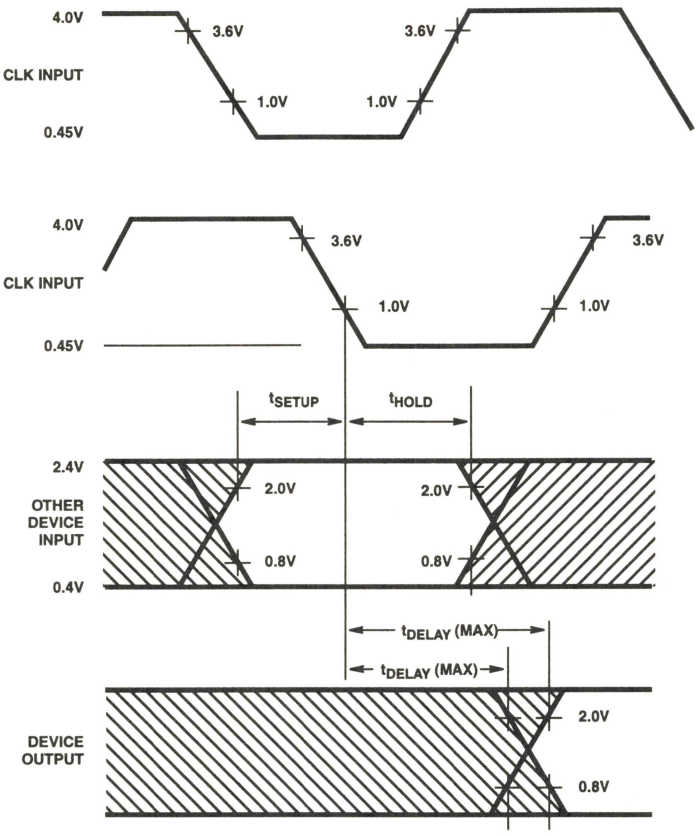
37. Asynchronous inputs are INTR, NMI, HOLD, PEREQ, ERROR, and BUSY. This specification is given only for testing purposes, to assure recognition at a specific CLK edge.
38. Delay from 1.0V on the CLK to 1.5V.
39. Output load: C_L = 100pF.
40. Delay measured from address reaching 1.5V to status reaching 1.5V.
41. Delay from 1.0V on the CLK to Float (no current drive) condition.
42. Delay from 1.0V on the CLK to 1.5V.

AC Test Conditions

TEST CONDITION	I_L (CONSTANT CURRENT SOURCE)	C_L
1	|2.0mA|	100pF
2	-6mA (V_{OH} to Float) 8mA (V_{OL} to Float)	100pF

AC Specifications (Continued)

C80C86-12, -16
I80C286-10, -12, -16
AC DRIVE AND MEASURE POINTS - CLK INPUT

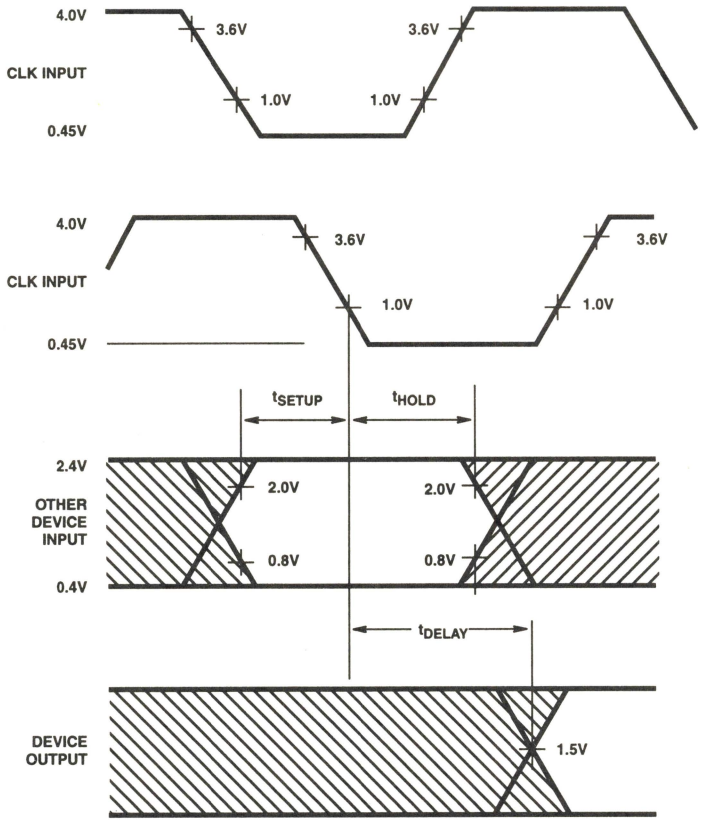


NOTE: For AC testing, input rise and fall times are driven at 1ns per volt.

FIGURE 32.

AC Specifications (Continued)

C80C286-20, -25
I80C286-20
AC DRIVE AND MEASURE POINTS - CLK INPUT



NOTE: Typical Output Rise/Fall Time is 6ns. For AC testing, input rise and fall times are driven at 1ns per volt.

FIGURE 33.

AC Electrical Specifications

82C284 and 82C288 Timing Specifications are given for reference only and no guarantee is implied.

82C284 Timing

SYMBOL	PARAMETER	10MHz		12.5MHz		16MHz		UNIT	TEST CONDITION
		MIN	MAX	MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS									
11	$\overline{SRDY}/\overline{SRDYEN}$ Setup Time	15	-	15	-	10	-	ns	
12	$\overline{SRDY}/\overline{SRDYEN}$ Hold Time	2	-	2	-	1	-	ns	
13	$\overline{ARDY}/\overline{ARDYEN}$ Setup Time	5	-	5	-	3	-	ns	(Note 43)
14	$\overline{ARDY}/\overline{ARDYEN}$ Hold Time	30	-	25	-	20	-	ns	(Note 43)
TIMING RESPONSES									
19	PCLK Delay	0	20	0	16	0	15	ns	C_L = 75pF, I_{OL} = 5mA, I_{OH} = 1mA

NOTE:

43. These times are given for testing purposes to ensure a predetermined action.

82C288 Timing

SYMBOL	PARAMETER	10MHz		12.5MHz		16MHz		UNIT	TEST CONDITION
		MIN	MAX	MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS									
12	CMDLY Setup Time	15	-	15	-	10	-	ns	
13	CMDLY Hold Time	1	-	1	-	0	-	ns	
TIMING RESPONSES									
16	ALE Active Delay	1	16	1	16	1	12	ns	
17	ALE Inactive Delay	-	19	-	19	-	15	ns	
19	DT/$\overline{R}$ Read Active Delay	-	23	-	23	-	18	ns	C_L = 150pF
20	DEN Read Active Delay	-	21	-	21	-	16	ns	I_{OL} = 16mA Max
21	DEN Read Inactive Delay	3	23	3	21	5	14	ns	I_{OL} = 1mA Max
22	DT/$\overline{R}$ Read Inactive Delay	5	24	5	18	5	14	ns	
23	DEN Write Active Delay	-	23	-	23	-	17	ns	
24	DEN Write Inactive Delay	3	23	3	23	3	15	ns	
29	Command Active Delay from CLK	3	21	3	21	3	15	ns	C_L = 300pF
30	Command Inactive Delay from CLK	3	20	3	20	3	15	ns	I_{OL} = 32mA Max

NOTE:

44. These times are given for testing purposes to ensure a predetermined action.

Waveforms

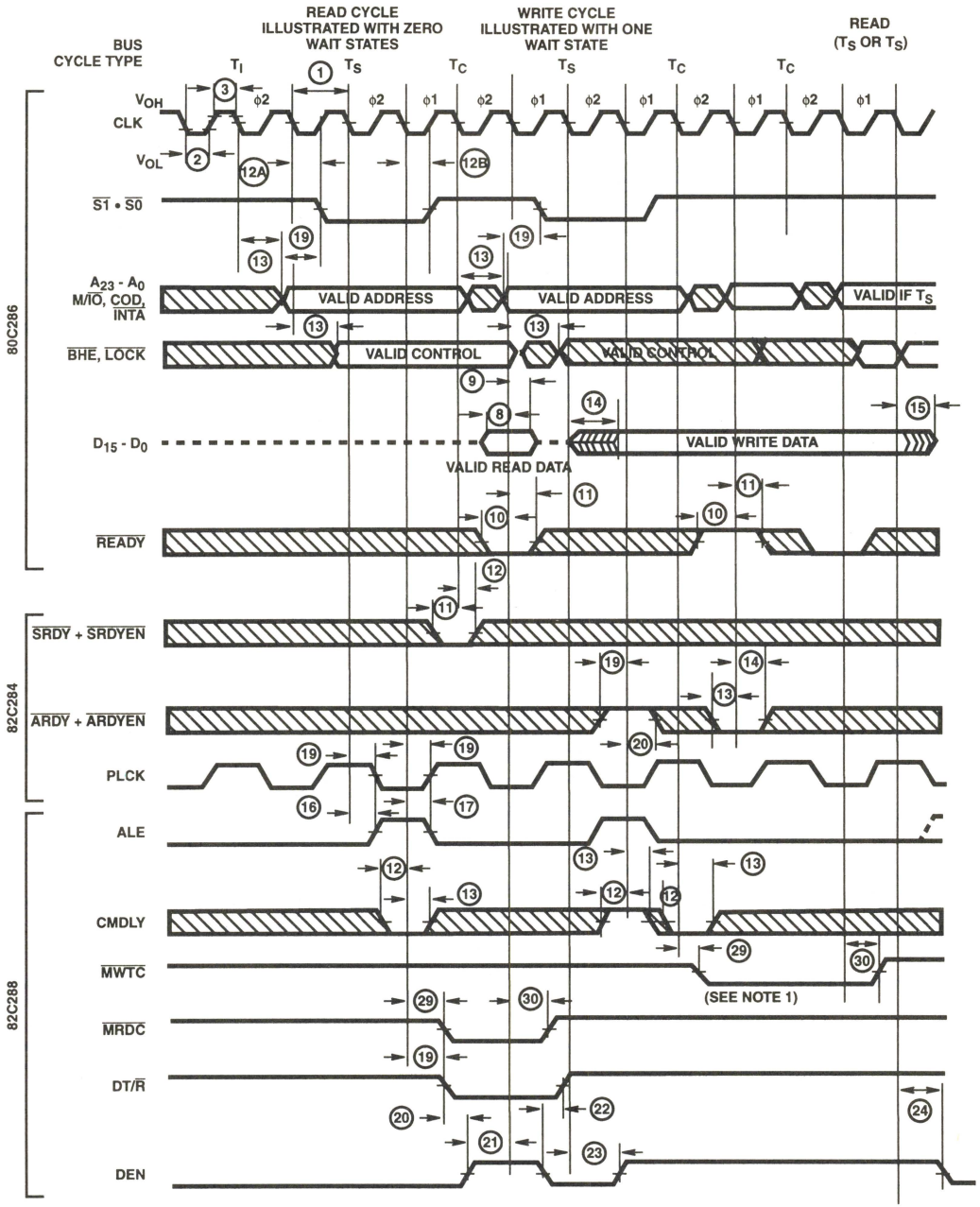


FIGURE 34. MAJOR CYCLE TIMING

NOTE: The modified timing is due to the CMDLY signal being active.

Waveforms (Continued)

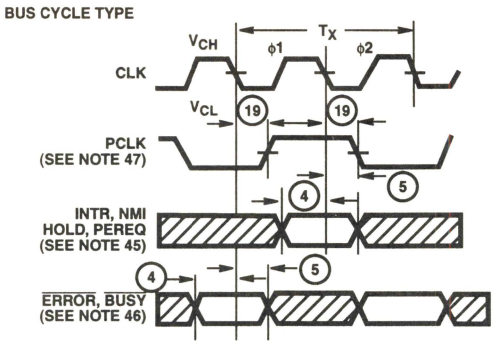


FIGURE 35. 80C286 ASYNCHRONOUS INPUT SIGNAL TIMING

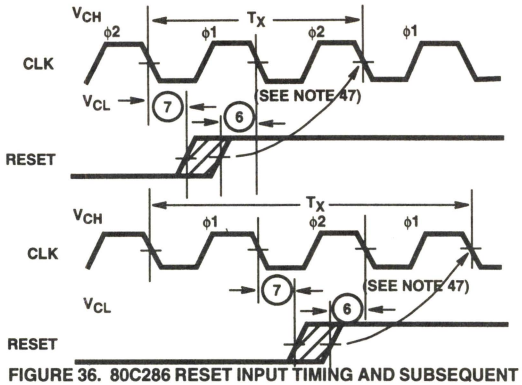


FIGURE 36. 80C286 RESET INPUT TIMING AND SUBSEQUENT PROCESSOR CYCLE PHASE

NOTES:

45. PCLK indicates which processor cycle phase will occur on the next CLK, PCLK may not indicate the correct phase until the first cycle is performed.
46. These inputs are asynchronous. The setup and hold times shown assure recognition for testing purposes.

NOTE:

47. When RESET meets the setup time shown, the next CLK will start or repeat $\phi1$ of a processor cycle.

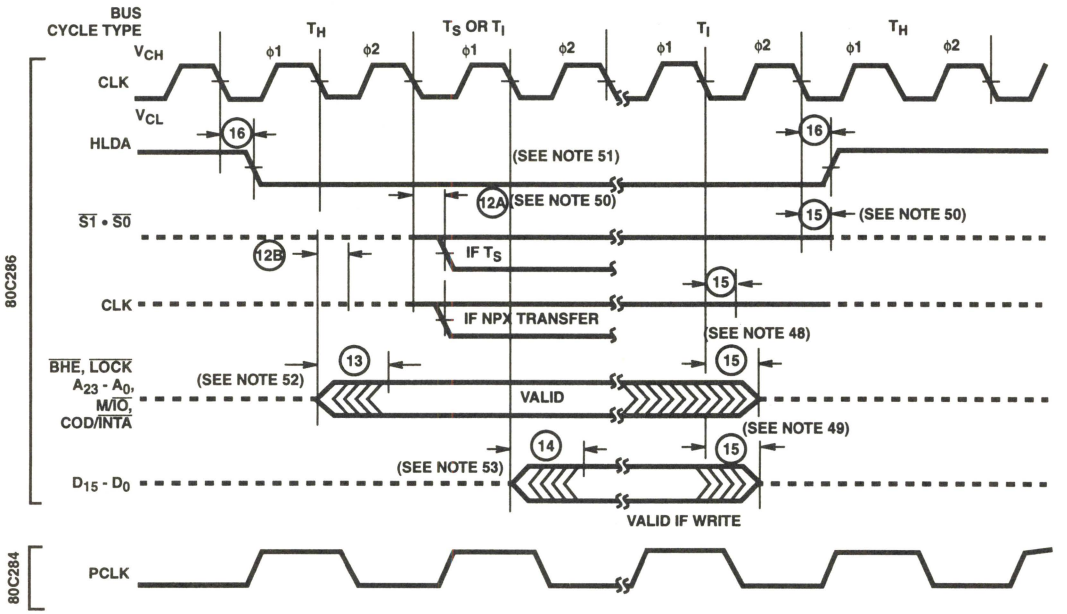
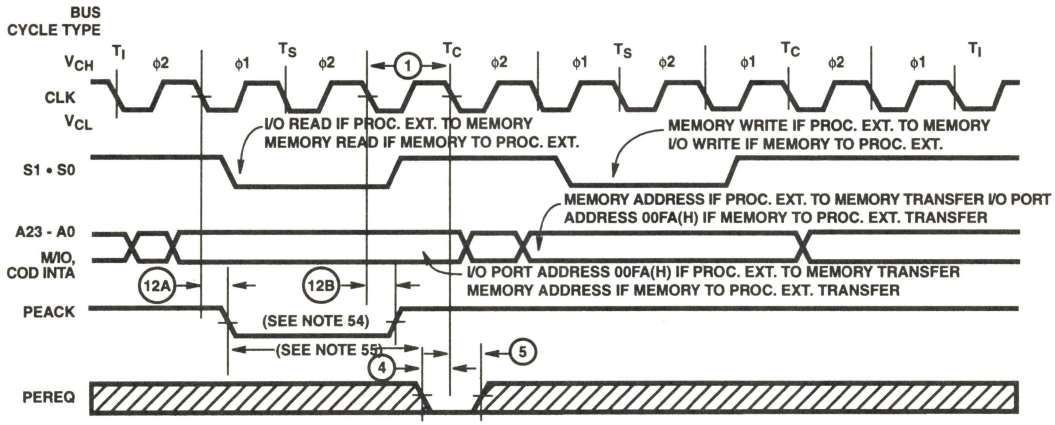


FIGURE 37. EXITING AND ENTERING HOLD

NOTES:

48. These signals may not be driven by the 80C286 during the time shown. The worst case in terms of latest float time is shown.
49. The data bus will be driven as shown if the cycle before T_I in the diagram was a write T_C.
50. The 80C286 puts its status pins in a high impedance logic one state during T_H.
51. For HOLD request set up to HLDA, refer to Figure 29.
52. $\overline{BHE}$ and $\overline{LOCK}$ are driven at this time but will not become valid until T_S.
53. The data bus will remain in a high impedance state if a read cycle is performed.

Waveforms (Continued)



ASSUMING WORD-ALIGNED MEMORY OPERAND. IF ODD ALIGNED, 80C286 TRANSFERS TO/FROM MEMORY BYTE-AT-A-TIME WITH TWO MEMORY CYCLES.

FIGURE 38. 80C286 PEREQ/$\overline{\text{PEACK}}$ TIMING FOR ONE TRANSFER ONLY

NOTES:

54. $\overline{\text{PEACK}}$ always goes active during the first bus operation of a processor extension data operand transfer sequence. The first bus operation will be either a memory read at operand address or I/O read at port address 00FA(H).

55. To prevent a second processor extension data operand transfer, the worst case maximum time (Shown above) is 3 x ① - $12A_{MAX}$ - $④_{MIN}$. The actual configuration dependent, maximum time is: 3 x ① - $12A_{MAX}$ - $④_{MIN}$ + N x 2 x ①. N is the number of extra T_C states added to either the first or second bus operation of the processor extension data operand transfer sequence.

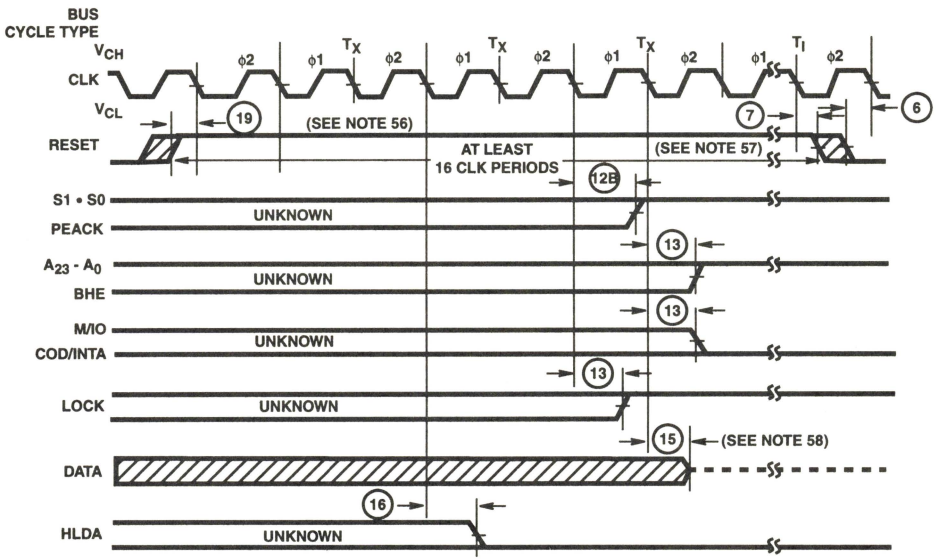


FIGURE 39. INITIAL 80C286 PIN STATE DURING RESET

NOTES:

56. Setup time for RESET ↑ may be violated with the consideration that φ1 of the processor clock may begin one system CLK period later.

57. Setup and hold times for RESET ↓ must be met for proper operation, but RESET ↓ may occur during φ1 or φ2.

58. The data bus is only guaranteed to be in a high impedance state at the time shown.

Waveforms (Continued)

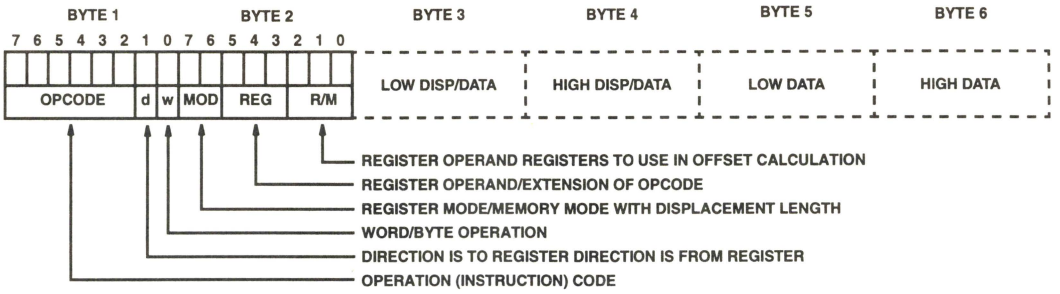


FIGURE 40A. SHORT OPCODE FORMAT EXAMPLE

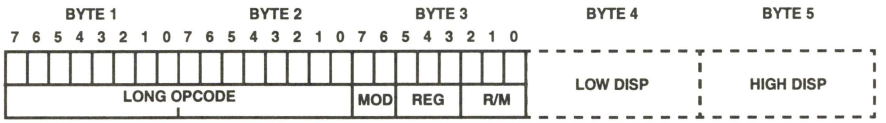


FIGURE 40B. LONG OPCODE FORMAT EXAMPLE

FIGURE 40. 80C286 INSTRUCTION FORMAT EXAMPLES

80C286 Instruction Set Summary

Instruction Timing Notes

The instruction clock counts listed below establish the maximum execution rate of the 80C286. With no delays in bus cycles, the actual clock count of an 80C286 program will average 5% more than the calculated clock count, due to instruction sequences which execute faster than they can be fetched from memory.

To calculate elapsed times for instruction sequences, multiply the sum of all instruction clock counts, as listed in the table below, by the processor clock period. An 12.5MHz processor clock has a clock period of 80 nanoseconds and requires an 80C286 system clock (CLK input) of 25MHz.

Instruction Clock Count Assumptions

1. The instruction has been perfected, decoded and is ready for execution. Control transfer instruction clock counts include all time required to fetch, decode, and prepare the next instruction for execution.
2. Bus cycles do not require wait states.
3. There are no processor extension data transfer or local bus HOLD requests.
4. No exceptions occur during instruction execution.

Instruction Set Summary Notes

Addressing displacements selected by the MOD field are not shown. If necessary they appear after the instruction fields shown.

Above/below refers to unsigned value.

Greater refers to more positive signed values.

Less refers to less positive (more negative) signed values

if d = 1, then "to" register; if d = 0 then "from" register

if w = 1, then word instruction; if w = 0, then byte instruction

if s = 0, then 16-bit immediate data form the operand

if s = 1, then an immediate data byte is sign-extended to form the 16-bit operand

x don't care

z used for string primitives for comparison with ZF FLAG

If two clock counts are given, the smaller refers to a register operand and the larger refers to a memory operand

* = add one clock if offset calculation requires summing 3 elements

n = number of times repeated

m = number of bytes of code in next instruction

Level (L) - Lexical nesting level of the procedure

The following comments describe possible exceptions, side effects and allowed usage for instructions in both operating modes of the 80C286.

Real Address Mode Only

1. This is a protected mode instruction. Attempted execution in real address mode will result in an undefined opcode exception (6).
2. A segment overrun exception (13) will occur if a word operand references at offset FFFF(H) is attempted.
3. This instruction may be executed in real address mode to initialize the CPU for protected mode.
4. The IOPL and NT fields will remain 0.
5. Processor extension segment overrun interrupt (9) will occur if the operand exceeds the segment limit.

Either Mode

6. An exception may occur, depending on the value of the operand.
7. $\overline{\text{LOCK}}$ is automatically asserted regardless of the presence or absence of the $\overline{\text{LOCK}}$ instruction prefix.
8. $\overline{\text{LOCK}}$ does not remain active between all operand transfers.

Protected Virtual Address Mode Only

9. A general protection exception (13) will occur if the memory operand cannot be used due to either a segment limit or access rights violation. If a stack segment limit is violated, a stack segment overrun exception (12) occurs.
10. For segment load operations, the CPL, RPL and DPL must agree with privilege rules to avoid an exception. The segment must be present to avoid a not-present exception (11). If the SS register is the destination and a segment not-present violation occurs, a stack exception (12) occurs.
11. All segment descriptor accesses in the GDT or LDT made by this instruction will automatically assert $\overline{\text{LOCK}}$ to maintain descriptor integrity in multiprocessor systems.
12. JMP, CALL, INT, RET, IRET instructions referring to another code segment will cause a general protection exception (13) if any privilege rule is violated.
13. A general protection exception (13) occurs if CPL $\neq$ 0.
14. A general protection exception (13) occurs if CPL > IOPL.
15. The IF field of the flag word is not updated if CPL > IOPL. The IOPL field is updated only if CPL = 0.
16. Any violation of privilege rules as applied to the selector operand does not cause a protection exception; rather, the instruction does not return a result and the zero flag is cleared.
17. If the starting address of the memory operand violates a segment limit, or an invalid access is attempted, a general protection exception (13) will occur before the ESC instruction is executed. A stack segment overrun exception (12) will occur if the stack limit is violated by the operand's starting address. If a segment limit is violated during an attempted data transfer then a processor extension segment overrun exception (9) occurs.
18. The destination of an INT, JMP, CALL, RET or IRET instruction must be in the defined limit of a code segment or a general protection exception (13) will occur.

80C286 Instruction Set Summary

FUNCTION	FORMAT				CLOCK COUNT		COMMENTS	
					REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE	REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE
DATA TRANSFER								
MOV = Move								
Register to Register/Memory	1000100w	mod reg r/m			2, 3 (Note 59)	2, 3 (Note 59)	2	9
Register/Memory to Register	1000101w	mod reg r/m			2, 5 (Note 59)	2, 5 (Note 59)	2	9
Immediate to Register/Memory	1100011w	mod 000 r/m	data	data if w = 1	2, 3 (Note 59)	2, 3 (Note 59)	2	9
Immediate to Register	1011w reg	data	data if w = 1		2	2		
Memory to Accumulator	1010000w	addr-low	addr-high		5	5	2	9
Accumulator to Memory	1010001w	addr-low	addr-high		3	3	2	9

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT				CLOCK COUNT		COMMENTS	
					REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE	REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE
Register/Memory to Segment Register	10001110	mod 0 reg r/m			2, 5 (Note 59)	17, 19 (Note 59)	2	9, 10, 11
Segment Register to Register/Memory	10001100	mod 0 reg r/m			2, 3 (Note 59)	2, 3 (Note 59)	2	9
PUSH = Push								
Memory	11111111	mod 110 r/m			5 (Note 59)	5 (Note 59)	2	9
Register	01010 reg				3	3	2	9
Segment Register	000 reg 110				3	3	2	9
Immediate	011010s0	data	data if s = 0		3	3	2	9
PUSHA = Push All	01100000				17	17	2	9
POP = Pop								
Memory	10001111	mod 000 r/m			5 (Note 59)	5 (Note 59)	2	9
Register	01011 reg				5	5	2	9
Segment Register	000 reg 111	(reg ≠ 01)			5	20	2	9, 10, 11
POPA = Pop All	01100001				19	19	2	9
XCHG = Exchange								
Register/Memory with Register	1000011w	mod reg r/m			3, 5 (Note 59)	3, 5 (Note 59)	2, 7	7, 9
Register with Accumulator	10010 reg				3	3		
IN = Input From								
Fixed Port	1110010w	port			5	5		14
Variable Port	1110110w				5	5		14
OUT = Output To								
Fixed Port	1110011w	port			3	3		14
Variable Port	1110111w				3	3		14
XLAT = Translate Byte to AL	11010111				5	5		9
LEA = Load EA to Register	10001101	mod reg r/m			3 (Note 59)	3 (Note 59)		
LDS = Load Pointer to DS	11000101	mod reg r/m	(mod ≠ 11)		7 (Note 59)	21 (Note 59)	2	9, 10, 11
LES = Load Pointer to ES	11000100	mod reg r/m	(mod ≠ 1)		7 (Note 59)	21 (Note 59)	2	9, 10, 11
LAHF Load AH with Flags	10011111				2	2		

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT				CLOCK COUNT		COMMENTS	
					REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE	REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE
SAHF = Store AH into Flags	10011110				2	2		
PUSHF = Push Flags	10011100				3	3	2	9
POPF = Pop Flags	10011101				5	5	2, 4	9, 15
ARITHMETIC								
ADD = Add								
Reg/Memory with Register to Either	000000dw	mod reg r/m			2, 7 (Note 59)	2, 7 (Note 59)	2	9
Immediate to Register/Memory	100000sw	mod 000 r/m	data	data if sw = 01	3, 7 (Note 59)	3, 7 (Note 59)	2	9
Immediate to Accumulator	0000010w	data	data if w = 1		3	3		
ADC = Add with Carry								
Reg/Memory with Register to Either	000100dw	mod reg r/m			2, 7 (Note 59)	2, 7 (Note 59)	2	9
Immediate to Register/Memory	100000sw	mod 010 r/m	data	data if sw = 01	3, 7 (Note 59)	3, 7 (Note 59)	2	9
Immediate to Accumulator	0001010w	data	data if w = 1		3	3		
INC = Increment								
Register/Memory	1111111w	mod 000 r/m			2, 7 (Note 59)	2, 7 (Note 59)	2	9
Register	01000 reg				2	2		
SUB = Subtract								
Reg/Memory and Register to Either	001010dw	mod reg r/m			2, 7 (Note 59)	2, 7 (Note 59)	2	9
Immediate from Register/Memory	100000sw	mod 101 r/m	data	data if sw = 01	3, 7 (Note 59)	3, 7 (Note 59)	2	9
Immediate from Accumulator	0010110w	data	data if w = 1		3	3		
SBB = Subtract with Borrow								
Reg/Memory and Register to Either	000110dw	mod reg r/m			2, 7 (Note 59)	2, 7 (Note 59)	2	9
Immediate from Register/Memory	100000sw	mod 011 r/m	data	data if sw = 01	3, 7 (Note 59)	3, 7 (Note 59)	2	9
Immediate from Accumulator	0001110w	data	data if w = 1		3	3		
DEC = Decrement								
Register/Memory	1111111w	mod 001 r/m			2, 7 (Note 59)	2, 7 (Note 59)	2	9
Register	01001 reg				2	2		

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT				CLOCK COUNT		COMMENTS	
					REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE	REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE
CMP = Compare								
Register/Memory with Register	0011101w	mod reg r/m			2, 6 (Note 59)	2, 6 (Note 59)	2	9
Register with Register/Memory	0011100w	mod reg r/m			2, 7 (Note 59)	2, 7 (Note 59)	2	9
Immediate with Register/Memory	100000sw	mod 111 r/m	data	data if sw = 01	3, 6 (Note 59)	3, 6 (Note 59)	2	9
Immediate with Accumulator	0011110w	data	data if w = 1		3	3		
NEG = Change Sign	1111011w	mod 011 r/m			2	7 (Note 59)	2	7
AAA = ASCII Adjust for Add	00110111				3	3		
DAA = Decimal Adjust for Add	00100111				3	3		
AAS = ASCII Adjust for Subtract	00111111				3	3		
DAS = Decimal Adlust for Subtract	00101111				3	3		
MUL = Multiply (Unsigned)	1111011w	mod 100 r/m						
Register - Byte					13	13		
Register - Word					21	21		
Memory - Byte					16 (Note 59)	16 (Note 59)	2	9
Memory - Word					24 (Note 59)	24 (Note 59)	2	9
IMUL = Integer Multiply (Signed)	1111011w	mod 101 r/m						
Register - Byte					13	13		
Register - Word					21	21		
Memory - Byte					16 (Note 59)	16 (Note 59)	2	9
Memory - Word					24 (Note 59)	24 (Note 59)	2	9
IMUL = Interger Immediate Multiply (Signed)	011010s1	mod reg r/m	data	data if s = 0	21, 24 (Note 59)	21, 24 (Note 59)	2	9
DIV = Divide (Unsigned)	1111011w	mod 110 r/m						
Register - Byte					14	14	6	6
Register - Word					22	22	6	6

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT				CLOCK COUNT		COMMENTS	
					REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE	REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE
Memory - Byte					17 (Note 59)	17 (Note 59)	2, 6	6, 9
Memory - Word					25 (Note 59)	25 (Note 59)	2, 6	6, 9
IDIV = Integer Divide (Signed)	1111011w	mod 111 r/m						
Register - Byte					17	17	6	6
Register - Word					25	25	6	6
Memory - Byte					20 (Note 59)	20 (Note 59)	2, 6	6, 9
Memory - Word					28 (Note 59)	28 (Note 59)	2, 6	6, 9
AAM = ASCII Adjust for Multiply	11010100	00001010			16	16		
AAD = ASCII Adjust for Divide	11010101	00001010			14	14		
CBW = Convert Byte to Word	10011000				2	2		
CWD = Convert Word to Double Word	10011001				2	2		
LOGIC								
Shift/Rotate Instructions								
Register/Memory by 1	1101000w	mod TTT r/m			2, 7 (Note 59)	2, 7 (Note 59)	2	9
Register/Memory by CL	1101001w	mod TTT r/m			5+n, 8+n (Note 59)	5+n, 8+n (Note 59)	2	9
Register/Memory by Count	1100000	mod TTT r/m	count		5+n, 8+n (Note 59)	5+n, 8+n (Note 59)	2	9
			TTT	Instruction				
			000	ROL				
			001	ROR				
			010	RCL				
			011	RCR				
			100	SHL/SAL				
			101	SHR				
			111	SAR				
AND = And								
Reg/Memory and Register to Either	001000dw	mod reg r/m			2, 7 (Note 59)	2, 7 (Note 59)	2	9

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT				CLOCK COUNT		COMMENTS	
					REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE	REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE
Immediate to Register/Memory	1000000w	mod 100 r/m	data	data if w = 1	3, 7 (Note 59)	3, 7 (Note 59)	2	9
Immediate to Accumulator	0010010w	data	data if w = 1		3	3		
TEST = And Function to Flags, No Result								
Register/Memory and Register	1000010w	mod reg r/m			2, 6 (Note 59)	2, 6 (Note 59)	2	9
Immediate Data and Register/Memory	1111011w	mod 000 r/m	data	data if w = 1	3, 6 (Note 59)	3, 6 (Note 59)	2	9
Immediate Data and Accumulator	1010100w	data	data if w = 1		3	3		
OR = Or								
Reg/Memory and Register to Either	000010dw	mod reg r/m			2, 7 (Note 59)	2, 7 (Note 59)	2	9
Immediate to Register/Memory	1000000w	mod 001 r/m	data	data if w = 1	3, 7 (Note 59)	3, 7 (Note 59)	2	9
Immediate to Accumulator	0000110w	data	data if w = 1		3	3		
XOR = Exclusive or								
Reg/Memory and Register to Either	001100dw	mod reg r/m			2, 7 (Note 59)	2, 7 (Note 59)	2	9
Immediate to Register/Memory	1000000w	mod reg r/m	data	data if w = 1	3, 7 (Note 59)	3, 7 (Note 59)	2	9
Immediate to Accumulator	0011010w	data	data if w = 1		3	3		
NOT = Invert Register/Memory	1111011w	mod 010 r/m			2, 7 (Note 59)	2, 7 (Note 59)	2	9
STRING MANIPULATION								
MOVS = Move Byte/Word	1010010w				5	5	2	9
CMPS = Compare Byte/Word	1010011w				8	8	2	9
SCAS = Scan Byte/Word	1010111w				7	7	2	9
LODS = Load Byte/Word to AL/AX	1010110w				5	5	2	9
STOS = Store Byte/Word from AL/A	1010101w				3	3	2	9
INS = Input Byte/Word from DX Port	0110110w				5	5	2	9, 14
OUTS = Output Byte/Word to DX Port	0110111w				5	5	2	9, 14
Repeated by Count in CX								
MOVS = Move String	11110011	1010010w			5 + 4n	5 + 4n	2	9

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT				CLOCK COUNT		COMMENTS	
					REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE	REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE
CMPS = Compare String	1111001z	1010011w			5 + 9n	5 + 9n	2, 8	8, 9
SCAS = Scan String	1111001z	1010111w			5 + 8n	5 + 8n	2, 8	8, 9
LODS = Load String	11110011	1010110w			5 + 4n	5 + 4n	2, 8	8, 9
STOS = Store String	11110011	1010101w			4 + 3n	4 + 3n	2, 8	8, 9
INS = Input String	11110011	0110110w			5 + 4n	5 + 4n	2	9, 14
OUTS = Output String	11110011	0110111w			5 + 4n	5 + 4n	2	9, 14
CONTROL TRANSFER								
CALL = Call								
Direct Within Segment	11101000	disp-low	disp-high		7 + m	7 + m	2	18
Register/Memory Indirect Within Segment	11111111	mod 010 r/m			7 + m, 11 + m (Note 59)	7 + m, 11 + m (Note 59)	2, 8	8, 9, 18
Direct Intersegment	10011010	Segment Offset			13 + m	26 + m	2	11, 12,18
Protected Mode Only (Direct Intersegment)		Segment Selector						
Via Call Gate to Same Privilege Level						41 + m		8, 11, 12, 18
Via Call Gate to Different Privilege Level, No Parameters						82 + m		8, 11, 12, 18
Via Call Gate to Different Privilege Level, X Parameters						86 + 4x + m		8, 11, 12, 18
Via TSS						177 + m		8, 11, 12, 18
Via Task Gate						182 + m		8, 11, 12, 18
Indirect Intersegment	11111111	mod 011 r/m	mod ≠ 11		16 + m (Note 59)	29 + m (Note 59)	2	8, 9, 11, 12, 18
Protected Mode Only (Indirect Intersegment)								
Via Call Gate to Same Privilege Level						44 + m (Note 59)		8, 9, 11, 12, 18
Via Call Gate to Different Privilege Level, No Parameters						83 + m (Note 59)		8, 9, 11, 12, 18
Via Call Gate to Different Privilege Level, X Parameters						90 + 4x + m (Note 59)		8, 9, 11, 12, 18
Via TSS						180 + m (Note 59)		8, 9, 11, 12, 18
Protected Mode Only (Indirect Intersegment) (Continued)								
Via Task Gate						185 + m (Note 59)		8, 9, 11, 12, 18

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT				CLOCK COUNT		COMMENTS	
					REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE	REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE
JMP = Unconditional Jump								
Short/Long	11101011	disp-low			7 + m	7 + m		18
Direct Within Segment	11101001	disp-low	disp-high		7 + m	7 + m		18
Register/Memory Indirect Within Segment	11111111	mod 100 r/m			7 + m, 11 + m (Note 59)	7 + m, 11 + m (Note 59)	2	9, 18
Direct Intersegment	11101010	Segment Offset			11 + m	23 + m		11, 12, 18
Protected Mode Only (Direct Intersegment)		Segment Selector						
Via Call Gate to Same Privilege Level						38 + m		8, 11,12,18
Via TSS						175 + m		8, 11,12,18
Via Task Gate						180 + m		8, 11,12,18
Indirect Intersegment	11111111	mod 101 r/m	mod ≠ 11		15 + m (Note 59)	26 + m (Note 59)	2	8, 9, 11, 12, 18
Protected Mode Only (Indirect Intersegment)								
Via Call Gate to Same Privilege Level						41 + m (Note 59)		8, 9, 11, 12, 18
Via TSS						178 + m (Note 59)		8, 9, 11, 12, 18
Via Task Gate						183 + m (Note 59)		8, 9, 11, 12, 18
RET = Return from CALL								
Within Segment	11000011				11 + m	11 + m	2	8, 9, 18
Within Segment Adding Immediate to SP	11000010	data-low	data-high		11 + m	11 + m	2	8, 9, 18
Intersegment	11001011				15 + m	25 + m	2	8, 9, 11, 12, 18
Intersegment Adding Immediate to SP	11001010	data-low	data-high		15 + m		2	8, 9, 11, 12, 18
Protected Mode Only (RET)								
To Different Privilege Level						55 + m		9, 11, 12, 18
JE/JZ = Jump on Equal Zero	01110100	disp			7 + m or 3	7 + m or 3		18
JL/JNGE = Jump on Less/Not Greater or Equal	01111100	disp			7 + m or 3	7 + m or 3		18
JLE/JNG = Jump on Less or Equal/not Greater	01111110	disp			7 + m or 3	7 + m or 3		18

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT				CLOCK COUNT		COMMENTS	
					REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE	REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE
JB/JNAE = Jump on Below/Not Above or Equal	01110010	disp			7 + m or 3	7 + m or 3		18
JBE/JNA = Jump on Below or Equal/Not Above	01110110	disp			7 + m or 3	7 + m or 3		18
JP/JPE = Jump on Parity/Parity Even	01111010	disp			7 + m or 3	7 + m or 3		18
JO = Jump on Overflow	01110000	disp			7 + m or 3	7 + m or 3		18
JS = Jump on Sign	01111000	disp			7 + m or 3	7 + m or 3		18
JNE/JNZ = Jump on Not Equal/Not Zero	01110101	disp			7 + m or 3	7 + m or 3		18
JNL/JGE = Jump on Not Less/Greater or Equal	01111101	disp			7 + m or 3	7 + m or 3		18
JNLE/JG = Jump on Not Less or Equal/Greater	01111111	disp			7 + m or 3	7 + m or 3		18
JNB/JAE = Jump on Not Below/Above or Equal	01110011	disp			7 + m or 3	7 + m or 3		18
JNBE/JA = Jump on Not Below or Equal/Above	01110111	disp			7 + m or 3	7 + m or 3		18
JNP/JPO = Jump on Not Par/Par Odd	01111011	disp			7 + m or 3	7 + m or 3		18
JNO = Jump on Not Overflow	01110001	disp			7 + m or 3	7 + m or 3		18
JNS = Jump on Not Sign	01111001	disp			7 + m or 3	7 + m or 3		18
LOOP Loop CX Times	11100010	disp			8 + m or 4	8 + m or 4		18
LOOPZ/LOOPE = Loop While Zero/Equal	11100001	disp			8 + m or 4	8 + m or 4		18
LOOPNZ/LOOPNE = Loop While Not Zero/Equal	11100000	disp			8 + m or 4	8 + m or 4		18
JCXZ = Jump on CX Zero	11100011	disp			8 + m or 4	8 + m or 4		18
ENTER = Enter Procedure	11001000	data-low	data-high	L			2, 8	8, 9
L = 0					11	11	2, 8	8, 9
L = 1					15	15	2, 8	8, 9
L > 1					16 + 4(L - 1)	16 + 4(L - 1)	2, 8	8, 9
LEAVE = Leave Procedure	11001001				5	5		
INT = Interrupt								
Type Specified	11001101	type			23 + m		2, 7, 8	
Type 3	11001100				23 + m		2, 7, 8	

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT				CLOCK COUNT		COMMENTS	
					REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE	REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE
INTO = Interrupt on Overflow	11001110				24 + m or 3 (3 if no interrupt)	(3 if no interrupt)	2, 6, 8	
Protected Mode Only								
Via Interrupt or Trap Gate to Same Privilege Level						40 + m		7, 8, 11, 12, 18
Via Interrupt or Trap Gate to Fit Different Pnvilege Level						78 + m		7, 8, 11, 12, 18
Via Task Gate						167 + m		7, 8, 11, 12, 18
IRET Interrupt Return	11001111				17 + m	31 + m	2, 4	8, 9, 11, 12, 15, 18
Protected Mode Only								
To Different Privilege Level						55 + m		8, 9, 11, 12, 15, 18
To Different Task (NT = 1)						169 + m		8, 9, 11, 12, 18
BOUND = Detect Value Out of Range	01100010	mod reg r/m			13 (Note 59)	13 (Use INT clock count if exception 5) (Note 59)	2, 6	6, 8, 9, 11, 12, 18
PROCESSOR CONTROL								
CLC = Clear Carry	11111000				2	2		
CMC = Complement Carry	11110101				2	2		
STC = Set Carry	11111001				2	2		
CLD = Clear Direction	11111100				2	2		
STD = Set Direction	11111101				2	2		
CLI = Clear Interrupt	11111010				3	3		14
STI = Set Interrupt	11111011				2	2		14
HLT = Halt	11110100				2	2		13
WAIT = Wait	10011011				3	3		
LOCK = Bus Lock Prefix	11110000				0	0		14
CTS = Clear Task Switched Flag	00001111	00000110			2	2	3	13

80C286 Instruction Set Summary (Continued)

FUNCTION	FORMAT				CLOCK COUNT		COMMENTS	
					REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE	REAL ADDRESS MODE	PROTECTED VIRTUAL ADDRESS MODE
ESC = Processor Extension Escape	11011TTT	mod LLL r/m			9-20 (Note 59)	9-20 (Note 59)	5, 8	8, 17
	(TTT LLL Are Opcode to Processor Extension)							
SEG = Segment Override Prefix	001 reg 110				0	0		
PROTECTION CONTROL								
LGDT = Load Global Descriptor Table Register	00001111	00000001	mod 010 r/m		11 (Note 59)	11 (Note 59)	2, 3	9, 13
SGDT = Store Global Desceptor Table Register	00001111	00000001	mod 000 r/m		11 (Note 59)	11 (Note 59)	2, 3	9
LIDT = Load Interrupt Descriptor Table Register	00001111	00000001	mod 011 r/m		12 (Note 59)	12 (Note 59)	2, 3	9, 13
SIDT = Store Interrupt Descriptor Table Register	00001111	00000001	mod 001 r/m		12 (Note 59)	12 (Note 59)	2, 3	9
LLDT = Load Local Descriptor Table Register From Register Memory	00001111	00000000	mod 010 r/m			17, 19 (Note 59)	1	9, 11, 13
SLDT = Store Local Descriptor Table Register To Register/Memory	00001111	00000000	mod 000 r/m			2, 3 (Note 59)	1	9
LTR = LTR = Local Task Register From Register/Memory	00001111	00000000	mod 011 r/m			17, 19 (Note 59)	1	9, 11, 13
STR = Store Task Register To Register Memory	00001111	00000000	mod 001 r/m			2, 3 (Note 59)	1	9
LMSW = Load Machine Status Word From Register/Memory	00001111	00000001	mod 110 r/m		3, 6 (Note 59)	3, 6 (Note 59)	2, 3	9, 13
SMSW = Store Machine Status Word	00001111	00000001	mod 100 r/m		2, 3 (Note 59)	2, 3 (Note 59)	2, 3	9
LAR = Load Access Rights From Register/Memory	00001111	00000010	mod reg r/m			14, 16 (Note 59)	1	9, 11, 16
LSL = Load Segment Limit From Register/Memory	00001111	00000011	mod reg r/m			14, 16 (Note 59)	1	9, 11, 16
ARPL = Adjust Requested Privilege Level: From Register/Memory		01100011	mod reg r/m		10, 11 (Note 59)	2	8, 9	
VERR = Verify Read Access: Register/Memory	00001111	00000000	mod 100 r/m		14, 16 (Note 59)	1	9, 11, 16	
VERR = Verify Write Access:	00001111	00000000	mod 101 r/m		14, 16 (Note 59)	1	9, 11, 16	

NOTE:

59. Shaded areas indicate instructions not available in 80G86/88 microsystems.

80C286 Machine Instruction Encoding Matrix

HI	LO 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	ADD b, f, r/m	ADD w, f, r/m	ADD b, t, r/m	ADD w, t, r/m	ADD b, ia	ADD w, ia	PUSH ES	POP ES	OR b, f, r/m	OR w, f, r/m	OR b, t, r/m	OR w, t, r/m	OR b, i	OR w, i	PUSH CS	PVAM n
1	ADC b, f, r/m	ADC w, f, r/m	ADC b, t, r/m	ADC w, t, r/m	ADC b, ia	ADC w, ia	PUSH SS	POP SS	SBB b, f, r/m	SBB w, f, r/m	SBB b, t, r/m	SBB w, t, r/m	SBB b, i	SBB w, i	PUSH DS	POP DS
2	AND b, f, r/m	AND w, f, r/m	AND b, t, r/m	AND w, t, r/m	AND b, ia	AND w, ia	SEG =ES	DAA	SUB b, f, r/m	SUB w, f, r/m	SUB b, t, r/m	SUB w, t, r/m	SUB b, i	SUB w, i	SEG =CS	DAS
3	XOR b, f, r/m	XOR w, f, r/m	XOR b, t, r/m	XOR w, t, r/m	XOR b, ia	XOR w, ia	SEG =SS	AAA	CMP b, f, r/m	CMP w, f, r/m	CMP b, t, r/m	CMP w, t, r/m	CMP b, i	CMP w, i	SEG =DS	AAS
4	INC AX	INC CX	INC DX	INC BX	INC SP	INC BP	INC SI	INC DI	DEC AX	DEC CX	DEC DX	DEC BX	DEC SP	DEC BP	DEC SI	DEC DI
5	PUSH AX	PUSH CX	PUSH DX	PUSH BX	PUSH SP	PUSH SI	PUSH SI	PUSH DI	POP AX	POP CX	POP DX	POP BX	POP SP	POP BP	POP SI	POP DI
6	PUSHA	POPA	BOUND	ARPL					PUSH w, i	IMUL w, t, r/m, i	PUSH b, i	IMUL b, t, r/m, i	INSB	INSW	OUTSB	OUTSW
7	JO	JNO	JB/ JNAE	JNB/ JAE	JE/ JZ	JNE/ JNZ	JBE/ JNA	JNBE/ JA	JS	JNS	JP/ JPE	JNP/ JPO	JL/ JNGE	JNL/ JGE	JLE/ JNG	JNLE/ JG
8	Immed b, r/m	Immed w, r/m	Immed b, r/m	Immed is, r/m	TEST b, r/m	TEST w, r/m	XCHG b, r/m	XCHG w, r/m	MOV b, f, r/m	MOV w, f, r/m	MOV b, t, r/m	MOV w, t, r/m	MOV sr, f, r/m	LEA	MOV sr, t, r/m	POP r/m
9	XCHG AX	XCHG CX	XCHG DX	XCHG BX	XCHG SP	XCHG BP	XCHG SI	XCHG DI	CBW	CWD	CALL i, d	WAIT	PUSHF	POPF	SAHF	LAHF
A	MOV m-AL	MOV m-AX	MOV AL-m	MOV AX-m	MOVSB	MOVSW	CMPSB	CMPSW	TEST b, i, a	TEST w, i, a	STOSB	STOSW	LODSB	LODSW	SCASB	SCASW
B	MOV i-AL	MOV i-CL	MOV i-DL	MOV i-BL	MOV i-AH	MOV i-CH	MOV i-DH	MOV i-BH	MOV i-AX	MOV i-CX	MOV i-DX	MOV i-BX	MOV i-SP	MOV i-BP	MOV i-SI	MOV i-DI
C	Shift b, i	Shift w, i	RET (i+SP)	RET	LES	LDS	MOV b, i, r/m	MOV w, i, r/m	ENTER	LEAVE	RET I, (i+SP)	RET I	INT Type 3	INT (any)	INTO	IRET
D	Shift b	Shift w	Shift b, CL	AAM	AAD		XLAT	ESC 0	ESC 1	ESC 2	ESC 3	ESC 4	ESC 5	ESC 6	ESC 6	ESC 7
E	LOOPNZ/ LOOPNE	LOOPZ/ LOOPE	LOOP	JCXZ	IN b	IN w	OUT b	OUT w	CALL d	JMP d	JMP i, d	JMP si, d	IN DX, b	IN DX, w	OUT DX, b	OUT DX, w
F	LOCK		REP	REPZ	HLT	CMC	Grp 1 b, r/m	Grp 1 w, r/m	CLC	STC	CLI	STI	CLD	STD	Grp 2 b, r/m	Grp 2 w, r/m

where:

80C286 Machine Instruction Encoding Matrix (Continued)

mod r/mm	000	001	010	011	100	101	110	111
Immed	ADD	OR	ADC	SBB	AND	SUB	XOR	CMP
Shift	ROL	ROR	RCL	RCR	SHL/SAL	SHR	-	SAR
Grp 1	TEST	-	NOT	NEG	MUL	IMUL	DIV	IDIV
Grp 2	INC	DEC	CALL id	CALL I, id	JMP id	JMP I, id	PUSH	-
PVAM 0	SLDT	STR	LLDT	LTR	VERR	VERW	-	-
PVAM 1	SGDT	SIDT	LGDT	LIDT	SMSW	-	LMSW	-
PVAM 2	LAR							
PVAM 3	LSL							
PVAM 6	CLTS							

b = byte operation
d = direct
f = from CPU reg
i = immediate
ia = immediate to AX
id = indirect
is = immediate byte sign extension
l = long i.e., intersegment
n = 2nd byte of PVAM instruction
m = memory
r/m = EA is second byte
is = short intrasegment
sr = segment register
t = to CPU register
v = variable
w = word operation
z = zero

Footnotes

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field

if mod = 00 then DISP = 0†, disp-low and disp-high are absent

if mod = 01 then DISP = disp-low sign extended to 16 bits, disp-high is absent

if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP

if r/m = 001 then EA = (BX) + (DI) + DISP

if r/m = 010 then EA = (BP) + (SI) + DISP

if r/m = 011 then EA = (BP) + (DI) + DISP

if r/m = 100 then EA = (SI) + DISP

if r/m = 101 then EA = (DI) + DISP

if r/m = 110 then EA + (BP) + DISP (Note 60)

if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data is required)

NOTE:

60. Except if mod = 00 and r/m = 110 then EQ = disp-high: disp-low.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

REG	SEGMENT REGISTER
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-BIT (w = 1)		8-BIT (w = 0)	
000	AX	000	AL
001	CX	001	CL
010	DX	010	DL
011	BX	011	BL
100	SP	100	AH
101	BP	101	CH
110	SI	110	DH
111	DI	111	BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

HARRIS SEMICONDUCTOR

80C286/883

High Performance Microprocessor with Memory Management and Protection

March 1997

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Compatible with NMOS 80286/883**
- **Static CMOS Design for Low Power Operation**
  - **ICCSB = 5mA Maximum**
  - **ICCOP = 185mA Maximum (80C286-10/883)**
  - **ICCOP = 220mA Maximum (80C286-12/883)**
- **Large Address Space**
  - **16 Megabytes Physical**
  - **1 Gigabyte Virtual per Task**
- **Integrated Memory Management, Four-Level Memory Protection and Support for Virtual Memory and Operating Systems**
- **Two 80C86 Upward Compatible Operating Modes**
  - **80C286/883 Real Address Mode**
  - **Protected Virtual Address Mode**
- **Compatible with 80287 Numeric Data Co-Processor**

Description

The Harris 80C286/883 is a static CMOS version of the NMOS 80286 microprocessor. The 80C286/883 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. The 80C286/883 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. The 80C286/883 includes memory management capabilities that map 230 (one gigabyte) of virtual address space per task into 2^{24} bytes (16 megabytes) of physical memory.

The 80C286/883 is upwardly compatible with 80C86 and 80C88 software (the 80C286/883 instruction set is a superset of the 80C86/80C88 instruction set). Using the 80C286/883 real address mode, the 80C286/883 is object code compatible with existing 80C86 and 80C88 software. In protected virtual address mode, the 80C286/883 is source code compatible with 80C86 and 80C88 software but may require upgrading to use virtual address as supported by the 80C286/883's integrated memory management and protection mechanism. Both modes operate at full 80C286/883 performance and execute a superset of the 80C86 and 80C88 instructions.

The 80C286/883 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The segment-not-present exception and restartable instructions.

Ordering Information

PACKAGE	TEMP. RANGE	10MHz	12.5MHz	16MHz	20MHz	25MHz	PKG. NO.
68 Pin PGA	0°C to +70°C	-	CG80C286-12	CG80C286-16	CG80C286-20	-	G68.B
	-40°C to +85°C	IG80C286-10	IG80C286-12	-	-	-	G68.B
	-55°C to +125°C	MG80C286-10/883	MG80C286-12/883	-	-	-	G68.B
		5962-9067801MXC	5962-9067802MXC	-	-	-	G68.B

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

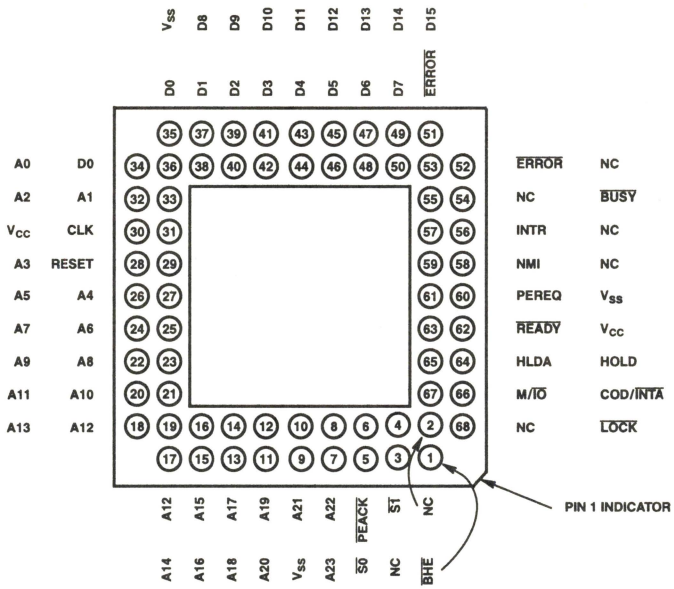
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File Number **2948.1**

Pinout

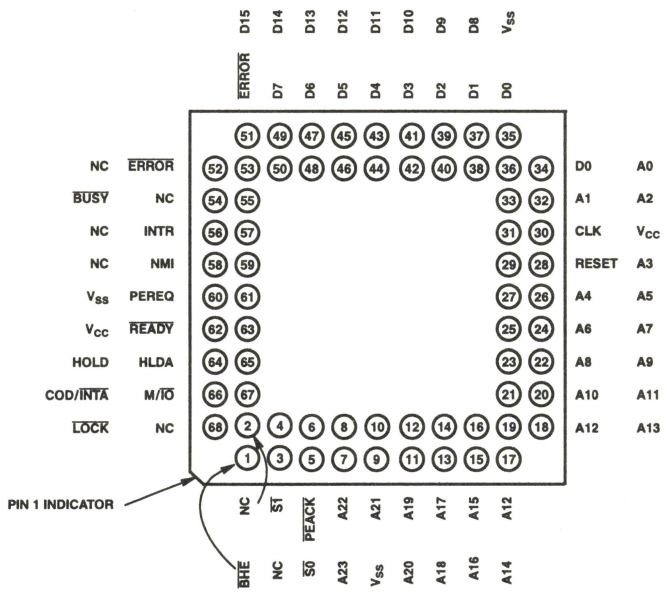
68 LEAD PGA, COMPONENT PAD VIEW

As viewed from underside of the component when mounted on the board.



P.C. BOARD VIEW

As viewed from the component side of the P.C. board.



Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage Applied. . . . . GND -1.0V to V_{CC} +1.0V
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Temperature (Soldering 10s) . . . . . +300°C
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
PGA Package	35°C/W	6°C/W

Gate Count . . . . . 22,500 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
System Clock (CLK) RISE Time (From 1.0V to 3.6V . . . . 8ns (Max)
System Clock (CLK) FALL Time (from 3.6V to 1.0V) . . . . 8ns (Max)
Input RISE and FALL Time (From 0.8V to 2.0V
80C286-10/883 . . . . . 10ns (Max)
80C286-12/883 . . . . . 8ns (Max)

TABLE 1. 80C286/883 D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input LOW Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-0.5	0.8	V
Input HIGH Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.0	V_{CC} +0.5	V
CLK Input LOW Voltage	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-0.5	1.0	V
CLK Input HIGH Voltage	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	3.6	V_{CC} +0.5	V
Output LOW Voltage	V_{OL}	I_{OL} = 2.0mA, V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
Output HIGH Voltage	V_{OH}	I_{OH} = -2.0mA, V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	3.0	-	V
		I_{OH} = -100µA, V_{CC} = 4.5V			V_{CC} -0.4	-	V
Input Leakage Current	I_I	V_{IN} = GND or V_{CC}, V_{CC} = 5.5V, Pins 29, 31, 57, 59, 61, 63-64	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	10	µA
Input Sustaining Current LOW	I_{BHL}	V_{CC} = 4.5V and 5.5V, V_{IN} = 1.0V, Note 1	1, 2, 3	-55°C ≤ T_A ≤ +125°C	38	200	µA
Input Sustaining Current HIGH	I_{BHH}	V_{CC} = 4.5V and 5.5V, V_{IN} = 3.0V, Note 2	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-50	-400	µA
Input Sustaining Current on $\overline{BUSY}$ and $\overline{ERROR}$ Pins	I_{SH}	V_{CC} = 4.5V and 5.5V V_{IN} = GND, Note 5	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-30	-500	µA
Output Leakage Current	I_O	V_O = GND or V_{CC} V_{CC} = 5.5V, Pins 1, 7-8, 10-28, 32-34	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	10	µA
Active Power Supply Current	I_{CCOP}	80C286-10/883, Note 4	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	185	mA
		80C286-12/883, Note 4			-	220	mA
Standby Power Supply Current	I_{CCSB}	V_{CC} = 5.5V, Note 3	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	5	mA

NOTES:

2. I_{BHL} should be measured after lowering V_{IN} to GND and then raising to 1.0V on the following pins: 36-51, 66, 67.
3. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering to 3.0V on the following pins: 4-6, 36-51, 66-68.
4. I_{CCSB} should be tested with the clock stopped in phase two of the processor clock cycle. V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, outputs unloaded.
5. I_{CCOP} measured at 10MHz for the 80C286-10/883 and 12.5MHz for the 80C286-12/883. V_{IN} = 2.4V or 0.4V, V_{CC} = 5.5V, outputs unloaded.
6. I_{SH} should be measured after raising V_{IN} to V_{CC} and then lowering to 0V on pins 53 and 54.

TABLE 2. 80C286/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

AC Timings are Referenced to 0.8V and 2.0V Points of the Signals as Illustrated in Datasheet Waveforms, Unless Otherwise Noted. Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	80C286/883				UNITS
					10MHz		12.5MHz		
					MIN	MAX	MIN	MAX	
System Clock (CLK) Period	1	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	50	-	40	-	ns
System Clock (CLK) Low Time	2	V_{CC} = 4.5V and 5.5V at 1.0V	9, 10, 11	-55°C ≤T_A ≤ +125°C	12	-	11	-	ns
System Clock (CLK) High Time	3	V_{CC} = 4.5V and 5.5V at 3.6V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	16	-	13	-	ns
Asynchronous Inputs SETUP Time (Note 1)	4	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	20	-	15	-	ns
Asynchronous Inputs HOLD Time (Note 1)	5	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	20	-	15	-	ns
RESET SETUP Time	6	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	19	-	10	-	ns
RESET HOLD Time	7	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	0	-	0	-	ns
Read Data SETUP Time	8	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	8	-	5	-	ns
Read Data HOLD Time	9	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	4	-	4	-	ns
$\overline{\text{READY}}$ SETUP Time	10	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	26	-	20	-	ns
$\overline{\text{READY}}$ HOLD Time	11	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤T_A ≤ +125°C	25	-	20	-	ns
Status/$\overline{\text{PEACK}}$ Active Delay, (Note 4)	12A	V_{CC} = 4.5V and 5.5V, C_L = 100pF I_L = I2mAI	9, 10, 11	-55°C ≤ T_A ≤ +125°C	1	22	1	21	ns
Status/$\overline{\text{PEACK}}$ Inactive Delay (Note 3)	12B	V_{CC} = 4.5V and 5.5V, C_L = 100pF I_L = I2mAI	9, 10, 11	-55°C ≤ T_A ≤ +125°C	1	30	1	24	ns
Address Valid Delay (Note 2)	13	V_{CC} = 4.5V and 5.5V, C_L = 100pF I_L = I2mAI	9, 10, 11	-55°C ≤ T_A ≤ +125°C	1	35	1	32	ns
Write Data Valid Delay, (Note 2)	14	V_{CC} = 4.5V and 5.5V, C_L = 100pF I_L = I2mAI	9, 10, 11	-55°C ≤ T_A ≤ +125°C	0	40	0	31	ns

TABLE 2. 80C286/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

AC Timings are Referenced to 0.8V and 2.0V Points of the Signals as Illustrated in Datasheet Waveforms, Unless Otherwise Noted. Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	80C286/883				UNITS
					10MHz		12.5MHz		
					MIN	MAX	MIN	MAX	
HLDA Valid Delay (Note 5)	15	V_{CC} = 4.5V and 5.5V, C_L = 100pF IL = I2mAI	9, 10, 11	-55°C ≤ T_A ≤ +125°C	0	47	0	25	ns

NOTES:

1. Asynchronous inputs are INTR, NMI, HOLD, PEREQ, ERROR, and BUSY. This specification is given only for testing purposes, to assure recognition at a specific CLK edge.
2. Delay from 1.0V on the CLK to 0.8V or 2.0V.
3. Delay from 1.0V on the CLK to 0.8V for Min (HOLD time) and to 2.0V for Max (inactive delay).
4. Delay from 1.0V on the CLK to 2.0V for Min (HOLD time) and to 0.8V for Max (active delay).
5. Delay from 1.0V on the CLK to 2.0V.

TABLE 3. 80C286/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	80C286/883				UNITS
					10MHz		12.5MHz		
					MIN	MAX	MIN	MAX	
CLK Input Capacitance	C_{CLK}	FREQ = 1MHz	5	T_A = +25°C	-	10	-	10	pF
Other Input Capacitance	C_{IN}	FREQ = 1MH	5	T_A = +25°C	-	10	-	10	pF
I/O Capacitance	$C_{I/O}$	FREQ = 1MH	5	T_A = +25°C	-	10	-	10	pF
Address/Status/Data Float Delay	15		1, 3, 4, 5	-55°C ≤ T_A ≤ +125°C	0	47	0	32	ns
Address Valid to Status SETUP Time	19	I_L = I2.0mAI	1, 2, 5	-55°C ≤ T_A ≤ +125°C	27	-	20	-	ns

NOTES:

1. Output Load: C_L = 100pF.
2. Delay measured from address either reaching 0.8V or 2.0V (valid) to status going active reaching 0.8V or status going inactive reaching 2.0V.
3. Delay from 1.0V on the CLK to Float (no current drive) condition.
4. I_L = -6mA (V_{OH} to Float), I_L = 8mA (V_{OL} to Float).
5. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C & D	Samples/5005	1, 7, 9

AC Electrical Specifications

82C284 and 82C288 Timing Specifications Are Given For Reference Only, And No Guarantee is Implied.

82C284 Timing

SYMBOL	PARAMETER	10MHz		12.5MHz		UNIT	TEST CONDITION
		MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS							
11	$\overline{SRDY}/\overline{SRDYEN}$ Setup Time	15	-	15	-	ns	
12	$\overline{SRDY}/\overline{SRDYEN}$ Hold Time	2	-	2	-	ns	
13	$\overline{ARDY}/\overline{ARDYEN}$ Setup Time	5	-	5	-	ns	(Note 1)
14	$\overline{ARDY}/\overline{ARDYEN}$ Hold Time	30	-	25	-	ns	(Note 1)
TIMING RESPONSES							
19	PCLK Delay	0	20	0	16	ns	C_L = 75pF, I_{OL} = 5mA, I_{OH} = -1mA

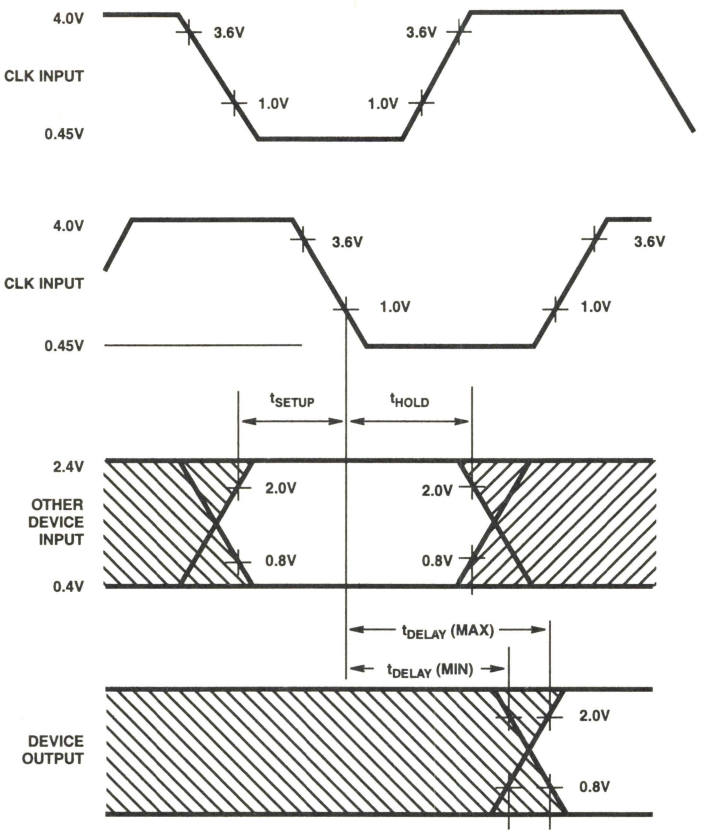
NOTE:

1. These times are given for testing purposes to ensure a predetermined action.

82C288 Timing

SYMBOL	PARAMETER	10MHz		12.5MHz		UNIT	TEST CONDITION
		MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS							
12	CMDLY Setup Time	15	-	15	-	ns	
13	CMDLY Hold Time	1	-	1	-	ns	
TIMING RESPONSES							
16	ALE Active Delay	1	16	1	16	ns	
17	ALE Inactive Delay	-	19	-	19	ns	
19	DT/$\overline{R}$ Read Active Delay	-	23	-	23	ns	C_L = 150pF
20	DEN Read Active Delay	0	21	0	21	ns	I_{OL} = 16mA Max
21	DEN Read Inactive Delay	3	23	3	21	ns	I_{OH} = -1mA Max
22	DT/$\overline{R}$ Read Inactive Delay	5	24	5	18	ns	
23	DEN Write Active Delay	-	23	-	23	ns	
24	DEN Write Inactive Delay	3	23	3	23	ns	
29	Command Active Delay from CLK	3	21	3	21	ns	C_L = 300pF
30	Command Inactive Delay from CLK	3	20	3	20	ns	I_{OL} = 32mA Max

AC Specifications

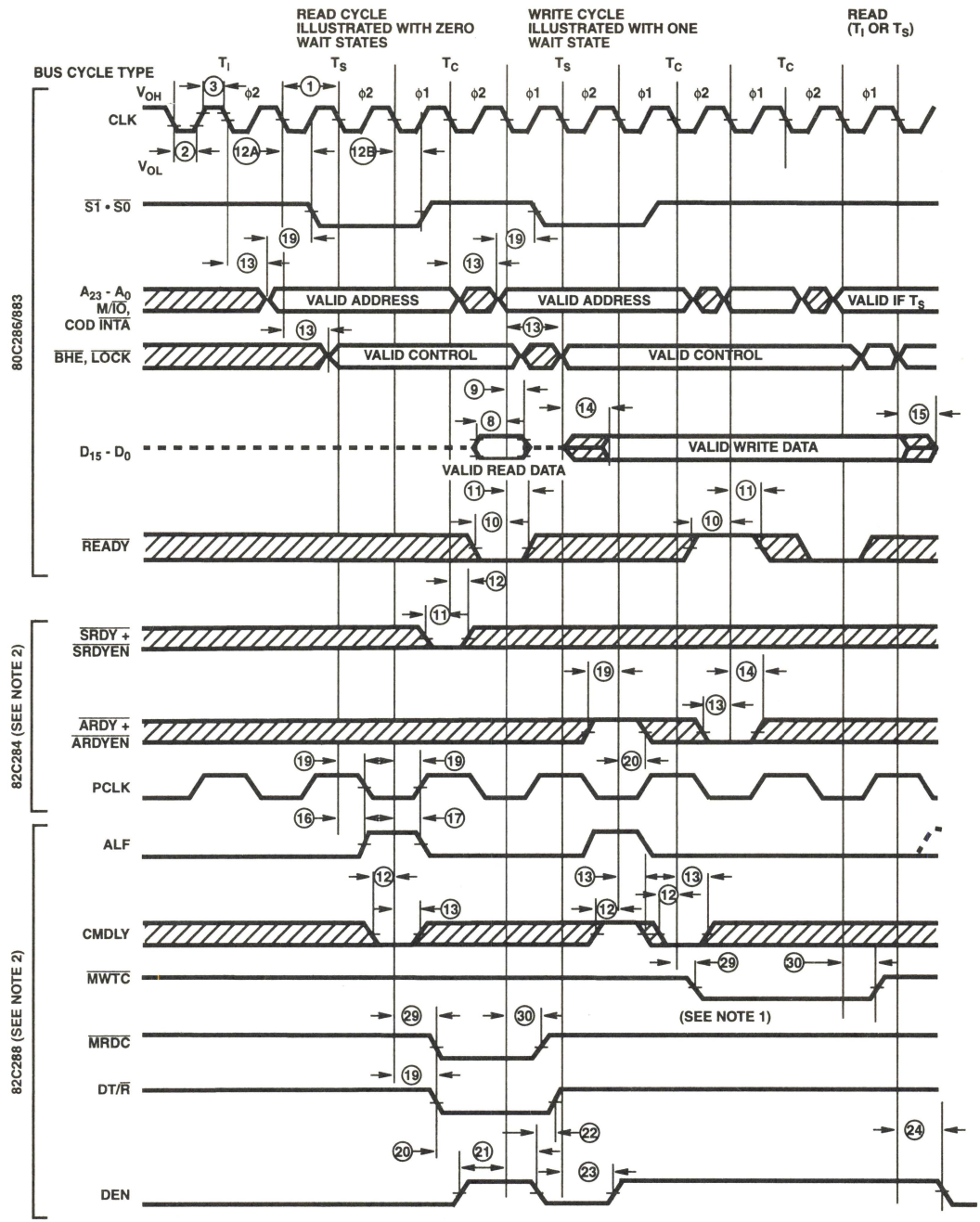


NOTE:

1. For AC testing, input rise and fall times are driven at 1ns per volt.

FIGURE 1. AC DRIVE AND MEASURE POINTS - CLK INPUT

Waveforms

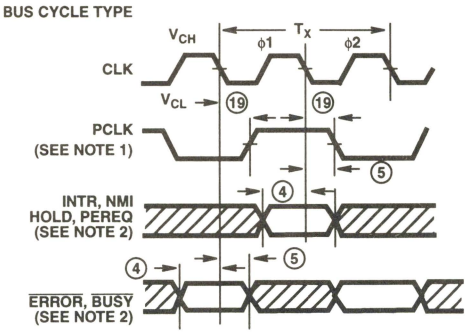


NOTES:

1. The modified timing is due to the CMDLY signal being active.
2. 82C254 and 82C288 Timing Waveforms are shown for reference only, and no guarantee is inplied.

FIGURE 2. MAJOR CYCLE TIMING

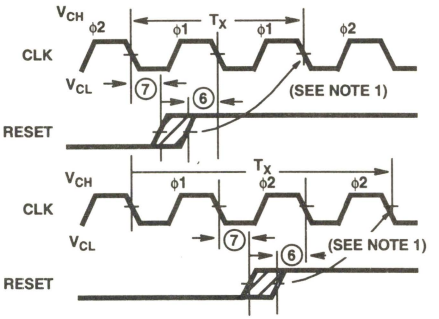
Waveforms (Continued)



NOTES:

1. PCLK indicates which processor cycle phase will occur on the next CLK. PCLK may not indicate the correct phase until the first cycle is performed.
2. These inputs are asynchronous. The setup and hold times shown assure recognition for testing purposes.

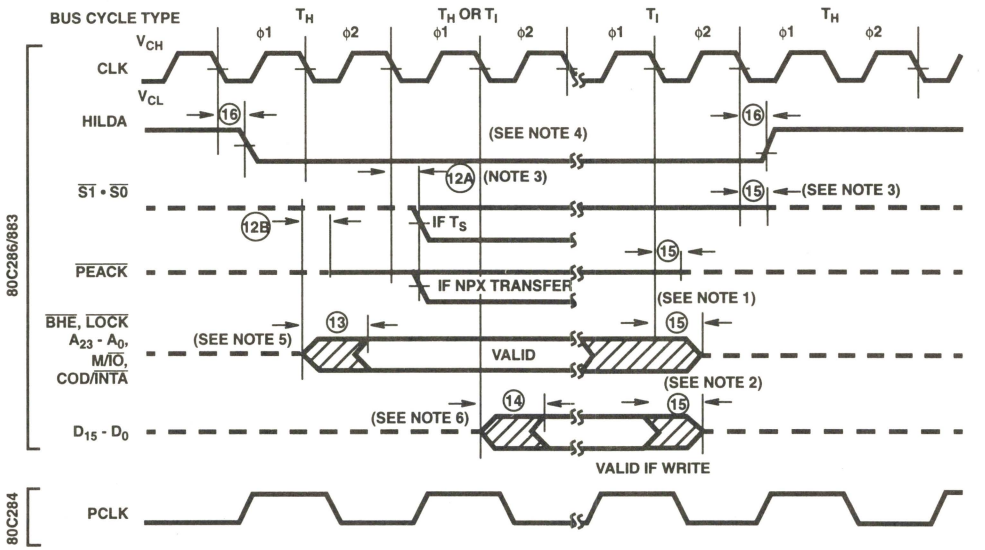
FIGURE 3. 80C286/883 ASYNCHRONOUS INPUT SIGNAL TIMING



NOTE:

1. When RESET meets the setup time shown, the next CLK will start or repeat φ1 of a processor cycle.

FIGURE 4. 80C286/883 RESET INPUT TIMING AND SUBSEQUENT PROCESSOR CYCLE PHASE

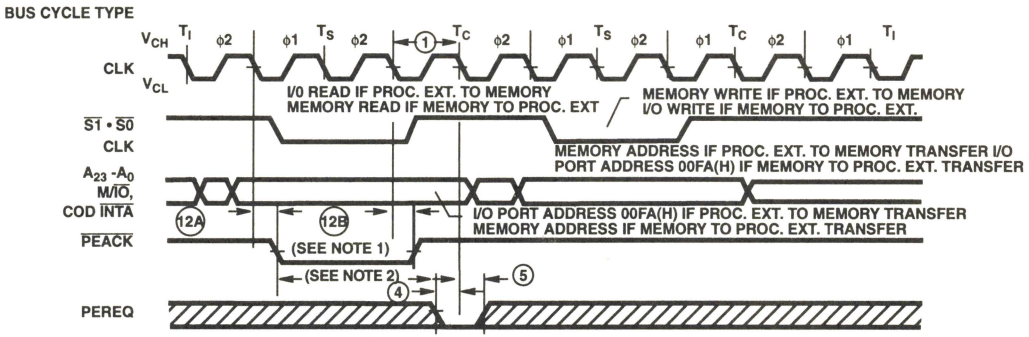


NOTES:

1. These signals may not be driven by the 80C286/883 during the time shown. The worst case in terms of latest float time is shown.
2. The data bus will be driven as shown if the last cycle before T_I in the diagram was a write T_C.
3. The 80C286/883 puts its status pins in a high impedance logic one state during T_H.
4. For HOLD request set up to HLDA, refer to Figure 8.
5. $\overline{BHE}$ and $\overline{LOCK}$ are driven at this time but will not become valid until T_S.
6. The data bus will remain in a high impedance state if a read cycle is performed.

FIGURE 5. EXITING AND ENTERING HOLD

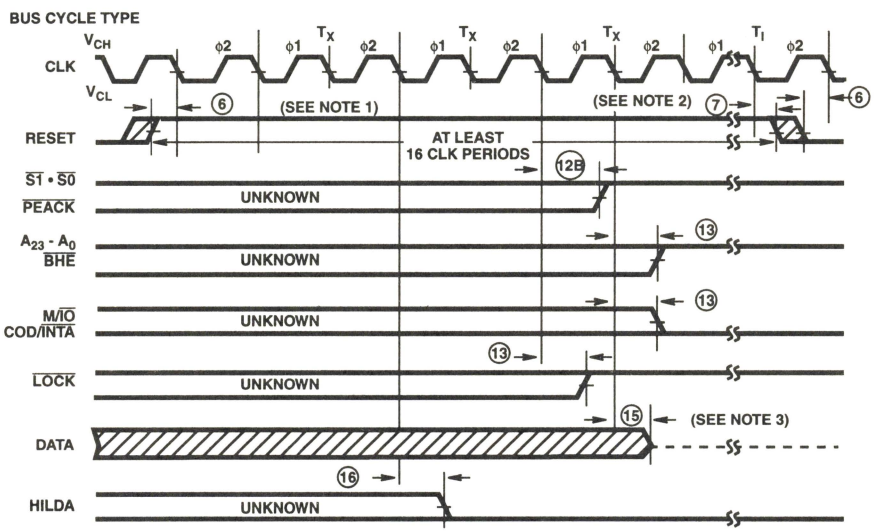
Waveforms (Continued)



NOTES:

1. $\overline{\text{PEACK}}$ always goes active during the first bus operation of a processor extension data operand transfer sequence. The first bus operation will be either a memory read at operand address or I/O read at port address 00FA(H).
2. To prevent a second processor extension data operand transfer, the worst case maximum time (shown above) is 3 x (1) - $12A_{MAX}$ -$(4)_{MIN}$ The actual, configuration dependent, maximum time is: 3 x (1) - $12A_{MAX}$ - $(4)_{MIN}$ +N x 2 x (1). N is the number of extra T_C states added to either the first or second bus operation of the processor extension data operand transfer sequence.

FIGURE 6. 80C286/883 PEREQ/PEACK TIMING FOR ONE TRANSFER ONLY

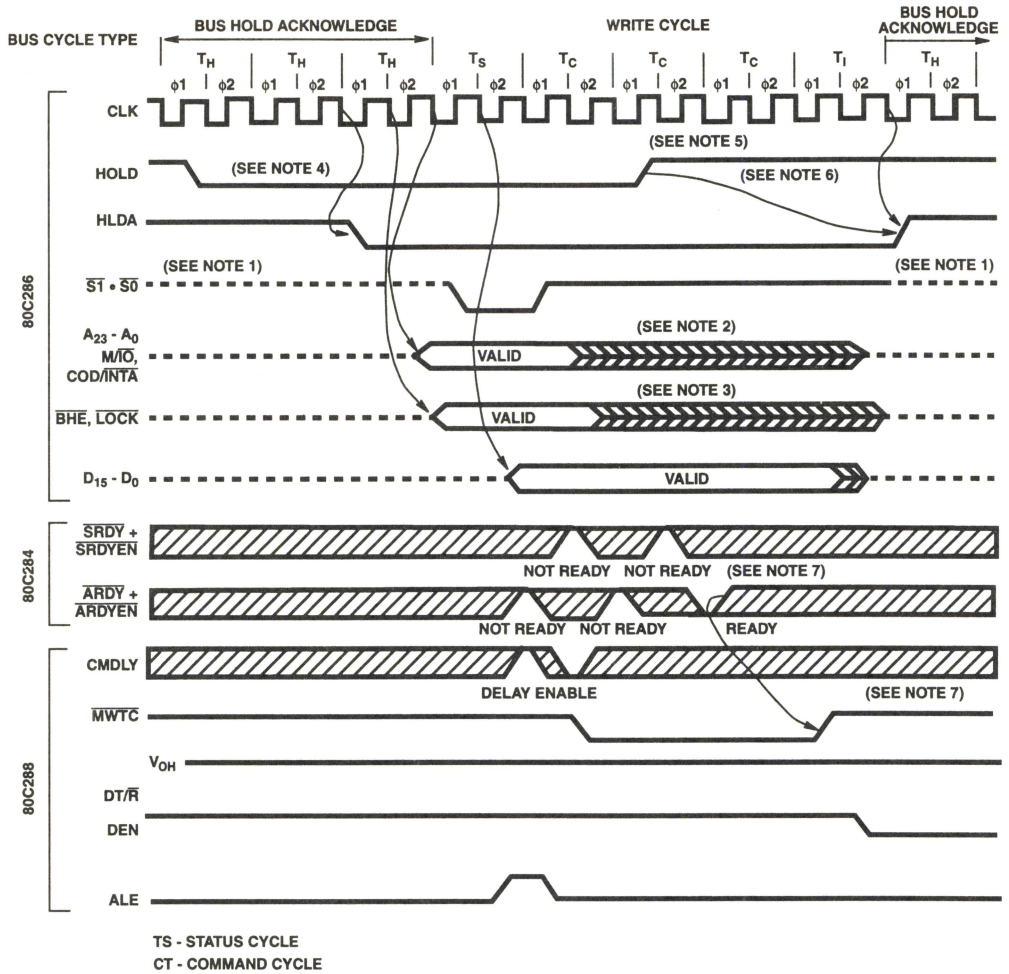


NOTES:

1. Setup time for RESET ↑ may be violated with the consideration that ϕ1 of the processor clock may begin one system CLK period later.
2. Setup and hold times for RESET ↓ must be met for proper operation, but RESET ↓ may occur during ϕ1 or ϕ2.
3. The data bus is only guaranteed to be in a high impedance state at the time shown.

FIGURE 7. INITIAL 80C286/883 PIN STATE DURING RESET

Waveforms (Continued)

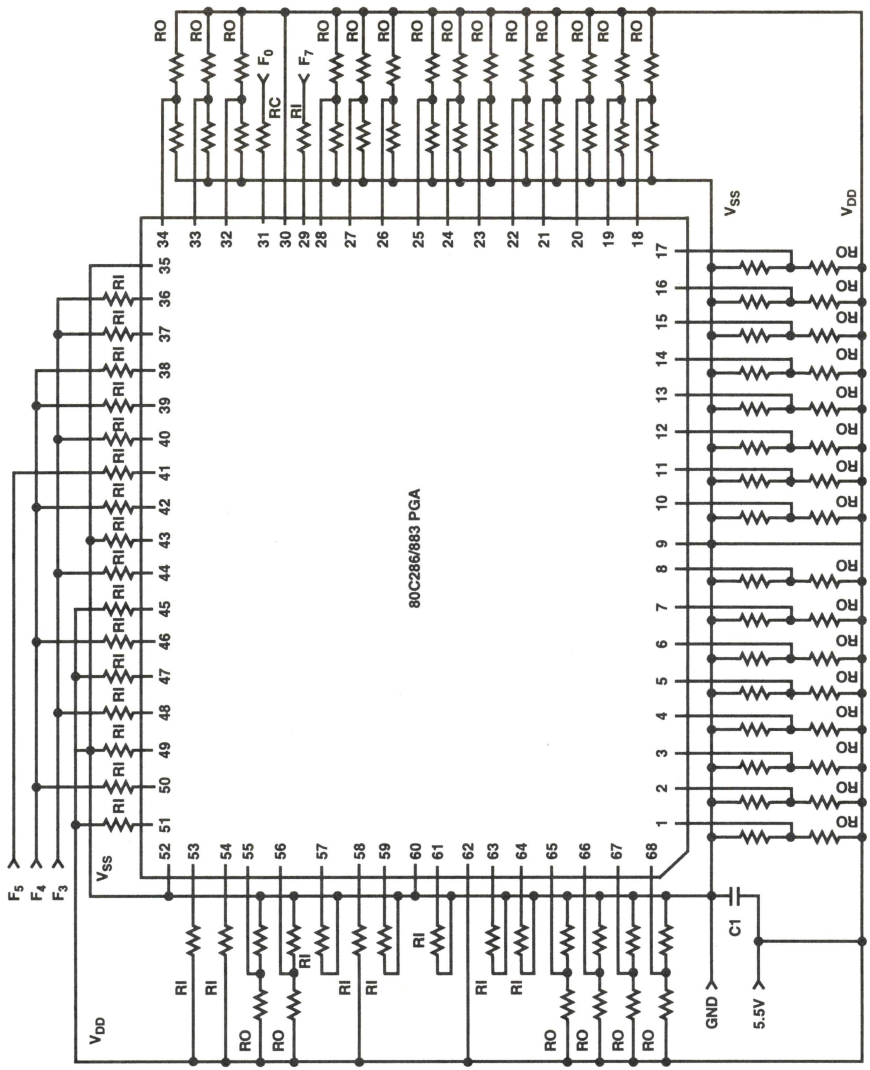


NOTES:

1. Status lines are held at a high impedance logic one by the 80C286 during a HOLD state.
2. Address, M/$\overline{IO}$ and COD/$\overline{INTA}$ may start floating during any T_C depending on when internal 80C286 bus arbiter decides to release bus to external HOLD. The float starts in $\phi 2$ of T_C.
3. $\overline{BHE}$ and $\overline{LOCK}$ may start floating after the end of any T_C depending on when internal 80C286 bus arbiter decides to release bus to external HOLD. The float starts in $\phi 1$ of T_C.
4. The minimum HOLD to HLDA time is shown. Maximum is one T_H longer.
5. The earliest HOLD time is shown. It will always allow a subsequent memory cycle if pending is shown.
6. The minimum HOLD to HLDA time is shown. Maximum is a function of the instruction, type of bus cycle and other machine state (i.e., Interrupts, Waits, Lock, etc.).
7. Asynchronous ready allows termination of the cycle. Synchronous ready does not signal ready in this example. Synchronous ready state is ignored after ready is signaled via the asynchronous input.

FIGURE 8. MULTIBUS WRITE TERMINATED BY ASYNCHRONOUS READY WITH BUS HOLD

Burn-In Circuit



NOTES:

8. Supply Voltage: V_{DD} = 5.5V, V_{SS} = 0.0V.
9. Input Voltage Limits: V_{IL} (Maximum) = 0.8V, V_{IH} (Minimum) = 2.0V
10. Component Values: RC = 1kΩ ±5%, RI = 10kΩ ±5%, RO = Two Series 2.7kΩ ±5%
11. Capacitor Values: C1 = 0.1 Microfarads
12. Oven Type and Frequency Requirements: Wakefield Oven Board f_0 = 100kHz, f_3 = 12.5kHz, f_4 = 6.25kHz, f_5 = 3.125kHz, f_7 = 781.25Hz.
13. Special Requirements: (a) ELECTROSTATIC DISCHARGE SENSITIVE. Proper Precautions Must be Used When Handling Units. (b) All Power Supplies Must be at Zero Volts When the Boards are Inserted into the Ovens. (c) When Powering Up, the Inputs Must be Held Below the V_{DD} Voltage. (d) If an Excessive Current is Indicated at Final Inspection, Check to See if a Part is Inserted Backwards or is Latched Up.

Die Characteristics

DIE DIMENSIONS:
286 x 283 x 19 ±1mils

METALLIZATION:
Type: Si-Al
Thickness: 8kÅ

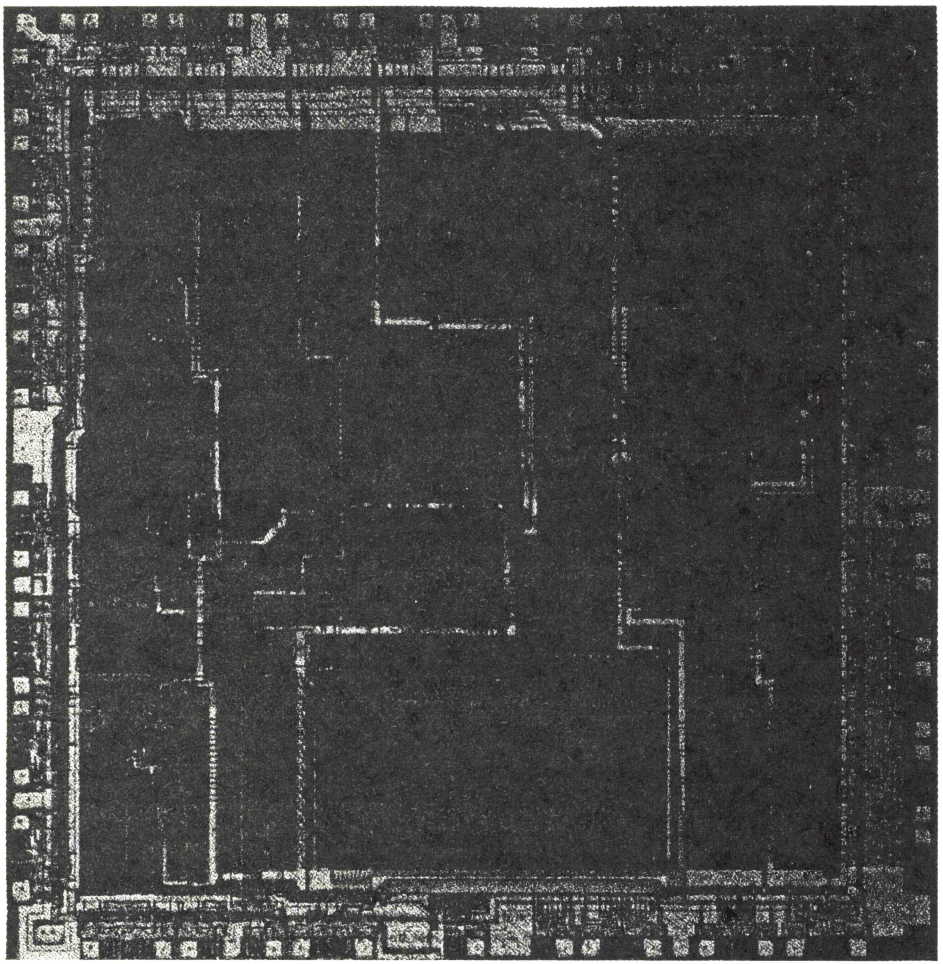
GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY: 2 X 10^5A/cm^2

LEAD TEMPERATURE: (10s Soldering): ≤ 300°C

Metallization Mask Layout

80C286/883



March 1997

CMOS 16-Bit Microprocessor

Features

- Compatible with NMOS 8086
- Completely Static CMOS Design
  - DC 5MHz (80C86)
  - DC 8MHz (80C86-2)
- Low Power Operation
  - ICCSB ..... 500μA Max
  - ICCOP ..... 10mA/MHz Typ
- 1MByte of Direct Memory Addressing Capability
- 24 Operand Addressing Modes
- Bit, Byte, Word and Block Move Operations
- 8-Bit and 16-Bit Signed/Unsigned Arithmetic
  - Binary, or Decimal
  - Multiply and Divide
- Wide Operating Temperature Range
  - C80C86 ..... $0^{o}C$ to $+70^{o}C$
  - I80C86 ..... $-40^{o}C$ to $+85^{o}C$
  - M80C86 ..... $-55^{o}C$ to $+125^{o}C$

Description

The Harris 80C86 high performance 16-bit CMOS CPU is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). Two modes of operation, minimum for small systems and maximum for larger applications such as multiprocessing, allow user configuration to achieve the highest performance level. Full TTL compatibility (with the exception of CLOCK) and industry standard operation allow use of existing NMOS 8086 hardware and software designs.

Ordering Information

PACKAGE	TEMP. RANGE	5MHz	8MHz	PKG. NO.
PDIP	$0^{o}C$ to $+70^{o}C$	CP80C86	CP80C86-2	E40.6
	$-40^{o}C$ to $+85^{o}C$	IP80C86	IP80C86-2	E40.6
PLCC	$0^{o}C$ to $+70^{o}C$	CS80C86	CS80C86-2	N44.65
	$-40^{o}C$ to $+85^{o}C$	IS80C86	IS80C86-2	N44.65
CERDIP	$0^{o}C$ to $+70^{o}C$	CD80C86	CD80C86-2	F40.6
	$-40^{o}C$ to $+85^{o}C$	ID80C86	ID80C86-2	F40.6
	$-55^{o}C$ to $+125^{o}C$	MD80C86/B	MD80C86-2/B	F40.6
SMD#	$-55^{o}C$ to $+125^{o}C$	8405201QA	8405202QA	F40.6
CLCC	$-55^{o}C$ to $+125^{o}C$	MR80C86/B	MR80C86-2/B	J44.A
SMD#	$-55^{o}C$ to $+125^{o}C$	8405201XA	8405202XA	J44.A

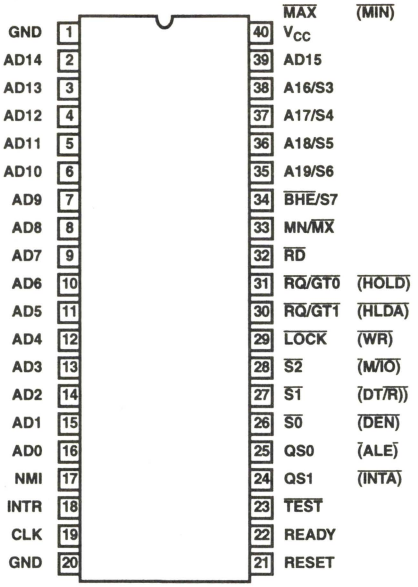
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Copyright © Harris Corporation 1997

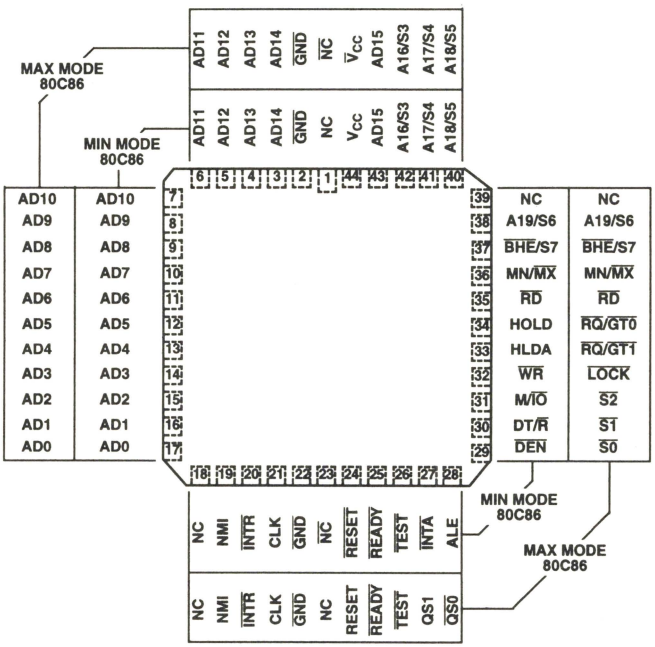
File Number 2957.1

Pinouts

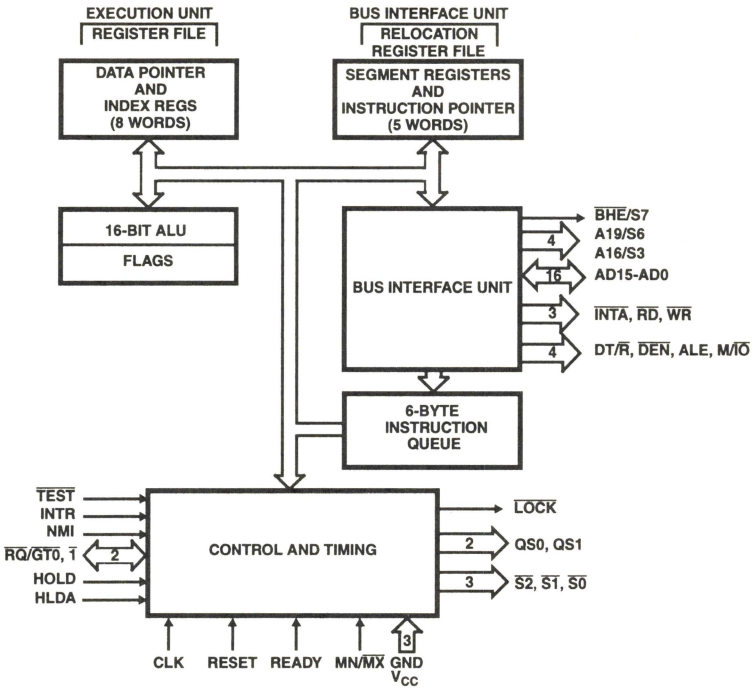
80C86 (DIP)
TOP VIEW

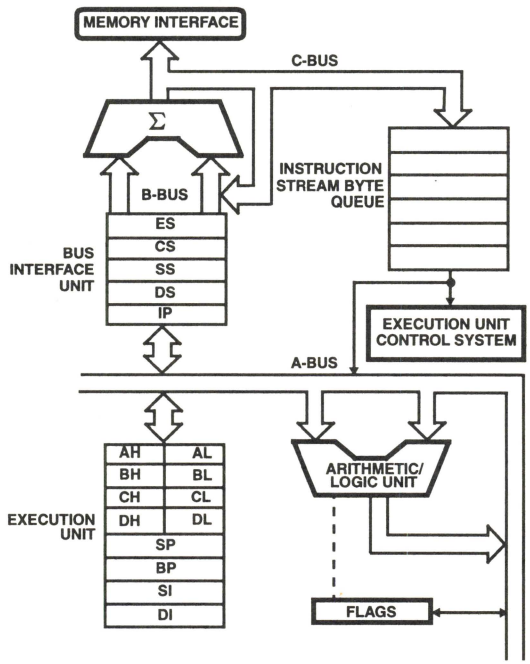


80C86 (PLCC, CLCC)
TOP VIEW



Functional Diagram





Pin Description

The following pin function descriptions are for 80C86 systems in either minimum or maximum mode. The "Local Bus" in these description is the direct multiplexed bus interface connection to the 80C86 (without regard to additional bus buffers).

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
AD15-AD0	2-16, 39	I/O	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address (T1) and data (T2, T3, TW, T4) bus. A0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D7-D0. It is LOW during Ti when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A0 to condition chip select functions (See $\overline{BHE}$). These lines are active HIGH and are held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence".
A19/S6 A18/S5 A17/S4 A16/S3	35-38	O	ADDRESS/STATUS: During T1, these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, TW, T4. S6 is always LOW. The status of the interrupt enable FLAG bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown. This information indicates which segment register is presently being used for data accessing. These lines are held at high impedance to the last valid logic level during local bus "hold acknowledge" or "grant sequence".
$\overline{BHE}$/S7	34	O	BUS HIGH ENABLE/STATUS: During T1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D15-D8. Eight bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S7 status information is available during T2, T3 and T4. The signal is active LOW, and is held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence", it is LOW during T1 for the first interrupt acknowledge cycle.
$\overline{RD}$	32	O	READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the M/$\overline{IO}$ or $\overline{S2}$ pin. This signal is used to read devices which reside on the 80C86 local bus. $\overline{RD}$ is active LOW during T2, T3 and TW of any read cycle, and is guaranteed to remain HIGH in T2 until the 80C86 local bus has floated. This line is held at a high impedance logic one state during "hold acknowledge" or "grand sequence".
READY	22	I	READY: is the acknowledgment from the addressed memory or I/O device that will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 82C84A Clock Generator to form READY. This signal is active HIGH. The 80C86 READY input is not synchronized. Correct operation is not guaranteed if the Setup and Hold Times are not met.

S4	S3	CHARACTERISTICS
0	0	Alternate Data
0	1	Stack
1	0	Code or None
1	1	Data

BHE	A0	CHARACTERISTICS
0	0	Whole Word
0	1	Upper Byte From/to Odd Address
1	0	Lower Byte From/to Even address
1	1	None

Pin Description (Continued)

The following pin function descriptions are for 80C86 systems in either minimum or maximum mode. The "Local Bus" in these description is the direct multiplexed bus interface connection to the 80C86 (without regard to additional bus buffers).

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
INTR	18	I	INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
$\overline{TEST}$	23	I	TEST: input is examined by the "Wait" instruction. If the $\overline{TEST}$ input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NON-MASKABLE INTERRUPT: is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	RESET: causes the processor to immediately terminate its present activity. The signal must transition LOW to HIGH and remain active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
VCC	40		VCC: +5V power supply pin. A 0.1µF capacitor between pins 20 and 40 is recommended for decoupling.
GND	1, 20		GND: Ground. Note: both must be connected. A 0.1µF capacitor between pins 1 and 20 is recommended for decoupling.
MN/$\overline{MX}$	33	I	MINIMUM/MAXIMUM: Indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

Minimum Mode System

The following pin function descriptions are for the 80C86 in minimum mode (i.e., MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described below.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
M/$\overline{IO}$	28	O	STATUS LINE: logically equivalent to $\overline{S2}$ in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{IO}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (M = HIGH, I/O = LOW). M/$\overline{IO}$ is held to a high impedance logic one during local bus "hold acknowledge".
$\overline{WR}$	29	O	WRITE: indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{IO}$ signal. $\overline{WR}$ is active for T2, T3 and TW of any write cycle. It is active LOW, and is held to high impedance logic one during local bus "hold acknowledge".
$\overline{INTA}$	24	O	INTERRUPT ACKNOWLEDGE: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3 and TW of each interrupt acknowledge cycle. Note that $\overline{INTA}$ is never floated.
ALE	25	O	ADDRESS LATCH ENABLE: is provided by the processor to latch the address into the 82C82/82C83 address latch. It is a HIGH pulse active during clock LOW of T1 of any bus cycle. Note that ALE is never floated.

Minimum Mode System (Continued)

The following pin function descriptions are for the 80C86 in minimum mode (i.e., MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described below.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
DT/$\overline{R}$	27	O	DATA TRANSMIT/RECEIVE: is needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in maximum mode, and its timing is the same as for M/$\overline{IO}$ (T = HIGH, R = LOW). DT/$\overline{R}$ is held to a high impedance logic one during local bus "hold acknowledge".
$\overline{DEN}$	26	O	DATA ENABLE: provided as an output enable for a bus transceiver in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle it is active from the middle of T2 until the middle of T4, while for a write cycle it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ is held to a high impedance logic one during local bus "hold acknowledge".
HOLD HLDA	31, 30	I O	HOLD: indicates that another master is requesting a local bus "hold". To be an acknowledged, HOLD must be active HIGH. The processor receiving the "hold" will issue a "hold acknowledge" (HLDA) in the middle of a T4 or TI clock cycle. Simultaneously with the issuance of HLDA, the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will lower HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

Maximum Mode System

The following pin function descriptions are for the 80C86 system in maximum mode (i.e., MN/$\overline{MX}$ - GND). Only the pin functions which are unique to maximum mode are described below.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{S0}$ $\overline{S1}$ $\overline{S2}$	26 27 28	O O O	STATUS: is active during T4, T1 and T2 and is returned to the passive state (1, 1, 1) during T3 or during TW when READY is HIGH. This status is used by the 82C88 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$ or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or TW is used to indicate the end of a bus cycle. These signals are held at a high impedance logic one state during "grant sequence".

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTICS
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

Maximum Mode System (Continued)

The following pin function descriptions are for the 80C86 system in maximum mode (i.e., MN/$\overline{MX}$ - GND). Only the pin functions which are unique to maximum mode are described below.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{RQ}/\overline{GT0}$ $\overline{RQ}/\overline{GT1}$	31, 30	I/O	REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT0}$ having higher priority than $\overline{RQ}/\overline{GT1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up bus hold device so it may be left unconnected. The request/grant sequence is as follows (see $\overline{RQ}/\overline{GT}$ Sequence Timing) 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the 80C86 (pulse 1). 2. During a T4 or TI clock cycle, a pulse 1 CLK wide from the 80C86 to the requesting master (pulse 2) indicates that the 80C86 has allowed the local bus to float and that it will enter the "grant sequence" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "grant sequence". 3. A pulse 1 CLK wide from the requesting master indicates to the 80C86 (pulse 3) that the "hold" request is about to end and that the 80C86 can reclaim the local bus at the next CLK. The CPU then enters T4 (or TI if no bus cycles pending). Each Master-Master exchange of the local bus is a sequence of 3 pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active low. If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met: 1. Request occurs on or before T2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next cycle. 2. A memory cycle will start within three clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
$\overline{LOCK}$	29	O	LOCK: output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a high impedance logic one state during "grant sequence". In MAX mode, $\overline{LOCK}$ is automatically generated during T2 of the first $\overline{INTA}$ cycle and removed during T2 of the second $\overline{INTA}$ cycle.
QS1, QSO	24, 25	O	QUEUE STATUS: The queue status is valid during the CLK cycle after which the queue operation is performed. QS1 and QS0 provide status to allow external tracking of the internal 80C86 instruction queue. Note that QS1, QS0 never become high impedance.

QSI	QSO	
0	0	No Operation
0	1	First byte of op code from queue
1	0	Empty the queue
1	1	Subsequent byte from queue

Functional Description

Static Operation

All 80C86 circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The CMOS 80C86 can operate from DC to the specified upper frequency limit. The processor clock may be stopped in either state (HIGH/LOW) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The 80C86 can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since 80C86 power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, the 80C86 power requirement is the standby current, (500μA maximum).

Internal Architecture

The internal functions of the 80C86 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the CPU functional diagram.

These units can interact directly, but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces "dead-time" on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

Memory Organization

The processor provides a 20-bit address to memory, which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Figure 1).

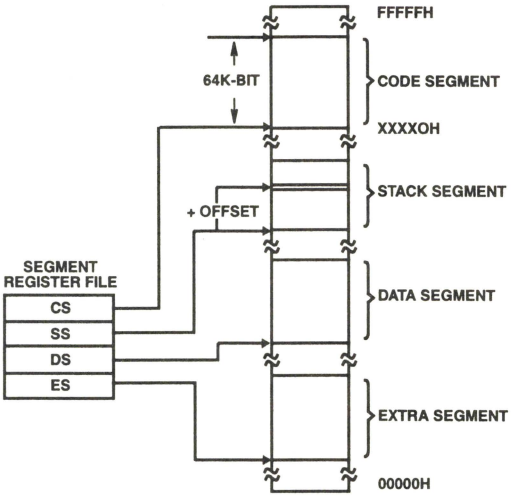


FIGURE 1. 80C86 MEMORY ORGANIZATION

TABLE 1.

TYPE OF MEMORY REFERENCE	DEFAULT SEGMENT BASE	ALTERNATE SEGMENT BASE	OFFSET
Instruction Fetch	CS	None	IP
Stack Operation	SS	None	SP
Variable (except following)	DS	CS, ES, SS	Effective Address
String Source	DS	CS, ES, SS	SI
String Destination	ES	None	DI
BP Used As Base Register	SS	CS, DS, ES	Effective Address

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the specific rules of Table 1. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into re-locatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster and more structured. (See Table 1).

Word (16-bit) operands can be located on even or odd address boundaries and are thus, not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory

accesses; one, if the word operand is on an even byte boundary and two, if it is on an odd byte boundary. Except for the performance penalty, this double access is transparent to the software. The performance penalty does not occur for instruction fetches; only word operands.

Physically, the memory is organized as a high bank (D15-D8) and a low bank (D7-D0) of 512K bytes addressed in parallel by the processor's address lines.

Byte data with even addresses is transferred on the D7-D0 bus lines, while odd addressed byte data (A0 HIGH) is transferred on the D15-D8 bus lines. The processor provides two enable signals, BHE and A_0, to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor at the byte level as necessary.

In referencing word data, the BIU requires one or two memory cycles depending on whether the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing word operands performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.

Certain locations in memory are reserved for specific CPU operations (See Figure 2). Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt service routines is accessed thru its own pair of 16-bit pointers (segment address pointer and offset address pointer). The first pointer, used as the offset address, is loaded into the IP and the second pointer, which designates the base address is loaded into the CS. At this point program control is transferred to the interrupt routine. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

Minimum and Maximum Operation Modes

The requirements for supporting minimum and maximum 80C86 systems are sufficiently different that they cannot be met efficiently using 40 uniquely defined pins. Consequently, the 80C86 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the 80C86 defines pins 24 through 31 and 34 in maximum mode. When the MN/$\overline{MX}$ pin is strapped to V_{CC}, the 80C86 generates bus control signals itself on pins 24 through 31 and 34.

The minimum mode 80C86 can be used with either a multiplexed or demultiplexed bus. This architecture provides the 80C86 processing power in a highly integrated form.

The demultiplexed mode requires two 82C82 latches (for 64K addressability) or three 82C82 latches (for a full megabyte of addressing). An 82C86 or 82C87 transceiver can also be used if data bus buffering is required. (See Figure 6A.) The 80C86 provides $\overline{DEN}$ and DT/$\overline{R}$ to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

The maximum mode employs the 82C88 bus controller (See Figure 6B). The 82C88 decodes status lines $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$, and provides the system with all bus control signals.

Moving the bus control to the 82C88 provides better source and sink current capability to the control lines, and frees the 80C86 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the 80C86 in maximum mode. These features allow coprocessors in local bus and remote bus configurations.

Bus Operation

The 80C86 has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40 lead package. This "local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of 82C82 address latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3 and T4 (see Figure 3). The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (TW) are inserted between T3 and T4. Each inserted wait state is the same duration as a CLK cycle. Periods can occur between 80C86 driven bus cycles. These are referred to as idle" states (T_I) or inactive CLK cycles. The processor uses these cycles for internal housekeeping and processing.

During T1 of any bus cycle, the ALE (Address Latch Enable) signal is emitted (by either the processor or the 82C88 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to Table 2.

TABLE 2.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTICS
0	0	0	Interrupt
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (No Bus Cycle)

Status bits S3 through S7 are time multiplexed with high order address bits and the $\overline{BHE}$ signal, and are therefore valid during T2 through T4. S3 and S4 indicate which segment register (see Instruction Set Description) was used for this bus cycle in forming the address, according to Table 3.

S5 is a reflection of the PSW interrupt enable bit. S3 is always zero and S7 is a spare status bit.

TABLE 3.

S4	S3	CHARACTERISTICS
0	0	Alternate Data (Extra Segment)
0	1	Stack
1	0	Code or None
1	1	Data

I/O Addressing

In the 80C86, I/O operations can address up to a maximum of 64K I/O byte registers or 32K I/O word registers. The I/O address appears in the same format as the memory address on bus lines A15-A0. The address lines A19-A16 are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the D7-D0 bus lines and odd addressed bytes on D15-D8. Care must be taken to ensure that each register within an 8-bit peripheral located on the lower portion of the bus be addressed as even.

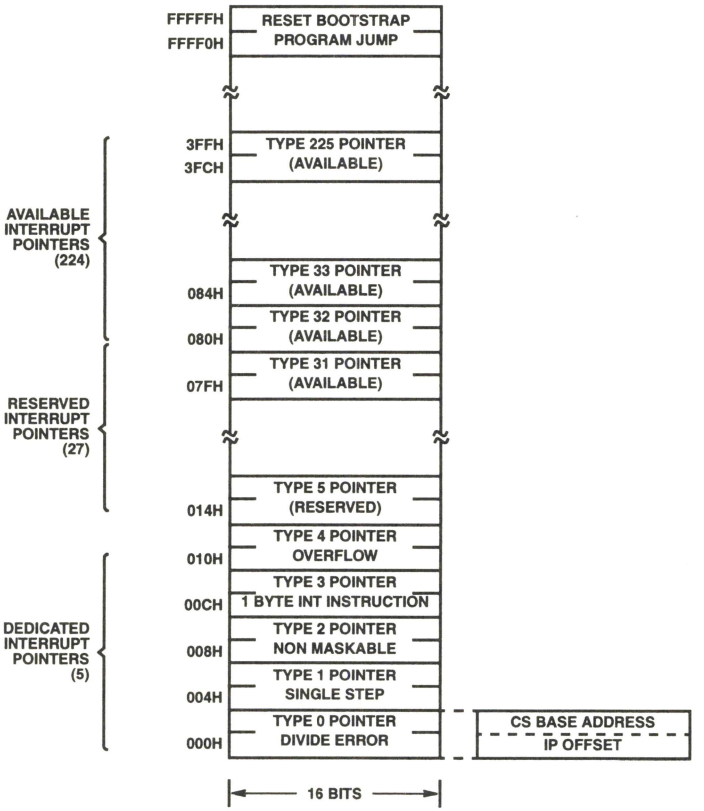


FIGURE 2. RESERVED MEMORY LOCATIONS

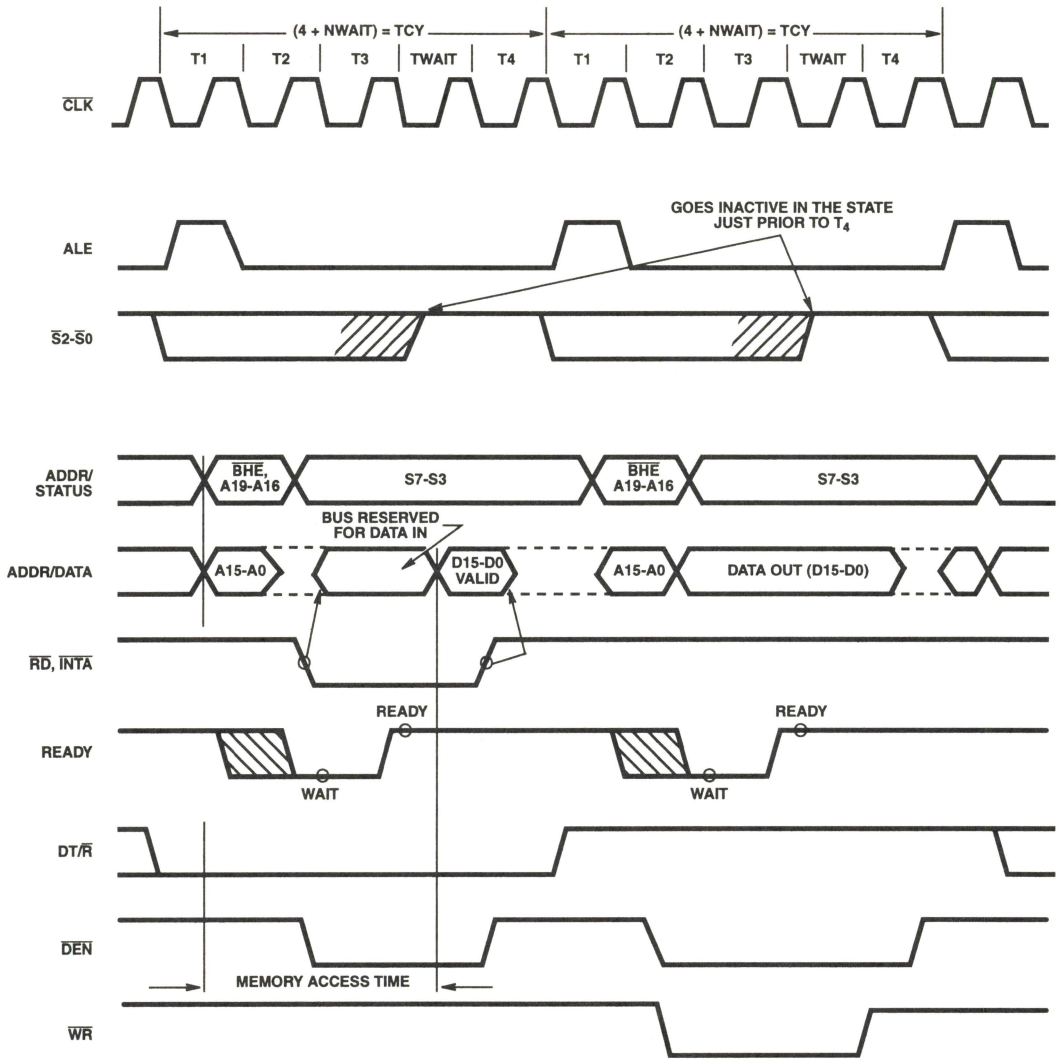


FIGURE 3. BASIC SYSTEM TIMING

External Interface

Processor RESET and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 80C86 RESET is required to be HIGH for greater than 4 CLK cycles. The 80C86 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 clock cycles. After this interval, the 80C86 operates normally beginning with the instruction in absolute location FFFF0H. (See Figure 2). The RESET input is internally synchronized to the processor clock. At initialization, the HIGH-to-LOW transition of RESET must occur no sooner than 50μs (or 4 CLK cycles, whichever is greater) after power-up, to allow complete initialization of the 80C86.

NMI will not be recognized prior to the second CLK cycle following the end of RESET. If NMI is asserted sooner than nine clock cycles after the end of RESET, the processor may execute one instruction before responding to the interrupt.

Bus Hold Circuitry

To avoid high current conditions caused by floating inputs to CMOS devices and to eliminate need for pull-up/down resistors, "bus-hold" circuitry has been used on the 80C86 pins 2-16, 26-32 and 34-39. (See Figure 4A and Figure 4B). These circuits will maintain the last valid logic state if no driving source is present (i.e., an unconnected pin or a driving source which goes to a high impedance state). To overdrive the "bus hold" circuits, an external driver must be capable of supplying approximately 400μA minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

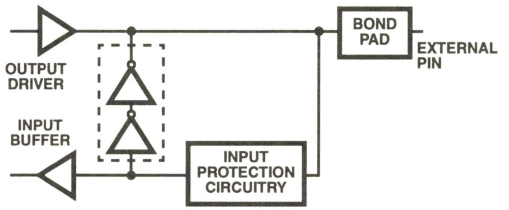


FIGURE 4A. BUS HOLD CIRCUITRY PIN 2-16, 34-39

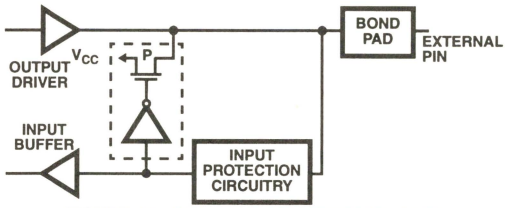


FIGURE 4B. BUS HOLD CIRCUITRY PIN 26-32

Interrupt Operations

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the Instruction Set Description. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256-element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH, which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8-bit type number during the interrupt acknowledge sequence, which is used to "vector" through the appropriate element to the new interrupt service program location. All flags and both the Code Segment and Instruction Pointer register are saved as part of the $\overline{\text{INTA}}$ sequence. These are restored upon execution of an Interrupt Return (IRET) instruction.

Non-Maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any positive transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during or after the servicing of NMI. Another positive edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

Maskable Interrupt (INTR)

The 80C86 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable flag (IF) status bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block type instruction. INTR may be removed anytime after the falling edge of the first $\overline{\text{INTA}}$ signal. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored, the enable bit will be zero unless specifically set by an instruction.

During the response sequence (Figure 5) the processor executes two successive (back-to-back) interrupt acknowledge cycles. The 80C86 emits the $\overline{LOCK}$ signal (Max mode only) from T2 of the first bus cycle until T2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is supplied to the 80C86 by the 82C59A Interrupt Controller, which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when it restores the FLAGS.

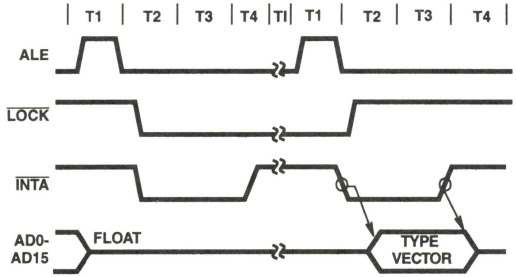


FIGURE 5. INTERRUPT ACKNOWLEDGE SEQUENCE

Halt

When a software "HALT" instruction is executed the processor indicates that it is entering the "HALT" state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In maximum mode the processor issues appropriate HALT status on $\overline{S2}$, $\overline{S1}$, $\overline{S0}$ and the 82C88 bus controller issues one ALE. The 80C86 will not leave the "HALT" state when a local bus "hold" is entered while in "HALT". In this case, the processor reissues the HALT indicator at the end of the local bus hold. An NMI or interrupt request (when interrupts enabled) or RESET will force the 80C86 out of the "HALT" state.

Read/Modify/Write (Semaphore)

Operations Via $\overline{Lock}$

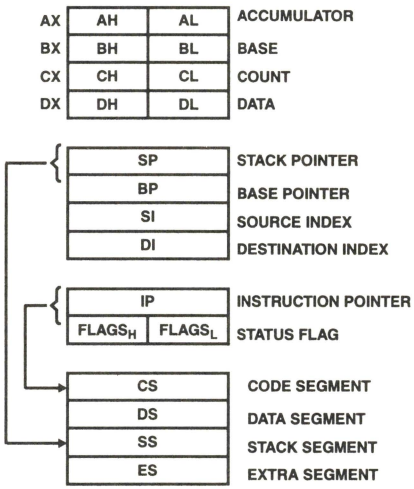
The LOCK status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This gives the processor the capability of performing read/modify/write operations on memory (via the Exchange Register With Memory instruction, for example) without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The LOCK signal is activated (forced LOW) in the clock cycle following decoding of the software "LOCK" prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the "LOCK" prefix instruction. While LOCK is active a request on a RQ/GT pin will be recorded and then honored at the end of the LOCK.

External Synchronization Via TEST

As an alternative to interrupts, the 80C86 provides a single software-testable input pin ($\overline{TEST}$). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the $\overline{TEST}$ input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the 80C86 three-states all output drivers while inputs and I/O pins are held at valid logic levels by internal bus-hold circuits. If interrupts are enabled, the 80C86 will recognize interrupts and process them when it regains control of the bus. The WAIT instruction is then refetched, and re-executed.

TABLE 4. 80C86 REGISTER



Basic System Timing

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 6A and 6B, respectively. In minimum mode, the MN/$\overline{MX}$ pin is strapped to VCC and the processor emits bus control signals (e.g. $\overline{RD}$, $\overline{WR}$, etc.) directly. In maximum mode, the MN/$\overline{MX}$ pin is strapped to GND and the processor emits coded status information which the 82C88 bus controller uses to generate MULTIBUS compatible bus control signals. Figure 3 shows the signal timing relationships.

System Timing - Minimum System

The read cycle begins in T1 with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the address/data bus (AD0-AD15) at this time, into the 82C82/82C83 latch. The $\overline{BHE}$ and A0 signals address the low, high or both bytes. From T1 to T4 the M/$\overline{IO}$ signal indicates a memory or I/O operation. At T2, the address is removed from the address/data bus and the bus is held at the last valid logic state by internal bus hold

devices. The read control signal is also asserted at T2. The read ($\overline{RD}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again three-state its bus drivers. If a transceiver (82C86/82C87) is required to buffer the 80C86 local bus, signals DT/R and $\overline{DEN}$ are provided by the 80C86.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/$\overline{IO}$ signal is again asserted to indicate a memory or I/O write operation. In T2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of T4. During T2, T3 and TW, the processor asserts the write control signal. The write ($\overline{WR}$) signal becomes active at the beginning of T2 as opposed to the read which is delayed somewhat into T2 to provide time for output drivers to become inactive.

The $\overline{BHE}$ and A0 signals are used to select the proper byte(s) of the memory/IO word to be read or written according to Table 5.

TABLE 5.

$\overline{BHE}$	A0	CHARACTERISTICS
0	0	Whole word
0	1	Upper Byte From/To Odd Address
1	0	Lower Byte From/To Even Address
1	1	None

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the D7-D0 bus lines and odd address bytes on D15-D8.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal ($\overline{INTA}$) is asserted in place of the read ($\overline{RD}$) signal and the address bus is held at the last valid logic state by internal bus hold devices. (See Figure 4). In the second of two successive $\overline{INTA}$ cycles a byte of information is read from the data bus (D7-D0) as supplied by the interrupt system logic (i.e., 82C59A Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into an interrupt vector lookup table, as described earlier.

Bus Timing - Medium Size Systems

For medium complexity systems the MN/$\overline{MX}$ pin is connected to GND and the 82C88 Bus Controller is added to the system as well as an 82C82/82C83 latch for latching the system address, and an 82C86/82C87 transceiver to allow for bus loading greater than the 80C86 is capable of handling. Signals ALE, $\overline{DEN}$, and DT/$\overline{R}$ are generated by the 82C88 instead of the processor in this configuration, although their timing remains relatively the same. The 80C86 status outputs ($\overline{S2}$, $\overline{S1}$ and $\overline{S0}$) provide type-of-cycle information and become 82C88 inputs. This bus cycle information specifies read (code, data or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 82C88 issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 82C88 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The 82C86/82C87 transceiver receives the usual T and $\overline{OE}$ inputs from the 82C88 DT/$\overline{R}$ and DEN signals.

The pointer into the interrupt vector table, which is passed during the second $\overline{INTA}$ cycle, can be derived from an 82C59A located on either the local bus or the system bus. If the master 82C59A Priority Interrupt Controller is positioned on the local bus, the 82C86/82C87 transceiver must be disabled when reading from the master 82C59A during the interrupt acknowledge sequence and software "poll".

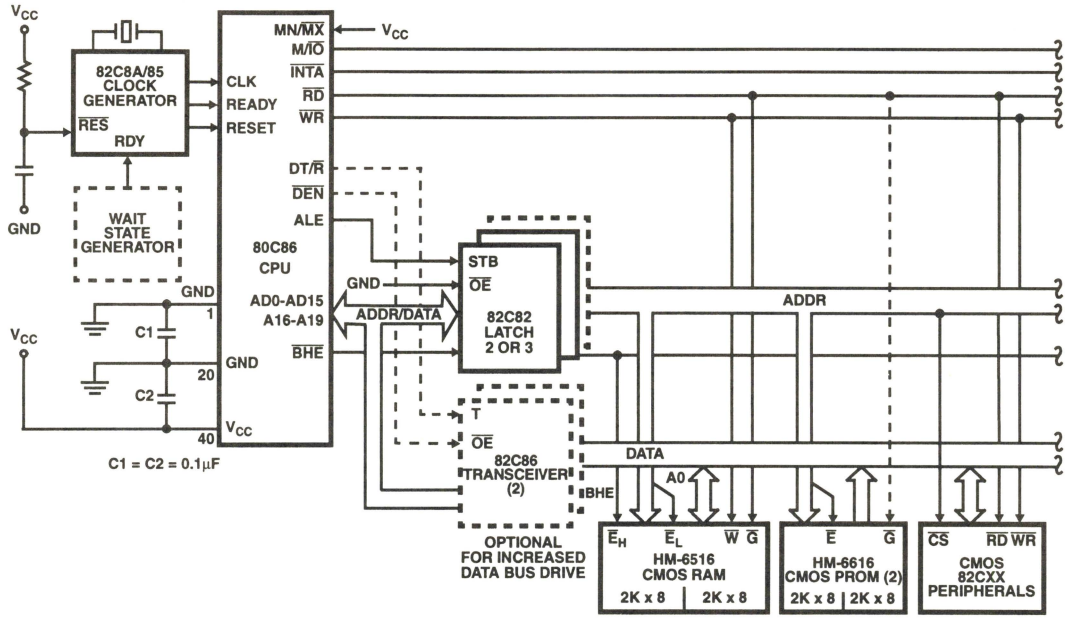


FIGURE 6A. MINIMUM MODE 80C86 TYPICAL CONFIGURATION

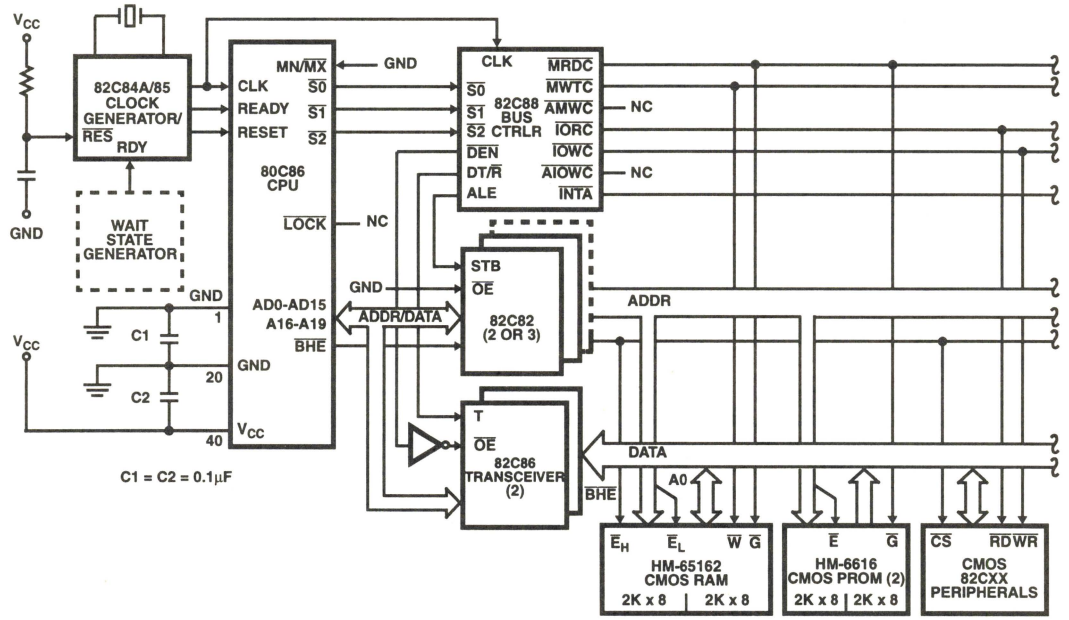


FIGURE 6B. MAXIMUM MODE 80C86 TYPICAL CONFIGURATION

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature
  Ceramic Packages . . . . . +175°C
  Plastic Packages . . . . . +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C
  (Lead tips only for surface mount packages)
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	50	N/A
PLCC Package	46	N/A
SBDIP Package	30	6
CLCC Package	40	6

Gate Count . . . . . 9750 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Operating Conditions

Operating Supply Voltage . . . . . +4.5V to +5.5V
  M80C86-2 ONLY . . . . . +4.75V to +5.25V

Operating Temperature Range: C80C86/-2 . . . . . 0°C to +70°C
  I80C86/-2 . . . . . -40°C to +85°C
  M80C86/-2 . . . . . -55°C to +125°C

DC Electrical Specifications

V_{CC} = 5.0V, ±10%; T_A = 0°C to +70°C (C80C86, C80C86-2)
V_{CC} = 5.0V, ±10%; T_A = -40°C to +85°C (I80C86, I80C86-2)
V_{CC} = 5.0V, ±10%; T_A = -55°C to +125°C (M80C86)
V_{CC} = 5.0V, ±5%; T_A = -55°C to +125°C (M80C86-2)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITION
V_{IH}	Logical One Input Voltage	2.0 2.2		V V	C80C86, I80C86 (Note 5) M80C86 (Note 5)
V_{IL}	Logical Zero Input Voltage		0.8	V	
V_{IHC}	CLK Logical One Input Voltage	V_{CC} -0.8		V	
V_{ILC}	CLK Logical Zero Input Voltage		0.8	V	
V_{OH}	Output High Voltage	3.0 V_{CC} -0.4		V V	I_{OH} = -2.5mA I_{OH} = -100µA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = +2.5mA
I_I	Input Leakage Current	-1.0	1.0	µA	V_{IN} = GND or V_{CC} DIP Pins 17-19, 21-23, 33
I_{BHH}	Input Current-Bus Hold High	-40	-400	µA	V_{IN} = - 3.0V (Note 1)
I_{BHL}	Input Current-Bus Hold Low	40	400	µA	V_{IN} = - 0.8V (Note 2)
I_O	Output Leakage Current	-	-10.0	µA	V_{OUT} = GND (Note 4)
I_{CCSB}	Standby Power Supply Current	-	500	µA	V_{CC} = - 5.5V (Note 3)
I_{CCOP}	Operating Power Supply Current	-	10	mA/MHz	FREQ = Max, V_{IN} = V_{CC} or GND, Outputs Open

Capacitance T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	25	pF	FREQ = 1MHz. All measurements are referenced to device GND
C_{OUT}	Output Capacitance	25	pF	FREQ = 1MHz. All measurements are referenced to device GND
$C_{I/O}$	I/O Capacitance	25	pF	FREQ = 1MHz. All measurements are referenced to device GND

NOTES:

2. IBHH should be measured after raising V_{IN} to V_{CC} and then lowering to 3.0V on the following pins 2-16, 26-32, 34-39.
3. IBHL should be measured after lowering V_{IN} to GND and then raising to 0.8V on the following pins: 2-16, 34-39.
4. ICCSB tested during clock high time after halt instruction executed. V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs unloaded.
5. IO should be measured by putting the pin in a high impedance state and then driving V_{OUT} to GND on the following pins: 26-29 and 32.
6. MN/$\overline{MX}$ is a strap option and should be held to V_{CC} or GND.

AC Electrical Specifications

V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C (C80C86, C80C86-2)
V_{CC} = 5.0V ±100%; T_A = -40°C to +85°C (I80C86, I80C86-2)
V_{CC} = 5.0V ±100%; T_A = -55°C to +125°C (M80C86)
V_{CC} = 5.0V ±5%; T_A = -55°C to +125°C (M80C86-2)

MINIMUM COMPLEXITY SYSTEM

SYMBOL		PARAMETER	80C86		80C86-2		UNITS	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS								
(1)	TCLCL	Cycle Period	200		125		ns	
(2)	TCLCH	CLK Low Time	118		68		ns	
(3)	TCHCL	CLK High Time	69		44		ns	
(4)	TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
(5)	TCL2C1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
(6)	TDVCL	Data In Setup Time	30		20		ns	
(7)	TCLDX1	Data In Hold Time	10		10		ns	
(8)	TR1VCL	RDY Setup Time into 82C84A (Notes 7, 8)	35		35		ns	
(9)	TCLR1X	RDY Hold Time into 82C84A (Notes 7, 8)	0		0		ns	
(10)	TRYHCH	READY Setup Time into 80C86	118		68		ns	
(11)	TCHRYX	READY Hold Time into 80C86	30		20		ns	
(12)	TRYLCL	READY Inactive to CLK (Note 9)	-8		-8		ns	
(13)	THVCH	HOLD Setup Time	35		20		ns	
(14)	TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (Note 8)	30		15		ns	
(15)	TILIH	Input Rise Time (Except CLK)		15		15	ns	From 0.8V to 2.0V
(16)	TIHIL	Input Fall Time (Except CLK)		15		15	ns	From 2.0V to 0.8V
TIMING RESPONSES								
(17)	TCLAV	Address Valid Delay	10	110	10	60	ns	C_L = 100pF
(18)	TCLAX	Address Hold Time	10		10		ns	C_L = 100pF
(19)	TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	C_L = 100pF
(20)	TCHSZ	Status Float Delay		80		50	ns	C_L = 100pF
(21)	TCHSV	Status Active Delay	10	110	10	60	ns	C_L = 100pF
(22)	TLHLL	ALE Width	TCLCH-20		TCLCH-10		ns	C_L = 100pF
(23)	TCLLH	ALE Active Delay		80		50	ns	C_L = 100pF
(24)	TCHLL	ALE Inactive Delay		85		55	ns	C_L = 100pF

AC Electrical Specifications

V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C (C80C86, C80C86-2)
V_{CC} = 5.0V ±100%; T_A = -40°C to +85°C (I80C86, I80C86-2)
V_{CC} = 5.0V ±100%; T_A = -55°C to +125°C (M80C86)
V_{CC} = 5.0V ±5%; T_A = -55°C to +125°C (M80C86-2) **(Continued)**

MINIMUM COMPLEXITY SYSTEM

SYMBOL		PARAMETER	80C86		80C86-2		UNITS	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
(25)	TLLAX	Address Hold Time to ALE Inactive	TCHCL-10		TCHCL-10		ns	C_L = 100pF
(26)	TCLDV	Data Valid Delay	10	110	10	60	ns	C_L = 100pF
(27)	TCLDX2	Data Hold Time	10		10		ns	C_L = 100pF
(28)	TWHDX	Data Hold Time After $\overline{WR}$	TCLCL-30		TCLCL-30		ns	C_L = 100pF
(29)	TCVCTV	Control Active Delay 1	10	110	10	70	ns	C_L = 100pF
(30)	TCHCTV	Control Active Delay 2	10	110	10	60	ns	C_L = 100pF
(31)	TCVCTX	Control Inactive Delay	10	110	10	70	ns	C_L = 100pF
(32)	TAZRL	Address Float to READ Active	0		0		ns	C_L = 100pF
(33)	TCLRL	$\overline{RD}$ Active Delay	10	165	10	100	ns	C_L = 100pF
(34)	TCLRH	$\overline{RD}$ Inactive Delay	10	150	10	80	ns	C_L = 100pF
(35)	TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL-45		TCLCL-40		ns	C_L = 100pF
(36)	TCLHAV	HLDA Valid Delay	10	160	10	100	ns	C_L = 100pF
(37)	TRLRH	$\overline{RD}$ Width	2TCLCL-75		2TCLCL-50		ns	C_L = 100pF
(38)	TWLWH	$\overline{WR}$ Width	2TCLCL-60		2TCLCL-40		ns	C_L = 100pF
(39)	TAVAL	Address Valid to ALE Low	TCLCH-60		TCLCH-40		ns	C_L = 100pF
(40)	TOLOH	Output Rise Time		20		15	ns	From 0.8V to 2.0V
(41)	TOHOL	Output Fall Time		20		15	ns	From 2.0V to 0.8V

NOTES:

7. Signal at 82C84A shown for reference only.
8. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
9. Applies only to T2 state (8ns into T3).

Waveforms

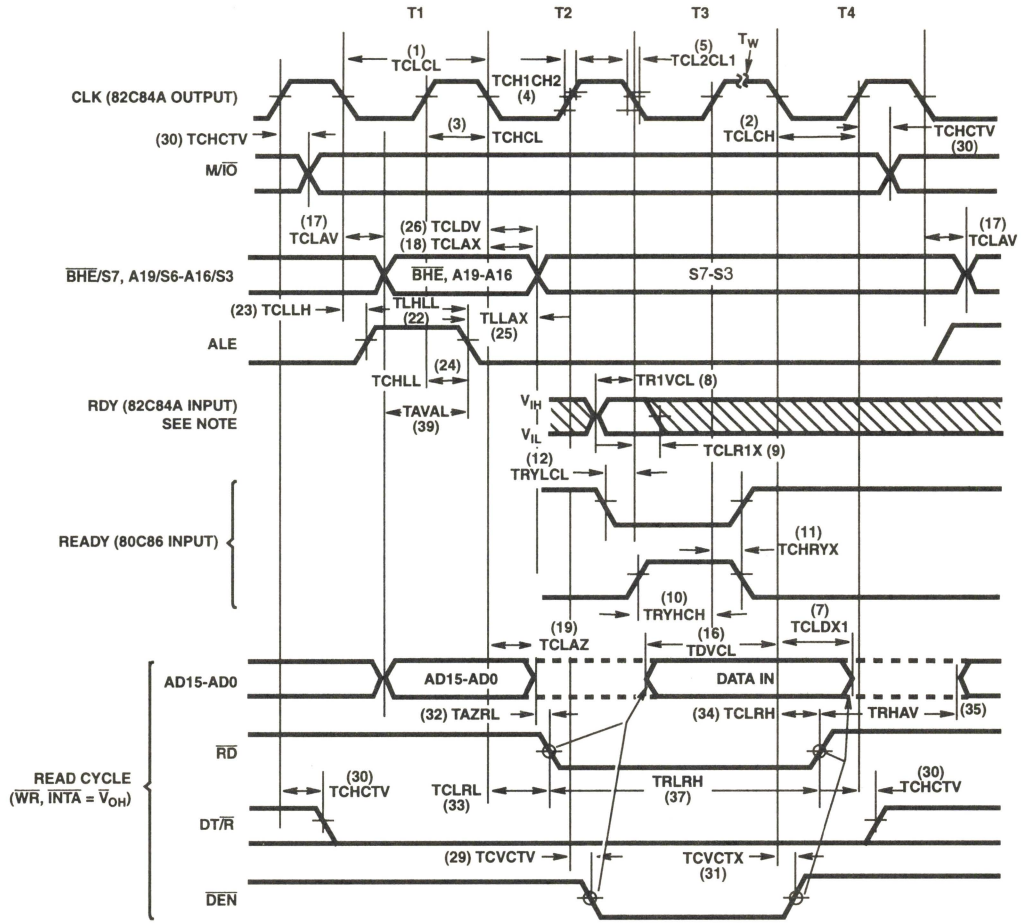


FIGURE 7A. BUS TIMING - MINIMUM MODE SYSTEM

NOTE: Signals at 82C84A are shown for reference only. RDY is sampled near the end of T2, T3, TW to determine if TW machine states are to be inserted.

Waveforms (Continued)

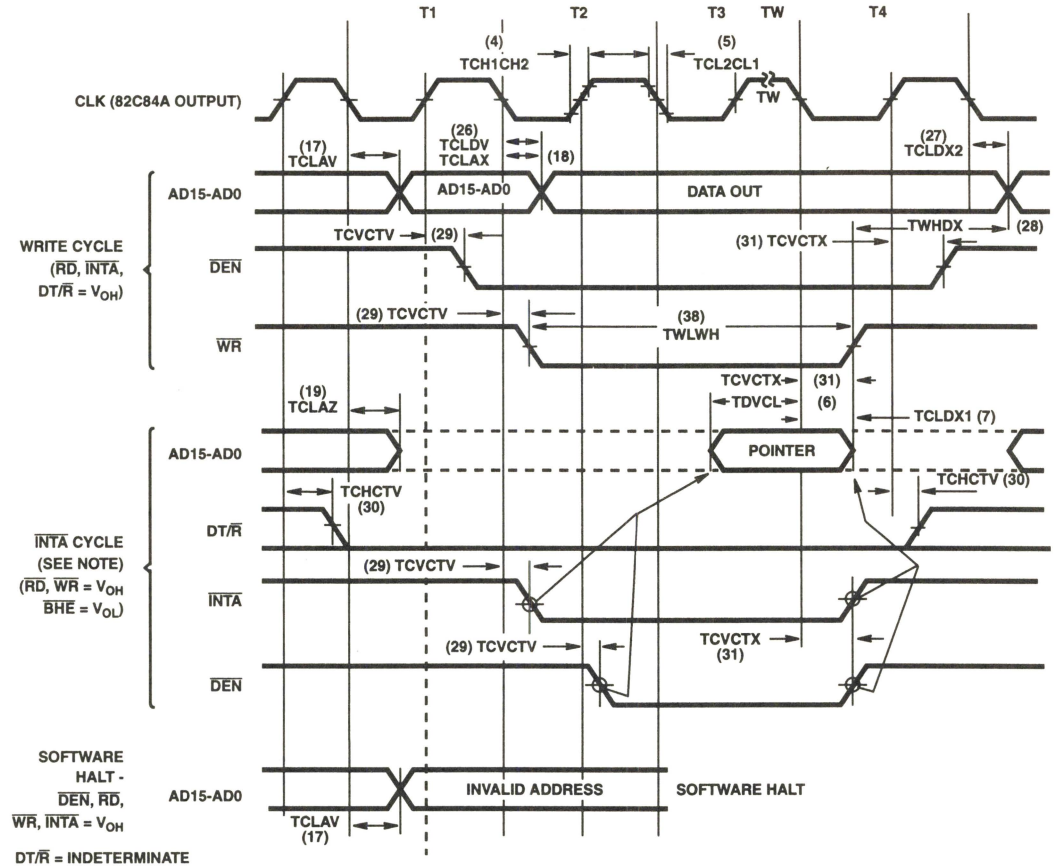


FIGURE 7B. BUS TIMING - MINIMUM MODE SYSTEM

NOTE: Two $\overline{\text{INTA}}$ cycles run back-to-back. The 80C86 local ADDR/DATA bus is floating during both $\overline{\text{INTA}}$ cycles. Control signals are shown for the second $\overline{\text{INTA}}$ cycle.

AC Electrical Specifications

V_{CC} = 5.0V ±10% T_A = 0°C to +70°C (C80C86, C80C86-2)
V_{CC} = 5.0V ±10%; T_A = -40°C to +85°C (I80C86, I80C86-2)
V_{CC} = 5.0V ±10%; T_A = -55°C to +125°C (M80C86)
V_{CC} = 5.0V ±5%; T_A = -55°C to +125°C (M80C86-2)

MAX MODE SYSTEM (USING 82C88 BUS CONTROLLER)

TIMING REQUIREMENTS			80C86		80C86-2			
SYMBOL		PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
(1)	TCLCL	CLK Cycle Period	200		125		ns	
(2)	TCLCH	CLK Low Time	118		68		ns	
(3)	TCHCL	CLK High Time	69		44		ns	
(4)	TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
(5)	TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
(6)	TDVCL	Data in Setup Time	30		20		ns	
(7)	TCLDX1	Data In Hold Time	10		10		ns	
(8)	TR1VCL	RDY Setup Time into 82C84A (Notes 10, 11)	35		35		ns	
(9)	TCLR1X	RDY Hold Time into 82C84A (Notes 10, 11)	0		0		ns	
(10)	TRYHCH	READY Setup Time into 80C86	118		68		ns	
(11)	TCHRYX	READY Hold Time into 80C86	30		20		ns	
(12)	TRYLCL	READY Inactive to CLK (Note 12)	-8		-8		ns	
(13)	TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{TEST}$) (Note 11)	30		15		ns	
(14)	TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time	30		15		ns	
(15)	TCHGX	$\overline{RQ}$ Hold Time into 80C86 (Note 13)	40	TCHCL+ 10	30	TCHCL+ 10	ns	
(16)	TILIH	Input Rise Time (Except CLK)		15		15	ns	From 0.8V to 2.0V
(17)	TIHIL	Input Fall Time (Except CLK)		15		15	ns	From 2.0V to 0.8V
TIMING RESPONSES								
(18)	TCLML	Command Active Delay (Note 10)	5	35	5	35	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(19)	TCLMH	Command Inactive (Note 10)	5	35	5	35	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(20)	TRYHSH	READY Active to Status Passive (Notes 12, 14)		110		65	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(21)	TCHSV	Status Active Delay	10	110	10	60	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(22)	TCLSH	Status Inactive Delay (Note 14)	10	130	10	70	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)

AC Electrical Specifications

V_{CC} = 5.0V ±10% T_A = 0°C to +70°C (C80C86, C80C86-2)
V_{CC} = 5.0V ±10%; T_A = -40°C to +85°C (I80C86, I80C86-2)
V_{CC} = 5.0V ±10%; T_A = -55°C to +125°C (M80C86)
V_{CC} = 5.0V ±5%; T_A = -55°C to +125°C (M80C86-2) **(Continued)**

MAX MODE SYSTEM (USING 82C88 BUS CONTROLLER)

TIMING REQUIREMENTS			80C86		80C86-2			
SYMBOL		PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
(23)	TCLAV	Address Valid Delay	10	110	10	60	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(24)	TCLAX	Address Hold Time	10		10		ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(25)	TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(26)	TCHSZ	Status Float Delay		80		50	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(27)	TSVLH	Status Valid to ALE High (Note 10)		20		20	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(28)	TSVMCH	Status Valid to MCE High (Note 10)		30		30	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(29)	TCLLH	CLK low to ALE Valid (Note 10)		20		20	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(30)	TCLMCH	CLK low to MCE High (Note 10)		25		25	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(31)	TCHLL	ALE Inactive Delay (Note 10)	4	18	4	18	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(32)	TCLMCL	MCE Inactive Delay (Note 10)		15		15	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(33)	TCLDV	Data Valid Delay	10	110	10	60	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(34)	TCLDX2	Data Hold Time	10		10		ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)

AC Electrical Specifications

V_{CC} = 5.0V ±10% T_A = 0°C to +70°C (C80C86, C80C86-2)
V_{CC} = 5.0V ±10%; T_A = -40°C to +85°C (I80C86, I80C86-2)
V_{CC} = 5.0V ±10%; T_A = -55°C to +125°C (M80C86)
V_{CC} = 5.0V ±5%; T_A = -55°C to +125°C (M80C86-2) **(Continued)**

MAX MODE SYSTEM (USING 82C88 BUS CONTROLLER)

TIMING REQUIREMENTS			80C86		80C86-2			
SYMBOL		PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
(35)	TCVNV	Control Active Delay (Note 10)	5	45	5	45	ns	C_L = 100pF for All 80C86 Outputs (In Addition to 80C86 Self Load)
(36)	TCVNX	Control Inactive Delay (Note 10)	10	45	10	45	ns	C_L = 100pF
(37)	TAZRL	Address Float to Read Active	0		0		ns	C_L = 100pF
(38)	TCLRL	$\overline{RD}$ Active Delay	10	165	10	100	ns	C_L = 100pF
(39)	TCLRH	$\overline{RD}$ Inactive Delay	10	150	10	80	ns	C_L = 100pF
(40)	TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL -45		TCLCL -40		ns	C_L = 100pF
(41)	TCHDTL	Direction Control Active Delay (Note 10)		50		50	ns	C_L = 100pF
(42)	TCHDTH	Direction Control Inactive Delay (Note 10)		30		30	ns	C_L = 100pF
(43)	TCLGL	$\overline{GT}$ Active Delay	10	85	0	50	ns	C_L = 100pF
(44)	TCLGH	$\overline{GT}$ Inactive Delay	10	85	0	50	ns	C_L = 100pF
(45)	TRLRH	$\overline{RD}$ Width	2TCLCL -75		2TCLCL -50		ns	C_L = 100pF
(46)	TOLOH	Output Rise Time		20		15	ns	From 0.8V to 2.0V
(47)	TOHOL	Output Fall Time		20		15	ns	From 2.0V to 0.8V

NOTES:

10. Signal at 82C84A or 82C88 shown for reference only.
11. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
12. Applies only to T2 state (8ns into T3).
13. The 80C86 actively pulls the $\overline{RQ}/\overline{GT}$ pin to a logic one on the following clock low time.
14. Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

Waveforms

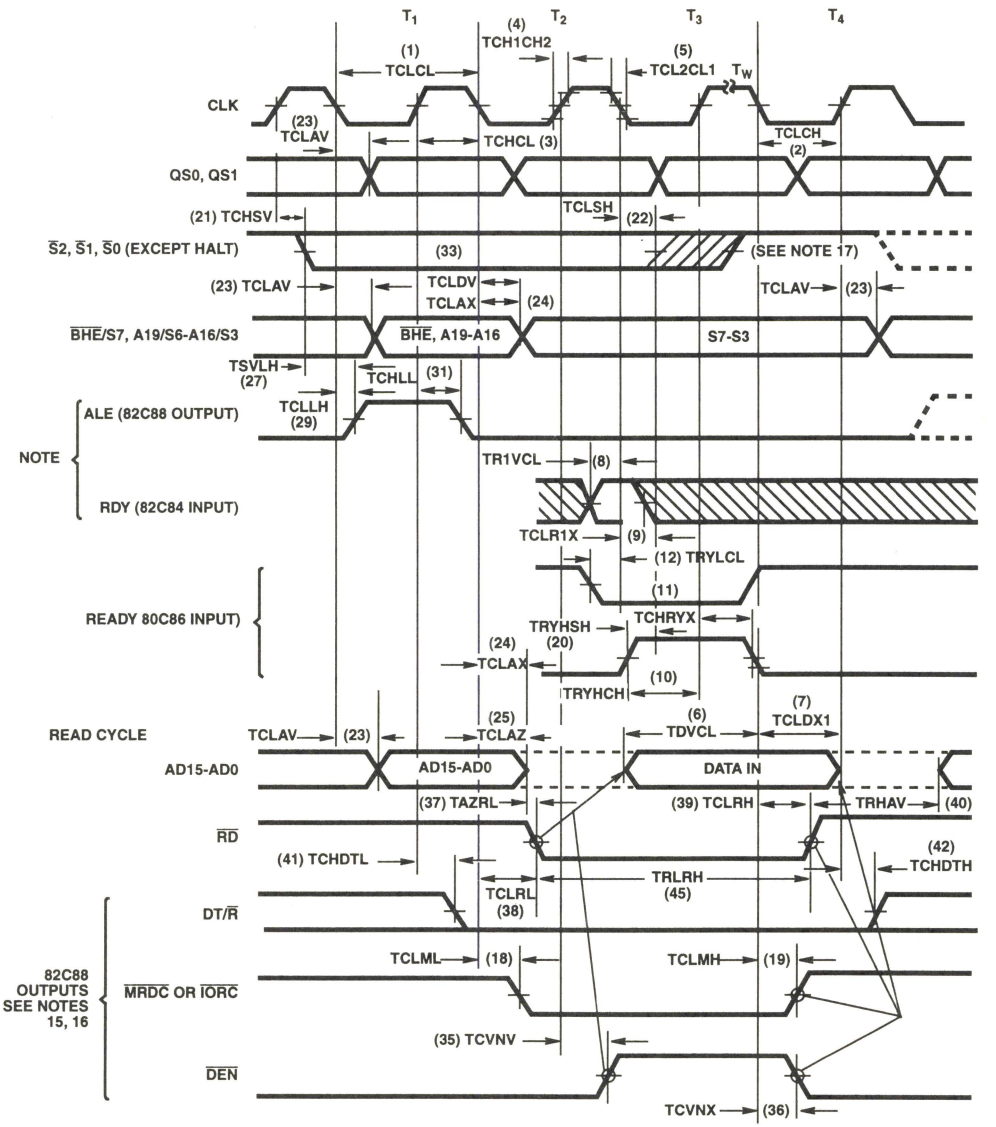


FIGURE 8A. BUS TIMING - MAXIMUM MODE (USING 82C88)

NOTES:

15. Signals at 82C84A or 82C88 are shown for reference only. RDY is sampled near the end of T2, T3, TW to determine if TW machine states are to be inserted.
16. The issuance of the 82C88 command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$, and $\overline{DEN}$) lags the active high 82C88 CEN.
17. Status inactive in state just prior to T4.

Waveforms (Continued)

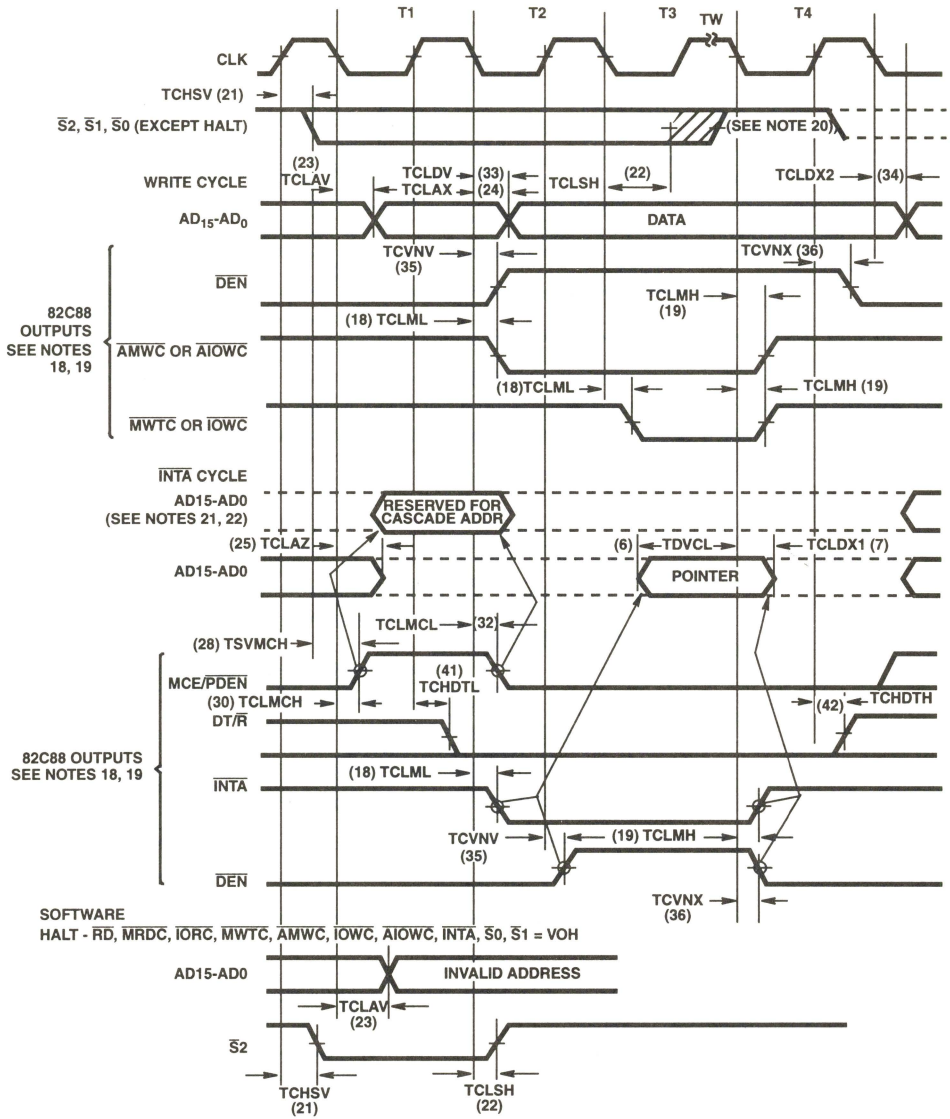
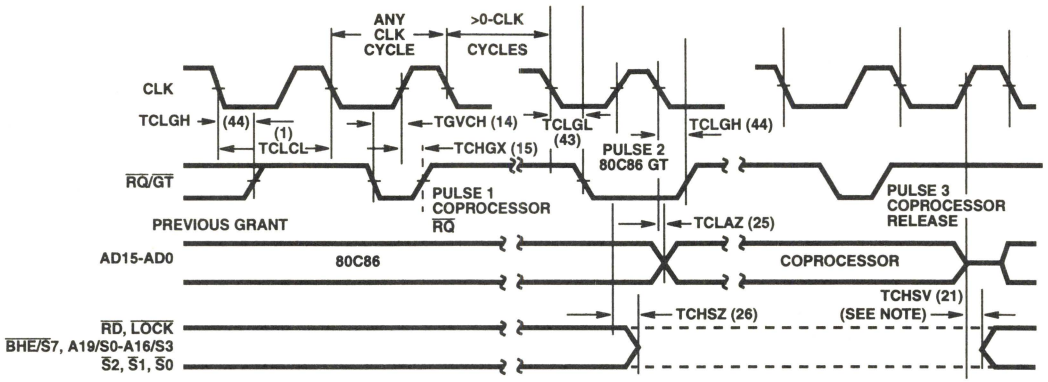


FIGURE 8B. BUS TIMING - MAXIMUM MODE (USING 82C88)

NOTES:

18. Signals at 82C84A or 82C86 are shown for reference only.
19. The issuance of the 82C88 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active high 82C88 CEN.
20. Status inactive in state just prior to T4.
21. Cascade address is valid between first and second INTA cycles.
22. Two INTA cycles run back-to-back. The 80C86 local ADDR/DATA bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.

Waveforms (Continued)



NOTE: The coprocessor may not drive the busses outside the region shown without risking contention.

FIGURE 9. REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)

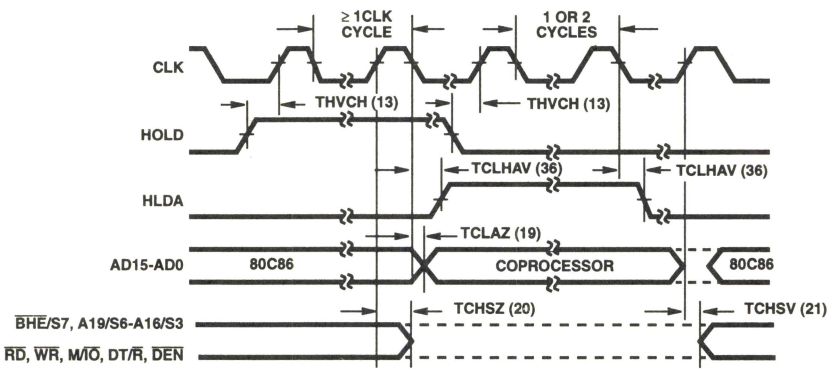
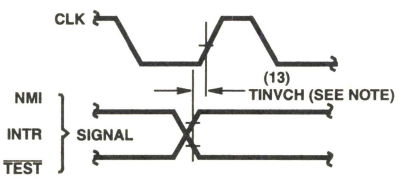


FIGURE 10. HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



NOTE: Setup requirements for asynchronous signals only to guarantee recognition at next CLK.

FIGURE 11. ASYNCHRONOUS SIGNAL RECOGNITION

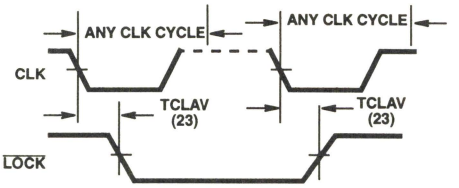


FIGURE 12. BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)

Waveforms (Continued)

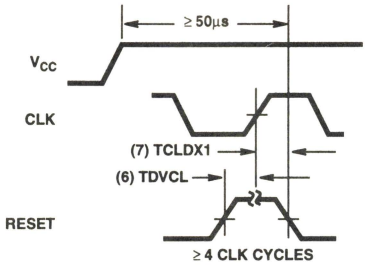
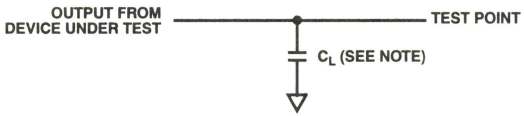


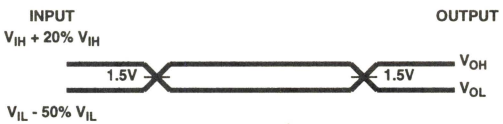
FIGURE 13. RESET TIMING

AC Test Circuit



NOTE: Includes stay and jig capacitance.

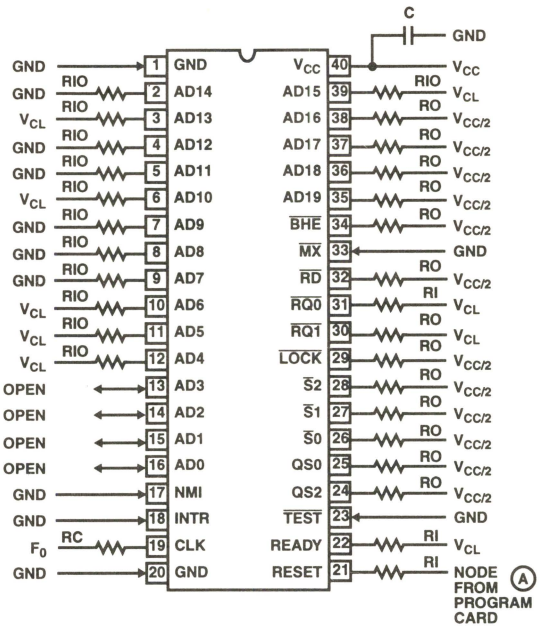
AC Testing Input, Output Waveform



NOTE: AC Testing: All input signals (other than CLK) must switch between V_{ILMAX} -50% V_{IL} and V_{IHMIN} +20% V_{IH}. CLK must switch between 0.4V and V_{CC}-0.4 Input rise and fall times are driven at 1ns/V.

Burn-In Circuits

MD80C86 CERDIP



NOTES:

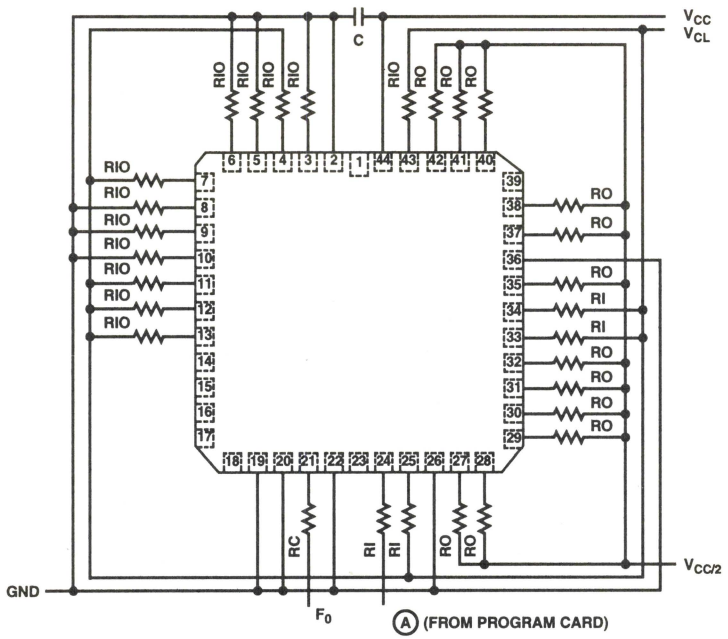
V_{CC} = 5.5V ±0.5V, GND = 0V.
Input voltage limits (except clock):
V_{IL} (maximum) = 0.4V
V_{IH} (minimum) = 2.6V, V_{IH} (clock) = (V_{CC} -0.4V) minimum.
$V_{CC/2}$ is external supply set to 2.7V ±10%.
V_{CL} is generated on program card (V_{CC} - 0.65V).
Pins 13 - 16 input sequenced instructions from internal hold devices.
F_0 = 100kHz ±10%.
Node (A) = a 40µs pulse every 2.56ms.

COMPONENTS:

1. RI = 10kΩ ±5%, 1/4W
2. RO = 1.2kΩ ±5%, 1/4W
3. RIO = 2.7kΩ ±5%, 1/4W
4. RC = 1kΩ ± 5%, 1/4W
5. C = 0.01µF (Minimum)

Burn-In Circuits (Continued)

MR80C86 CLCC



NOTES:

V_{CC} = 5.5V ±0.5V, GND = 0V.
Input voltage limits (except clock):
V_{IL} (maximum) = 0.4V
V_{IH} (minimum) = 2.6V, V_{IH} (clock) = (V_{CC} -0.4V) minimum.
$V_{CC/2}$ is external supply set to 2.7V ±10%.
V_{CL} is generated on program card (V_{CC} - 0.65V).
Pins 13 - 16 input sequenced instructions from internal hold devices.
F_0 = 100kHz ±10%.
Node (A) = a 40µs pulse every 2.56ms.

COMPONENTS:

1. RI = 10kΩ ±5%, 1/4W
2. RO = 1.2kΩ ±5%, 1/4W
3. RIO = 2.7kΩ ±5%, 1/4W
4. RC = 1kΩ ± 5%, 1/4W
5. C = 0.01µF (Minimum)

Metallization Topology

DIE DIMENSIONS:
249.2 x 290.9 x 19

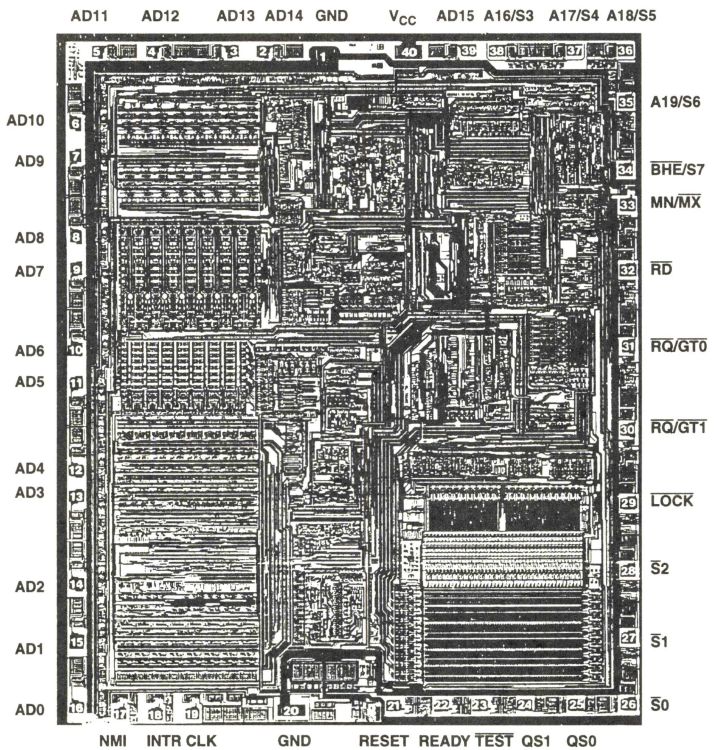
METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ ±2kÅ

WORST CASE CURRENT DENSITY:
1.5×10^5 A/cm^2

Metallization Mask Layout

80C86



Instruction Set Summary

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	76543210	76543210	76543210	76543210
DATA TRANSFER				
MOV = MOVE:				
Register/Memory to/from Register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to Register/Memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w 1
Immediate to Register	1 0 1 1 w reg	data	data if w 1	
Memory to Accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	
Accumulator to Memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
Register/Memory to Segment Register ††	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment Register to Register/Memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		
PUSH = Push:				
Register/Memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m		
Register	0 1 0 1 0 reg			
Segment Register	0 0 0 reg 1 1 0			
POP = Pop:				
Register/Memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m		
Register	0 1 0 1 1 reg			
Segment Register	0 0 0 reg 1 1 1			
XCHG = Exchange:				
Register/Memory with Register	1 0 0 0 0 1 1 w	mod reg r/m		
Register with Accumulator	1 0 0 1 0 reg			
IN = Input from:				
Fixed Port	1 1 1 0 0 1 0 w	port		
Variable Port	1 1 1 0 1 1 0 w			
OUT = Output to:				
Fixed Port	1 1 1 0 0 1 1 w	port		
Variable Port	1 1 1 0 1 1 1 w			
XLAT = Translate Byte to AL	1 1 0 1 0 1 1 1			
LEA = Load EA to Register2	1 0 0 0 1 1 0 1	mod reg r/m		
LDS = Load Pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m		
LES = Load Pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m		
LAHF = Load AH with Flags	1 0 0 1 1 1 1 1			
SAHF = Store AH into Flags	1 0 0 1 1 1 1 0			
PUSHF = Push Flags	1 0 0 1 1 1 0 0			
POPF = Pop Flags	1 0 0 1 1 1 0 1			
ARITHMETIC				
ADD = Add:				
Register/Memory with Register to Either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to Register/Memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s:w = 01
Immediate to Accumulator	0 0 0 0 0 1 0 w	data	data if w = 1	
ADC = Add with Carry:				
Register/Memory with Register to Either	0 0 0 1 0 0 d w	mod reg r/m		

Instruction Set Summary (Continued)

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	76543210	76543210	76543210	76543210
Immediate to Register/Memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s:w = 01
Immediate to Accumulator	0 0 0 1 0 1 0 w	data	data if w = 1	
INC = Increment:				
Register/Memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m		
Register	0 1 0 0 0 reg			
AAA = ASCII Adjust for Add	0 0 1 1 0 1 1 1			
DAA = Decimal Adjust for Add	0 0 1 0 0 1 1 1			
SUB = Subtract:				
Register/Memory and Register to Either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from Register/Memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s:w = 01
Immediate from Accumulator	0 0 1 0 1 1 0 w	data	data if w = 1	
SBB = Subtract with Borrow				
Register/Memory and Register to Either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from Register/Memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s:w = 01
Immediate from Accumulator	0 0 0 1 1 1 0 w	data	data if w = 1	
DEC = Decrement:				
Register/Memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m		
Register	0 1 0 0 1 reg			
NEG = Change Sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m		
CMP = Compare:				
Register/Memory and Register	0 0 1 1 1 0 d w	mod reg r/m		
Immediate with Register/Memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s:w = 01
Immediate with Accumulator	0 0 1 1 1 1 0 w	data	data if w = 1	
AAS = ASCII Adjust for Subtract	0 0 1 1 1 1 1 1			
DAS = Decimal Adjust for Subtract	0 0 1 0 1 1 1 1			
MUL = Multiply (Unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
IMUL = Integer Multiply (Signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
AAM = ASCII Adjust for Multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
DIV = Divide (Unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
IDIV = Integer Divide (Signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
AAD = ASCII Adjust for Divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
CBW = Convert Byte to Word	1 0 0 1 1 0 0 0			
CWD = Convert Word to Double Word	1 0 0 1 1 0 0 1			
LOGIC				
NOT = Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m		
SHL/SAL = Shift Logical/Arithmetic Left	1 1 0 1 0 0 v w	mod 1 0 0 r/m		
SHR = Shift Logical Right	1 1 0 1 0 0 v w	mod 1 0 1 r/m		
SAR = Shift Arithmetic Right	1 1 0 1 0 0 v w	mod 1 1 1 r/m		
ROL = Rotate Left	1 1 0 1 0 0 v w	mod 0 0 0 r/m		
ROR = Rotate Right	1 1 0 1 0 0 v w	mod 0 0 1 r/m		
RCL = Rotate Through Carry Flag Left	1 1 0 1 0 0 v w	mod 0 1 0 r/m		

Instruction Set Summary (Continued)

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	76543210	76543210	76543210	76543210
RCR = Rotate Through Carry Right	1 1 0 1 0 0 v w	mod 0 1 1 r/m		
AND = And:				
Reg./Memory and Register to Either	0 0 1 0 0 0 0 d w	mod reg r/m		
Immediate to Register/Memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w = 1
Immediate to Accumulator	0 0 1 0 0 1 0 w	data	data if w = 1	
TEST = And Function to Flags, No Result:				
Register/Memory and Register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate Data and Register/Memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w = 1
Immediate Data and Accumulator	1 0 1 0 1 0 0 w	data	data if w = 1	
OR = Or:				
Register/Memory and Register to Either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to Register/Memory	1 0 0 0 0 0 0 w	mod 1 0 1 r/m	data	data if w = 1
Immediate to Accumulator	0 0 0 0 1 1 0 w	data	data if w = 1	
XOR = Exclusive or:				
Register/Memory and Register to Either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to Register/Memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w = 1
Immediate to Accumulator	0 0 1 1 0 1 0 w	data	data if w = 1	
STRING MANIPULATION				
REP = Repeat	1 1 1 1 0 0 1 z			
MOVS = Move Byte/Word	1 0 1 0 0 1 0 w			
CMPS = Compare Byte/Word	1 0 1 0 0 1 1 w			
SCAS = Scan Byte/Word	1 0 1 0 1 1 1 w			
LODS = Load Byte/Word to AL/AX	1 0 1 0 1 1 0 w			
STOS = Stor Byte/Word from AL/A	1 0 1 0 1 0 1 w			
CONTROL TRANSFER				
CALL = Call:				
Direct Within Segment	1 1 1 0 1 0 0 0	disp-low	disp-high	
Indirect Within Segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m		
Direct Intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high	
		seg-low	seg-high	
Indirect Intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m		
JMP = Unconditional Jump:				
Direct Within Segment	1 1 1 0 1 0 0 1	disp-low	disp-high	
Direct Within Segment-Short	1 1 1 0 1 0 1 1	disp		
Indirect Within Segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m		
Direct Intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high	
		seg-low	seg-high	
Indirect Intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m		
RET = Return from CALL:				
Within Segment	1 1 0 0 0 0 1 1			
Within Seg Adding Immed to SP	1 1 0 0 0 0 1 0	data-low	data-high	

Instruction Set Summary (Continued)

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	76543210	76543210	76543210	76543210
Intersegment	11001011			
Intersegment Adding Immediate to SP	11001010	data-low	data-high	
JE/JZ = Jump on Equal/Zero	01110100	disp		
JL/JNGE = Jump on Less/Not Greater or Equal	01111100	disp		
JLE/JNG = Jump on Less or Equal/ Not Greater	01111110	disp		
JB/JNAE = Jump on Below/Not Above or Equal	01110010	disp		
JBE/JNA = Jump on Below or Equal/Not Above	01110110	disp		
JP/JPE = Jump on Parity/Parity Even	01111010	disp		
JO = Jump on Overflow	01110000	disp		
JS = Jump on Sign	01111000	disp		
JNE/JNZ = Jump on Not Equal/Not Zero	01110101	disp		
JNL/JGE = Jump on Not Less/Greater or Equal	01111101	disp		
JNLE/JG = Jump on Not Less or Equal/Greater	01111111	disp		
JNB/JAE = Jump on Not Below/Above or Equal	01110011	disp		
JNBE/JA = Jump on Not Below or Equal/Above	01110111	disp		
JNP/JPO = Jump on Not Par/Par Odd	01111011	disp		
JNO = Jump on Not Overflow	01110001	disp		
JNS = Jump on Not Sign	01111001	disp		
LOOP = Loop CX Times	11100010	disp		
LOOPZ/LOOPE = Loop While Zero/Equal	11100001	disp		
LOOPNZ/LOOPNE = Loop While Not Zero/Equal	11100000	disp		
JCXZ = Jump on CX Zero	11100011	disp		
INT = Interrupt				
Type Specified	11001101	type		
Type 3	11001100			
INTO = Interrupt on Overflow	11001110			
IRET = Interrupt Return	11001111			
PROCESSOR CONTROL				
CLC = Clear Carry	11111000			
CMC = Complement Carry	11110101			
STC = Set Carry	11111001			
CLD = Clear Direction	11111100			
STD = Set Direction	11111101			
CLI = Clear Interrupt	11111010			
ST = Set Interrupt	11111011			
HLT = Halt	11110100			
WAIT = Wait	10011011			
ESC = Escape (to External Device)	11011xxx	mod x x r/m		
LOCK = Bus Lock Prefix	11110000			

Instruction Set Summary (Continued)

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	76543210	76543210	76543210	76543210

NOTES:
AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS= Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction
if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = O†, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high:disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP †
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)
† except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.
†† MOV CS, REG/MEMORY not allowed.

if s:w = 01 then 16-bits of immediate data form the operand.
if s:w. = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1; if v = 1 then "count" in (C_L)
x = don't care
z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

001 reg 11 0

REG is assigned according to the following table:

16-BIT (w = 1)	8-BIT (w = 0)	SEGMENT
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	00 ES
101 BP	101 CH	00 ES
110 SI	110 DH	00 ES
111 DI	111 BH	00 ES

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS =

X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Mnemonics © Intel, 1978

HARRIS SEMICONDUCTOR

80C88

March 1997

CMOS 8/16-Bit Microprocessor

Features

- Compatible with NMOS 8088
- Direct Software Compatibility with 80C86, 8086, 8088
- 8-Bit Data Bus Interface; 16-Bit Internal Architecture
- Completely Static CMOS Design
  - DC 5MHz (80C88)
  - DC 8MHz (80C88-2)
- Low Power Operation
  - ICCSB ..... 500μA Maximum
  - ICCOP ..... 10mA/MHz Maximum
- 1 Megabyte of Direct Memory Addressing Capability
- 24 Operand Addressing Modes
- Bit, Byte, Word, and Block Move Operations
- 8-Bit and 16-Bit Signed/Unsigned Arithmetic
- Bus-Hold Circuitry Eliminates Pull-up Resistors
- Wide Operating Temperature Ranges
  - C80C88 ..... $0^{o}C$ to $+70^{o}C$
  - I80C88 ..... $-40^{o}C$ to $+85^{o}C$
  - M80C88 ..... $-55^{o}C$ to $+125^{o}C$

Description

The Harris 80C88 high performance 8/16-bit CMOS CPU is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). Two modes of operation, MINimum for small systems and MAXimum for larger applications such as multiprocessing, allow user configuration to achieve the highest performance level.

Full TTL compatibility (with the exception of CLOCK) and industry-standard operation allow use of existing NMOS 8088 hardware and Harris CMOS peripherals.

Complete software compatibility with the 80C86, 8086, and 8088 microprocessors allows use of existing software in new designs.

Ordering Information

PACKAGE	TEMPERATURE RANGE	5MHz	8MHz	PKG. NO.
Plastic DIP	$0^{o}C$ to $+70^{o}C$	CP80C88	CP80C88-2	E40.6
	$-40^{o}C$ to $+85^{o}C$	IP80C88	IP80C88-2	E40.6
PLCC	$0^{o}C$ to $+70^{o}C$	CS80C88	CS80C88-2	N44.65
	$-40^{o}C$ to $+85^{o}C$	IS80C88	IS80C88-2	N44.65
CERDIP	$0^{o}C$ to $+70^{o}C$	CD80C88	CD80C88-2	F40.6
	$-40^{o}C$ to $+85^{o}C$	ID80C88	ID80C88-2	F40.6
	$-55^{o}C$ to $+125^{o}C$	MD80C88/B	MD80C88-2/B	F40.6
SMD#	$-55^{o}C$ to $+125^{o}C$	5962-8601601QA	-	F40.6
LCC	$-55^{o}C$ to $+125^{o}C$	MR80C88/B	MR80C88-2/B	J44.A
SMD#	$-55^{o}C$ to $+125^{o}C$	5962-8601601XA	-	J44.A

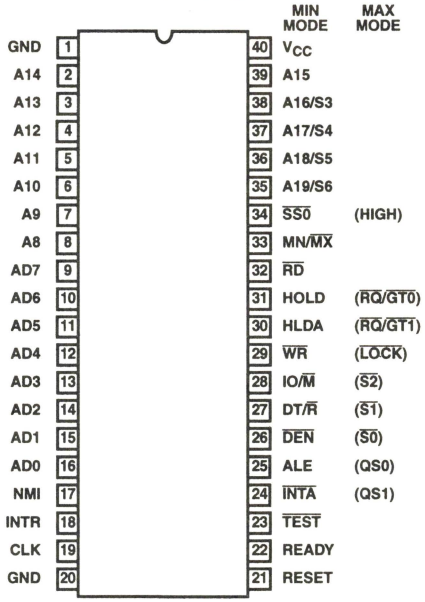
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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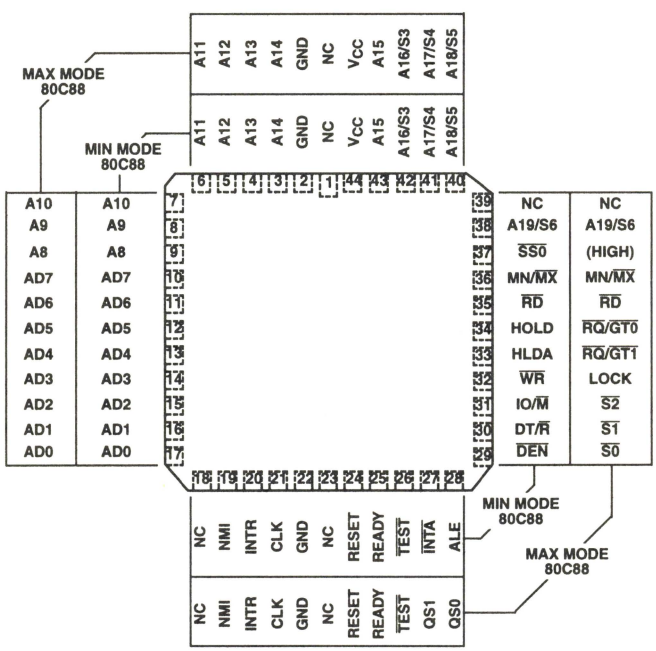
File Number **2949.1**

Pinouts

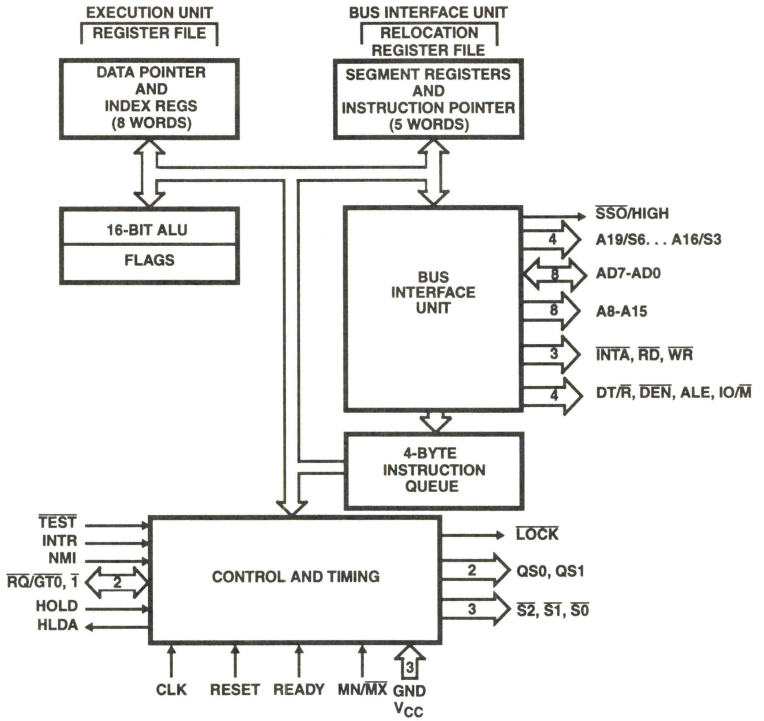
80C88 (DIP)
TOP VIEW

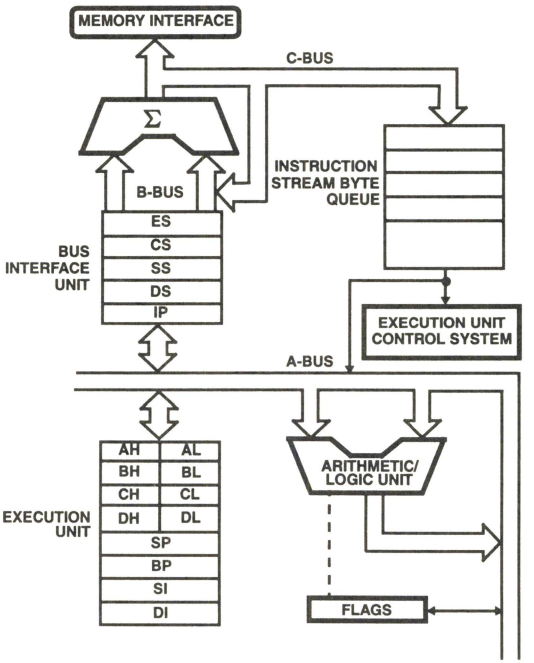


80C88 (PLCC/LCC)
TOP VIEW



Functional Diagram





Pin Description

The following pin function descriptions are for 80C88 systems in either minimum or maximum mode. The "local bus" in these descriptions is the direct multiplexed bus interface connection to the 80C88 (without regard to additional bus buffers).

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
AD7-AD0	9-16	I/O	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address (T1) and data (T2,T3,Tw and T4) bus. These lines are active HIGH and are held at high impedance to the last valid level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence"
A15-A8	2-8, 39	O	ADDRESS BUS: These lines provide address bits 8 through 15 for the entire bus cycle (T1-T4). These lines do not have to be latched by ALE to remain valid. A15-A8 are active HIGH and are held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence".
A19/S6, A18/S5, A17/S4, A16/S3	35 36 37 38	O O O O	ADDRESS/STATUS: During T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, TW and T4. S6 is always LOW. The status of the interrupt enable flag bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown. This information indicates which segment register is presently being used for data accessing. These lines are held at high impedance to the last valid logic level during local bus "hold acknowledge" or "grant Sequence".
$\overline{RD}$	32	O	READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the IO/$\overline{M}$ pin or $\overline{S2}$. This signal is used to read devices which reside on the 80C88 local bus. $\overline{RD}$ is active LOW during T2, T3, Tw of any read cycle, and is guaranteed to remain HIGH in T2 until the 80C88 local bus has floated. This line is held at a high impedance logic one state during "hold acknowledge" or "grant sequence".
READY	22	I	READY: is the acknowledgment from the address memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 82C84A clock generator to from READY. This signal is active HIGH. The 80C88 READY input is not synchronized. Correct operation is not guaranteed if the set up and hold times are not met.
INTR	18	I	INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
$\overline{TEST}$	23	I	TEST: input is examined by the "wait for test" instruction. If the $\overline{TEST}$ input is LOW, execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NONMASKABLE INTERRUPT: is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	RESET: cases the processor to immediately terminate its present activity. The signal must transition LOW to HIGH and remain active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V_{CC}	40		V_{CC}: is the +5V power supply pin. A 0.1µF capacitor between pins 20 and 40 recommended for decoupling.
GND	1, 20		GND: are the ground pins (both pins must be connected to system ground). A 0.1µF capacitor between pins 1 and 20 is recommended for decoupling.
MN/$\overline{MX}$	33'	I	MINIMUM/MAXIMUM: indicates the mode in which the processor is to operate. The two modes are discussed in the following sections.

S4	S3	CHARACTERISTICS
0	0	Alternate Data
0	1	Stack
1	0	Code or None
1	1	Data

Pin Description (Continued)

The following pin function descriptions are for 80C88 system in minimum mode (i.e., MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to the minimum mode are described; all other pin functions are as described above.

MINIMUM MODE SYSTEM

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
IO/$\overline{M}$	28	O	STATUS LINE: is an inverted maximum mode $\overline{S2}$. It is used to distinguish a memory access from an I/O access. IO/$\overline{M}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O = HIGH, M = LOW). IO/$\overline{M}$ is held to a high impedance logic one during local bus "hold acknowledge".
$\overline{WR}$	29	O	Write: strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the IO/$\overline{M}$ signal. $\overline{WR}$ is active for T2, T3, and Tw of any write cycle. It is active LOW, and is held to high impedance logic one during local bus "hold acknowledge".
$\overline{INTA}$	24	O	INTA: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3 and Tw of each interrupt acknowledge cycle. Note that $\overline{INTA}$ is never floated.
ALE	25	O	ADDRESS LATCH ENABLE: is provided by the processor to latch the address into the 82C82/82C83 address latch. It is a HIGH pulse active during clock low of T1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	DATA TRANSMIT/RECEIVE: is needed in a minimum system that desires to use an 82C86/82C87 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in the maximum mode, and its timing is the same as for IO/$\overline{M}$ (T = HIGH, R = LOW). This signal is held to a high impedance logic one during local bus "hold acknowledge".
$\overline{DEN}$	26	O	DATA ENABLE: is provided as an output enable for the 82C86/82C87 in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access, and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle, it is active from the middle of T2 until the middle of T4, while for a write cycle, it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ is held to high impedance logic one during local bus "hold acknowledge".
HOLD, HLDA	31 30	I O	HOLD: indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgment, in the middle of a T4 or T1 clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the set up time.
$\overline{SS0}$	34	O	STATUS LINE: is logically equivalent to $\overline{S0}$ in the maximum mode. The combination of $\overline{SS0}$, IO/$\overline{M}$ and DT/$\overline{R}$ allows the system to completely decode the current bus cycle status. $\overline{SS0}$ is held to high impedance logic one during local bus "hold acknowledge".

IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SS0}$	CHARACTERISTICS
1	0	0	Interrupt Acknowledge
1	0	1	Read I/O Port
1	1	0	Write I/O Port
1	1	1	Halt
0	0	0	Code Access
0	0	1	Read Memory
0	1	0	Write Memory
0	1	1	Passive

Pin Description (Continued)

The following pin function descriptions are for 80C88 system in maximum mode (i.e., MN/$\overline{MX}$ = GND). Only the pin functions which are unique to the maximum mode are described; all other pin functions are as described above.

MAXIMUM MODE SYSTEM

<table>
<tr><th>SYMBOL</th><th>PIN NUMBER</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>$\overline{S0}$
$\overline{S1}$
$\overline{S2}$</td><td>26
27
28</td><td>O
O
O</td><td>STATUS: is active during clock high of T4, T1 and T2, and is returned to the passive state (1, 1, 1) during T3 or during Tw when READY is HIGH. This status is used by the 82C88 bus controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$ or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or Tw is used to indicate the end of a bus cycle.
These signals are held at a high impedance logic one state during "grant sequence".
<table>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>CHARACTERISTICS</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Code Access</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table>
</td></tr>
<tr><td>$\overline{RQ}$/GT0,
$\overline{RQ}$/GT1</td><td>31
30</td><td>I/O</td><td>REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}$/GT0 having higher priority than $\overline{RQ}$/GT1. $\overline{RQ}$/GT has internal bus-hold high circuitry and, if unused, may be left unconnected. The request/grant sequence is as follows (see $\overline{RQ}$/GT Timing Sequence):
1. A pulse of one CLK wide from another local bus master indicates a local bus request ("hold") to the 80C88 (pulse 1).
2. During a T4 or T1 clock cycle, a pulse one clock wide from the 80C88 to the requesting master (pulse 2), indicates that the 80C88 has allowed the local bus to float and that it will enter the "grant sequence" state at the next CLK. The CPUs bus interface unit is disconnected logically from the local bus during "grant sequence".
3. A pulse one CLK wide from the requesting master indicates to the 80C88 (pulse 3) that the "hold" request is about to end and that the 80C88 can reclaim the local bus at the next CLK. The CPU then enters T4 (or T1 if no bus cycles pending).
Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after bus exchange. Pulses are active LOW.
If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conjugations are met:
1. Request occurs on or before T2.
2. Current cycle is not the low bit of a word.
3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.
4. A locked instruction is not currently executing.
If the local bus is idle when the request is made the two possible events will follow:
1. Local bus will be released during the next clock.
2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.</td></tr>
<tr><td>$\overline{LOCK}$</td><td>29</td><td>O</td><td>LOCK: indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active (LOW). The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a high impedance logic one state during "grant sequence". In Max Mode, $\overline{LOCK}$ is automatically generated during T2 of the first $\overline{INTA}$ cycle and removed during T2 of the second $\overline{INTA}$ cycle.</td></tr>
<tr><td>QS1, QS0</td><td>24, 25</td><td>O</td><td>QUEUE STATUS: provide status to allow external tracking of the internal 80C88 instruction queue.
The queue status is valid during the CLK cycle after which the queue operation is performed. Note that the queue status never goes to a high impedance statue (floated).
<table>
<tr><th>QS1</th><th>QS0</th><th>CHARACTERISTICS</th></tr>
<tr><td>0</td><td>0</td><td>No Operation</td></tr>
<tr><td>0</td><td>1</td><td>First Byte of Opcode from Queue</td></tr>
<tr><td>1</td><td>0</td><td>Empty the Queue</td></tr>
<tr><td>1</td><td>1</td><td>Subsequent Byte from Queue</td></tr>
</table>
</td></tr>
<tr><td>-</td><td>34</td><td>O</td><td>Pin 34 is always a logic one in the maximum mode and is held at a high impedance logic one during a "grant sequence".</td></tr>
</table>

Functional Description

Static Operation

All 80C88 circuitry is static in design. Internal registers, counters and latches are static and require not refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The CMOS 80C88 can operate from DC to the specified upper frequency limit. The processor clock may be stopped in either state (high/low) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The 80C88 can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for start-up.

Static design also allows very low frequency operation (as low as DC). In a power critical situation, this can provide extremely low power operation since 80C88 power dissipation is directly related to operation frequency. As the system frequency is reduced, so is the operating power until, at a DC input frequency, the power requirement is the 80C88 standby current.

Internal Architecture

The internal functions of the 80C88 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the CPU block diagram.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 4 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 1 byte in the queue, the BIU will attempt a byte fetch memory cycle. This greatly reduces "dead time": on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides unrelocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

Memory Organization

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra, and stack segments of up to 64K bytes each, with each segment falling on 16 byte boundaries. (See Figure 1).

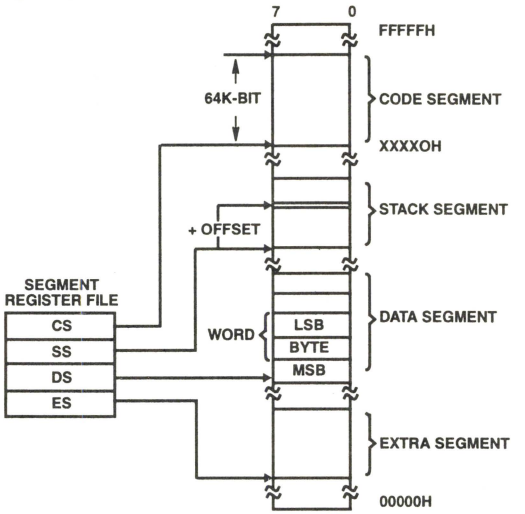


FIGURE 1. MEMORY ORGANIZATION

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to specific rules as shown in Table 1. All information in one segment type share the same logical attributes (e.g., code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

TABLE 1.

MEMORY REFERENCE NEED	SEGMENT REGISTER USED	SEGMENT SELECTION RULE
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when: relative to stack, destination of string operation, or explicitly overridden.
External Data (Global)	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment override.

Word (16-bit) operands can be located on even or odd address boundaries. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location.

The BIU will automatically execute two fetch or write cycles for 16-bit operands.

Certain locations in memory are reserved for specific CPU operations. (See Figure 2). Locations from addresses FFFF0H through FFFFFH are reserved for operations including a jump to initial system initialization routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt service routines is accessed through its own pair of 16-bit pointers - segment address pointer and offset address pointer. The first pointer, used as the offset address, is loaded into the IP, and the second pointer, which designates the base address, is loaded into the CS. At this point program control is transferred to the interrupt routine. The pointer elements are assumed to have been stored at their respective places in reserved memory prior to the occurrence of interrupts.

Minimum and Maximum Modes

The requirements for supporting minimum and maximum 80C88 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the 80C88 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the 80C88 defines pins 24 through 31 and 34 in maximum mode. When the MN/$\overline{MX}$ pins is strapped to V_{CC}, the 80C88 generates bus control signals itself on pins 24 through 31 and 34.

The minimum mode 80C88 can be used with either a muliplexed or demultiplexed bus. This architecture provides the 80C88 processing power in a highly integrated form.

The demultiplexed mode requires one latch (for 64K addressability) or two latches (for a full megabyte of addressing). An 82C86 or 82C87 transceiver can also be used if data bus buffering is required. (See Figure 3). The 80C88 provides $\overline{DEN}$ and DT/$\overline{R}$ to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

The maximum mode employs the 82C88 bus controller (See Figure 4). The 82C88 decode status lines S0, S1 and S2, and provides the system with all bus control signals. Moving the bus control to the 82C88 provides better source and sink current capability to the control lines, and frees the 80C88 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the 80C88 in maximum mode. These features allow coprocessors in local bus and remote bus configurations.

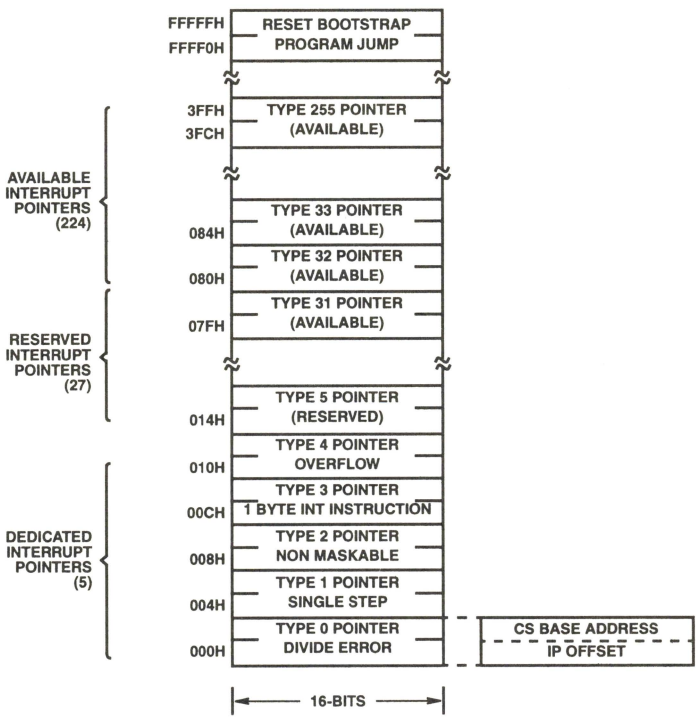


FIGURE 2. RESERVED MEMORY LOCATIONS

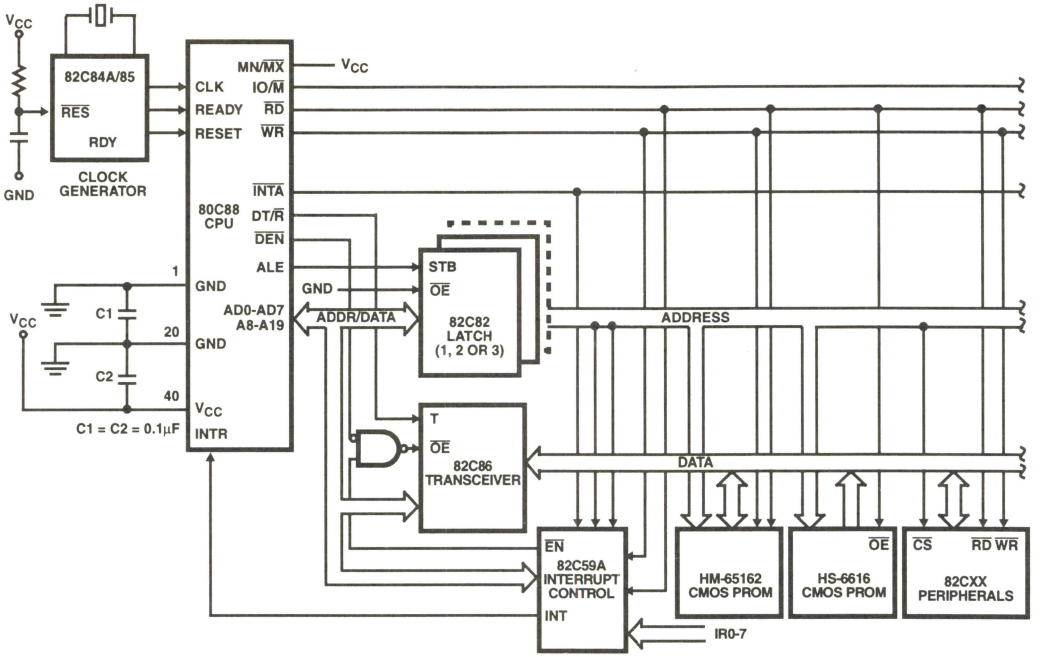


FIGURE 3. DEMULTIPLEXED BUS CONFIGURATION

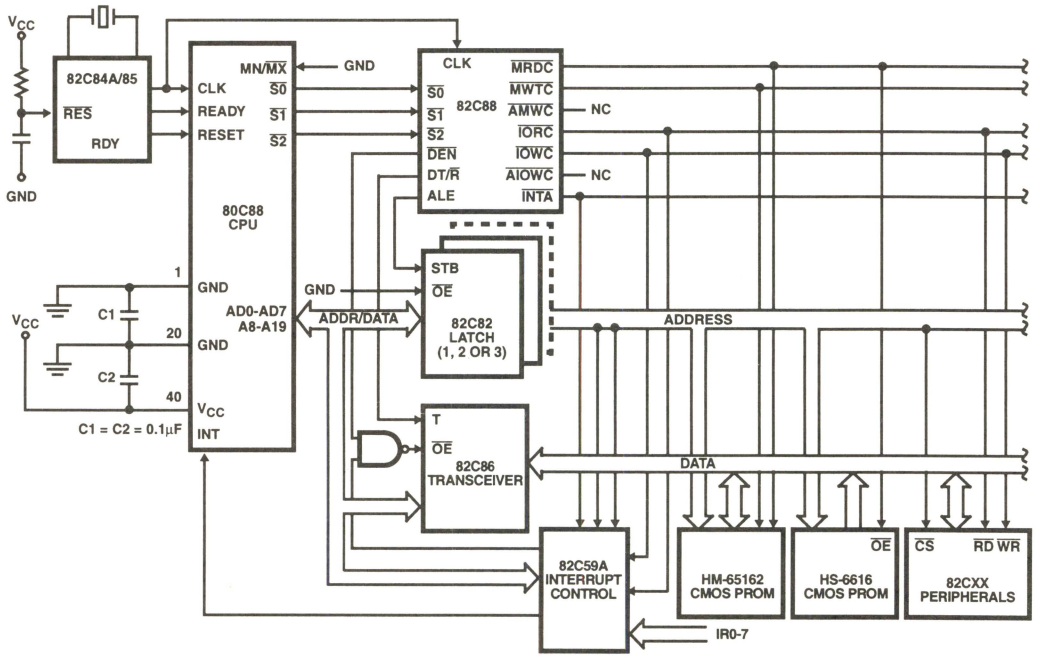


FIGURE 4. FULLY BUFFERED SYSTEM USING BUS CONTROLLER

Bus Operation

The 80C88 address/data bus is broken into three parts: the lower eight address/data bits (AD0-AD7), the middle eight address bits (A8-A15), and the upper four address bits (A16-A19). The address/data bits and the highest four address bits are time multiplexed. This technique provides the most efficient use of pins on the processor, permitting the use of standard 40 lead package. The middle eight address bits are not multiplexed, i.e., they remain valid throughout each bus cycle. In addition, the bus can be demultiplexed at the processor with a single address latch if a standard, nonmultiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3 and T4. (See Figure 5). The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a "Not Ready" indication is given by the addressed device, "wait" states (TW) are inserted between T3 and T4. Each inserted "wait" state is of the same duration as a CLK cycle. Periods can occur between 80C88 driven bus cycles. These are referred to as "idle" states (TI), or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T1 of any bus cycle, the ALE (Address latch enable) signal is emitted (by either the processor or the 82C88 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to Table 2.

Status bits S3 through S6 are multiplexed with high order address bits and are therefore valid during T2 through T4. S3 and S4 indicate which segment register was used to this bus cycle in forming the address according to Table 3.

S5 is a reflection of the PSW interrupt enable bit. S6 is always equal to 0.

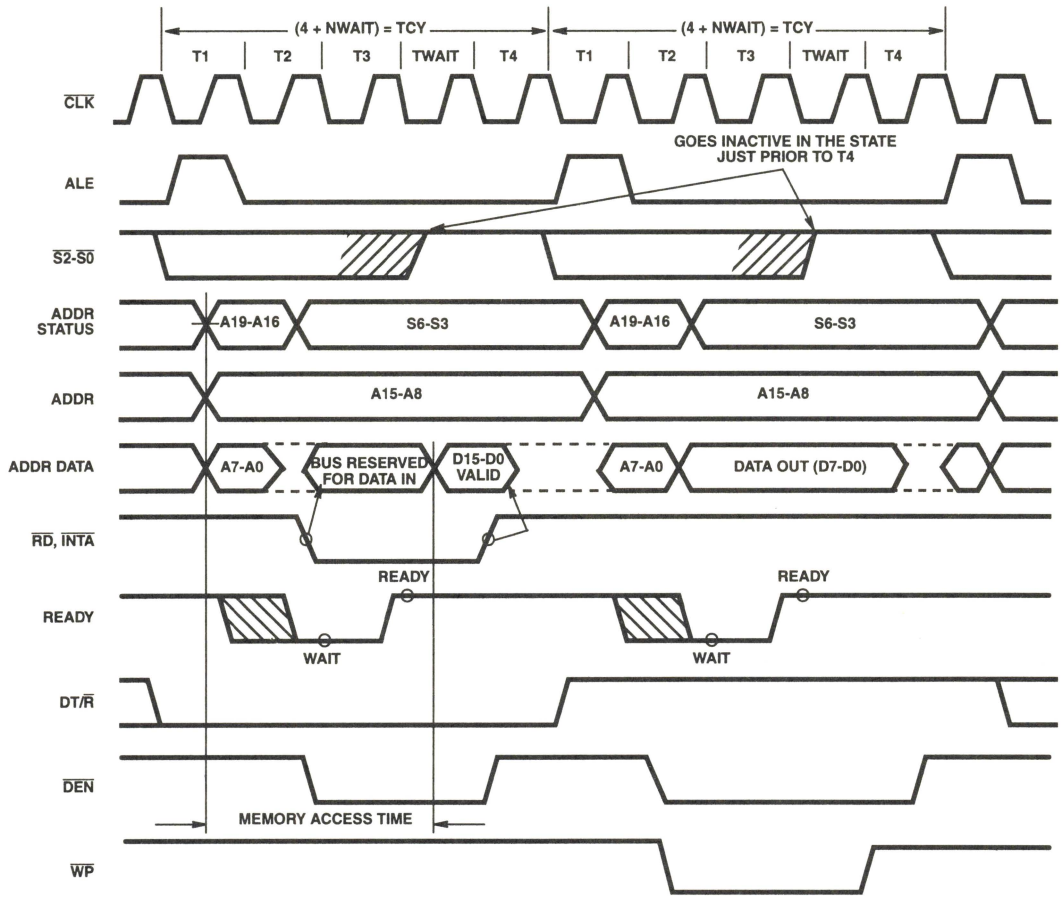


FIGURE 5. BASIC SYSTEM TIMING

TABLE 2.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTICS
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (No Bus Cycle)

TABLE 3.

S4	S3	CHARACTERISTICS
0	0	Alternate Data (Extra Segment)
0	1	Stack
1	0	Code or None
1	1	Data

I/O Addressing

In the 80C88, I/O operations can address up to a maximum of 64K I/O registers. The I/O address appears in the same format as the memory address on bus lines A15-A0. The address lines A19-A16 are zero in I/O operations. The variable I/O instructions, which use register DX as a pointer, have full address capability, while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space. I/O ports are addressed in the same manner as memory locations.

Designers familiar with the 8085 or upgrading an 8085 design should note that the 8085 addresses I/O with an 8-bit address on both halves of the 16-bit address bus. The 80C88 uses a full 16-bit address on its lower 16 address lines.

External Interface

Processor Reset and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 80C88 RESET is required to be HIGH for greater than four clock cycles. The 80C88 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 clock cycles. After this interval the 80C88 operates normally, beginning with the instruction in absolute location FFFFOH (see Figure 2). The RESET input is internally synchronized to the processor clock. At initialization, the HIGH to LOW transition of RESET must occur no sooner than 50μs after power up, to allow complete initialization of the 80C88.

NMI will not be recognized if asserted prior to the second CLK cycle following the end of RESET.

Bus Hold Circuitry

To avoid high current conditions caused by floating inputs to CMOS devices and to eliminate the need for pull-up/down resistors, "bus-hold" circuitry has been used on 80C88 pins 2-16, 26-32 and 34-39 (see Figure 6A and 6B). These circuits maintain a valid logic state if no driving source is present (i.e., an unconnected pin or a driving source which goes to a high impedance state).

To override the "bus hold" circuits, an external driver must be capable of supplying 400μA minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible. Power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

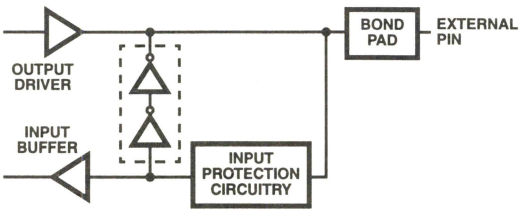


FIGURE 6A. BUS HOLD CIRCUITRY PIN 2-16, 35-39

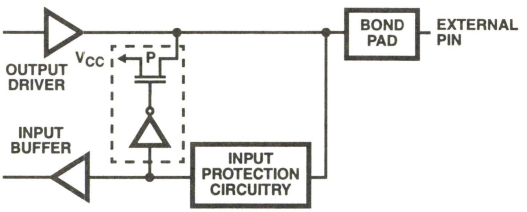


FIGURE 6B. BUS HOLD CIRCUITRY PIN 26-32, 34

Interrupt Operations

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the instruction set description. Hardware interrupts can be classified as nonmaskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256 element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (see Figure 2), which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8-bit type number, during the interrupt acknowledge sequence, which is used to vector through the appropriate element to the new interrupt service program location.

Non-Maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt (NMI) pin which has higher priority than the maskable interrupt request (INTR) pin. A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW to High transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two clock cycles, but is not required to be synchronized to the clock. An high going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves (2 bytes in the case of word moves) of a block type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure.

The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

Maskable Interrupt (INTR)

The 80C88 provides a singe interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable (IF) flag bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK.

To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block type instruction. INTR may be removed anytime after the falling edge of the first $\overline{INTA}$ signal. During interrupt response sequence, further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt, or single step). The FLAGS register, which is automatically pushed onto the stack, reflects the state of the processor prior to the interrupt. The enable bit will be zero until the old FLAGS register is restored, unless specifically set by an instruction.

During the response sequence (see Figure 7), the processor executes two successive (back-to-back) interrupt acknowledge cycles. The 80C88 emits to $\overline{LOCK}$ signal (maximum mode only) from T2 of the first bus cycle until T2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is fetched from the external interrupt system (e.g., 82C59A PIC) which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table.

An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. INTR may be removed anytime after the falling edge of the first $\overline{INTA}$ signal. The interrupt return instruction includes a flags pop which returns the status of the original interrupt enable bit when it restores the flags.

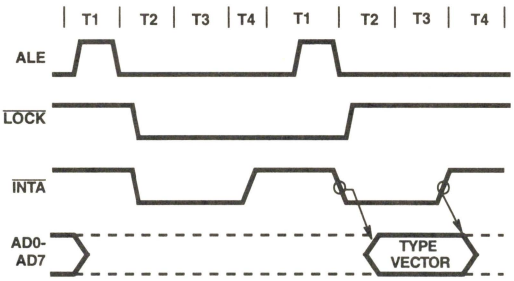


FIGURE 7. INTERRUPT ACKNOWLEDGE SEQUENCE

Halt

When a software HALT instruction is executed, the processor indicates that it is entering the HALT state in one of two ways, depending upon which mode is strapped. In minimum mode, the processor issues ALE, delayed by one clock cycle, to allow the system to latch the halt status. Halt status is available on IO/$\overline{M}$, DT/$\overline{R}$, and $\overline{SS0}$. In maximum mode, the processor issues appropriate HALT status on $\overline{S2}$, $\overline{S1}$ and $\overline{S0}$, and the 82C88 bus controller issues one ALE. The 80C88 will not leave the HALT state when a local bus hold is entered while in HALT. In this case, the processor reissues the HALT indicator at the end of the local bus hold. An interrupt request or RESET will force the 80C88 out of the HALT state.

Read/Modify/Write (Semaphore) Operations Via $\overline{LOCK}$

The $\overline{LOCK}$ status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This allows the processor to perform read/modify/write operations on memory (via the "exchange register with memory" instruction), without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The $\overline{LOCK}$ signal is activated (LOW) in the clock cycle following decoding of the $\overline{LOCK}$ prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the $\overline{LOCK}$ prefix. While $\overline{LOCK}$ is active, a request on a $\overline{RQ}$/$\overline{GT}$ pin will be recorded, and then honored at the end of the $\overline{LOCK}$.

External Synchronization Via $\overline{TEST}$

As an alternative to interrupts, the 80C88 provides a single software-testable input pin ($\overline{TEST}$). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the $\overline{TEST}$ input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the 80C88 three-states all output drivers while inputs and I/O pins are held at valid logic levels by internal bus-hold circuits. If interrupts are enabled, the 80C88 will recognize interrupts and process them when it regains control of the bus.

Basic System Timing

In minimum mode, the MN/$\overline{MX}$ pin is strapped to V_{CC} and the processor emits bus control signals ($\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, etc.) directly. In maximum mode, the MN/$\overline{MX}$ pin is strapped to GND and the processor emits coded status information which the 82C88 bus controller uses to generate MULTIBUS™ compatible bus control signals.

System Timing - Minimum System

The read cycle begins in T1 with the assertion of the address latch enable (ALE) signal (see Figure 5). The trailing (low going) edge of this signal is used to latch the address information, which is valid on the address data bus (ADO-AD7) at this time, into the 82C82/82C83 latch. Address lines A8 through A15 do not need to be latched because they remain valid throughout the bus cycle. From T1 to T4 the IO/$\overline{M}$ signal indicates a memory or I/O operation. At T2 the address is removed from the address data bus and the bus is held at the last valid logic state by internal bus-hold devices. The read control signal is also asserted at T2. The read ($\overline{RD}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again three-state its bus drivers. If a transceiver (82C86/82C87) is required to buffer the local bus, signals DT/$\overline{R}$ and $\overline{DEN}$ are provided by the 80C88.

A write cycle also begins with the assertion of ALE and the emission of the address. The IO/$\overline{M}$ signal is again asserted to indicate a memory or I/O write operation. In T2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of T4. During T2, T3, and Tw, the processor asserts the write control signal. The write ($\overline{WR}$) signal becomes active at the beginning of T2, as opposed to the read, which is delayed somewhat into T2 to provide time for output drivers to become inactive.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge ($\overline{INTA}$) signal is asserted in place of the read ($\overline{RD}$) signal and the address bus is held at the last valid logic state by internal bus-hold devices (see Figure 6). In the second of two successive $\overline{INTA}$ cycles, a byte of information is read from the data bus, as supplied by the interrupt system logic (i.e., 82C59A priority interrupt controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into the interrupt vector lookup table, as described earlier.

Bus Timing - Medium Complexity Systems

For medium complexity systems, the MN/$\overline{MX}$ pin is connected to GND and the 82C88 bus controller is added to the system, as well as an 82C82/82C83 latch for latching the system address, and an 82C86/82C87 transceiver to allow for bus loading greater than the 80C88 is capable of handling (see Figure 8). Signals ALE, $\overline{DEN}$, and DT/$\overline{R}$ are generated by the 82C88 instead of the processor in this configuration, although their timing remains relatively the same. The 80C88 status outputs ($\overline{S2}$, $\overline{S1}$ and $\overline{S0}$) provide type of cycle information and become 82C88 inputs. This bus cycle information specifies read (code, data or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 82C88 thus issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 82C88 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The 82C86/82C87 transceiver receives the usual T and $\overline{OE}$ inputs from the 82C88 DT/$\overline{R}$ and $\overline{DEN}$ outputs.

The pointer into the interrupt vector table, which is passed during the second $\overline{INTA}$ cycle, can derive from an 82C59A located on either the local bus or the system bus. If the master 82C59A priority interrupt controller is positioned on the local bus, the 82C86/82C87 transceiver must be disabled when reading from the master 82C59A during the interrupt acknowledge sequence and software "poll".

The 80C88 Compared to the 80C86

The 80C88 CPU is a 8-bit processor designed around the 8086 internal structure. Most internal functions of the 80C88 are identical to the equivalent 80C86 functions. The 80C88 handles the external bus the same way the 80C86 does with the distinction of handling only 8-bits at a time. Sixteen-bit operands are fetched or written in two consecutive bus cycles. Both processors will appear identical to the software engineer, with the exception of execution time. The internal register structure is identical and all instructions have the same end result. Internally, there are three differences between the 80C88 and the 80C86. All changes are related to the 8-bit bus interface.

- The queue length is 4 bytes in the 80C88, whereas the 80C86 queue contains 6 bytes, or three words. The queue was shortened to prevent overuse of the bus by the BIU when prefetching instructions. This was required because of the additional time necessary to fetch instructions 8-bits at a time.
- To further optimize the queue, the prefetching algorithm was changed. The 80C88 BIU will fetch a new instruction to load into the queue each time there is a 1 byte space available in the queue. The 80C86 waits until a 2 byte space is available.
- The internal execution time of the instruction set is affected by the 8-bit interface. All 16-bit fetches and writes from/to memory take an additional four clock cycles. The CPU is also limited by the speed of instruction fetches. This latter problem only occurs when a series of simple operations occur. When the more sophisticated instructions of the 80C88 are being used, the queue has time to fill the execution proceeds as fast as the execution unit will allow.

MULTIBUS™ is a patented Intel bus.

The 80C88 and 80C86 are completely software compatible by virtue of their identical execution units. Software that is system dependent may not be completely transferable, but software that is not system dependent will operate equally as well on an 80C88 or an 80C86.

The hardware interface of the 80C88 contains the major differences between the two CPUs. The pin assignments are nearly identical, however, with the following functional changes:

- A8-A15: These pins are only address outputs on the 80C88. These address lines are latched internally and remain valid throughout a bus cycle in a manner similar to the 8085 upper address lines.
- $\overline{BHE}$ has no meaning on the 80C88 and has been eliminated.
- $\overline{SS0}$ provides the $\overline{S0}$ status information in the minimum mode. This output occurs on pin 34 in minimum mode only. DT/$\overline{R}$, IO/$\overline{M}$ and $\overline{SS0}$ provide the complete bus status in minimum mode.
- IO/$\overline{M}$ has been inverted to be compatible with the 8085 bus structure.
- ALE is delayed by one clock cycle in the minimum mode when entering HALT, to allow the status to be latched with ALE.

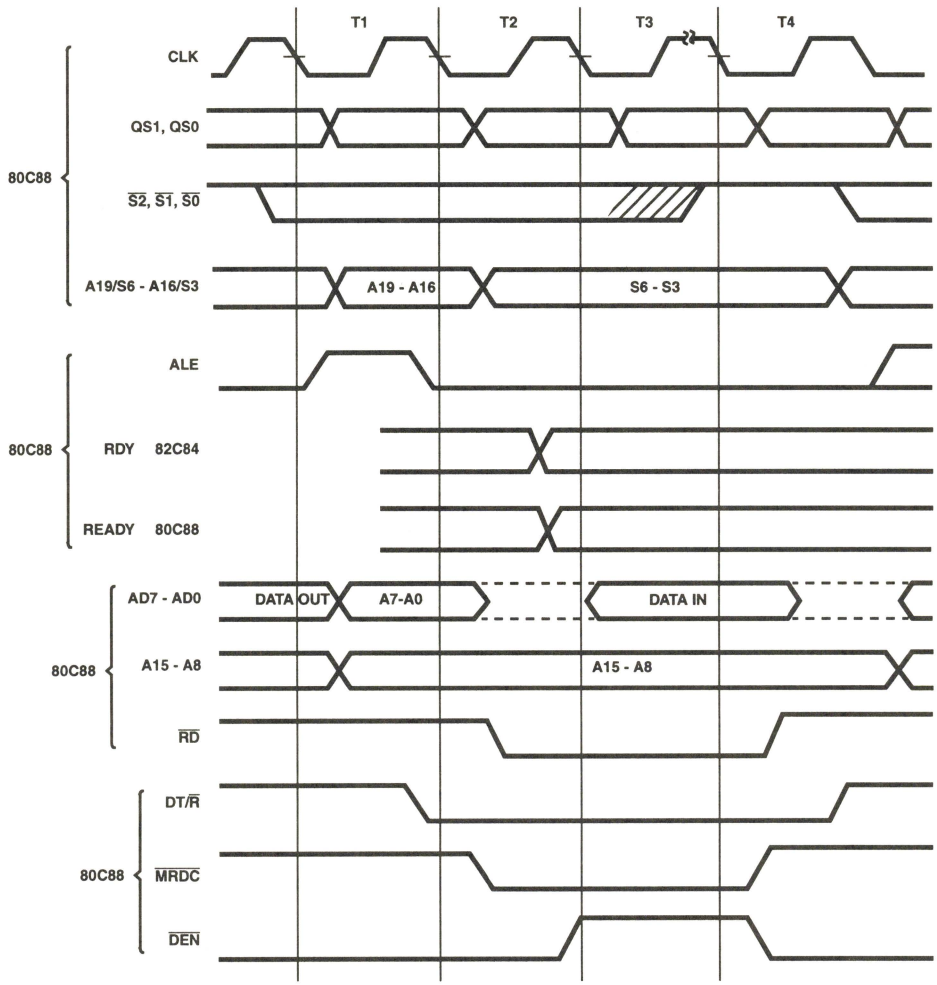


FIGURE 8. MEDIUM COMPLEXITY SYSTEM TIMING

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
M80C88-2 Only . . . . . +4.75V to +5.25V
Operating Temperature Range
C80C88/-2 . . . . . 0^oC to $+70^oC$
I80C88/-2 . . . . . -40^oC to $+85^oC$
M80C88/-2 . . . . . -55^oC to $+125^oC$

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	50	-
PLCC Package	46	-
SBDIP Package	30	N/A
CLCC Package	40	N/A

Maximum Junction Temperature
Ceramic Package . . . . . $+175^oC$
Plastic Package . . . . . $+150^oC$
Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$
(Lead tips only for surface mount packages)

Die Characteristics

Gate Count . . . . . 9750 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5.0V, ±10%; T_A = 0^oC to $+70^oC$ (C80C88, C80C88-2)
V_{CC} = 5.0V, ±10%; T_A = -40^oC to $+85^oC$ (I80C88, I80C88-2)
V_{CC} = 5.0V, ±10%; T_A = -55^oC to $+125^oC$ (M80C88)
V_{CC} = 5.0V, ±5%; T_A = -55^oC to $+125^oC$ (M80C88-2)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITION
V_{IH}	Logical One Input Voltage	2.0 2.2	-	V V	C80C88, I80C88 (Note 4) M80C88 (Note 4)
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
VIHC	CLK Logical One Input Voltage	V_{CC} -0.8	-	V	
VILC	CLK Logical Zero Input Voltage	-	0.8	V	
V_{OH}	Output High Voltage	3.0 V_{CC} -0.4	-	V V	IOH = -2.5mA IOH = -100µA
V_{OL}	Output Low Voltage	-	0.4	V	IOL = +2.5mA
I_I	Input Leakage Current	-1.0	1.0	µA	V_{IN} = 0V or V_{CC} Pins 17-19, 21-23, 33
IBHH	Input Current-Bus Hold High	-40	-400	µA	V_{IN} = - 3.0V (Note 1)
IBHL	Input Current-Bus Hold Low	40	400	µA	V_{IN} = - 0.8V (Note 2)
I_O	Output Leakage Current	-	-10.0	µA	V_{OUT} = 0V (Note 5)
ICCSB	Standby Power Supply Current	-	500	µA	V_{CC} = 5.5V (Note 3)
ICCOP	Operating Power Supply Current	-	10	mA/MHz	FREQ = Max, V_{IN} = V_{CC} or GND, Outputs Open

NOTES:

1. IBHH should be measured after raising V_{IN} to V_{CC} and then lowering to 3.0V on the following pins 2-16, 26-32, 34-39.
2. IBHL should be measured after lowering V_{IN} to GND and then raising to 0.8V on the following pins: 2-16, 35-39.
3. ICCSB tested during clock high time after HALT instruction executed. V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs unloaded.
4. MN/$\overline{MX}$ is a strap option and should be held to V_{CC} or GND.
5. IO should be measured by putting the pin in a high impedance state and then driving V_{OUT} to GND on the following pins: 26-29 and 32.

Capacitance T_A = 25^oC

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	25	pF	FREQ = 1MHz. All measurements are referenced to device GND
COUT	Output Capacitance	25	pF	FREQ = 1MHz. All measurements are referenced to device GND
CI/O	I/O Capacitance	25	pF	FREQ = 1MHz. All measurements are referenced to device GND

AC Electrical Specifications

V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C (C80C88, C80C88-2)
V_{CC} = 5.0V ±100%; T_A = -40°C to +85°C (I80C88, I80C88-2)
V_{CC} = 5.0V ±100%; T_A = -55°C to +125°C (M80C88)
V_{CC} = 5.0V ±5%; T_A = -55°C to +125°C (M80C88-2)

MINIMUM COMPLEXITY SYSTEM

SYMBOL		PARAMETER	80C88		80C88-2		UNITS	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS								
(1)	TCLCL	CLK Cycle Period	200	-	125	-	ns	
(2)	TCLCH	CLK Low Time	118	-	68	-	ns	
(3)	TCHCL	CLK High Time	69	-	44	-	ns	
(4)	TCH1CH2	CLK Rise Time	-	10	-	10	ns	From 1.0V to 3.5V
(5)	TCL2CL1	CLK Fall Time	-	10	-	10	ns	From 3.5V to 1.0V
(6)	TDVCL	Data In Setup Time	30	-	20	-	ns	
(7)	TCLDX1	Data In Hold Time	10	-	10	-	ns	
(8)	TR1VCL	RDY Setup Time into 82C84A (Notes 6, 7)	35	-	35	-	ns	
(9)	TCLR1X	RDY Hold Time into 82C84A (Notes 6, 7)	0	-	0	-	ns	
(10)	TRYHCH	READY Setup Time into 80C88	118	-	68	-	ns	
(11)	TCHRYX	READY Hold Time into 80C88	30	-	20	-	ns	
(12)	TRYLCL	READY Inactive to CLK (Note 8)	-8	-	-8	-	ns	
(13)	THVCH	HOLD Setup Time	35	-	20	-	ns	
(14)	TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (Note 7)	30	-	15	-	ns	
(15)	TILIH	Input Rise Time (Except CLK)	-	15	-	15	ns	From 0.8V to 2.0V
(16)	TIHIL	Input Fall Time (Except CLK)	-	15	-	15	ns	From 2.0V to 0.8V
TIMING RESPONSES								
(17)	TCLAV	Address Valid Delay	10	110	10	60	ns	CL = 100pF
(18)	TCLAX	Address Hold Time	10	-	10	-	ns	CL = 100pF
(19)	TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	CL = 100pF
(20)	TCHSZ	Status Float Delay	-	80	-	50	ns	CL = 100pF
(21)	TCHSV	Status Active Delay	10	110	10	60	ns	CL = 100pF
(22)	TLHLL	ALE Width	TCLCH-20	-	TCLCH-10	-	ns	CL = 100pF
(23)	TCLLH	ALE Active Delay	-	80	-	50	ns	CL = 100pF
(24)	TCHLL	ALE Inactive Delay	-	85	-	55	ns	CL = 100pF

AC Electrical Specifications

V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C (C80C88, C80C88-2)
V_{CC} = 5.0V ±100%; T_A = -40°C to +85°C (I80C88, I80C88-2)
V_{CC} = 5.0V ±100%; T_A = -55°C to +125°C (M80C88)
V_{CC} = 5.0V ±5%; T_A = -55°C to +125°C (M80C88-2) **(Continued)**

MINIMUM COMPLEXITY SYSTEM

SYMBOL		PARAMETER	80C88		80C88-2		UNITS	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
(25)	TLLAX	Address Hold Time to ALE Inactive	TCHCL-10	-	TCHCL-10	-	ns	CL = 100pF
(26)	TCLDV	Data Valid Delay	10	110	10	60	ns	CL = 100pF
(27)	TCLDX2	Data Hold Time	10	-	10	-	ns	CL = 100pF
(28)	TWHDX	Data Hold Time After $\overline{WR}$	TCLCL-30	-	TCLCL-30	-	ns	CL = 100pF
(29)	TCVCTV	Control Active Delay 1	10	110	10	70	ns	CL = 100pF
(30)	TCHCTV	Control Active Delay 2	10	110	10	60	ns	CL = 100pF
(31)	TCVCTX	Control Inactive Delay	10	110	10	70	ns	CL = 100pF
(32)	TAZRL	Address Float to READ Active	0	-	0	-	ns	CL = 100pF
(33)	TCLRL	$\overline{RD}$ Active Delay	10	165	10	100	ns	CL = 100pF
(34)	TCLRH	$\overline{RD}$ Inactive Delay	10	150	10	80	ns	CL = 100pF
(35)	TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL-45	-	TCLCL-40	-	ns	CL = 100pF
(36)	TCLHAV	HLDA Valid Delay	10	160	10	100	ns	CL = 100pF
(37)	TRLRH	$\overline{RD}$ Width	2TCLCL-75	-	2TCLCL-50	-	ns	CL = 100pF
(38)	TWLWH	$\overline{WR}$ Width	2TCLCL-60	-	2TCLCL-40	-	ns	CL = 100pF
(39)	TAVAL	Address Valid to ALE Low	TCLCH-60	-	TCLCH-40	-	ns	CL = 100pF
(40)	TOLOH	Output Rise Time	-	15	-	15	ns	From 0.8V to 2.0V
(41)	TOHOL	Output Fall Time	-	15	-	15	ns	From 2.0V to 0.8V

NOTES:

6. Signal at 82C84A shown for reference only.
7. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
8. Applies only to T2 state (8ns into T3).

Waveforms

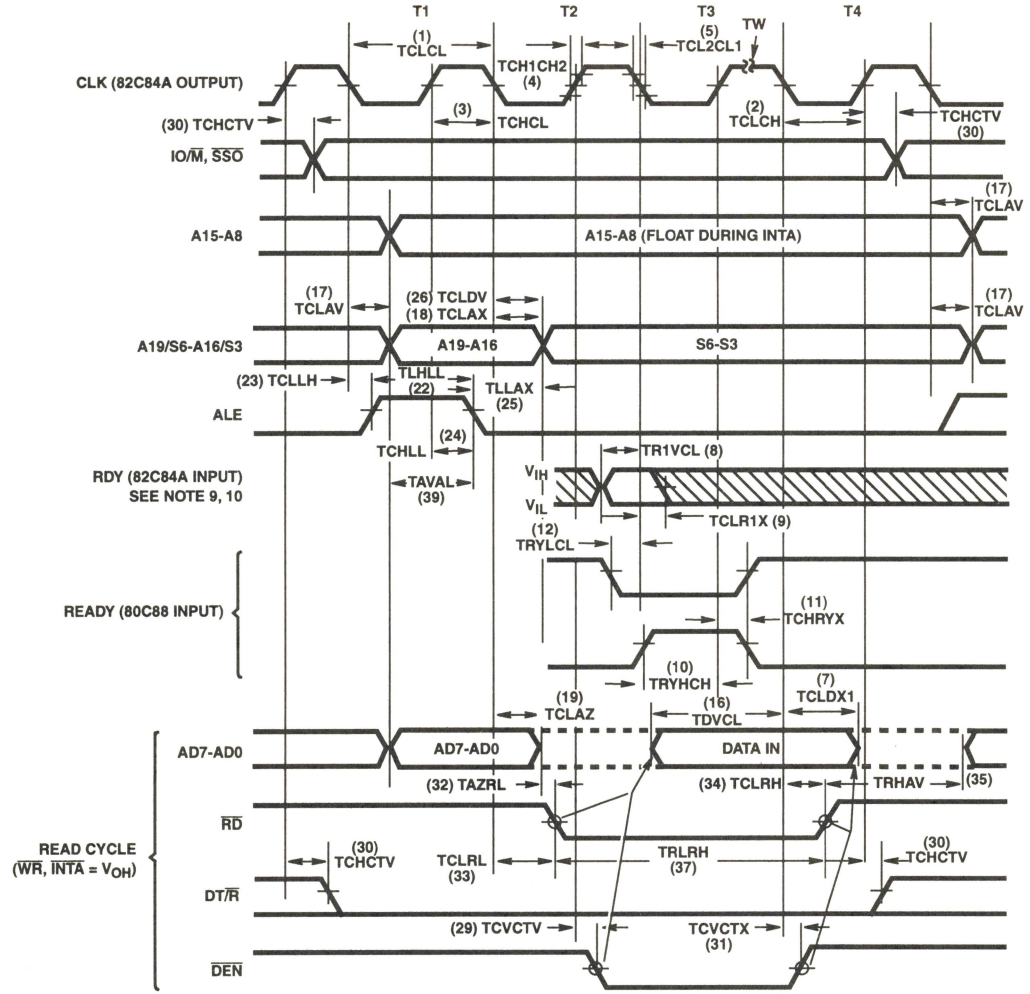


FIGURE 9. BUS TIMING - MINIMUM MODE SYSTEM

NOTES:

9. RDY is sampled near the end of T2, T3, TW to determine if TW machine states are to be inserted.
10. Signals at 82C84A are shown for reference only.

Waveforms (Continued)

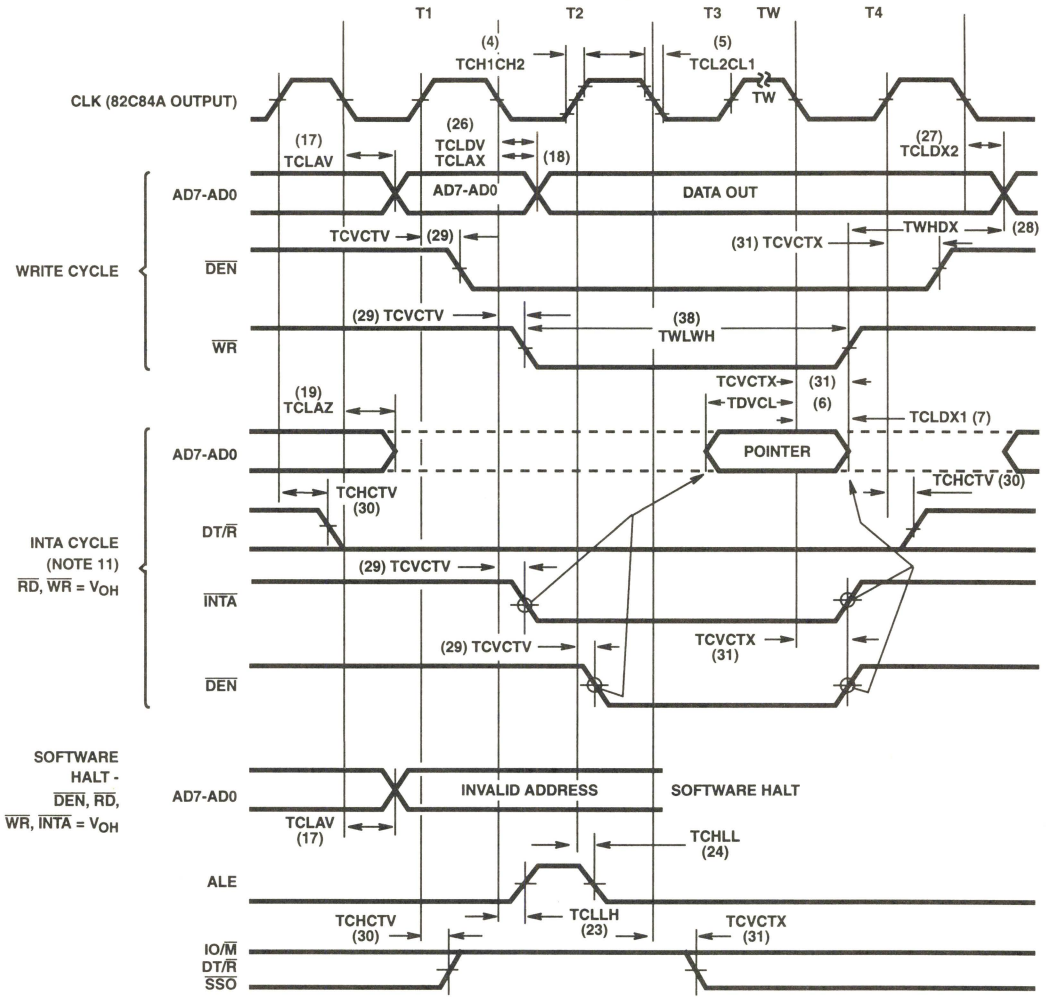


FIGURE 10. BUS TIMING - MINIMUM MODE SYSTEM (Continued)

NOTES:

11. Two $\overline{\text{INTA}}$ cycles run back-to-back. The 80C88 local ADDR/DATA bus is floating during both $\overline{\text{INTA}}$ cycles. Control signals are shown for the second $\overline{\text{INTA}}$ cycle.
12. Signals at 82C84A are shown for reference only.

AC Electrical Specifications

V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C (C80C88, C80C88-2)
V_{CC} = 5.0V ±10%; T_A = -40°C to +85°C (I80C88, I80C88-2)
V_{CC} = 5.0V ±10%; T_A = -55°C to +125°C (M80C88)
V_{CC} = 5.0V ±5%; T_A = -55°C to +125°C (M80C88-2)

MAX MODE SYSTEM (USING 82C88 BUS CONTROLLER)

SYMBOL		PARAMETER	80C88		80C88-2		UNITS	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS								
(1)	TCLCL	CLK Cycle Period	200	-	125	-	ns	
(2)	TCLCH	CLK Low Time	118	-	68	-	ns	
(3)	TCHCL	CLK High Time	69	-	44	-	ns	
(4)	TCH1CH2	CLK Rise Time	-	10	-	10	ns	From 1.0V to 3.5V
(5)	TCL2CL1	CLK Fall Time	-	10	-	10	ns	From 3.5V to 1.0V
(6)	TDVCL	Data in Setup Time	30	-	20	-	ns	
(7)	TCLDX1	Data In Hold Time	10	-	10	-	ns	
(8)	TR1VCL	RDY Setup Time into 82C84 (Notes 13, 14)	35	-	35	-	ns	
(9)	TCLR1X	RDY Hold Time into 82C84 (Notes 13, 14)	0	-	0	-	ns	
(10)	TRYHCH	READY Setup Time into 80C88	118	-	68	-	ns	
(11)	TCHRYX	READY Hold Time into 80C88	30	-	20	-	ns	
(12)	TRYLCL	READY Inactive to CLK (Note 15)	-8	-	-8	-	ns	
(13)	TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{TEST}$) (Note 14)	30	-	15	-	ns	
(14)	TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time	30	-	15	-	ns	
(15)	TCHGX	$\overline{RQ}$ Hold Time into 80C88 (Note 16)	40	TCHCL+ 10	30	TCHCL+ 10	ns	
(16)	TILIH	Input Rise Time (Except CLK)	-	15	-	15	ns	From 0.8V to 2.0V
(17)	TIHIL	Input Fall Time (Except CLK)	-	15	-	15	ns	From 2.0V to 0.8V
TIMING RESPONSES								
(18)	TCLML	Command Active Delay (Note 13)	5	35	5	35	ns	CL = 100pF for all 80C88 outputs in addition to internal loads.
(19)	TCLMH	Command Inactive (Note 13)	5	35	5	35	ns	
(20)	TRYHSH	READY Active to Status Passive (Notes 15, 17)	-	110	-	65	ns	
(21)	TCHSV	Status Active Delay	10	110	10	60	ns	
(22)	TCLSH	Status Inactive Delay (Note 17)	10	130	10	70	ns	
(23)	TCLAV	Address Valid Delay	10	110	10	60	ns	
(24)	TCLAX	Address Hold Time	10	-	10	-	ns	
(25)	TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
(26)	TCHSZ	Status Float Delay	-	80	-	50	ns	
(27)	TSVLH	Status Valid to ALE High (Note 13)	-	20	-	20	ns	
(28)	TSVMCH	Status Valid to MCE High (Note 13)	-	30	-	30	ns	
(29)	TCLLH	CLK Low to ALE Valid (Note 13)	-	20	-	20	ns	
(30)	TCLMCH	CLK Low to MCE High (Note 13)	-	25	-	25	ns	
(31)	TCHLL	ALE Inactive Delay (Note 13)	4	18	4	18	ns	

AC Electrical Specifications

V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C (C80C88, C80C88-2)
V_{CC} = 5.0V ±10%; T_A = -40°C to +85°C (I80C88, I80C88-2)
V_{CC} = 5.0V ±10%; T_A = -55°C to +125°C (M80C88)
V_{CC} = 5.0V ±5%; T_A = -55°C to +125°C (M80C88-2) **(Continued)**

MAX MODE SYSTEM (USING 82C88 BUS CONTROLLER)

SYMBOL		PARAMETER	80C88		80C88-2		UNITS	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
(32)	TCLMCL	MCE Inactive Delay (Note 13)	-	15	-	15	ns	CL = 100pF for all 80C88 outputs in addition to internal loads.
(33)	TCLDV	Data Valid Delay	10	110	10	60	ns	
(34)	TCLDX2	Data Hold Time	10	-	10	-	ns	
(35)	TCVNV	Control Active Delay (Note 13)	5	45	5	45	ns	
(36)	TCVNX	Control Inactive Delay (Note 13)	10	45	10	45	ns	
(37)	TAZRL	Address Float to Read Active	0	-	0	-	ns	
(38)	TCLRL	$\overline{RD}$ Active Delay	10	165	10	100	ns	
(39)	TCLRH	$\overline{RD}$ Inactive Delay	10	150	10	80	ns	
(40)	TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL -45	-	TCLCL -40	-	ns	
(41)	TCHDTL	Direction Control Active Delay (Note 13)	-	50	-	50	ns	
(42)	TCHDTH	Direction Control Inactive Delay (Note 1)	-	30	-	30	ns	
(43)	TCLGL	$\overline{GT}$ Active Delay	0	85	0	50	ns	
(44)	TCLGH	$\overline{GT}$ Inactive Delay	0	85	0	50	ns	
(45)	TRLRH	$\overline{RD}$ Width	2TCLCL -75	-	2TCLCL -50	-	ns	
(46)	TOLOH	Output Rise Time	-	15	-	15	ns	From 0.8V to 2.0V
(47)	TOHOL	Output Fall Time	-	15	-	15	ns	From 2.0V to 0.8V

NOTES:

13. Signal at 82C84A or 82C88 shown for reference only.
14. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
15. Applies only to T2 state (8ns into T3).
16. The 80C88 actively pulls the $\overline{RQ}/\overline{GT}$ pin to a logic one on the following clock low time.
17. Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

Waveforms

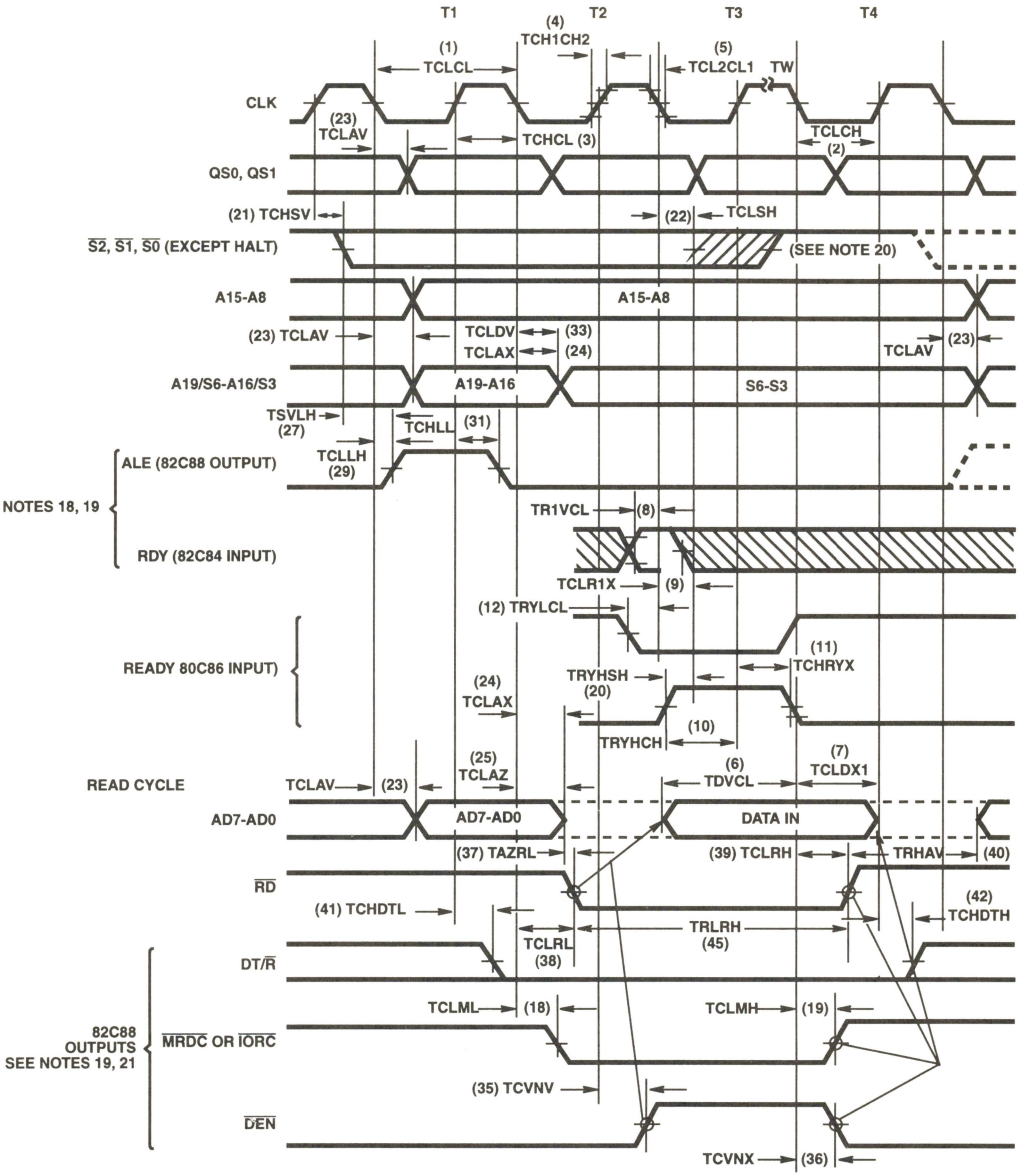


FIGURE 11. BUS TIMING - MAXIMUM MODE (USING 82C88)

NOTES:

18. RDY is sampled near the end of T2, T3, TW to determine if TW machine states are to be inserted.
19. Signals at 82C84A or 82C88 are shown for reference only.
20. Status inactive in state just prior to T4.
21. The issuance of the 82C88 command and control signals ($\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$, and $\overline{\text{DEN}}$) lags the active high 82C88 CEN.

Waveforms (Continued)

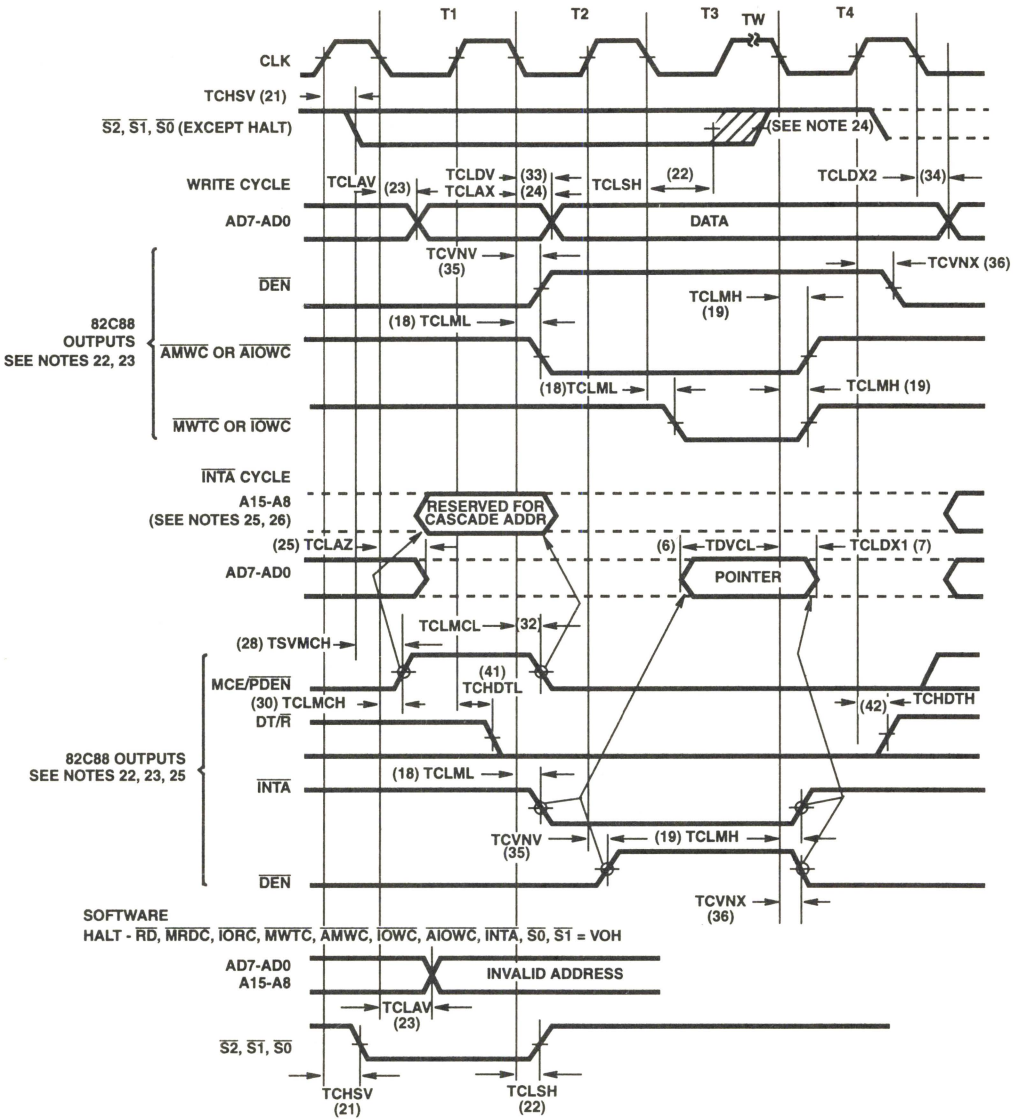


FIGURE 12. BUS TIMING - MAXIMUM MODE SYSTEM (USING 82C88) (Continued)

NOTES:

22. Signals at 82C84A or 82C86 are shown for reference only.
23. The issuance of the 82C88 command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ and $\overline{DEN}$) lags the active high 82C88 CEN.
24. Status inactive in state just prior to T4.
25. Cascade address is valid between first and second $\overline{INTA}$ cycles.
26. Two $\overline{INTA}$ cycles run back-to-back. The 80C88 local ADDR/DATA bus is floating during both $\overline{INTA}$ cycles. Control for pointer address is shown for second $\overline{INTA}$ cycle.

Waveforms (Continued)

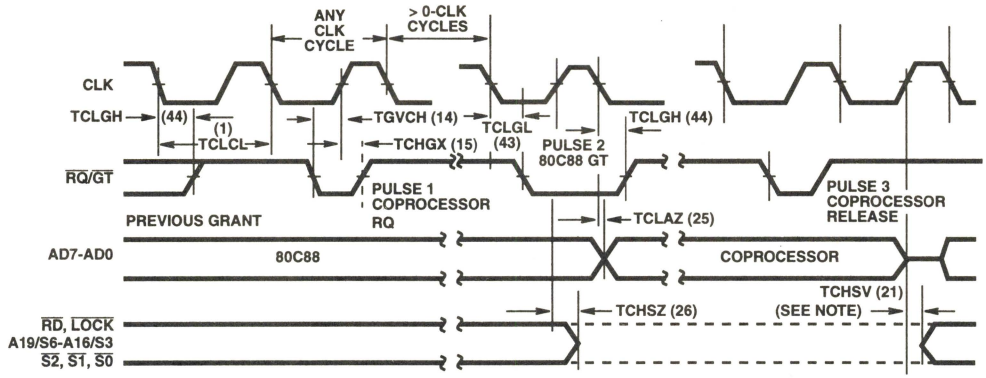


FIGURE 13. REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)

NOTE: The coprocessor may not drive the busses outside the region shown without risking contention.

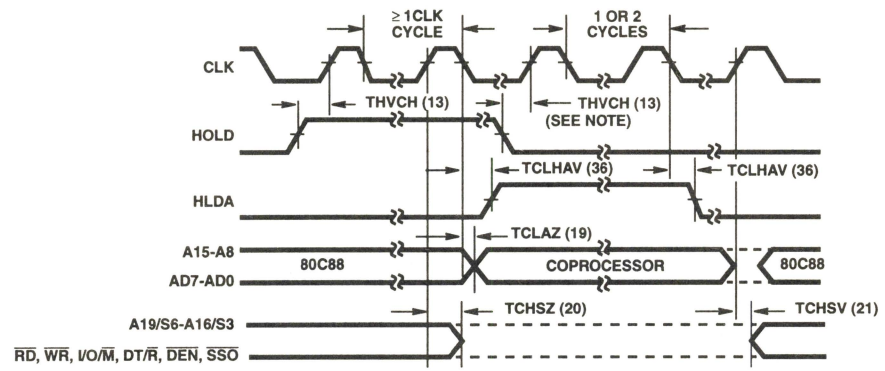


FIGURE 14. HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)

NOTE: Setup requirements for asynchronous signals only to guarantee recognition at next CLK.

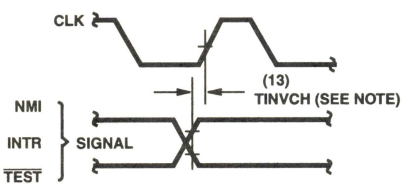


FIGURE 15. ASYNCHRONOUS SIGNAL RECOGNITION

NOTE: Setup requirements for asynchronous signals only to guarantee recognition at next CLK.

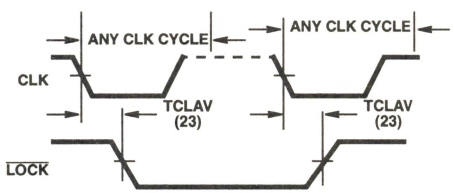


FIGURE 16. BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)

Waveforms (Continued)

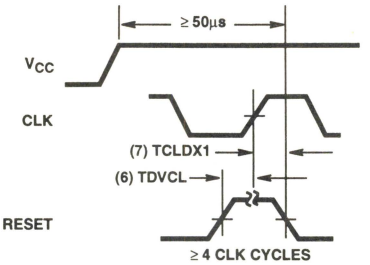
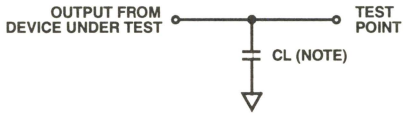


FIGURE 17. RESET TIMING

AC Test Circuit



NOTE: Includes stay and jig capacitance.

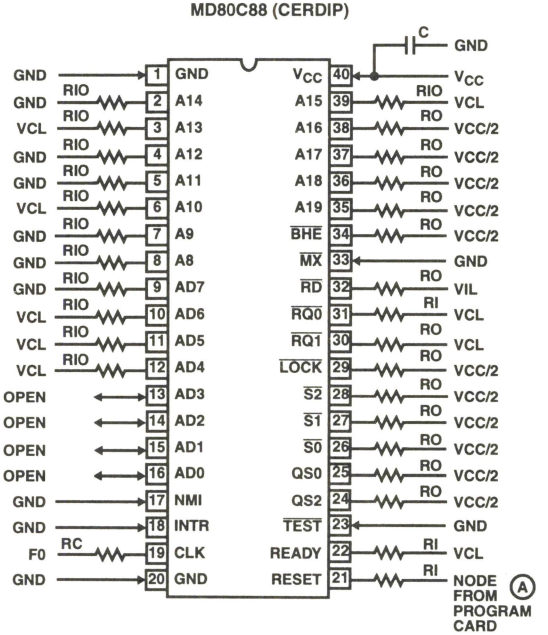
AC Testing Input, Output Waveform



AC Testing: All input signals (other than CLK) must switch between V_{ILMAX} -50% V_{IL} and V_{IHMIN} +20% V_{IH}. CLK must switch between 0.4V and V_{CC} -0.4V. Input rise and fall times are driven at 1ns/V.

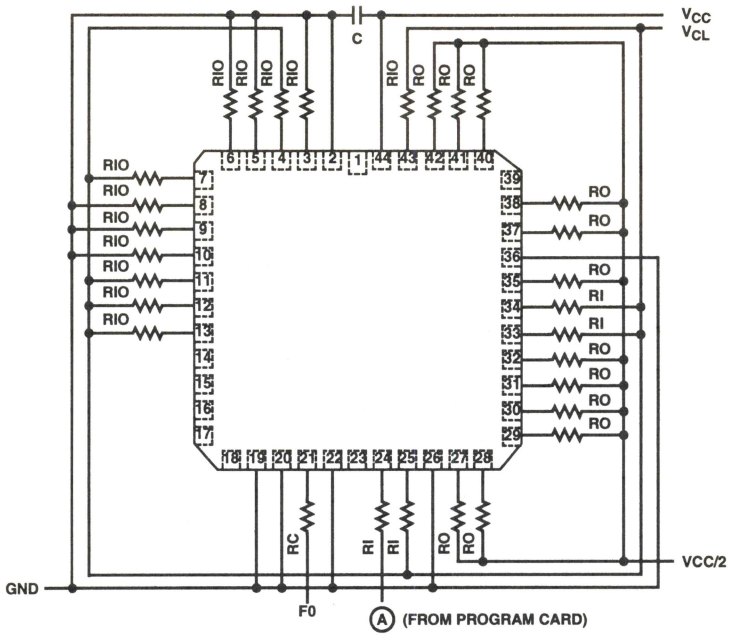
Burn-In Circuits

MD80C88 (CERDIP)



Burn-In Circuits (Continued)

MR80C88 (CLCC)



NOTES:

1. V_{CC} = 5.5V ±0.5V, GND = 0V.
2. Input voltage limits (except clock):
   V_{IL} (Maximum) = 0.4V
   V_{IH} (Minimum) = 2.6V, V_{IH} (Clock) = V_{CC} - 0.4V) minimum.
3. VCC/2 is external supply set to 2.7V ±10%.
4. V_{CL} is generated on program card (V_{CC} - 0.65V).
5. Pins 13 - 16 input sequenced instructions from internal hold devices, (DIP Only).
6. F0 = 100kHz ±10%.
7. Node (A) = a 40µs pulse every 2.56ms.

COMPONENTS:

1. RI = 10kΩ ±5%, 1/4W
2. RO = 1.2kΩ ±5%, 1/4W
3. RIO = 2.7kΩ ±5%, 1/4W
4. RC = 1kΩ ±5%, 1/4W
5. C = 0.01µF (Minimum)

Die Characteristics

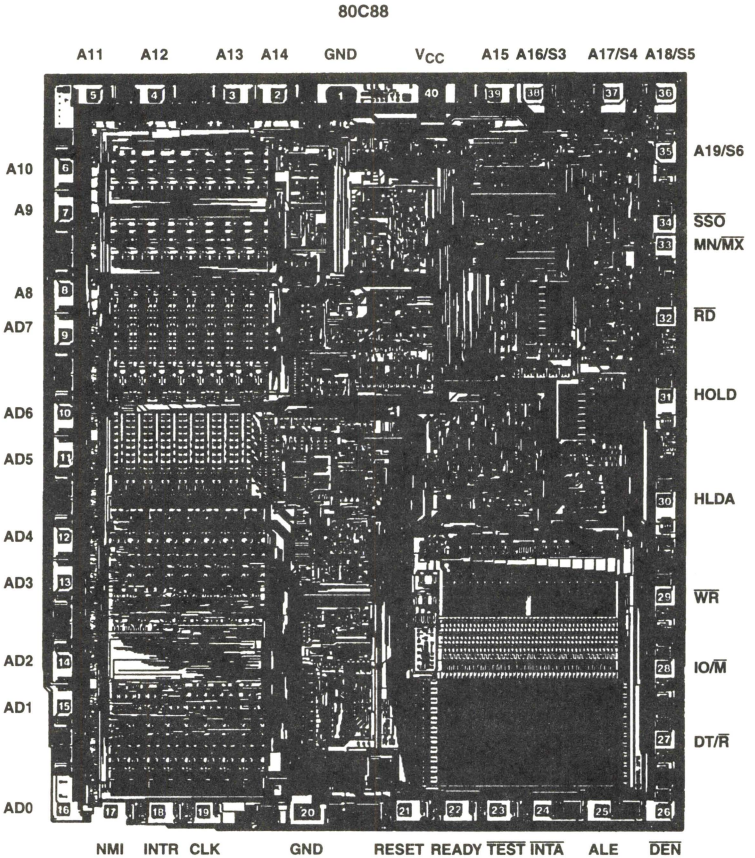
DIE DIMENSIONS:
249.2 x 290.9 x 19 ±1mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
1.5 x 10^5 A/cm^2

Metallization Mask Layout



Instruction Set Summary

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	76543210	76543210	76543210	76543210
DATA TRANSFER				
MOV = MOVE:				
Register/Memory to/from Register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to Register/Memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w 1
Immediate to Register	1 0 1 1 w reg	data	data if w 1	
Memory to Accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	
Accumulator to Memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
Register/Memory to Segment Register ††	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment Register to Register/Memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		
PUSH = Push:				
Register/Memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m		
Register	0 1 0 1 0 reg			
Segment Register	0 0 0 reg 1 1 0			
POP = Pop:				
Register/Memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m		
Register	0 1 0 1 1 reg			
Segment Register	0 0 0 reg 1 1 1			
XCHG = Exchange:				
Register/Memory with Register	1 0 0 0 0 1 1 w	mod reg r/m		
Register with Accumulator	1 0 0 1 0 reg			
IN = Input from:				
Fixed Port	1 1 1 0 0 1 0 w	port		
Variable Port	1 1 1 0 1 1 0 w			
OUT = Output to:				
Fixed Port	1 1 1 0 0 1 1 w	port		
Variable Port	1 1 1 0 1 1 1 w			
XLAT = Translate Byte to AL	1 1 0 1 0 1 1 1			
LEA = Load EA to Register2	1 0 0 0 1 1 0 1	mod reg r/m		
LDS = Load Pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m		
LES = Load Pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m		
LAHF = Load AH with Flags	1 0 0 1 1 1 1 1			
SAHF = Store AH into Flags	1 0 0 1 1 1 1 0			
PUSHF = Push Flags	1 0 0 1 1 1 0 0			
POPF = Pop Flags	1 0 0 1 1 1 0 1			
ARITHMETIC				
ADD = Add:				
Register/Memory with Register to Either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to Register/Memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s:w = 01
Immediate to Accumulator	0 0 0 0 0 1 0 w	data	data if w = 1	
ADC = Add with Carry:				
Register/Memory with Register to Either	0 0 0 1 0 0 d w	mod reg r/m		

Instruction Set Summary (Continued)

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	76543210	76543210	76543210	76543210
Immediate to Register/Memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s:w = 01
Immediate to Accumulator	0 0 0 1 0 1 0 w	data	data if w = 1	
INC = Increment:				
Register/Memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m		
Register	0 1 0 0 0 reg			
AAA = ASCII Adjust for Add	0 0 1 1 0 1 1 1			
DAA = Decimal Adjust for Add	0 0 1 0 0 1 1 1			
SUB = Subtract:				
Register/Memory and Register to Either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from Register/Memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s:w = 01
Immediate from Accumulator	0 0 1 0 1 1 0 w	data	data if w = 1	
SBB = Subtract with Borrow				
Register/Memory and Register to Either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from Register/Memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s:w = 01
Immediate from Accumulator	0 0 0 1 1 1 0 w	data	data if w = 1	
DEC = Decrement:				
Register/Memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m		
Register	0 1 0 0 1 reg			
NEG = Change Sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m		
CMP = Compare:				
Register/Memory and Register	0 0 1 1 1 0 d w	mod reg r/m		
Immediate with Register/Memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s:w = 01
Immediate with Accumulator	0 0 1 1 1 1 0 w	data	data if w = 1	
AAS = ASCII Adjust for Subtract	0 0 1 1 1 1 1 1			
DAS = Decimal Adjust for Subtract	0 0 1 0 1 1 1 1			
MUL = Multiply (Unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
IMUL = Integer Multiply (Signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
AAM = ASCII Adjust for Multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
DIV = Divide (Unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
IDIV = Integer Divide (Signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
AAD = ASCII Adjust for Divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
CBW = Convert Byte to Word	1 0 0 1 1 0 0 0			
CWD = Convert Word to Double Word	1 0 0 1 1 0 0 1			
LOGIC				
NOT = Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m		
SHL/SAL = Shift Logical/Arithmetic Left	1 1 0 1 0 0 v w	mod 1 0 0 r/m		
SHR = Shift Logical Right	1 1 0 1 0 0 v w	mod 1 0 1 r/m		
SAR = Shift Arithmetic Right	1 1 0 1 0 0 v w	mod 1 1 1 r/m		
ROL = Rotate Left	1 1 0 1 0 0 v w	mod 0 0 0 r/m		
ROR = Rotate Right	1 1 0 1 0 0 v w	mod 0 0 1 r/m		
RCL = Rotate Through Carry Flag Left	1 1 0 1 0 0 v w	mod 0 1 0 r/m		

Instruction Set Summary (Continued)

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	76543210	76543210	76543210	76543210
RCR = Rotate Through Carry Right	1 1 0 1 0 0 v w	mod 0 1 1 r/m		
AND = And:				
Reg./Memory and Register to Either	0 0 1 0 0 0 0 d w	mod reg r/m		
Immediate to Register/Memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w = 1
Immediate to Accumulator	0 0 1 0 0 1 0 w	data	data if w = 1	
TEST = And Function to Flags, No Result:				
Register/Memory and Register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate Data and Register/Memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w = 1
Immediate Data and Accumulator	1 0 1 0 1 0 0 w	data	data if w = 1	
OR = Or:				
Register/Memory and Register to Either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to Register/Memory	1 0 0 0 0 0 0 w	mod 1 0 1 r/m	data	data if w = 1
Immediate to Accumulator	0 0 0 0 1 1 0 w	data	data if w = 1	
XOR = Exclusive or:				
Register/Memory and Register to Either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to Register/Memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w = 1
Immediate to Accumulator	0 0 1 1 0 1 0 w	data	data if w = 1	
STRING MANIPULATION				
REP = Repeat	1 1 1 1 0 0 1 z			
MOVS = Move Byte/Word	1 0 1 0 0 1 0 w			
CMPS = Compare Byte/Word	1 0 1 0 0 1 1 w			
SCAS = Scan Byte/Word	1 0 1 0 1 1 1 w			
LODS = Load Byte/Word to AL/AX	1 0 1 0 1 1 0 w			
STOS = Stor Byte/Word from AL/A	1 0 1 0 1 0 1 w			
CONTROL TRANSFER				
CALL = Call:				
Direct Within Segment	1 1 1 0 1 0 0 0	disp-low	disp-high	
Indirect Within Segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m		
Direct Intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high	
		seg-low	seg-high	
Indirect Intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m		
JMP = Unconditional Jump:				
Direct Within Segment	1 1 1 0 1 0 0 1	disp-low	disp-high	
Direct Within Segment-Short	1 1 1 0 1 0 1 1	disp		
Indirect Within Segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m		
Direct Intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high	
		seg-low	seg-high	
Indirect Intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m		
RET = Return from CALL:				
Within Segment	1 1 0 0 0 0 1 1			
Within Seg Adding Immed to SP	1 1 0 0 0 0 1 0	data-low	data-high	

Instruction Set Summary (Continued)

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	76543210	76543210	76543210	76543210
Intersegment	11001011			
Intersegment Adding Immediate to SP	11001010	data-low	data-high	
JE/JZ = Jump on Equal/Zero	01110100	disp		
JL/JNGE = Jump on Less/Not Greater or Equal	01111100	disp		
JLE/JNG = Jump on Less or Equal/ Not Greater	01111110	disp		
JB/JNAE = Jump on Below/Not Above or Equal	01110010	disp		
JBE/JNA = Jump on Below or Equal/Not Above	01110110	disp		
JP/JPE = Jump on Parity/Parity Even	01111010	disp		
JO = Jump on Overflow	01110000	disp		
JS = Jump on Sign	01111000	disp		
JNE/JNZ = Jump on Not Equal/Not Zero	01110101	disp		
JNL/JGE = Jump on Not Less/Greater or Equal	01111101	disp		
JNLE/JG = Jump on Not Less or Equal/Greater	01111111	disp		
JNB/JAE = Jump on Not Below/Above or Equal	01110011	disp		
JNBE/JA = Jump on Not Below or Equal/Above	01110111	disp		
JNP/JPO = Jump on Not Par/Par Odd	01111011	disp		
JNO = Jump on Not Overflow	01110001	disp		
JNS = Jump on Not Sign	01111001	disp		
LOOP = Loop CX Times	11100010	disp		
LOOPZ/LOOPE = Loop While Zero/Equal	11100001	disp		
LOOPNZ/LOOPNE = Loop While Not Zero/Equal	11100000	disp		
JCXZ = Jump on CX Zero	11100011	disp		
INT = Interrupt				
Type Specified	11001101	type		
Type 3	11001100			
INTO = Interrupt on Overflow	11001110			
IRET = Interrupt Return	11001111			
PROCESSOR CONTROL				
CLC = Clear Carry	11111000			
CMC = Complement Carry	11110101			
STC = Set Carry	11111001			
CLD = Clear Direction	11111100			
STD = Set Direction	11111101			
CLI = Clear Interrupt	11111010			
ST = Set Interrupt	11111011			
HLT = Halt	11110100			
WAIT = Wait	10011011			
ESC = Escape (to External Device)	11011xxx	mod x x r/m		
LOCK = Bus Lock Prefix	11110000			

Instruction Set Summary (Continued)

MNEMONIC AND DESCRIPTION	INSTRUCTION CODE			
	76543210	76543210	76543210	76543210

NOTES:
AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS= Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction
if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0†, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high:disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP †
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)
† except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.
†† MOV CS, REG/MEMORY not allowed.

if s:w = 01 then 16-bits of immediate data form the operand.
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1; if v = 1 then "count" in (C_L)
x = don't care
z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

001 reg 11 0

REG is assigned according to the following table:

16-BIT (w = 1)	8-BIT (w = 0)	SEGMENT
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS =

X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Mnemonics © Intel, 1978

MICROPROCESSOR PRODUCTS 4

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CDP1800-Series CMOS Peripherals Can Be Used with CMOS and NMOS Processors

RCA I/O TYPE	DESCRIPTION AND FUNCTION	RCA	MICROPROCESSOR BUS					INPUT LEVELS	(NOTE 2) FANOUT (TTL LOADS)
			MULTIPLEXED			NONMULTIPLEXED			
			RCA/ MOTOR-OLA	INTEL	INTEL/ NSC	ZILOG	ROCK-WELL		
		1800 SERIES	68HC05 6805	8048, 8051 80C48, 80C51 8049, 80C49 8088	8085 80C85 NSC800	Z80	6502 65C02		
I/O PORTS									
CDP1851	Programmable I/O Port	Yes	Note 1	Note 1	Note 1	Yes	Yes	CMOS	1
CDP1852	Byte-Wide I/O Port	Yes	Yes	Yes	Yes	Yes	Yes	CMOS	1
CDP1857	4-Bit Bus Buffer/ Separator	Yes	Yes	Yes	Yes	Yes	Yes	CMOS	1
CDP1872	8-Bit Input Port	Yes	Yes	Yes	Yes	Yes	Yes	CMOS	3
CDP1874	8-Bit Input Port	Yes	Yes	Yes	Yes	Yes	Yes	CMOS	3
CDP1875	8-Bit Input Port	Yes	Yes	Yes	Yes	Yes	Yes	CMOS	3
MEMORY I/O DECODERS									
CDP1853	N-Bit 1 of 8 Decoder	Yes	Yes	Yes	Yes	Yes	Yes	CMOS	1
CDP1881	6-Bit Latch/Decoder	Yes	Yes	Yes	Yes	Yes	Yes	CMOS	1
CDP1882	6-Bit Latch/Decoder	Yes	Yes	Yes	Yes	Yes	Yes	CMOS	1
CDP1883	7-Bit Latch/Decoder	Yes	Yes	Yes	Yes	Yes	Yes	CMOS	1
SERIAL I/O									
CDP1854A (Note 3)	UART	Yes	Note 1	Note 1	Note 1	Note 1	Note 1	CMOS	1
CDP6402	UART	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	CMOS	1
MULTIPLY/DIVIDE									
CDP1855	8-Bit Programmable MDU	Yes	Note 1	Note 1	Note 1	Note 1	Note 1	CMOS	1
KEYBOARD INTERFACE									
CDP1871A	Keyboard Encoder	Yes	Note 1	Note 1	Note 1	Note 1	Note 1	CMOS	
TIMER FUNCTIONS									
CDP1878	Dual Counter-Timer	Yes	Note 1	Note 1	Note 1	Yes	Yes	CMOS	1
CDP1879	Real-Time Clock	Yes	Use 6818, A	Use 6818, A	Use 6818, A	Yes	Yes	CMOS	1
INTERRUPT CONTROL									
CDP1877	Programmable Interrupt Controller	Yes	No	No	No	No	No	CMOS	1

NOTES:

1. Yes but requires additional "glue parts".
2. 1 TTL load, i.e., ≤ 0.4V at 1.6mA
3. Operating in 1800 compatible mode (mode 1). Otherwise see CDP6402 for mode 0 information.

80CXXX Family Peripheral Cross Reference

HARRIS	INTEL	NEC	OKI	MITSUBISHI	VLSI	OTHER
PERIPHERALS						
82C37A-5	82C37A-5	µPD71037 µPD8237A-5	MSM82C37A-5	M5M82C37A-4, -5	VL82C37A-4 VL82C37A-5	TMP82C37A-5 CA82C37A-5
82C37A 82C237			MSM82C37A		VL82C37A-8	KS82C37A SMC82C37A
82C37A-12 82C237-12						
82C54	82C54	µPD71054	MSM82C54	M5M82C54-6 M5M82C54	VL82C54-8	AM82C54 KS82C54 CA82C54 TMP82C54
82C54-10	82C54-2		MSM82C54-2			AM82C54-2 KS82C54-10 TMP82C54-2
82C54-12						
82C55A-5		µPD82C55A-5	MSM82C55A-5	M5M82C55A-5		
82C55A	82C55A-2	µPD71055 µPD8255A-2	MSM82C55A-2			AM82C55A KS82C55A CA82C55A UM82C55A
82C59A-5				M5M82C59A		
82C59A	82C59A-2	µPD71059 µPD8259A	MSM82C59-2		VL82C59A-8	AM82C59A-2 CA82C59A KS82C59A TMP82C59A
82C59A-12						
UARTS						
82C50A					VL82C50A	INS82C50A CA82C50A WD82C50A KS82C50A
82C52						CA82C52 KS82C52
BUS SUPPORT						
82C284-10	82C284-10					KS82C284-10
82C284-12	82C284-12					KS82C284-12
82C82		µPD71082				
82C83H		µPD71083				
82C84A	82C84A 82C84A-5	µPD71084	MSM82C84A MSM82C84A-5 MSM82C84A-2		VL82C84A-8	CA82C84A KS82C84A
82C85						
82C86H		µPD71086				MMI82C86
82C87H		µPD71087				MMI82C87
82C88	82C88	µPD71088 µPD8288	MSM82C88 MSM82C88-2		VL82C88-8	CA82C88 KS82C88

CDP1851, CDP1851C

March 1997

CMOS Programmable I/O Interface

Features

- 20 Programmable I/O Lines
- Programmable for Operation in Four Modes:
  - Input
  - Output
  - Bidirectional
  - Bit-programmable
- Operates in Either I/O or Memory Space

Ordering Information

PACKAGE	TEMP. RANGE	5V	10V	PKG. NO.
PDIP	-40°C to +85°C	CDP1851CE	CDP1851E	E40.6
Burn-In		CDP1851CEX	-	E40.6
SBDIP	-40°C to +85°C	CDP1851CD	-	D40.6
Burn-In		CDP1851CDX	CDP1851DX	D40.6

Description

THE CDP1851 and CDP1851C are CMOS programmable two-port I/Os designed for use as general-purpose I/O devices. They are directly compatible with CDP1800-series microprocessors functioning at maximum clock frequency. Each port can be programmed in either byte-I/O or bit-programmable modes for interfacing with peripheral devices such as printers and keyboards.

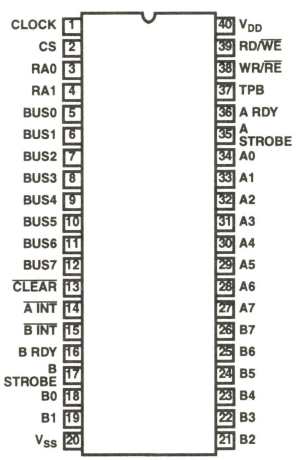
Both ports A and B can be separately programmed to be 8-bit input or output ports with handshaking control lines, RDY and STROBE. Only port A can be programmed to be a bidirectional port. This configuration provides a means for communicating with a peripheral device or microprocessor system on a single 8-bit bus for both transmitting and receiving data. Handshaking signals are provided to maintain proper bus access control. Port A handshaking lines are used for input control and port B handshaking lines are used for output; therefore port B must be in the bit-programmable mode where handshaking is not used.

Ports A and B can be separately bit programmed so that each individual line can be designated as an input or output line. The handshaking lines may also be individually programmed as input or output when port A is not in bidirectional mode.

The CDP1851 has a supply-voltage range of 4V to 10.5V, and the CDP1851C has a range of 4V to 6.5V. Both types are supplied in 40-lead dual-in-line plastic (E suffix) or hermetic ceramic (D suffix) packages. The CDP1851C is also available in chip form (H suffix).

Pinout

CDP1851, CDP1851C
(PDIP, SBDIP)
TOP VIEW



CDP1851 Programming Modes

MODE	(8) PORT A DATA PINS	(2) PORT A HANDSHAKING PINS	(8) PORT B DATA PINS	(2) PORT B HANDSHAKING PINS
Input	Accept Input Data	READY, STROBE	Accept Input Data	READY, STROBE
Output	Output Data	READY, STROBE	Output Data	READY, STROBE
Bidirectional (Port A Only)	Transfer Input/Output Data	Input Handshaking for Port A	Must be Previously Set to Bit-Programmable Mode	Output Handshaking for Port A
Bit-Programmable	Programmed Individually as Inputs or Outputs	Programmed Individually as Inputs or Outputs	Programmed Individually as Inputs or Outputs	Programmed Individually as Inputs or Outputs

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Absolute Maximum Ratings

DC Supply-Voltage Range, (V_{DD})
(Voltage Referenced to V_{SS} Terminal)
CDP1851 . . . . . -0.5 to+11V
CDP1851C . . . . . -0.5 to +7V
Input Voltage Range, All Inputs . . . . . -0.5 to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA
Device Dissipation Per Output Transistor
For T_A = Full Package-Temperature Range
(All Package Type) 40mW
Operating-Temperature Range (T_A)
Package Type D, H . . . . . -55°C to +125°C
Package Type E . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	50	N/A
SBDIP Package	36	12

Maximum Storage Temperature Range (T_{STG}) . . . . -65°C to +150°C
Maximum Lead Temperature (During Soldering)
At Distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from Case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Operating Conditions

At T_A = Full Package-Temperature Range. For Maximum Reliability, Operating Conditions Should be Selected so that Operation is Always within the Following Ranges:

PARAMETER	LIMITS				UNITS
	CDP1851		CDP1851C		
	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Functional Diagram

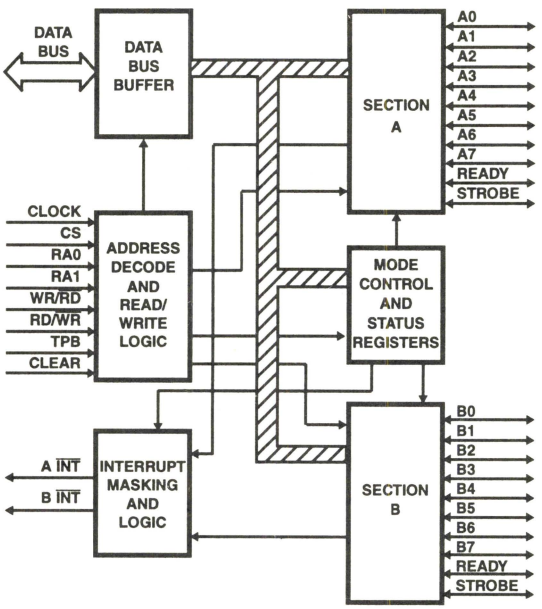


FIGURE 1. FUNCTIONAL DIAGRAM FOR CDP1851 AND CDP1851C

Static Electrical Specifications At T_A = -40°C to +85°C, V_{DD} 5%, Unless Otherwise Specified

PARAMETER		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS CDP1851 MIN	LIMITS CDP1851 (NOTE1) TYP	LIMITS CDP1851 MAX	LIMITS CDP1851C MIN	LIMITS CDP1851C (NOTE1) TYP	LIMITS CDP1851C MAX	UNITS
Quiescent Device Current	I_{DD}	-	0, 5	5	-	0.01	50	-	0.02	200	µA
		-	0, 10	10	-	1	200	-	-	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	-	1.6	3.2	-	mA
		0.5	0, 10	10	2.6	5.2	-	-	-	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	-	-1.15	-2.3	-	mA
		9.5	0, 10	10	-2.6	-5.2	-	-	-	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 9.5	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	-	±1	-	-	±1	µA
			0, 10	10	-	-	±2	-	-	-	µA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	-	±1	-	-	±1	µA
		0, 10	0, 10	10	-	-	±1	-	-	-	µA
Operating Current (Note 3)	I_{DD1}	-	0, 5	5	-	1.5	3	-	1.5	3	mA
		-	0, 10	10	-	6	12	-	-	-	mA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = 25°C and nominal V_{DD}.
2. $I_{OL} = I_{OH}$ = 1µA
3. Operating current is measured at 200kHz for V_{DD} = 5V and 400kHz for V_{DD} = 10V, with open output (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2MHz).

Functional Description

The CDP1851 has four modes of operation: input, output, bidirectional, and bit-programmable. Port A is programmable in all modes; port B is programmable in all but the bidirectional mode. A control byte must be loaded into the control register to program the ports. In the input and output modes, each port has two handshaking signals, STROBE and RDY. In the bidirectional mode, port A has four handshaking signals: A RDY and A STROBE for input, B RDY and B STROBE for output. If port A is programmed in the bidirectional mode, port B must be programmed in the bit-programmable mode. Each terminal of port A or B may be individually programmed for input or output in the bit-programmable mode. Since handshaking is not used in this mode, the RDY and STROBE lines may also be used for bit-programming if port A is not in the bidirectional mode.

Input Mode

When a peripheral device has data to input, it sends a STROBE pulse to the PIO. The leading edge of this pulse clears the RDY line, inhibiting further transmission from the peripheral. The trailing edge of the STROBE pulse latches the data into the PIO buffer register and also activates the INT line to signal the CPU to read this data. The INT pin can be wired to the INT pin of the CPU or the EF lines for polling. The CPU

then executes an input or a load instruction, depending on the mapping technique used. In either case the proper code must be asserted on the RAO, RA1, and CS lines to read the buffer register (see Table 6).

The $\overline{INT}$ line is deactivated on the leading edge of TPB. The trailing edge of TPB sets the RDY line to signal the peripheral that the port is ready to be loaded with new data. If RDY is low when the input mode is entered (i.e. after a reset), a "dummy" read must be done to set RDY high and signal the peripheral device that the port is ready to be loaded.

Output Mode

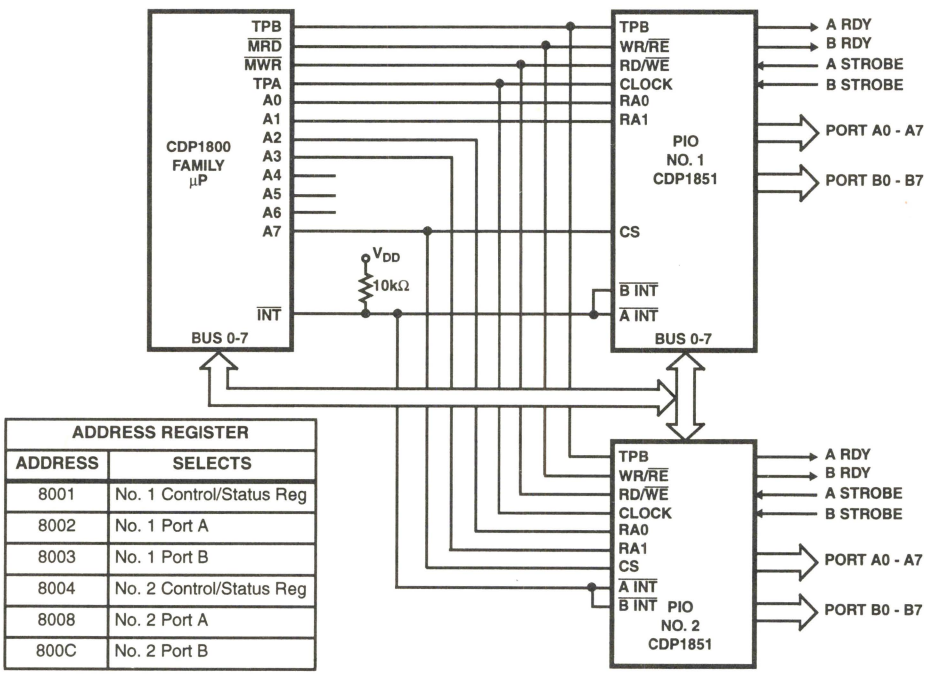
A peripheral STROBE pulse sent to the PIO generates an interrupt to signal the CPU that the peripheral device is ready for data. The CPU executes the proper output or store instruction. Data are then read from memory and placed on the bus. The data are latched into the port buffer at the end of the window when RE/$\overline{WE}$ = 0 and WR/$\overline{RE}$ = 1. The RDY line is also set at this time, indicating to the peripheral that there is data in the port buffer. The $\overline{INT}$ line is deactivated at the beginning of the window. After the peripheral reads valid port data, it can send another STROBE pulse, clearing the RDY line and activating the $\overline{INT}$ line as in the input mode.

Bidirectional Mode

This mode programs port A to function as both an input and output port. The bidirectional feature allows the peripheral to control port direction by using both sets of handshake signals. The port A handshaking pins are used to control input data from peripheral to PIO, while the port B handshaking pins are used to control output data from PIO to peripheral. Data are transferred in the same manner as the input and output modes. Since A INT is used for both input and output, the status register must be read to determine what condition caused A INT to be activated (see Table 5).

Bit-Programmable Mode

This mode allows individual bits of port A or port B to be programmed as inputs or outputs. To output data to bits programmed as outputs, the CPU loads a data byte into the 8-bit port as in the output mode (no handshaking). Only bits programmed for outputs latch this data. Data must be stable when reading from bits programmed as inputs, since the input bits do not latch. When the CDP1851 inputs data to the CPU the CPU also reads the output bits latched during the last output cycle. The RDY and STROBE lines may be used for I/O by using the STROBE/RDY I/O control byte in Table 2. An additional feature available in the bit-programmable mode is the ability to generate interrupts based on input/output byte combinations. These interrupts can be programmed to occur on logic conditions (AND, OR, NAND, and NOR) generated by the eight I/O lines of each port (The STROBE and RDY lines cannot generate interrupts).



ADDRESS REGISTER	
ADDRESS	SELECTS
8001	No. 1 Control/Status Reg
8002	No. 1 Port A
8003	No. 1 Port B
8004	No. 2 Control/Status Reg
8008	No. 2 Port A
800C	No. 2 Port B

FIGURE 2. MEMORY SPACE I/O. THIS CONFIGURATION ALLOWS UP TO FOUR CDP1851s TO OCCUPY MEMORY SPACE 8XXX WITH NO ADDITIONAL HARDWARE (A4-A5 AND A6-A7 ARE USED AS RA0 AND RA1 ON THE THIRD AND FOURTH PIO's)

Programming

Initialization and Controls

The CDP1851 PIO must be cleared by a low on the $\overline{\text{CLEAR}}$ input during power-on to set it for programming. Once programmed, modes can be changed without clearing except when exiting the bit-programmable mode. A low on the $\overline{\text{CLEAR}}$ input sets both ports to the input modes, disables interrupts, unmasks all bit-programmed interrupt bits, and resets the status register, A RDY, and B RDY.

Mode Setting

The control register must be sequentially loaded with the appropriate mode set control bytes in order as shown in Table 1 (i.e. input mode then output mode, etc.). Port A is set with the SET A bit = 1 and port B is set with the SET B bit = 1. If a port is set to the bit-programmable mode, the bit-programming control byte from Table 2 must be loaded. A bit is programmed for output with the I/O bit = 1 and for input with the I/O bit = 0. The STROBE and RDY lines may be programmed for input or output with the STROBE/RDY control byte of Table 2. Input data on the STROBE and RDY lines is detected by reading the status register. When using the STROBE or RDY lines for output, the control byte must be loaded every time output data is to be changed. To program logical conditions that will generate an interrupt, the interrupt control byte of Table 3 must be loaded. An interrupt mask of the eight I/O lines may be loaded next, if bit D4 (mask follows) of the interrupt control byte = 1. The I/O lines are masked if the corresponding bit of the interrupt mask register is 1, otherwise it is monitored. Any combination of masked bits are permissible, except all bits masked (mask = FF).

$\overline{\text{INT}}$ Enable Disable

To enable or disable the $\overline{\text{INT}}$ line in all modes, the interrupt ENABLE/DISABLE byte must be loaded (see Table 4). Interrupts can also be detected by reading the status register (see Table 5). All interrupts should be disabled when programming or false interrupts may occur. The $\overline{\text{INT}}$ outputs are open drain NMOS devices that allow wired O Ring (use 10K pull-up registers).

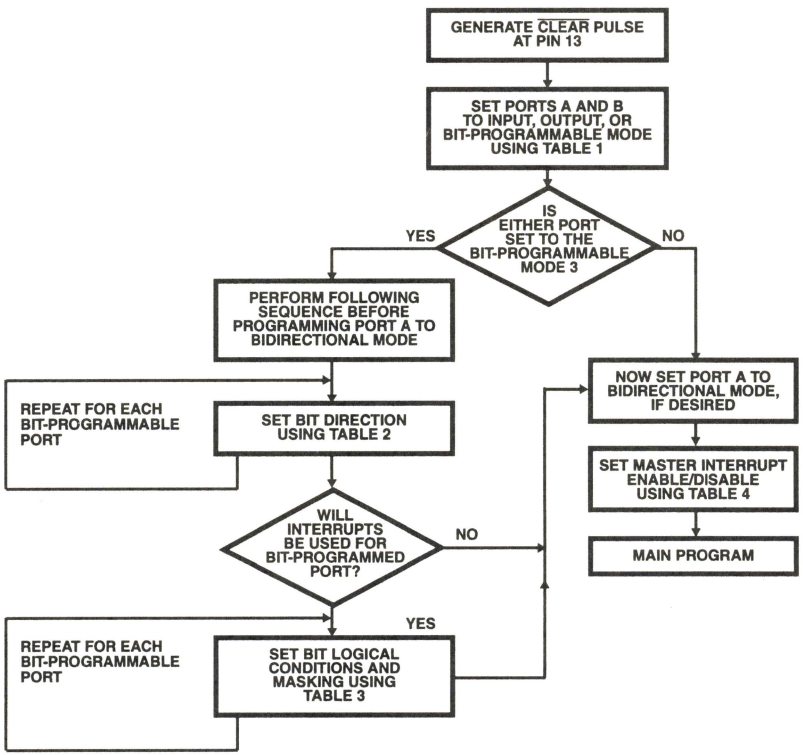


FIGURE 3. A FLOW CHART GUIDE TO CDP1851 MODE PROGRAMMING

NOTES:

1. STROBE/READY I/O Control Byte (Table 2) is also used to output data to STROBE and READY lines when bit-programmed.
2. Status register (Table 2) is used to input data from STROBE and READY lines when bit-programmed.
3. Interrupt status is also read from status register.

TABLE 1. (RA1 = 0, RA0 = 1)

(NOTE 1) MODE SET	7	6	5	4	3	2	1	0
Input	0	0	X	Set B	Set A	X	1	1
Output	0	1	X	Set B	Set A	X	1	1
Bit-Programmable	1	1	X	Set B	Set A	X	1	1
Bidirectional	1	0	X	X	Set A	X	1	1

NOTE:

1. Modes should be set in order as shown in Table 1.

If either port is set for bit-programmable mode, the two following control bytes should immediately follow:

TABLE 2. (RA1 = 0, RA0 = 1)

	7	6	5	4	3	2	1	0
Bit-Programming (Note 1)	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
STROBE/RDY I/O Control (Notes 2 - 8)	D7	D6	D5	D4	D3	D2	D1	D0

NOTES:

1. Output = 1, Input = 0
2. (D1) 0 = Port A, 1 = Port B
3. (D2) 0 = No change to RDY line function, 1 = Change per bit (D6)
4. (D3) 0 = No change to STROBE line function, 1 = Change per bit (D7)
5. (D4) RDY line output data
6. (D5) STROBE line output data
7. (D6) RDY line used as:
   Output = 1
   Input = 0
8. (D7) STROBE line used as:
   Output = 1
   Input = 0

If interrupts will be used for either bit-programmed port, the following control bytes should be loaded.

TABLE 3. (RA1 = 0, RA0 = 1)

INTERRUPT CONTROL	7	6	5	4	3	2	1	0
Logical Conditions and Mask	0	D6	D5	D4	D3	1	0	1

NOTES:

1. (D3) 0 = Port A, 1 = Port B
2. (D4) 0 = No change in mask, 1 = Mask follows (See Table 3A)
3. (D5)(D6) 0, 0 = NAND; 1, 0 = OR; 0, 1 = NOR; 1, 1 = AND

TABLE 3A. (RA1 = 0, RA0 = 1)

INTERRUPT CONTROL	7	6	5	4	3	2	1	0
Mask Register (If D4 = 1)	B7 Mask	B6 Mask	B5 Mask	B4 Mask	B3 Mask	B2 Mask	B1 Mask	B0 Mask

NOTE:

1. If Bn Mask = 1 then mask Bit (for n = 0 to 7)

TABLE 4. (RA1 = 0, RA0 = 1)

INTERRUPT CONTROL	7	6	5	4	3	2	1	0
Interrupt Enable/Disable	$\overline{INT}$ Enable	X	X	X	A/B	0	0	1

NOTES:

1. $\overline{INT}$ Enable = 1, $\overline{INT}$ Enabled
   = 0, $\overline{INT}$ Disabled
2. A/B = 0, Port A
   = 1, Port B

TABLE 5. (RA1 = 0, RA0 = 1)

	7	6	5	4	3	2	1	0
Status Register	D7	D6	D5	D4	D3	D2	D1	D0

NOTES:

1. All Modes
   (D0) B $\overline{INT}$ status (1 means set)
   (D1) A $\overline{INT}$ status (1 means set)
2. Bidirectional Mode Only
   (D2) 1 = A $\overline{INT}$ was caused by A STROBE
   (D3) 1 = A $\overline{INT}$ was caused by B STROBE
3. Bit-Programmable Mode
   (D4) A RDY input data
   (D5) A STROBE input data
   (D6) B RDY input data
   (D7) B STROBE input data

TABLE 6. CPU CONTROLS

(NOTE 1) CS	RA1	RA0	RD/$\overline{WE}$	WR/$\overline{RE}$	ACTION
0	X	X	X	X	No-op bus three-stated
X	0	0	X	X	No-op bus three-stated
X	X	X	0	0	No-op bus three-stated
X	X	X	1	1	No-op bus three-stated
X	X	X	1	1	No-op bus three-stated
1	0	1	1	0	Read status register (Note 1)
1	0	1	0	1	Load control register
1	1	0	1	0	Read port A (Note 1)
1	1	0	0	1	Load port A
1	1	1	1	0	Read port B (Note 1)
1	1	1	0	1	Load port B

NOTE:

1. Read = RD/$\overline{WE}$ = 1 and WR/$\overline{RE}$ = 0 is latched on trailing edge of CLOCK.

TABLE 7. MEMORY I/O USE

	RD/$\overline{WE}$ INPUT	WR/$\overline{RE}$ INPUT	TPB INPUT	
I/O Space	$\overline{MRD}$	TPB	TPB	} CPU Terminals
Memory Space	$\overline{MWR}$	$\overline{MRD}$	TPB	

} PIO Terminal

Function Pin Definition

CLOCK (Input):

Positive input pulse that latches READ and CS on its trailing edge.

CS - CHIP SELECT (Input)

A high-level voltage at this input selects the CDP1851 PIO.

RA0 - REGISTER ADDRESS 0 (Input):

This input and RA1 are used to select either the ports or the control/status registers.

RA1 - REGISTER ADDRESS 1(Input):

See RAO

BUS 0 - BUS 7:

Bidirectional CPU data bus.

$\overline{\text{CLEAR}}$ (Input)

A low-level voltage at this input resets both ports to the input mode, and also resets the status register, A RDY, B RDY, and interrupt enable (disabling interrupts).

$\overline{\text{A INT}}$ - $\overline{\text{A INTERRUPT}}$ (Output):

A low-level voltage at this output indicates the presence of one of the interrupt conditions listed in Table 3. This output is an open-drain NMOS device (to allow wired O Ring) and must be tied to a pullup resistor, normally 10kΩ.

$\overline{\text{B INT}}$ - $\overline{\text{B INTERRUPT}}$ (Output):

A low-level voltage at this output indicates the presence of one of the interrupt conditions listed in Table 3. This output is also an open-drain NMOS device and must be tied to a pullup resistor.

B RDY - B READY (Output):

This output is a handshaking or data bit I/O line in the bit-programmable mode.

B STROBE (Input):

An input handshaking line for port B in the input and output modes, and for port A when it is in the bidirectional mode. It can be used as a data bit I/O line in the bit-programmable mode except when port A is not programmed as bidirectional.

B0 - B7:

Data input or output lines for port B.

V_{SS}

Ground

A0 - A7:

Data input or output lines for port A.

A STROBE (Input):

An input handshaking line for port A in the input, output, and bidirectional modes. It can also be used as a data bit I/O line when port A is in the bit-programmable mode.

ARDY - AREADY (Output):

A output handshaking line or data bit I/O line.

TPB (Input):

A positive input pulse used as a data load, set, or reset strobe.

WR/$\overline{\text{RE}}$ - WRITE/$\overline{\text{READ ENABLE}}$ (Input):

A positive input used to write data from the CDP1851 to the CPU bus.

RD/$\overline{\text{WE}}$ - READ/$\overline{\text{WRITE ENABLE}}$ (Input):

A positive input used to read data from the CPU bus to the CDP1851 bus.

V_{DD}:

Positive supply voltage.

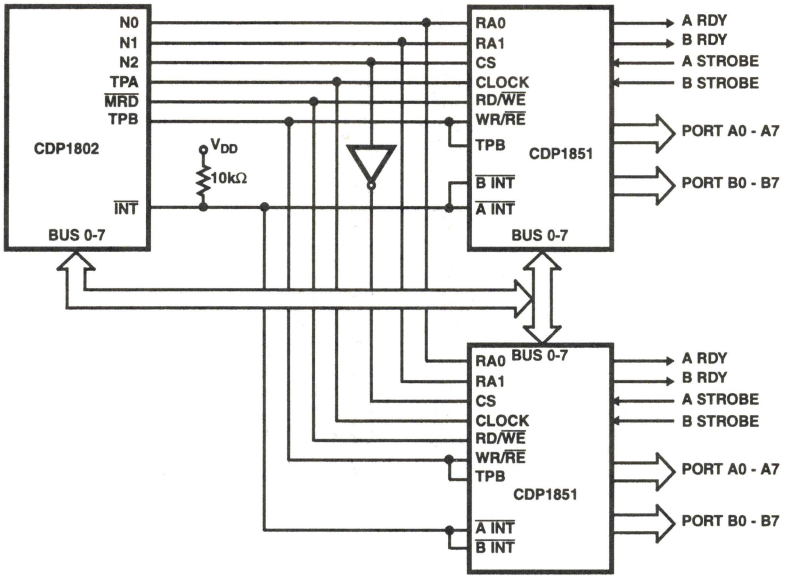


FIGURE 4. I/O SPACE I/O

Dynamic Electrical Specifications

At T_A = -40°C to +85°C, V_{DD} ±5%, t_r, t_f = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF

PARAMETER		V_{DD} (V)	LIMITS						UNITS
			CDP1851			CDP1851C			
			MIN	(NOTE 1) TYP	(NOTE 2) MAX	MIN	(NOTE 1) TYP	(NOTE 2) MAX	
INPUT MODE SEE FIGURES 4 AND 5									
Minimum Setup Times:									
Chip Select to CLOCK	t_{CSCL}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
RD/$\overline{WE}$ to CLOCK	t_{RWCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
WR/$\overline{RE}$ to CLOCK	t_{WRCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
Data in to STROBE	t_{DIST}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
Minimum Hold Times:									
Chip Select After CLOCK	t_{HCSCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
Address After TPB	t_{HATPB}	5	-	-50	0	-	-50	0	ns
		10	-	-25	0	-	-	-	ns
Data In After STROBE	t_{HSTDI}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Data Bus Out After Address	t_{HADOH}	5	50	325	500	50	325	500	ns
		10	25	165	250	-	-	-	ns
Propagation Delay Times:									
TPB to $\overline{INT}$	t_{PINT}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	ns
STROBE to $\overline{INT}$	t_{STINT}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	ns
TPB to RDY	t_{TPRDY}	5	-	250	375	-	250	375	ns
		10	-	125	200	-	-	-	ns
STROBE to RDY	t_{STRDY}	5	-	260	400	-	260	400	ns
		10	-	130	200	-	-	-	ns
Minimum Pulse Widths:									
CLOCK	t_{WCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
TPB	t_{WTPB}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
STROBE	t_{WST}	5	-	100	150	-	100	150	ns
		10	-	50	75	-	-	-	ns
Access Time, Address to Data Bus Out	t_{ADA}	5	-	325	500	-	325	500	ns
		10	-	165	250	-	-	-	ns

NOTES:

1. Typical values are for T_A = 25°C and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.

Test Circuit and Waveforms

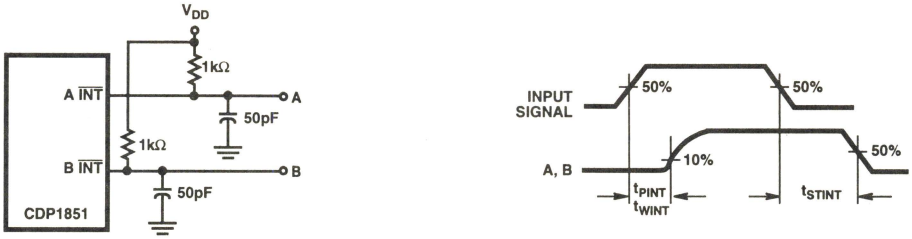


FIGURE 5. INTERRUPT SIGNAL PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS

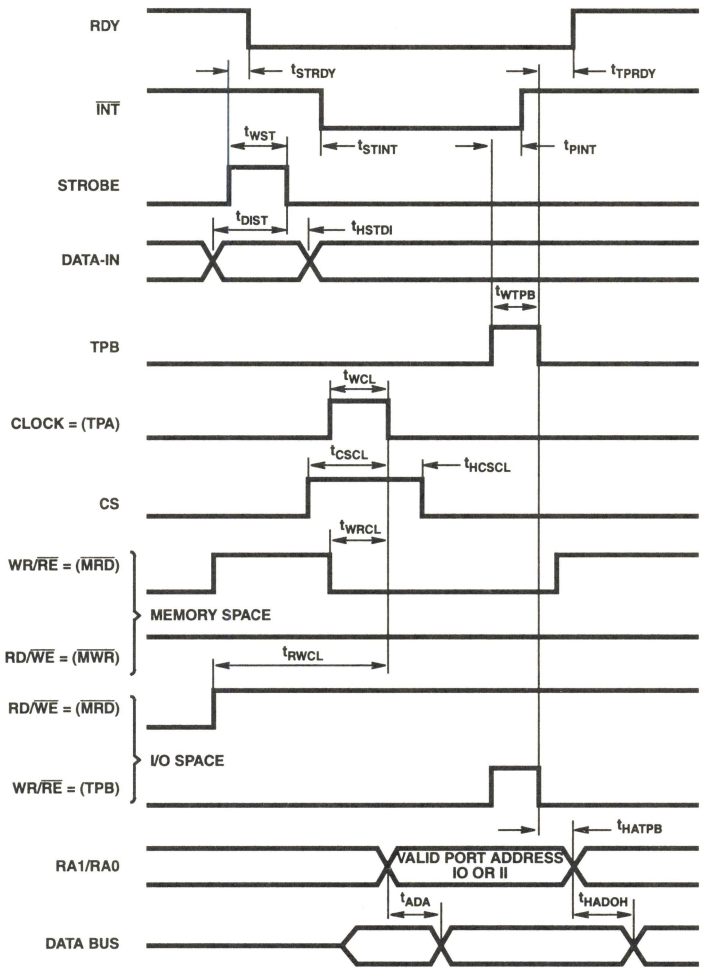


FIGURE 6. INPUT MODE TIMING WAVEFORMS

Dynamic Electrical Specifications At T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF

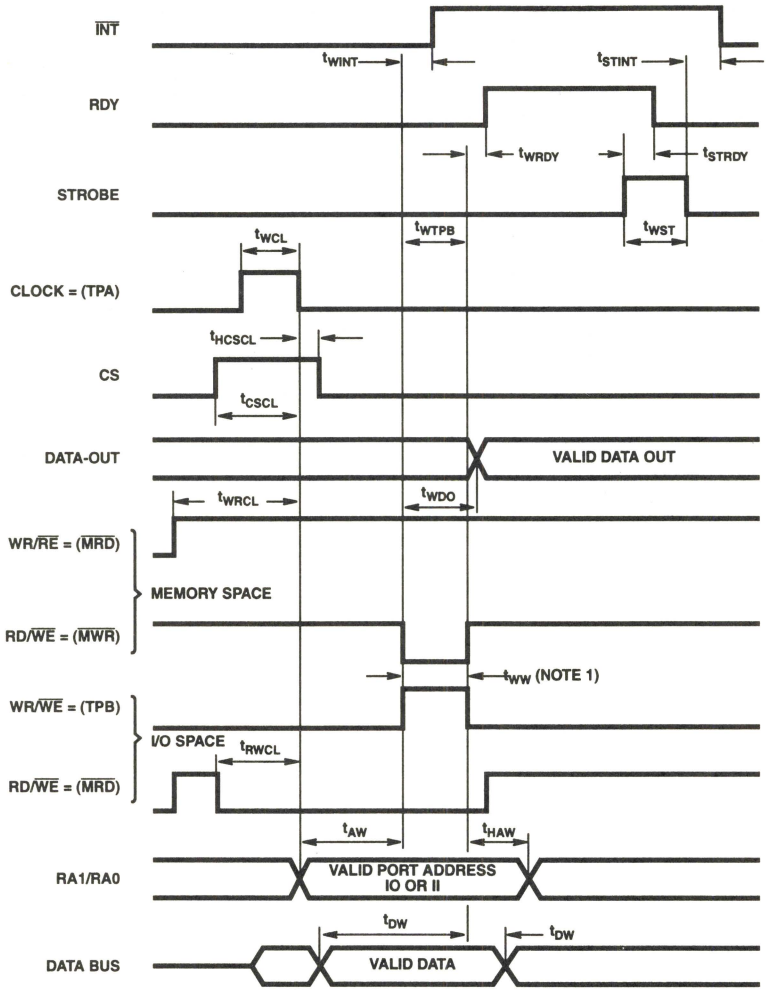
PARAMETERS		V_{DD} (V)	LIMITS						UNITS
			CDP1851			CDP1851C			
			MIN	(NOTE 1) TYP	(NOTE 2) MAX	MIN	(NOTE 1) TYP	(NOTE 2) MAX	
OUTPUT MODE SEE FIGURES 4 AND 6									
Minimum Setup Times:									
Chip Select to CLOCK	t_{CSCL}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
RD/$\overline{WE}$ to CLOCK	t_{RWCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
WR/$\overline{RE}$ to CLOCK	t_{WRCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
Address to WRITE (Note 3)	t_{AW}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Data Bus to WRITE (Note 3)	t_{DW}	5	-	80	120	-	80	120	ns
		10	-	40	60	-	-	-	ns
Minimum Hold Times:									
Chip Select After CLOCK	t_{HCSCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
Address After WRITE (Note 3)	t_{HAW}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Data Bus After WRITE (Note 3)	t_{HDW}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Propagation Delay Times:									
WRITE to Data Out (Note 3)	t_{WDO}	5	-	225	350	-	225	350	ns
		10	-	125	200	-	-	-	ns
WRITE to $\overline{INT}$ (Note 3)	t_{WINT}	5	-	300	450	-	300	450	ns
		10	-	150	225	-	-	-	ns
WRITE to RDY (Note 3)	t_{WRDY}	5	-	350	525	-	350	525	ns
		10	-	175	275	-	-	-	ns
STROBE to $\overline{INT}$	t_{STINT}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	ns
STROBE to RDY	t_{STRDY}	5	-	260	400	-	260	400	ns
		10	-	130	200	-	-	-	ns

Dynamic Electrical Specifications At T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF

PARAMETERS		V_{DD} (V)	LIMITS						UNITS
			CDP1851			CDP1851C			
			MIN	(NOTE 1) TYP	(NOTE 2) MAX	MIN	(NOTE 1) TYP	(NOTE 2) MAX	
Minimum Pulse Widths:									
CLOCK	t_{WCL}	5	-	75	120	-	75	120	ns
		10	-	40	60	-	-	-	ns
STROBE	t_{WST}	5	-	100	150	-	100	150	ns
		10	-	50	75	-	-	-	ns
WRITE (Note 3)	t_{WW}	5	-	175	275	-	175	275	ns
		10	-	90	150	-	-	-	ns

NOTES:

1. Typical values are for T_A = 25°C and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.
3. WRITE is the overlap of RD/$\overline{WE}$ = 0 and WR/$\overline{RE}$ = 1.



NOTE:

1. Write is the overlap of WR/RE = 1 and RD/WE = 0

FIGURE 7. OUTPUT MODE TIMING WAVEFORMS

CDP1852, CDP1852C

March 1997

Byte-Wide Input/Output Port

Features

- Static Silicon-Gate CMOS Circuitry
- Parallel 8-Bit Data Register and Buffer
- Handshaking Via Service Request Flip-Flop
- Low Quiescent and Operating Power
- Interfaces Directly with CDP1800-Series Microprocessors
- Single Voltage Supply
- Full Military Temperature Range (-55°C to +125°C)

Ordering Information

PACKAGE	TEMP. RANGE	5V	10V	PKG. NO.
PDIP	-40°C to +85°C	CDP1852CE	CDP1852E	E24.6
SBDIP	-40°C to +85°C	CDP1852CD	CDP1852D	D24.6

Description

The CDP1852 and CDP1852C are parallel, 8-bit, mode-programmable input/output ports. They are compatible and will interface directly with CDP1800-series microprocessors. They are also useful as 8-bit address latches when used with the CDP1800 multiplexed address bus and as I/O ports in general-purpose applications.

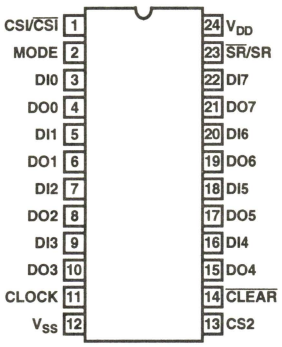
The mode control is used to program the device as an input port (mode = 0) or as an output port (mode = 1). The $\overline{SR}$/SR output can be used as a signal to indicate when data is ready to be transferred. In the input mode, a peripheral device can strobe data into the CDP1852, and microprocessor can read that data by device selection. In the output mode, a microprocessor strobes data into the CDP1852, and handshaking is established with a peripheral device when the CDP1852 is deselected.

In the input mode, data at the data-in terminals (DI0-DI7) is strobed into the port's 8-bit register by a high (1) level on the clock line. The negative high-to-low transition of the clock latches the data in the register and sets the service request output low ($\overline{SR}$/SR = 0). When CS1/$\overline{CS1}$ and CS2 are high (CS1/$\overline{CS1}$ and CS2 = 1), the three-state output drivers are enabled and data in the 8-bit register appear at the data-out terminals (D00-D07). When either CS1/$\overline{CS1}$ or CS2 goes low (CS1/$\overline{CS1}$ or CS2 = 0), the data-out terminals are three-stated and the service request output returns high ($\overline{SR}$/SR =1).

In the output mode, the output drivers are enabled at all times. Data at the data-in terminals (DI0-DI7) is strobed into the 8-bit register when CS1/$\overline{CS1}$ is low (CS1/$\overline{CS1}$ = 0) and CS2 and the clock are high (1), and are present at the data-out terminals (D00-D07). The negative high-to-low transition of the clock latches the data in the register. The $\overline{SR}$/SR output goes high ($\overline{SR}$/SR = 1) when the device is deselected (CS1/$\overline{CS1}$ = 1 or CS2 = 0) and returns low ($\overline{SR}$/SR = 0) on the following trailing edge of the clock.

Pinout

24 LEAD DIP
TOP VIEW



Typical CDP1802 Microprocessor System

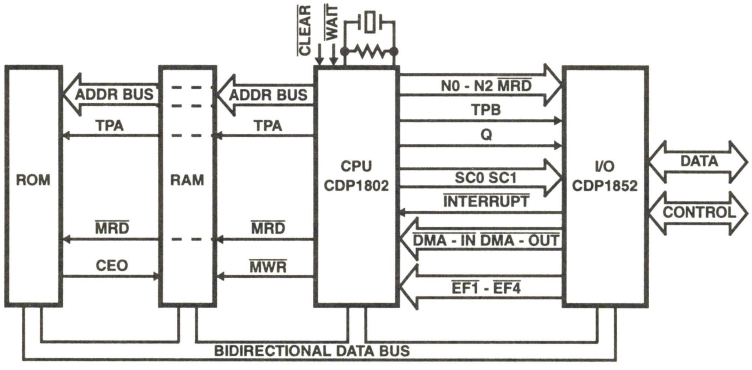


FIGURE 1.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Absolute Maximum Ratings

DC Supply-voltage Range, (V_{DD})
(Voltage Referenced to V_{SS} Terminal)
CDP1852 .....-0.5 to +11V
CDP1852C .....-0.5 to +7V
Input Voltage Range, All Inputs ..... -0.5 to V_{DD} +0.5V
DC Input Current, Any One Input.....±10mA
Device Dissipation Per Output Transistor..... 100mW
For T_A = Full Package-Temperature Range
(All Package Type)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	65	N/A
SBDIP Package	65	20

Operating-Temperature Range (T_A)
Package Type D, H .....-55°C to +125°C
Package Type E.....-40°C to +85°C
Storage Temperature Range (T_{STG}).....-65°C to +150°C
Lead Temperature (During Soldering):.....+265°C
At Distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from Case for 10s max

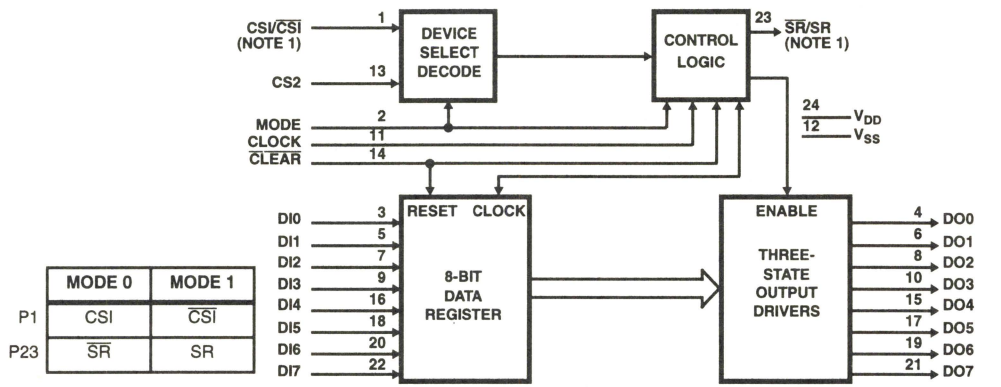
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

At T_A = Full Package Temperature Range. For Maximum Reliability, Operating Conditions Should be Selected so that Operation is Always within the Following Ranges:

PARAMETER	LIMITS				UNITS
	CDP1852		CDP1852C		
	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Functional Diagram



NOTE:

1. Polarity depends on mode.

FIGURE 2. FUNCTIONAL BLOCK DIAGRAM FOR CDP1852

A $\overline{\text{CLEAR}}$ control is provided for resetting the port's register (DO0-DO7 = 0) and service request flip-flop (input mode: $\overline{\text{SR}}$/ SR = 1 and output mode: $\overline{\text{SR}}$/SR = 0).

The CDP1852 is functionally identical to the CDP1852C. The CDP1852 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1852C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1852 and CDP1852C are supplied in 24-lead, hermetic, dual-in-line ceramic packages (D suffix), in 24-lead dual-in-line plastic packages (E suffix). The CDP1852C is also available in chip form (H suffix).

Logic Diagram

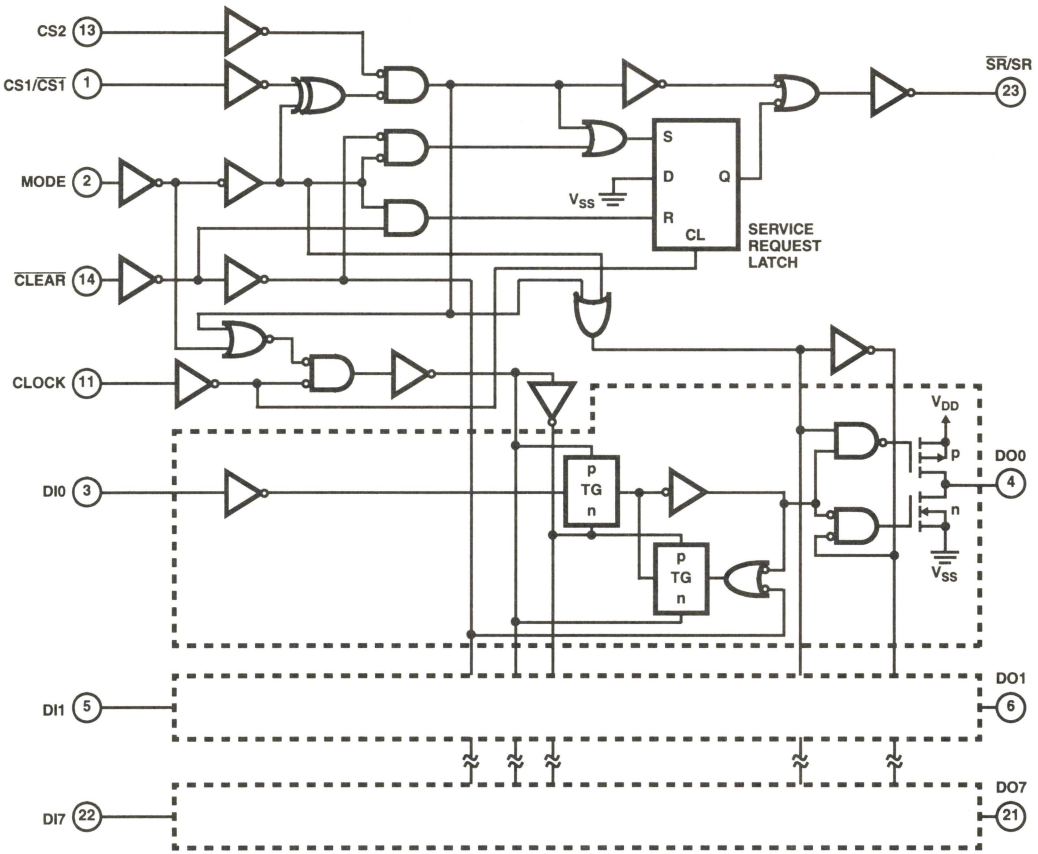


FIGURE 3. CDP1852 LOGIC DIAGRAM

Static Electrical Specifications At T_A = -40°C to +85°C, Unless Otherwise Specified

PARAMETER		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS CDP1852 MIN	LIMITS CDP1852 (NOTE1) TYP	LIMITS CDP1852 MAX	LIMITS CDP1852C MIN	LIMITS CDP1852C (NOTE1) TYP	LIMITS CDP1852C MAX	UNITS
Quiescent Device Current	I_{DD}	-	0, 5	5	-	-	10	-	-	50	µA
		-	0, 10	10	-	-	100	-	-	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	-	1.6	3.2	-	mA
		0.5	0, 10	10	3	6	-	-	-	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	-	-1.15	-2.3	-	mA
		9.5	0, 10	10	-3	-6	-	-	-	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V

Static Electrical Specifications At T_A = -40°C to +85°C, Unless Otherwise Specified (Continued)

PARAMETER		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS CDP1852 MIN	LIMITS CDP1852 (NOTE1) TYP	LIMITS CDP1852 MAX	LIMITS CDP1852C MIN	LIMITS CDP1852C (NOTE1) TYP	LIMITS CDP1852C MAX	UNITS
Output Voltage High Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 9.5	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	-	0, 5	5	-	-	±1	-	-	±1	µA
		-	0, 10	10	-	-	±2	-	-	-	µA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	-	±1	-	-	±1	µA
		0, 10	0, 10	10	-	-	±2	-	-	-	µA
Operating Current (Note 3)	I_{DD1}	-	0, 5	5	-	130	300	-	150	300	µA
		-	0, 10	10	-	550	800	-	-	-	µA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	5	7.5	-	-	-	pF

NOTES:

1. Typical values are for T_A = 25°C and nominal V_{DD}.
2. $I_{OL} = I_{OH}$ = 1µA
3. Operating current is measured at 2MHz in an CDP1802 system with open outputs and a program of 6N55, 6NAA, 6N55, 6NAA,....

Dynamic Electrical Specifications At T_A = -40°C to +85°C, V_{DD} = ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, and 1 TTL Load

PARAMETER		V_{DD} (V)	LIMITS MIN	LIMITS (NOTE 1) TYP	LIMITS MAX	UNITS
MODE 0 - INPUT PORT (See Figure 4)						
Minimum Select Pulse Width	t_{SW}	5	-	180	360	ns
		10	-	90	180	ns
Minimum Write Pulse Width	t_{WW}	5	-	90	180	ns
		10	-	45	90	ns
Minimum Clear Pulse Width	t_{CLR}	5	-	80	160	ns
		10	-	40	80	ns

Dynamic Electrical Specifications At T_A = -40°C to +85°C, V_{DD} = ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, and 1 TTL Load **(Continued)**

PARAMETER		V_{DD} (V)	LIMITS MIN	(NOTE 1) TYP	MAX	UNITS
Minimum Data Setup Time	t_{DS}	5	-	-10	0	ns
		10	-	-5	0	ns
Minimum Data Hold Time	t_{DH}	5	-	75	150	ns
		10	-	35	75	ns
Data Out Hold Time (Note 2)	t_{DOH}	5	30	185	370	ns
		10	15	100	200	ns
Propagation Delay Times, t_{PLH}, t_{PHL} Select to Data Out (Note 2)	t_{SDO}	5	30	185	370	ns
		10	15	100	200	ns
Clear to SR	t_{RSR}	5	-	170	340	ns
		10	-	85	170	ns
Clock to SR	t_{CSR}	5	-	110	220	ns
		10	-	55	110	ns
Select to SR	t_{SSR}	5	-	120	240	ns
		10	-	60	120	ns

NOTES:

1. Typical values are for T_A = 25°C and nominal V_{DD}.
2. Minimum value is measured from CS2, maximum value is measured from CS1/$\overline{CS1}$.

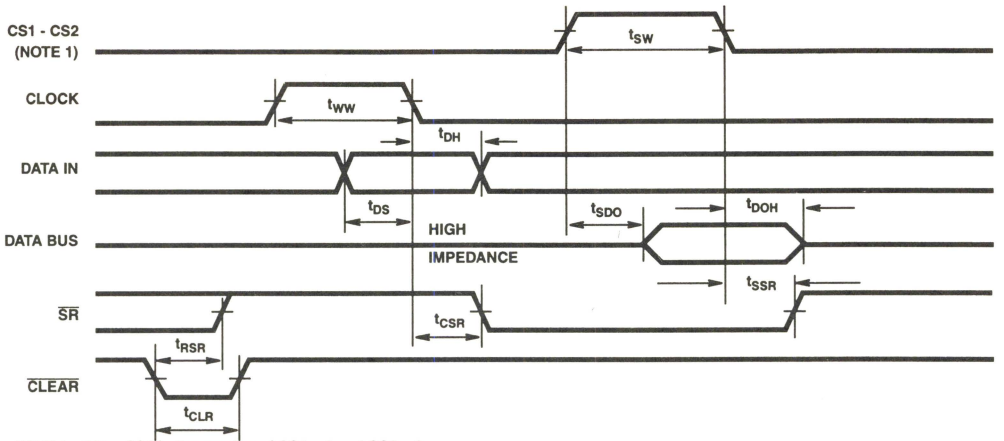
Input Port Mode 0 - Typical Operation

General Operation

When the mode control is tied to V_{SS}, the CDP1852 becomes an input port. In this mode, the peripheral device places data into the CDP1852 with a strobe pulse and the CDP1852 signals the microprocessor that data is ready to be transferred on the strobe's trailing edge via the $\overline{SR}$ output line. The CDP1802 then issues an input instruction that enables the CDP1852 to place the information from the peripheral device on the data bus to be entered into a memory location and the accumulator of the microprocessor.

Detailed Operation (See Figure 5)

The STROBE from the peripheral device places DATA into the 8-bit register of the CDP1852 when it goes high and latches the DATA on its trailing edge. The $\overline{SR}$ output is set low on the strobe's trailing edge. This output is connected to a flag line of the CDP1802 microprocessor and software polling will determine that the flag line has gone low and peripheral data is ready to be transferred. The CDP1802 then issues an input instruction that places an N_X line high. With the $\overline{MRD}$ line also high, the CDP1852 is selected and its output drivers place the DATA from the peripheral device on the DATA BUS. When the CDP1802 selected the CDP1852, it also selected and addressed the memory via one of the 16 internal address registers selected by an internal "X" register. The data from the CDP1852 is therefore entered into the memory [Bus → M(R(X))]. The data is also transferred to the D register (accumulator) in the microprocessor (Bus → D). When the CDP1802's execute cycle is completed, the CDP1852 is deselected by the N_X line returning low and its data output pins are three-stated. The $\overline{SR}$ output returns high.



NOTE 1. CS1 • CS2 is the overlap of CS1 = 1 and CS2 = 1.

MODE 0 TRUTH TABLE

CLOCK	† CS1-CS2	$\overline{CLEAR}$	DATA OUT EQUALS
X	0	X	High Impedance
0	1	0	0
0	1	1	Data Latch
1	1	X	Data In

† CS1 • CS2: CS1 = 1, CS2 = 1

SERVICE REQUEST TRUTH TABLE

CLOCK ↓	CS1 or CS2 or $\overline{CLEAR}$ ↓
$\overline{SR}$/SR 0	$\overline{SR}$/SR 1

FIGURE 4. MODE 0 INPUT PORT TIMING WAVEFORMS AND TRUTH TABLES

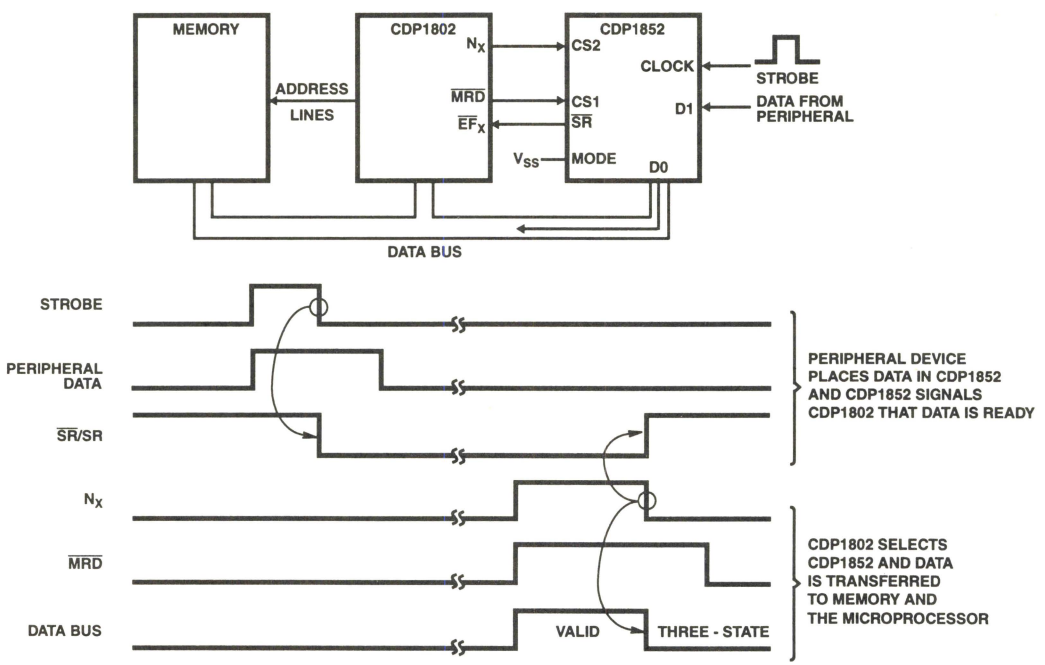


FIGURE 5. INPUT PORT MODE 0 FUNCTIONAL DIAGRAM AND WAVEFORMS - TYPICAL OPERATION

Dynamic Electrical Specifications At T_A = -40°C to +85°C, V_{DD} = ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, and 1 TTL Load

PARAMETER		V_{DD} (V)	LIMITS MIN	LIMITS (NOTE 1) TYP	LIMITS MAX	UNITS
MODE 1- OUTPUT PORT (See Figure 6)						
Minimum Clock Pulse Width	t_{CLK}	5	-	130	260	ns
		10	-	65	130	ns
Minimum Write Pulse Width	t_{WW}	5	-	130	260	ns
		10	-	65	130	ns
Minimum Clear Pulse Width	t_{CLR}	5	-	60	120	ns
		10	-	30	60	ns
Minimum Data Setup Time	t_{DS}	5	-	-10	0	ns
		10	-	-5	0	ns
Minimum Data Hold Time	t_{DH}	5	-	75	150	ns
		10	-	35	75	ns
Minimum Select-After-Clock Hold Time	t_{SH}	5	-	-10	0	ns
		10	-	-5	0	ns
Propagation Delay Times, t_{PLH}, t_{PHL} Clear to Data Out	t_{RDO}	5	-	140	280	ns
		10	-	70	140	ns
Write to Data Out	t_{WDO}	5	-	220	440	ns
		10	-	110	220	ns
Data In to Data Out	t_{DDO}	5	-	100	200	ns
		10	-	50	100	ns
Clear to SR	t_{RSR}	5	-	120	240	ns
		10	-	60	120	ns
Clock to SR	t_{CSR}	5	-	120	240	ns
		10	-	60	120	ns
Select to SR	t_{SSR}	5	-	120	240	ns
		10	-	60	120	ns

NOTE:

1. Typical values are for T_A = 25°C and nominal V_{DD}.

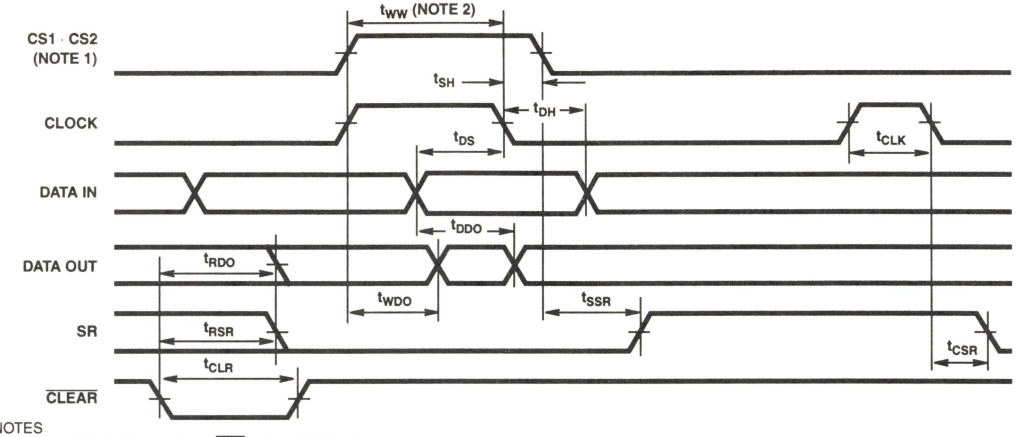
Output Port Mode 1 - Typical Operation

General Operation

Connecting the mode control to V_{DD} configures the CDP1852 as an output port. The output drivers are always on in this mode, so any data in the 8-bit register will be present at the data-out lines when the CDP1852 is selected. The N line and $\overline{MRD}$ connections between the CDP1852 and CDP1802 remain the same as in the input mode configuration, but now the clock input of the CDP1852 is tied to the TPB output of the CDP1802 and the SR output of the CDP1852 will be used to signal the peripheral device that valid data is present on its input lines. The microprocessor issues an output instruction, and data from the memory is strobed into the CDP1852 with the TPB pulse. When the CDP1852 is deselected, the SR output goes high to signal the peripheral device.

Detailed Operation (See Figure 7)

The CDP1802 issues an output instruction. The N_X line goes high and the $\overline{MRD}$ line goes low. The memory is accessed M(R(X)) → BUS and places data on the DATA BUS. This data are strobed into the 8-bit register of the CDP1852 when TPB goes high and latched on the TPB's trailing edge. The valid data thus appears on the CDP1852 output lines. When the CDP1802 output instruction cycle is complete, the N_X line goes low and the SR output goes high. SR will remain high until the trailing edge of the next TPB pulse, when it will return low.



NOTES
1. CS1 • CS2 is the overlap of $\overline{CS1}$ = 0 and CS2 = 1.
2. Write is the overlap of CS1 • CS2 and CLOCK.

MODE 1 TRUTH TABLE

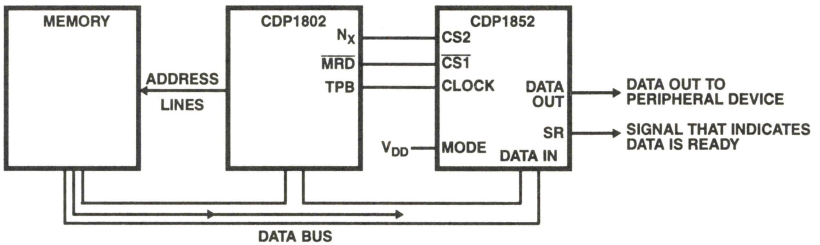
CLOCK	† $\overline{CS1}$-CS2	$\overline{CLEAR}$	DATA OUT EQUALS
0	X	0	0
0	X	1	Data Latch
X	0	1	Data Latch
1	1	X	Data In

† $\overline{CS1}$ • CS2 : $\overline{CS1}$ = 0, CS2 = 1

SERVICE REQUEST TRUTH TABLE

$\overline{CS1}$ or CS2 ↓	CLOCK or $\overline{CLEAR}$ ↓
$\overline{SR}$/SR 1	$\overline{SR}$/SR 0

FIGURE 6. MODE 1 OUTPUT PORT TIMING WAVEFORMS AND TRUTH TABLES



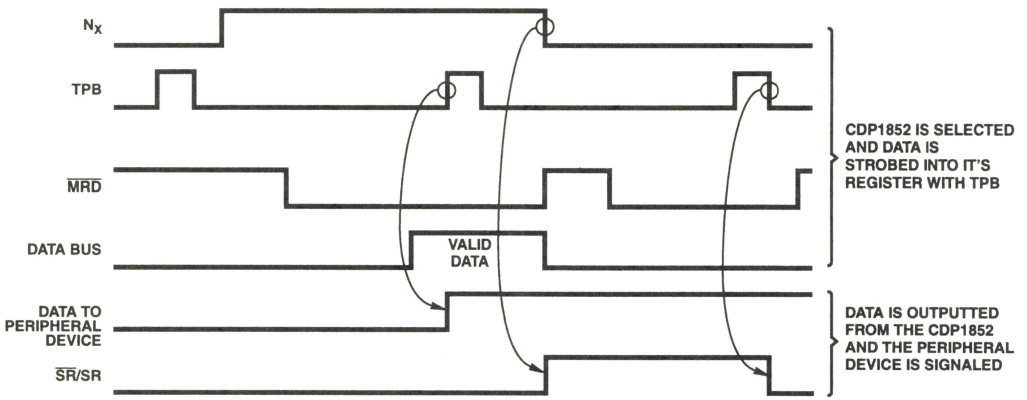


FIGURE 7. OUTPUT PORT MODE 1 FUNCTIONAL DIAGRAM AND WAVEFORMS - TYPICAL OPERATION

Application Information

In a CDP1800 series microprocessor-based system where $\overline{MRD}$ is used to distinguish between INP and OUT instructions, an INP instruction is assumed to occur at the beginning of every I/O cycle because $\overline{MRD}$ starts high. Therefore, at the start of an OUT instruction, which uses the same 3-bit N code as that used for selection of an input port, the input device is selected for a short time (see Figure 8). This condition forces SR low and sets the internal SR latch (see Figure 3). In a small system with unique N codes for inputs and outputs, this situation does not arise. Using the CDP1853 N-bit decoder or equivalent logic to decode the N lines after TPA prevents dual selection in larger systems (see Figure 9 and Figure 10).

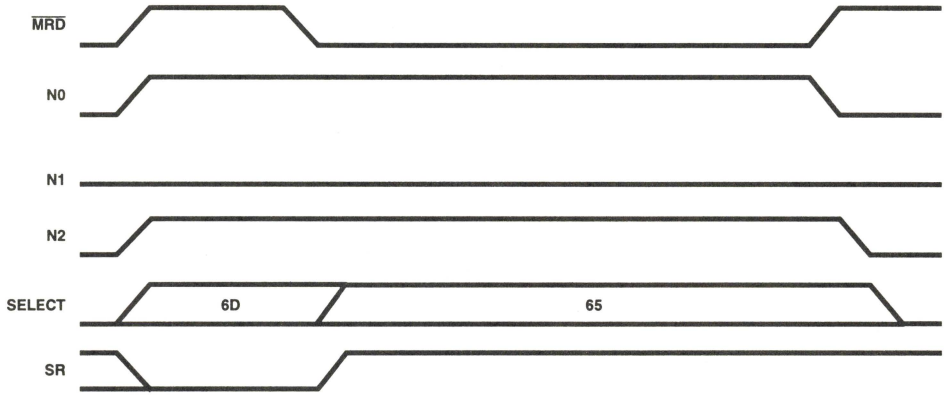


FIGURE 8. EXECUTION OF A "65" OUTPUT INSTRUCTION SHOWING MOMENTARY SELECTION OF INPUT PORT "D"

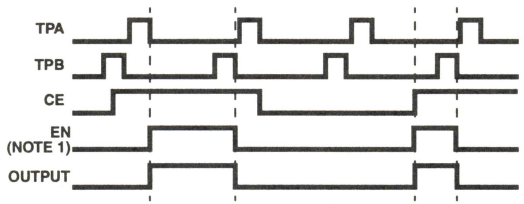


FIGURE 9. CDP1853 TIMING WAVEFORMS

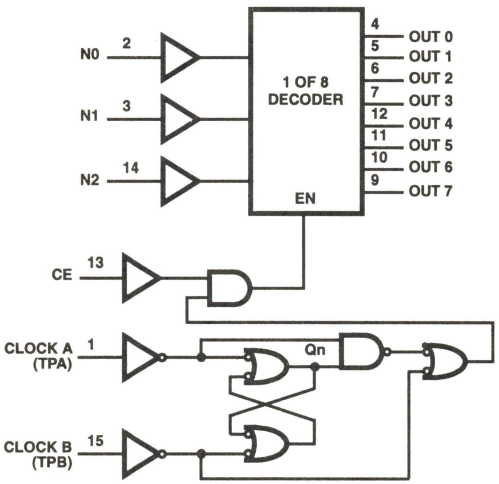


FIGURE10. CDP1853 FUNCTIONAL DIAGRAM

NOTE:

1. Output enabled when EN = HIGH. Internal signal shown for reference only (See Figure 1).

HARRIS SEMICONDUCTOR

CDP1852/3, CDP1852C/3

March 1997

High-Reliability Byte-Wide Input/Output Port

Features

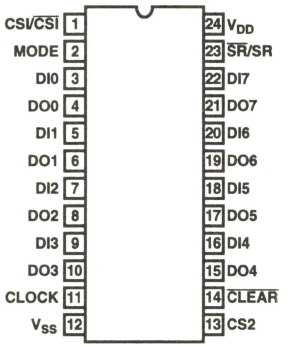
- Static Silicon-Gate CMOS Circuitry
- Parallel 8-Bit Data Register and Buffer
- Handshaking Via Service Request Flip-Flop
- Low Quiescent and Operating Power
- Interfaces Directly with CDP1800-Series Microprocessors
- Single Voltage Supply
- Full Military Temperature Range (-55°C to +125°C)

Ordering Information

PACKAGE	TEMP. RANGE	5V	10V	PKG. NO
SBDIP	-55°C to +125°C	CDP1852CD3	CDP1852D3	D24.6

Pinout

CDP1852/3, CDP1852C/3 (SBDIP)
TOP VIEW



Description

The CDP1852/3 and CDP1852C/3 are parallel, 8-bit, mode-programmable input/output ports. They are compatible and will interface directly with CDP1800-Series microprocessors. They are also useful as 8-bit address latches when used with the CDP1800 multiplexed address bus and as I/O ports in general-purpose applications.

The mode control is used to program the device as an input port (mode = 0) or as an output port (mode = 1). The $\overline{SR}$/SR output can be used as a signal to indicate when data is ready to be transferred. In the input mode, a peripheral device can strobe data into the CDP1852/3, and microprocessor can read that data by device selection. In the output mode, a microprocessor strobes data into the CDP1852/3, and handshaking is established with a peripheral device when the CDP1852/3 is deselected.

In the input mode, data at the data-in terminals (DI0-DI7) is strobed into the port's 8-bit register by a high (1) level on the clock line. The negative high-to-low transition of the clock latches the data in the register and sets the service request output low (SR/SR = 0). When CS1/$\overline{CS1}$ and CS2 are high (CS1/$\overline{CS1}$ and CS2 = 1), the three-state output drivers are enabled and data in the 8-bit register appear at the data-out terminals (DO0-DO7). When either CS1/$\overline{CS1}$ or CS2 goes low (CS1/$\overline{CS1}$ or CS2 = 0), the data-out terminals are tristated and the service request output returns high ($\overline{SR}$/SR =1).

In the output mode, the output drivers are enabled at all times. Data at the data-in terminals (DI0-DI7) is strobed into the 8-bit register when CS1/$\overline{CS1}$ is low (CS1/$\overline{CS1}$ = 0) and CS2 and the clock are high (1), and are present at the data-out terminals (DO0-DO7). The negative high-to-low transition of the clock latches the data in the register. The $\overline{SR}$/SR output goes high ($\overline{SR}$/SR = 1) when the device is deselected (CS1/$\overline{CS1}$ = 1 or CS2 = 0) and returns low ($\overline{SR}$/SR = 0) on the following trailing edge of the clock.

A $\overline{CLEAR}$ control is provided for resetting the port's register (DO0-DO7 = 0) and service request flip-flop (input mode: $\overline{SR}$/SR = 1 and output mode: $\overline{SR}$/SR = 0).

The CDP1852/3 is functionally identical to the CDP1852C/3. The CDP1852/3 has a recommended operating voltage range of 4V to 10.5V, and the CDP1852C/3 has a recommended operating voltage range of 4V to 6.5V.

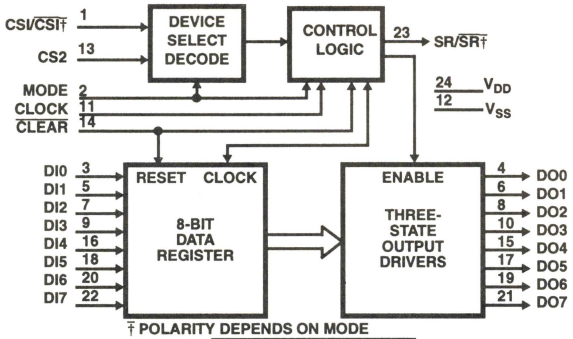
The CDP1852/3 and CDP1852C/3 are supplied in 24-lead, dual-in-line side-brazed ceramic packages (D suffix).

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1694.2**

Block Diagram of CDP1852/3



	MODE = 0	MODE = 1
P1	CSI	$\overline{CSI}$
P23	$\overline{SR}$	SR

FIGURE 1.

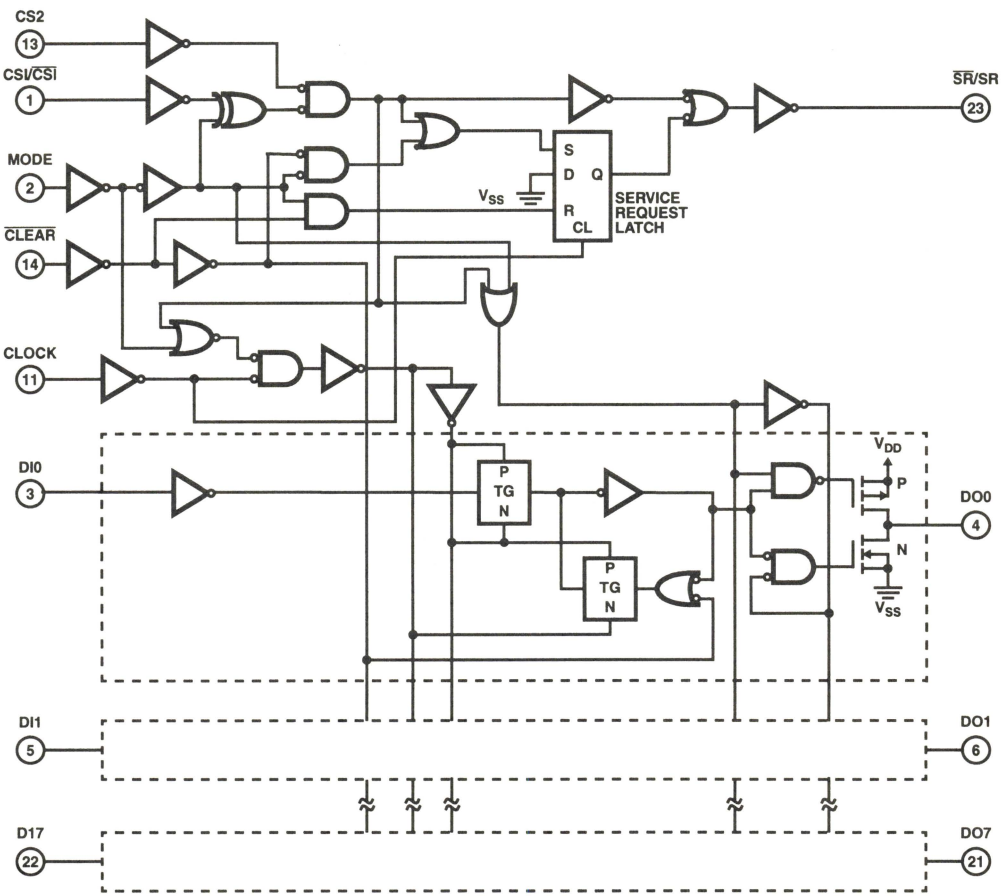


FIGURE 2. CDP1852/3 LOGIC DIAGRAM

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD}):
(All Voltages Referenced to V_{SS} Terminal)
CDP1852/3 . . . . . -0.5V to +11V
CDP1852C/3 . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, any One Input . . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	65	20

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type D . . . . . -55°C to +125°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 in (1.59 ± 0.79mm)
From Case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions T_A = Full-Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges.

PARAMETER	LIMITS				UNITS
	CPP1852/3		CDP1852C/3		
	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Static Electrical Specifications V_{IN} = 0 or V_{DD}, Except as Noted

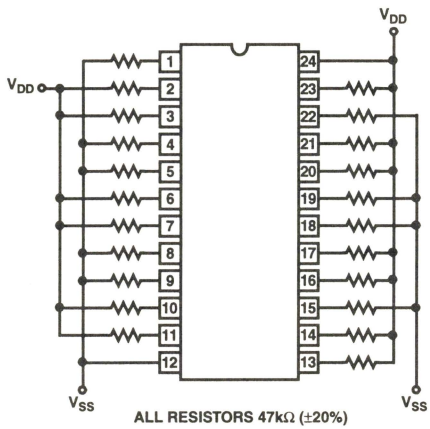
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			MIN	MAX	MIN	MAX	
Quiescent Device Current (Note 1)	I_{DD}	V_{DD} = 5V	-	10	-	100	µA
		V_{DD} = 10V	-	20	-	300	µA
Output Low Drive (Sink) Current	I_{OL}	V_{DD} = 5V, V_O = 0.4V	2.6	-	1.9	-	mA
		V_{DD} = 10V, V_O = 0.5V	6.1	-	4.1	-	mA
Output High Drive (Source) Current	I_{OH}	V_{DD} = 5V, V_O = 4.6V	-1.8	-	-1.3	-	mA
		V_{DD} = 10V, V_O = 9.5V	-4.4	-	-2.9	-	mA
Output Voltage Low Level	V_{OL}	V_{DD} = 5V, I_{OL} = 0µA	-	0.1	-	0.2	V
		V_{DD} = 10V, I_{OL} = 0µA	-	0.1	-	0.2	V
Output Voltage High Level	V_{OH}	V_{DD} = 5V, I_{OL} = 0µA	4.9	-	4.8	-	V
		V_{DD} = 10V, I_{OL} = 0µA	9.9	-	9.8	-	V
Input Low Voltage	V_{IL}	V_{DD} = 5V, V_O = 0.2, 4.8V	-	1.5	-	1.5	V
		V_{DD} = 10V, V_O = 0.2, 9.8V	-	3	-	3	V
Input High Voltage	V_{IH}	V_{DD} = 5V, V_O = 0.2, 4.8V	3.5	-	3.5	-	V
		V_{DD} = 10V, V_O = 0.2, 9.8V	7	-	7	-	V
Input Leakage Low	I_{IL}	V_{DD} = 5V, V_{IN} = 0V	-	-1	-	-5	µA
		V_{DD} = 10V, V_{IN} = 0V	-	-1	-	-5	µA
Input Leakage High	I_{IH}	V_{DD} = 5V, V_{IN} = 5V	-	1	-	5	µA
		V_{DD} = 10V, V_{IN} = 10V	-	1	-	5	µA

Static Electrical Specifications V_{IN} = 0 or V_{DD}, Except as Noted **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS -55°C, +25°C MIN	LIMITS -55°C, +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
Three-State Output Leakage Low	I_{OZL}	V_{DD} = 5V, V_O = 0V	-	-1	-	-5	µA
		V_{DD} = 10V, V_O = 0V	-	-1	-	-5	µA
Three-State Output Leakage High	I_{OZH}	V_{DD} = 5V, V_O = 5V	-	1	-	5	µA
		V_{DD} = 10V, V_O = 10V	-	1	-	5	µA
Input Capacitance	C_{IN}	Note 2	-	10	-	10	pF
Output Capacitance	C_{OUT}	Note 2	-	15	-	15	pF

NOTES:
1. The CDP1852C/3 meets all 5V static electrical specifications of the CDP1852/3 except +125°C quiescent device current for which the limit is I_{DD} = 300µA.
2. Input and output capacitance are guaranteed but not tested.

Static Burn-In Circuit



TYPE NO.	V_{DD}	TEMPERATURE	TIME
CDP1852/3	11V	+125°C	160 Hrs. Min.
CDP1852C/3	7V	+125°C	160 Hrs. Min.

Dynamic Electrical Specifications Mode = 0 Input Port, See Figure 3, Input t_r, $t_f \leq$ 15ns; C_L = 50pF

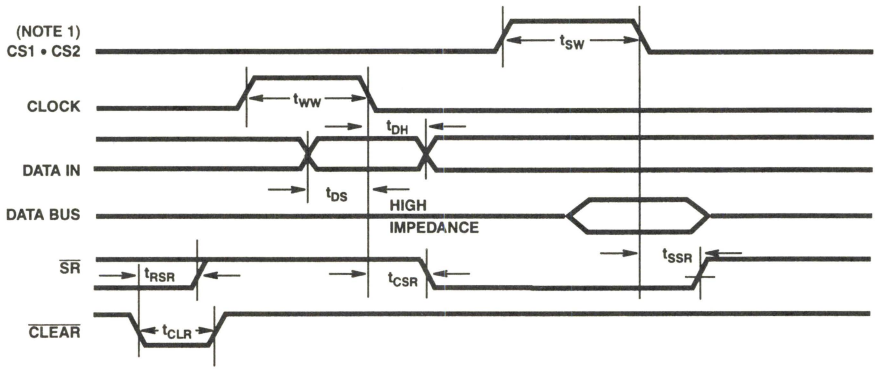
PARAMETER	SYMBOL	V_{DD} VOLTS	LIMITS (NOTE 1) -55°C, +25°C (NOTE 1) MIN	LIMITS (NOTE 1) -55°C, +25°C MAX	LIMITS (NOTE 1) +125°C (NOTE 1) MIN	LIMITS (NOTE 1) +125°C MAX	UNITS
Select Duration	t_{SW}	5	250	-	360	-	ns
		10	150	-	180	-	ns
Clock Pulse Width	t_{WW}	5	150	-	200	-	ns
		10	90	-	110	-	ns
Clear Pulse Width	t_{CLR}	5	110	-	160	-	ns
		10	50	-	80	-	ns
Data-In to Clock Fall Setup Time	t_{DS}	5	-10	-	-10	-	ns
		10	-5	-	-5	-	ns

Dynamic Electrical Specifications Mode = 0 Input Port, See Figure 3, Input t_r, $t_f \leq 15ns$; $C_L = 50pF$ **(Continued)**

PARAMETER	SYMBOL	V_{DD} VOLTS	LIMITS (NOTE 1) -55°C, +25°C (NOTE 1) MIN	-55°C, +25°C MAX	+125°C (NOTE 1) MIN	+125°C MAX	UNITS
Data-In After Clock Fall Hold Time	t_{DH}	5	150	-	170	-	ns
		10	70	-	100	-	ns
Propagation Delay Times: Clear to $\overline{SR}$	t_{RSR}	5	-	200	-	340	ns
		10	-	110	-	170	ns
Clock to $\overline{SR}$	t_{CSR}	5	-	175	-	220	ns
		10	-	110	-	130	ns
Deselect to $\overline{SR}$	t_{SSR}	5	-	175	-	240	ns
		10	-	110	-	120	ns

NOTE:

1. Time required by a device to allow for the indicated function.



NOTE:

1. CS1 • CS2 is the overlap of CS1 = 1 and CS2 = 1.

MODE = 0 TRUTH TABLE			
CLOCK	CS1 • CS2 (Note 1)	$\overline{CLEAR}$	DATA OUT EQUALS
X	0	X	High Impedance
0	1	0	0
0	1	1	Data Latch
1	1	X	Data In

SERVICE REQUEST TRUTH TABLE	
Clock = ↘	CS1 or CS2 = or $\overline{CLEAR}$ = 0 ↘
$\overline{SR}$ = 0	$\overline{SR}$ = 1

NOTE:

1. CS1 • CS2 = CS1 = 1, CS2 = 1.

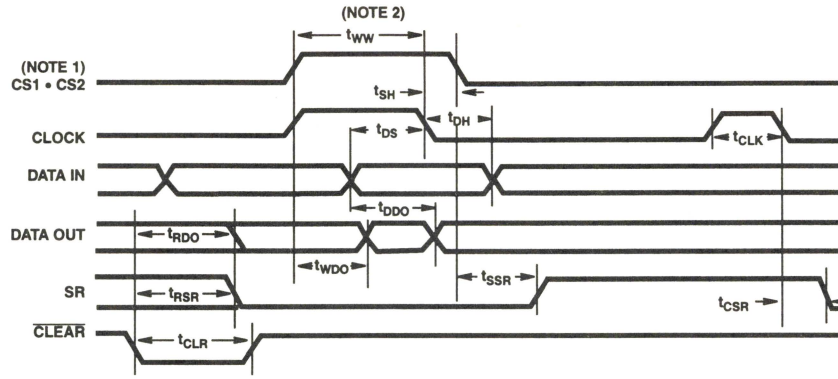
FIGURE 3. MODE = 0 INPUT PORT TIMING WAVEFORMS AND TRUTH TABLES

Dynamic Electrical Specification Mode = 1 Output Port, See Figure 4, Input t_r, $t_f \leq 15ns$; $C_L = 50pF$

PARAMETER	SYMBOL	V_{DD} VOLTS	LIMITS (NOTE 1) -55°C, +25°C (NOTE 1) MIN	-55°C, +25°C MAX	+125°C (NOTE 1) MIN	+125°C MAX	UNITS
Clock Pulse Width	t_{CLK}	5	170	-	260	-	ns
		10	90	-	130	-	ns
Write Width Duration	t_{WW}	5	200	-	260	-	ns
		10	110	-	130	-	ns
Clear Pulse Width	t_{CLR}	5	110	-	135	-	ns
		10	60	-	75	-	ns
Data-In to Clock Fall Setup Time	t_{DS}	5	-10	-	-10	-	ns
		10	-5	-	-5	-	ns
Data Hold from Write Termination	t_{DH}	5	130	-	170	-	ns
		10	70	-	90	-	ns
Select-After Clock-Fall Hold Time	t_{SH}	5	0	-	0	-	ns
		10	0	-	0	-	ns
Propagation Delay Times: Clear to Data	t_{RDO}	5	-	215	-	290	ns
		10	-	140	-	190	ns
Write to Data Out	t_{WDO}	5	-	250	-	350	ns
		10	-	130	-	190	ns
Data In to Data Out	t_{DDO}	5	-	150	-	200	ns
		10	-	80	-	100	ns
Clear to SR	t_{RSR}	5	-	175	-	240	ns
		10	-	120	-	160	ns
Clock to SR	t_{CSR}	5	-	170	-	240	ns
		10	-	90	-	120	ns
Deselect to SR	t_{SSR}	5	-	170	-	240	ns
		10	-	90	-	120	ns

NOTE:

1. Time required by a device to allow for the indicated function.



NOTES:

1. CS1 • CS2 is the overlap of the $\overline{CS1}$ = 0 and CS2 = 1.
2. Write is the overlap of CS1 • CS2 and clock.

MODE = 1 TRUTH TABLE			
CLOCK	$\overline{CS1}$ • **CS2** (NOTE 1)	$\overline{CLEAR}$	**DATA OUT EQUALS**
0	X	0	0
0	X	1	Data Latch
X	0	1	Data Latch
1	1	X	Data In

SERVICE REQUEST TRUTH TABLE	
$\overline{CS1}$ ↗ or CS2 ↘	Clock • ($\overline{CS1}$ • $\overline{CS2}$) ↘ or $\overline{CLEAR}$ = 0
SR = 1	SR = 0

NOTE:

1. $\overline{CS1}$ • CS2 = $\overline{CS1}$ = 0, CS2 = 1

FIGURE 4. MODE = 1 OUTPUT PORT TIMING WAVEFORMS AND TRUTH TABLES

CDP1853, CDP1853C

March 1997

N-Bit 1 of 8 Decoder

Features

- **Provides Direct Control of Up to 7 Input and 7 Output Devices**
- **CHIP ENABLE (CE) Allows Easy Expansion for Multi-level I/O Systems**

Ordering Information

PACKAGE	TEMP. RANGE	5V	10V	PKG. NO.
PDIP	-40°C to +85°C	CDP1853CE	CDP1853E	E16.3
Burn-In		CDP1853CEX	-	E16.3
SBDIP	-40°C to +85°C	CDP1853CD	CDP1853D	D16.3
Burn-In		CDP1853CDX	-	D16.3

Description

The CDP1853 and CDP1853C are 1 of 8 decoders designed for use in general purpose microprocessor systems. These devices, which are functionally identical, are specifically designed for use as gated N-bit decoders and interface directly with the 1800-series microprocessors without additional components. The CDP1853 has a recommended operating voltage range of 4V to 10.5V, and the CDP1853C has a recommended operating voltage range of 4V to 6.5V.

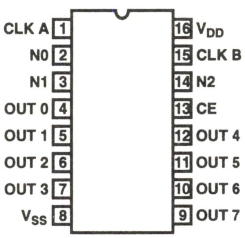
When CHIP ENABLE (CE) is high, the selected output will be true (high) from the trailing edge of CLOCK A (high-to-low transition) to the trailing edge of CLOCK B (high-to-low transition). All outputs will be low when the device is not selected (CE = 0) and during conditions of CLOCK A and CLOCK B as shown in Figure 2. The CDP1853 inputs N0, N1, N2, CLOCK A, and CLOCK B are connected to an 1800-series microprocessor outputs N0, N1, N2, TPA, and TPB respectively, when used to decode I/O commands as shown in Figure 5. The CHIP ENABLE (CE) input provides the capability for multiple levels of decoding as shown in Figure 6.

The CDP1853 can also be used as a general 1 of 8 decoder for I/O and memory system applications as shown in Figure 4.

The CDP1853 and CDP1853C are supplied in hermetic 16-lead dual-in-line ceramic (D suffix) and plastic (E suffix) packages.

Pinout

16 LEAD DIP
TOP VIEW



CDP1853 Functional Diagram

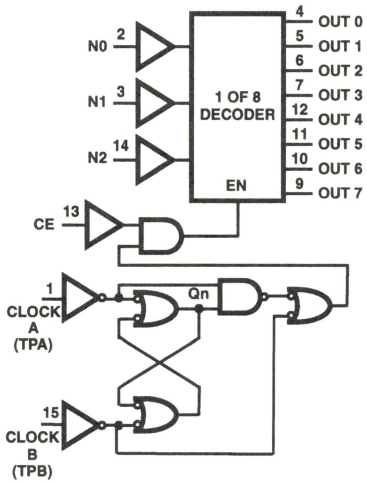


FIGURE 1.

TRUTH TABLE

CE	CL A	CL B	EN
1	0	0	Qn-1†
1	0	1	1
1	1	0	0
1	1	1	1
0	X	X	0

N2	N1	N0	EN	0	1	2	3	4	5	6	7
0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
X	X	X	0	0	0	0	0	0	0	0	0

1 = High level, 0 = Low level, X = Don't care
† Qn-1 = Enable remains in previous state.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1853 . . . . . -0.5V to +11V
CDP1853C . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, any One Input . . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	85	N/A
SBDIP Package	85	22

Operating Temperature Range (T_A)
Ceramic Packages (D Suffix Types) . . . . . -55°C to +125°C
Plastic Packages (E Suffix Types) . . . . . -40°C to +85°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At distance 1/16 ± 1/32 In. (1.59 ± 0.79mm) from case for 10s max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications At T_A = -40 to +85°C, Unless Otherwise Specified

PARAMETER		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS CDP1853 MIN	LIMITS CDP1853 (NOTE1) TYP	LIMITS CDP1853 MAX	LIMITS CDP1853C MIN	LIMITS CDP1853C (NOTE1) TYP	LIMITS CDP1853C MAX	UNITS
Quiescent Device Current	I_L	-	-	5	-	1	10	-	5	50	µA
		-	-	10	-	10	100	-	-	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	-	1.6	3.2	-	mA
		0.5	0, 10	10	2.6	5.2	-	-	-	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	-	-1.15	-2.3	-	mA
		9.5	0, 10	10	-2.6	-5.2	-	-	-	-	mA
Output Voltage Low Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High Level	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		1, 9	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
		1, 9	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	-	±1	-	-	±1	µA
			0, 10	10	-	-	±1	-	-	-	µA
Operating Current (Note 3)	I_{DD1}	0, 5	0, 5	5	-	50	100	-	50	100	µA
		0, 10	0, 10	10	-	150	300	-	-	-	µA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = +25°C and nominal voltage.
2. $I_{OL} = I_{OH}$ = 1µA
3. Operating current measured in a CDP1802 system at 2MHz with outputs floating.

Recommended Operating Conditions At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS				UNITS
	CDP1853		CDP1853C		
	MIN	MAX	MIN	MAX	
Supply Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Dynamic Electrical Specifications At T_A = -40 to +85°C, V_{DD} = ±5%, $V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$, t_R, t_F = 20ns, C_L = 100pF, Unless Otherwise Specified

PARAMETER		V_{DD} (V)	LIMITS						UNITS
			CDP1853			CDP1853C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time:									
CE to Output	t_{EOH}, t_{EOL}	5	-	175	275	-	175	275	ns
		10	-	90	150	-	-	-	ns
N to Output	t_{NOH}, t_{NOL}	5	-	225	350	-	225	350	ns
		10	-	120	200	-	-	-	ns
Clock A to Output	t_{AO}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	ns
Clock B to Output	t_{BO}	5	-	175	275	-	175	275	ns
		10	-	90	150	-	-	-	ns
Minimum Pulse Widths:									ns
Clock A	t_{CACA}	5	-	50	75	-	50	75	ns
		10	-	25	50	-	-	-	ns
Clock B	t_{CBCB}	5	-	50	75	-	50	75	ns
		10	-	25	50	-	-	-	ns

NOTES:

1. Maximum limits of minimum characteristics are the values above which all devices function.
2. Typical values are for T_A = +25°C and nominal voltages.

Timing Diagrams

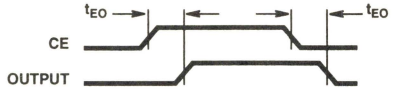


FIGURE 2A. CE TO OUTPUT (0-7) DELAY TIME

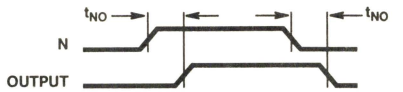


FIGURE 2B. N LINES TO OUTPUT (0-7) DELAY TIME

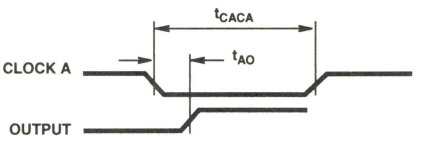


FIGURE 2C. CLOCK A TO OUTPUT (0-7) DELAY TIME

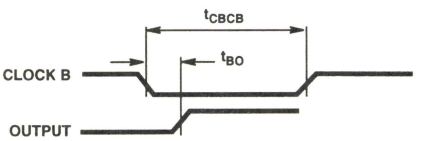
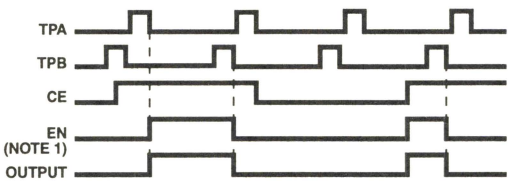


FIGURE 2D. CLOCK B TO OUTPUT (0-7) DELAY TIME

FIGURE 2. PROPAGATION DELAY TIME DIAGRAMS



NOTE 1. OUTPUT ENABLED WHEN EN = HIGH
INTERNAL SIGNAL SHOWN FOR
REFERENCE ONLY (SEE FIGURE 1)

FIGURE 3. TIMING DIAGRAM

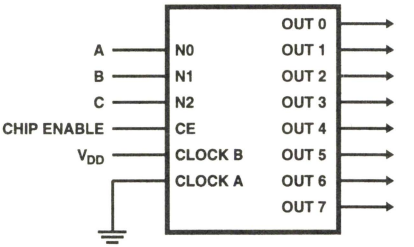


FIGURE 4. N-BIT DECODER USED AS A 1 OF 8 DECODER

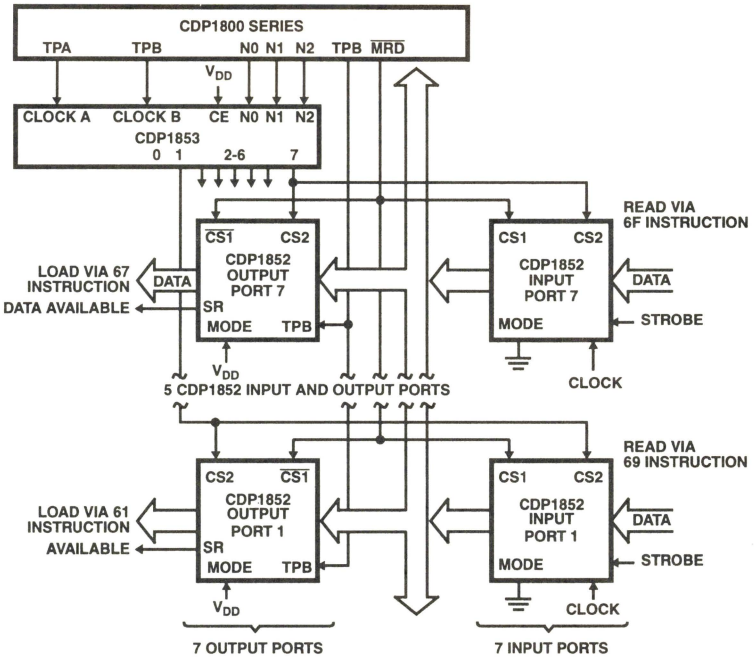


FIGURE 5. N-BIT DECODER IN A ONE-LEVEL I/O SYSTEM

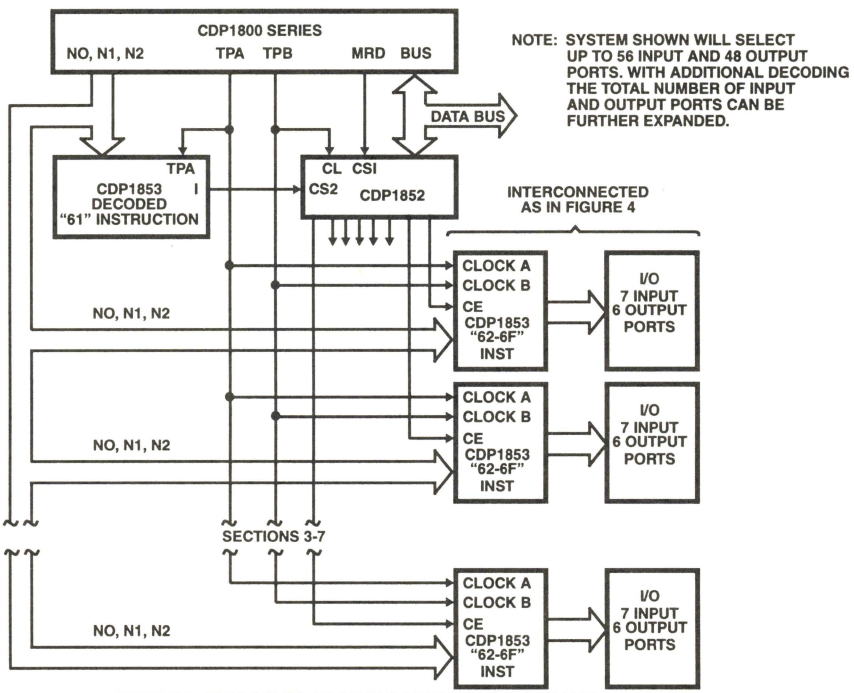


FIGURE 6. TWO-LEVEL I/O USING CDP1853 AND CDP1852

HARRIS SEMICONDUCTOR

CDP1853C/3

March 1997

High-Reliability CMOS N-Bit 1 of 8 Decoder

Features

- **Provides Direct Control of Up to 7 Input and 7 Output Devices When used with a CDP1800-Series Microprocessor**
- **CHIP ENABLE (CE) Allows Easy Expansion for Multi-level I/O Systems**

Ordering Information

PACKAGE	TEMP. RANGE	5V	10V	PKG. NO.
SBDIP	-55°C to +125°C	CDP1853CD3	-	D16.3

Description

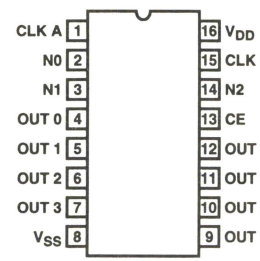
The CDP1853/3 and CDP1853C/3 are high-reliability 1 of 8 decoders designed for use in general purpose microprocessor systems. These devices, which are functionally identical, are specifically designed for use as gated N-bit decoders and interface directly with the 1800-Series microprocessors without additional components. The CDP1853/3 has a recommended operating voltage range of 4V to 10.5V, and the CDP1853C/3 has a recommended operating voltage range of 4V to 6.5V.

When CHIP ENABLE (CE) is high, the selected output will be true (high) from the trailing edge of CLOCK A (high-to-low transition) to the trailing edge of CLOCK B (high-to-low transition). All outputs will be low when the device is not selected (CE = 0) and during conditions of CLOCK A and CLOCK B as shown in Figure 2. The CDP1853/3 inputs N0, N1, N2, CLOCK A, and CLOCK B are connected to 1800-series microprocessor outputs N0, N1, N2, TPA, and TPB respectively, when used to decode I/O commands as shown in Figure 5. The CHIP ENABLE (CE) input provides the capability for multiple levels of decoding as shown in Figure 6.

The CDP1853/3 can also be used as a general purpose 1 of 8 decoder for I/O and memory system applications as shown in Figure 4.

Pinout

16 LEAD SBDIP
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1713.2**

CDP1853/3 Functional Diagram

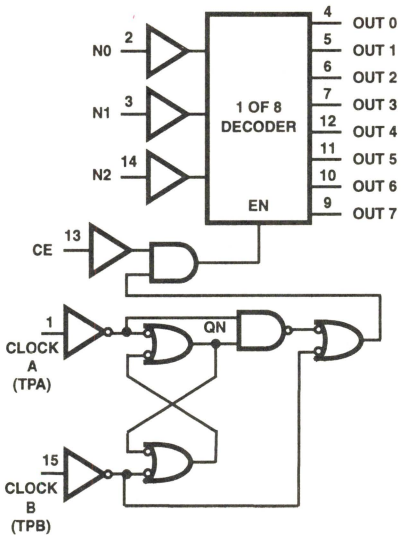


FIGURE 1.

TRUTH TABLE

CE	CL A	CL B	EN
1	0	0	Qn-1(Note 2)
1	0	1	1
1	1	0	0
1	1	1	1
0	X	X	0

N2	N1	N0	EN	0	1	2	3	4	5	6	7
0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
X	X	X	0	0	0	0	0	0	0	0	0

NOTES:

1. 1 = High level, 0 = Low level, X = Don't care.
2. Qn-1 = Enable remains in previous state.

Static Electrical Specifications

PARAMETER	SYMBOL	CONDITIONS			LIMITS				UNITS
					-55°C, +25°C		+125°C		
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	MAX	MIN	MAX	
Quiescent Device Current	I_{SS} (Note 1)	-	0, 5	5	-50	-	-100	-	µA
		-	0, 10	10	-500	-	-1000	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	-	5	2.3	-	1.6	-	mA
		0.5	-	10	3.7	-	2.6	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	-	5	-	-1.7	-	-1.2	mA
		9.5	-	10	-	-3.7	-	-2.6	mA
Output Voltage Low-Level	V_{OL} (Note 2)	-	0, 5	5	-	0.1	-	0.2	V
		-	0, 10	10	-	0.1	-	0.2	V
Output Voltage High-Level	V_{OH} (Note 2)	-	0, 5	5	4.9	-	4.8	-	V
		-	0, 10	10	9.9	-	9.8	-	V
Input Low Voltage	V_{IL}	0.8, 4.2	-	5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	V
Input High Voltage	V_{IH}	0.8, 4.2	-	5	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	V
Input Leakage Low	I_{IL}	-	0	5	-1	-	-5	-	µA
		-	0	10	-1	-	-5	-	µA
Input Leakage High	I_{IH}	-	5	5	-	1	-	5	µA
		-	10	10	-	1	-	5	µA
Input Capacitance	C_{IN} (Note 2)	-	-	-	-	10	-	10	pF
Output Capacitance	C_{OUT} (Note 2)	-	-	-	-	15	-	15	pF

NOTES:

1. The CDP1853C meets all 5V static electrical characteristics of the CDP1853 except quiescent device current for which the limits are: I_{SS} = -500µA at -55°C and +25°C and I_{SS} = -1000µA at +125°C.
2. Guaranteed but not tested.

Dynamic Electrical Specifications

See Figure 2, C_L = 100pF, t_R, t_F = 15ns

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			MIN	MAX	MIN	MAX	
Propagation Delay Time:	t_{EOH}	5	-	175	-	275	ns
Chip Enable (CE) to Output High		10	-	90	-	150	ns

Dynamic Electrical Specifications

See Figure 2, C_L = 100pF, t_R, t_F = 15ns

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			MIN	MAX	MIN	MAX	
Disable to Output Low	t_{EOL}	5	-	295	-	400	ns
		10	-	200	-	250	ns
N Input to Output	t_{NO}	5	-	225	-	315	ns
		10	-	120	-	165	ns
Clock A to Output Low	t_{AO}	5	-	210	-	300	ns
		10	-	110	-	150	ns
Clock B to Output Low	t_{BO}	5	-	295	-	400	ns
		10	-	200	-	250	ns
Pulse Width:	t_{CACA}	5	50	-	75	-	ns
Clock A		10	25	-	50	-	ns
Clock B	t_{CBCB}	5	50	-	75	-	ns
		10	25	-	50	-	ns

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS				UNITS
	CDP1853/3		CDP1853C/3		
	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1853/3 . . . . . -0.5V to +11V
CDP1853C/3 . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input . . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	85	22

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type D . . . . . -55°C to +125°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ±1/32 In. (1.59 ± 0.79mm)
from case for 10s max . . . . . +265°C

Timing Diagrams

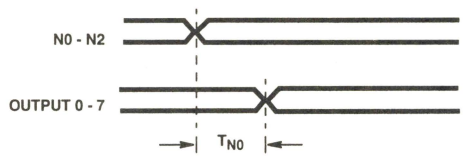


FIGURE 2A. N - INPUTS TO OUTPUTS DELAY TIME

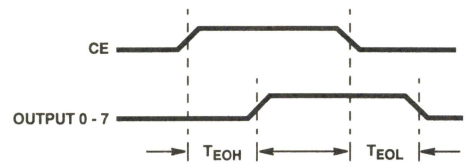


FIGURE 2B. CE TO OUTPUT DELAY TIME

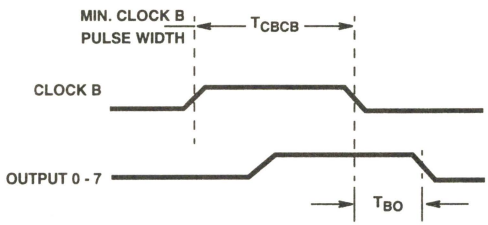
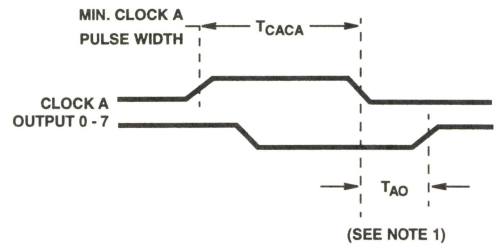


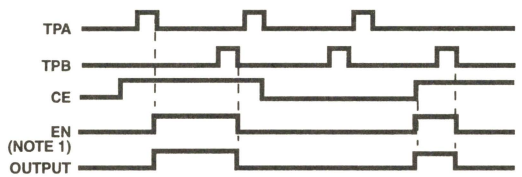
FIGURE 2C. CLOCK B TO OUTPUT DELAY TIME



NOTE:
1. To measure T_{AO}, Clock B must be tied low.

FIGURE 2D. CLOCK A TO OUTPUT DELAY TIME

FIGURE 2. PROPAGATION DELAY TIME DIAGRAMS



NOTE:
1. Output enabled when EN = high. Internal signal shown for reference only (see Figure 1).

FIGURE 3. TIMING DIAGRAM

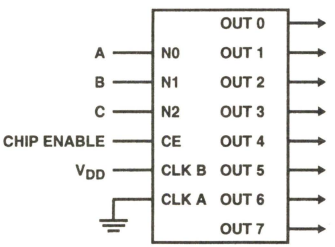


FIGURE 4. N-BIT DECODER USED AS A 1 OF 8 DECODER

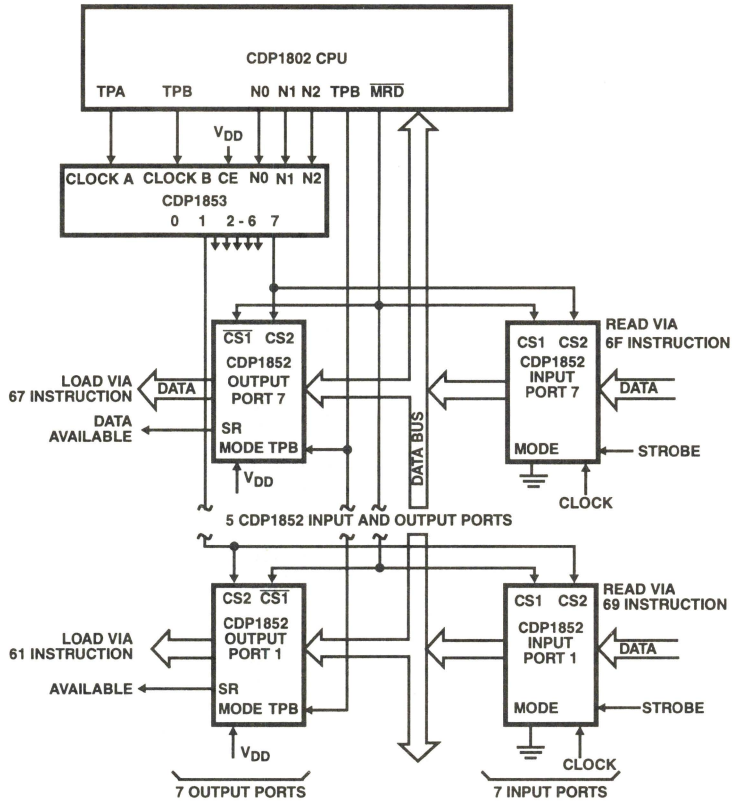
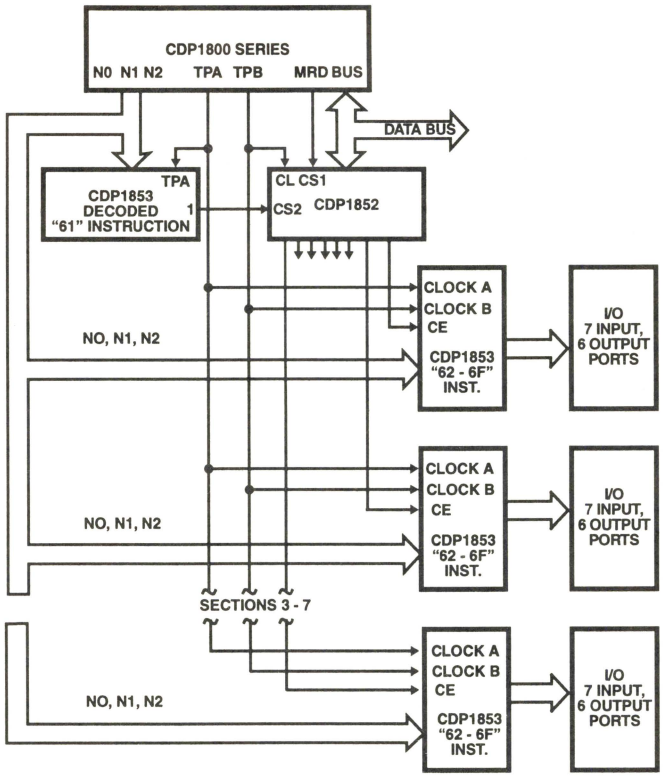


FIGURE 5. N-BIT DECODER IN A ONE LEVEL I/O SYSTEM

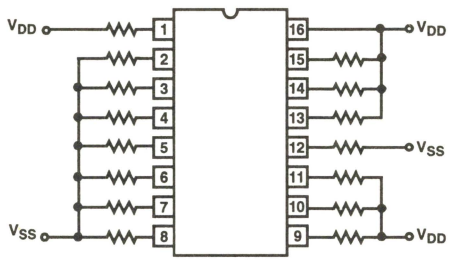


NOTE:

1. System shown will select up to 56 input and 48 output ports. With additional decoding, the total number of input and output ports can be further expanded.

FIGURE 6. TWO LEVEL I/O USING CDP1853 AND CDP1852

Bias/Static Burn-In Circuit



TYPE	V_{DD}	TEMPERATURE	TIME
CDP1853C	7V	+125°C	160 Hrs.

NOTE:

1. All resistors are 47kΩ ±20%.

CDP1855, CDP1855C

8-Bit Programmable Multiply/Divide Unit

March 1997

Features

- **Cascadable Up to 4 Units for 32-Bit by 32-Bit Multiply or 64 ÷ 32-Bit Divide**
- **8-Bit by 8-Bit Multiply or 16 ÷ 8-Bit Divide in 5.6μs at 5V or 2.8μs at 10V**
- **Direct Interface to CDP1800-Series Microprocessors**
- **Easy Interface to Other 8-Bit Microprocessors**
- **Significantly Increases Throughput of Microprocessor Used for Arithmetic Calculations**

Ordering Information

PACKAGE	TEMP. RANGE	5V	10V	PKG. NO.
PDIP	-40°C to +85°C	CDP1855CE	CDP1855E	E28.6
Burn-In		CDP1855CEX	-	E28.6
SBDIP	-40°C to +85°C	CDP1855CD	CDP1855D	D28.6
Burn-In		CDP1855CDX	-	D28.6

Description

The CDP1855 and CDP1855C are CMOS 8-bit multiply/divide units which can be used to greatly increase the capabilities of 8-bit microprocessors. They perform multiply and divide operations on unsigned, binary operators. In general, microprocessors do not contain multiply or divide instructions and even efficiently coded multiply or divide subroutines require considerable memory and execution time. These multiply/divide units directly interface to the CDP1800-series microprocessors via the N-lines and can easily be configured to fit in either the memory or I/O space of other 8-bit microprocessors.

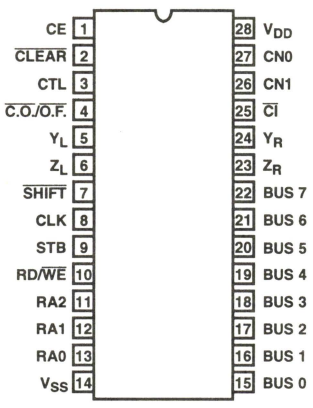
The multiple/divide unit is based on a method of multiplying by add and shift right operations and dividing by subtract and shift left operations. The device is structured to permit cascading identical units to handle operands up to 32 bits.

The CDP1855 and CDP1855C are functionally identical. They differ in that the CDP1855 has a recommended operating voltage range of 4V to 10.5V, and the CDP1855C, a recommended operating voltage range of 4V to 6.5V.

The CDP1855 and CDP1855C types are supplied in a 28 lead hermetic dual-in-line ceramic package (D suffix) and in a 28 lead dual-in-line plastic package (E suffix). The CDP1855C is also available in chip form (H suffix).

Pinout

28 LEAD DIP
TOP VIEW



Circuit Configuration

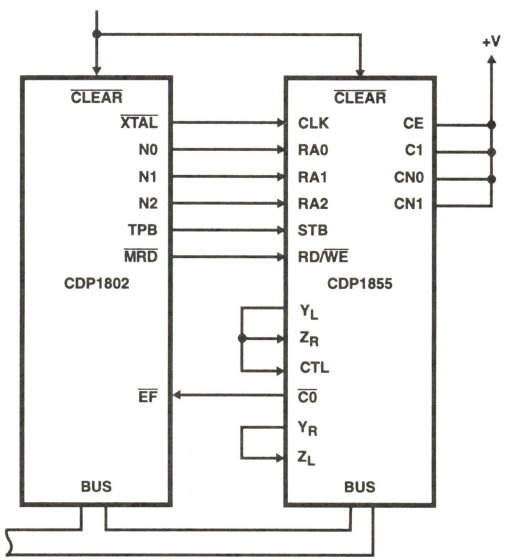


FIGURE 1. MDU ADDRESSED AS I/O DEVICE

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1053.2**

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1855 . . . . . -0.5V to +11V
CDP1855C . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	55	N/A
SBDIP Package	50	12

Device Dissipation Per Output Transistor
For T_A = Full Package-Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A) . . . . . -40°C to +85°C
Storage Temperature Range (T_{STg}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ± 1/32 In. (1.59 ± 0.79mm)
from case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications At T_A = -40 to +85°C, V_{DD} ±10%, Unless Otherwise Specified

PARAMETER		CONDITIONS			LIMITS						UNITS
					CDP1855			CDP1855C			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE1) TYP	MAX	MIN	(NOTE1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	0.01	50	-	0.02	200	µA
		-	0, 10	10	-	1	200	-	-	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	-	1.6	3.2	-	mA
		0.5	0, 10	10	2.6	5.2	-	-	-	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	-	-1.15	-2.3	-	mA
		9.5	0, 10	10	-2.6	-5.2	-	-	-	-	mA
Output Voltage Low Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 9.5	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	-	0, 5	5	-	-	±1	-	-	±1	µA
		-	0, 10	10	-	-	±1	-	-	-	µA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	-	±1	-	-	±1	µA
		0, 10	0, 10	10	-	-	±10	-	-	-	µA
Operating Current (Note 3)	I_{DD1}	-	0, 5	5	-	1.5	-	-	1.5	3	mA
		-	0, 10	10	-	6	12	-	-	-	mA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = +25°C and nominal V_{DD}.
2. $I_{OL} = I_{OH}$ = 1µA
3. Operating current is measured at 3.2MHz with open outputs.

Recommended Operating Conditions At T_A = Full package temperature range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	V_{DD} (V)	LIMITS				UNITS
		CDP1855		CDP1855C		
		MIN	MAX	MIN	MAX	
DC Operating Voltage Range	-	4	10.5	4	6.5	V
Input Voltage Range	-	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Maximum Clock Input Frequency	5	3.2	-	3.2	-	MHz
	10	6.4	-	-	-	MHz
Minimum 8 x 8 Multiply (16 ÷ 8 Divide) Time	5	-	5.6	-	5.6	µs
	10	-	2.8	-	-	µs

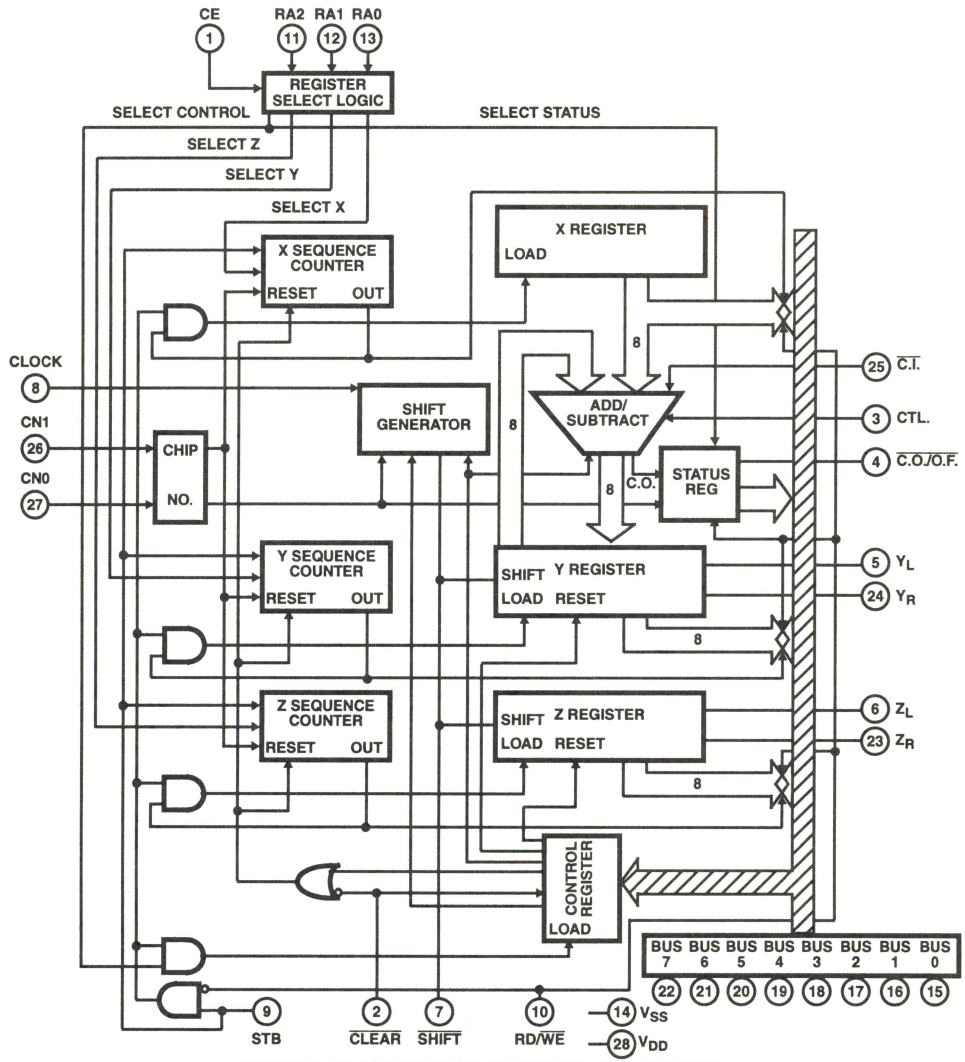


FIGURE 2. BLOCK DIAGRAM OF CDP1855 AND CDP1855C

Functional Description

The CDP1855 is a multiply-divide unit (MDU) designed to be compatible with CDP1800 series microprocessor systems. It can, in fact, be interfaced to most 8-bit microprocessors (see Figure 5). The CDP1855 performs binary multiply or divide operations as directed by the microprocessor. It can do a 16N-bit by 8N-bit divide yielding a 8N-bit result plus and 8N-bit remainder. The multiply is an 8N-bit by 8N-bit operation with a 16N-bit result. The "N" represent the number of cascaded CDP1855's and can be 1, 2, 3 or 4. All operations require 8N + 1 shift pulses (See "DELAY NEEDED WITH AND WITHOUT PRESCALER").

The CDP1855 contains three registers, X, Y, and Z, which are loaded with the operands prior to an operation and contain the results at the completion. In addition, the control register must be loaded to initiate a multiply or divide. There is also a status register which contains an overflow flag as shown in the "CONTROL REGISTER BIT ASSIGNMENT TABLE". The register address lines (RA0-RA1) are used to select the appropriate register for loading or reading. The RD/$\overline{WE}$ and STB lines are used in conjunction with the RA lines to determine the exact MDU response (See "CONTROL TRUTH TABLE").

When multiple MDU's are cascaded, the loading of each register is done sequentially. For example, the first selection of register X for loading loads the most significant CDP1855, the second loads the next significant, and so on. Registers are also read out sequentially. This is accomplished by internal counters on each MDU which are decremented by STB during each register selection. When the counter matches the chip number (CN1, CN0 lines), the device is selected. These counters must be cleared with a clear on pin 2 or with bit 6 in the control word (See "CONTROL REGISTER BIT ASSIGNMENT TABLE") in order to start each sequence of accesses with the most significant device.

The CDP1855 has a built in clock prescaler which can be selected via bit 7 in the control register. The prescaler may be necessary in cascaded systems operating at high frequencies or in systems where a suitable clock frequency is not readily available. Without the prescaler select, the shift frequency is equal to the clock input frequency. With the prescaler selected, the rate depends on the number of MDU's as defined by bits 4 and 5 of the control word (See "CONTROL REGISTER BIT ASSIGNMENT TABLE").

1. For one MDU, the clock frequency is divided by 2.
2. For two MDU's the clock frequency is divided by 4.
3. For 3 or 4 MDU's, the clock frequency is divided by 8.

Operation

1. Initialization and Controls

The CDP1855 must be cleared by a low on pin 2 during power-on which prevents bus contention problems at the Y_L, Y_R and Z_L, Z_R terminals and also resets the sequence counters and the shift pulse generator.

Prior to loading any other registers the control register must be loaded to specify the number of MDU's being used (See "CONTROL REGISTER BIT ASSIGNMENT TABLE").

Once the number of devices has been specified and the sequence counters cleared with a clear pulse or bit 6 of the control word, the X, Y, and Z registers can be loaded as defined in the "CONTROL TRUTH TABLE". All bytes of the X register can be loaded, then all bytes of the Y, and then all bytes of the Z, or they can be loaded randomly. Successive loads to a given register will always proceed sequentially from the most significant byte to the least significant byte, as previously described. Resetting the sequence counters select the most significant MDU. In a four MDU system, loading all MDU's results in the sequence counter pointing to the first MDU again. In all other configurations (1, 2, or 3 MDU's), the sequence counter must be reset prior to each series of register reads or writes.

2. Divide Operation

For the divide operation, the divisor is loaded in the X register. The dividend is loaded in the Y and Z registers with the more significant half in the Y register and the less significant half in the Z register. These registers may be loaded in any order, and after loading is completed, a control word is loaded to specify a divide operation and the number of MDU's and also to reset the sequence counters and Y or Z register and select the clock option if desired. Clearing the sequence counters with bit 6 will set the MDU's up for reading the results.

The X register will be unaltered by the operation. The quotient will be in the Z register while the remainder will be in the Y register. An overflow will be indicated by the $\overline{C.O./O.F.}$ of the most significant MDU and can also be determined by reading the status byte.

While the CDP1855 is specified to perform 16 by 8-bit divides, if the quotient of a divide operation exceeds the size of the Z register(s) (8N-bits - where N is the number of cascaded CDP1855's) the overflow bit in the Status Register will be set. Neither the quotient in Z nor the remainder in Y will represent a valid answer. This will always be the result of a division performed when the divisor (X) is equal to or less than the most significant 8N-bits of the dividend (Y).

The MDU can still be used for such computations if the divide is done in two steps. The dividend is split into two parts-the more significant 8N-bits and the less significant 8N-bits-and a divide done on each part. Each step yields an 8N-bit result for a total quotient of 16N-bits.

The first step consists of dividing the more significant 8N-bits by the divisor. This is done by clearing the Y register(s), loading the Z register(s) with the more significant 8N-bits of the dividend, and loading the X register(s) with the divisor. A division is performed and the resultant value in Z represents the more significant 8N-bits of the final quotient. The Z register(s) value must be unloaded and saved by the processor.

A second division is performed using the remainder from the first division (in Y) as the more significant 8N-bits of the dividend and the less significant half of the original dividend loaded into the Z register. The divisor in X remains unaltered and is, by definition, larger than the remainder from the first division which is in Y. The resulting value in Z becomes the less significant 8N-bits of the final quotient and the value in Y is, as usual, the remainder.

Extending this technique to more steps allows division of any size number by an 8N-bit divisor.

Note that division by zero is never permitted and must be tested for and handled in software.

The following example illustrates the use of this algorithm.

Example:

Assume three MDU's capable of a by 24-bit division. The problem is to divide 00F273, 491C06H by 0003B4H.

Step 1:	000000	,	00F273	/	0003B4	=	000041	R=0001BF
	Y		Z(MS)		X		Z1	Y1
Step 2:	0001BF	,	491C06	/	0003B4	=	78C936	R=00000E
	Y1		Z(LS)		X		Z2	Y2
Result:	000041	,	78C936		R=00000E			
	Z1		Z2		Y2			

The Z register can simply be reset using bit 2 of the control word and another divide can be done in order to further divide the remainder.

3. Multiply Operation

For a multiply operation the two numbers to be multiplied are loaded in the X and Z registers. The result is in the Y and Z register with Y being the more significant half and Z the less significant half. The X register will be unchanged after the operation is completed.

The original contents of the Y register are added to the product of X and Z. Bit 3 of the control word will reset register Y to 0 if desired.

Functional Description of CDP1855 Terminals

CE - Chip Enable (Input):

A high on this pin enables the CDP1855 MDU to respond to the select lines. All cascaded MDU's must be enabled together. CE also controls the three-state $\overline{C.O./O.F.}$, output of the most significant MDU.

$\overline{Clear}$ (Input):

The CDP1855 MDU(s) must be cleared upon power-on with a low-on this pin. The clear signal resets the sequence counters, the shift pulse generator, and bits 0 and 1 of the control register.

CTL - Control (Input):

This is an input pin. All CTL pins must be wired together and to the Y_L of the most significant CDP1855 MDU and to the Z_R of the least significant CDP1855 MDU. This signal is used to indicate whether the registers are to be operated on or only shifted.

$\overline{C.O./O.F.}$ - $\overline{Carry\ Out/Over\ Flow}$ (Output):

This is a three-state output pin. It is the CDP1855 $\overline{Carry\ Out}$ signal and is connected to $\overline{CI}$ ($\overline{CARRY\text{-}IN}$) of the next more significant CDP1855 MDU, except for on the most significant MDU. On that MDU it is an overflow indicator and is enabled when chip enables is true. A low on this pin indicates that an overflow has occurred. The overflow signal is latched each time the control register is loaded, but is only meaningful after a divide command.

Y_L, Y_R - Y-Left, Y-Right:

These are three-state bi-directional pins for data transfer between the Y registers of cascaded CDP1855 MDU's. The Y_R pin is an output and Y_L is an input during a multiply and the reverse is true at all other times. The Y_L pin must be connected to the Y_R pin of the next more significant MDU. An exception is that the Y_L pin of the most significant CDP1855 MDU must be connected to the Z_R pin of the least significant MDU and to the CTL pins of all MDU's. Also the Y_R pin of the least significant MDU is tied to the Z_L pin of the most significant MDU.

Z_L, Z_R - Z-Left, Z-Right:

These are three-state bi-directional pins for data transfers between the "Z" registers of cascaded MDU's. The Z_R pin is an output and Z_L is an input during a multiply and the reverse is true at all other times. The Z_L pin must be tied to the Y_R pin of the next more significant MDU. An exception is that the Z_L in of the most significant MDU must be connected to the Y_R pin of the least significant MDU. Also, the Z_R pin of the least significant MDU is tied to the Y_L of the most significant MDU.

$\overline{Shift}$ - $\overline{Shift\ Clock}$:

This is a three-state bi-directional pin. It is an output on the most significant MDU. And an input on all other MDU's. It provides the MDU system timing pulses. All $\overline{SHIFT}$ pins must be connected together for cascaded operation. A maximum of the 8N +1 shifts are required for an operation where "N" equals the number of MDU devices that are cascaded.

CLK - Clock (Input):

This pin should be grounded on all but the most significant MDU. There is an optional reduction of clock frequency available on this pin if so desired, controlled by bit 7 of the control byte.

STB - Strobe (Input):

When RD/WE is low, data is latched from bus lines on the falling edge of this signal. It may be asynchronous to the clock. Strobe also increments the selected register's sequence counter during reads and writes. TPB would be used in CDP1800 systems.

RD/$\overline{WE}$ - Read/$\overline{Write\ Enable}$ (Input):

This signal defines whether the selected register is to be read from or written to. In 1800 systems use $\overline{MRD}$ if MDU's are addressed as I/O devices, $\overline{MWR}$ is used if MDU's are addressed as memory devices.

RA2, RA1, RA0 - Register Address (Input):

These input signals define which register is to be read from or written to. It can be seen in the "CONTROL TRUTH TABLE" that RA2 can be used as a chip enable. It is identical to the CE pin, except only CE controls the three-state $\overline{C.O./O.F.}$ on the most significant MDU. In 1800 systems use N lines if MDU's are used as I/O devices, use address lines or function of address lines if MDU's are used as memory devices.

Bus 0 - Bus 7 - Bus Lines:

Three-state bi-directional bus for direct interface with CDP1800 series and other 8-bit microprocessors.

Z_R - Z-Right:

See Pin 6.

Y_R - Y-Right:

See Pin 5.

$\overline{CI}$- $\overline{Carry\ In}$ (Input):

This is an input for the carry from the next less significant MDU. On the least significant MDU it must be high (V_{DD}) on all others it must be connected to the $\overline{CO}$ pin of the next less significant MDU.

CN1, CN0 - Chip Number (Input):

These two input pins are wired high or low to indicate the MDU position in the cascaded chain. Both are high for the most significant MDU regardless of how many CDP1855 MDU's are used. Then CN1 = high and CN0 = low for the next MDU and so forth.

V_{SS} - Ground:

Power supply line.

V_{DD} - V+:

Power supply line.

CONTROL TRUTH TABLE

INPUTS (NOTE 1)						
CE	RA2 (N2)	RA1 (N1)	RA0 (N0)	RD/$\overline{WE}$ (MRD)	STB (TPB)	RESPONSE
0	X	X	X	X	X	No Action (Bus Floats)
X	0	X	X	X	X	No Action (Bus Floats)
1	1	0	0	1	X	X to Bus } Increment Sequence Counter When STB and RD = 1
1	1	0	1	1	X	Z to Bus } Increment Sequence Counter When STB and RD = 1
1	1	1	0	1	X	Y to Bus } Increment Sequence Counter When STB and RD = 1
1	1	1	1	1	X	Status to Bus
1	1	0	0	0	1	Load X from Bus } Increment Sequence Counter
1	1	0	1	0	1	Load Z from Bus } Increment Sequence Counter
1	1	1	0	0	1	Load Y from Bus } Increment Sequence Counter
1	1	1	1	0	1	Load Control Register
1	1	X	X	0	0	No Action (Bus Floats)

NOTE:

1. ( ) = 1800 System Signals. 1 = High Level, 0 = Low Level, X = High or Low Level.

CONTROL REGISTER BIT ASSIGNMENT TABLE

BUS 7	BUS 6	BUS 5	BUS 4	BUS 3	BUS 2	BUS 1	BUS 0

REGISTER RESET

B1	B0	OPERATION SELECT
0	0	No Operation
0	1	Multiply
1	0	Divide
1	1	Illegal State

B2 = 1, RESET Z REGISTER
B3 = 1, RESET Y REGISTER

B5	B4	NO. OF MDU's
1	1	One MDU
1	0	Two MDU's
0	1	Three MDU's
0	0	Four MDU's

NO. OF MDU's	SHIFT RATE
1	Clock ÷ 2
2	Clock ÷ 4
3	Clock ÷ 8
4	Clock ÷ 8

B6 = 1, RESET SEQUENCE COUNTER

B7 = 1, SELECT SHIFT RATE OPTIONS: ⟶
B7 = 0, SHIFT = CLOCK FREQUENCY RATE

STATUS REGISTER

	STATUS BYTE							
BIT	7	6	5	4	3	2	1	0
OUTPUT	0	0	0	0	0	0	0	O.F.

NOTES:

1. O.F. = 1 if overflow (only valid after a divide has been done)
2. Bits 1 - 7 are read as 0 always.

DELAY NEEDED WITH AND WITHOUT PRESCALER

8N + 1 Shifts/Operation at 1 Clock Cycle/Shift
N = Number of MDU's, S = Shift Rate

NO. OF MDU's	WITHOUT PRESCALER		WITH PRESCALER		
	SHIFTS = 8N +1 NEEDED	(NOTE 1) MACHINE CYCLES NEEDED	SHIFTS = S (8N +1) NEEDED	(NOTE 1) MACHINE CYCLES NEEDED	SHIFT RATE
1	9	2 (1 NOP)	18	3 (1 NOP)	2
2	17	2 (1 NOP)	68	9 (3 NOPs)	4
3	25	3 (1 NOP)	200	25 (9 NOPs)	8
4	33	4 (2 NOPs)	264	33 (11 NOPs)	8

NOTE:

1. NOP instruction is shown for machine cycles needed (3/NOP). Other instructions may be used.

CDP1855 Interfacing Schemes

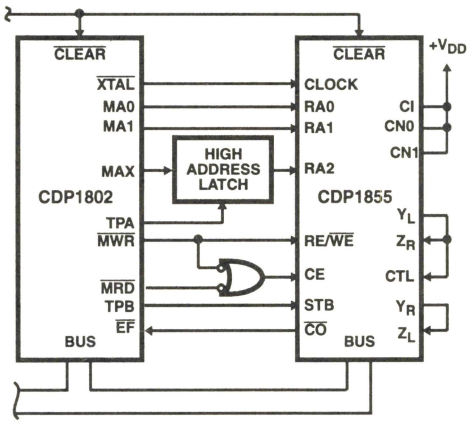


FIGURE 3. REQUIRED CONNECTION FOR MEMORY MAPPED ADDRESSING OF THE MDU

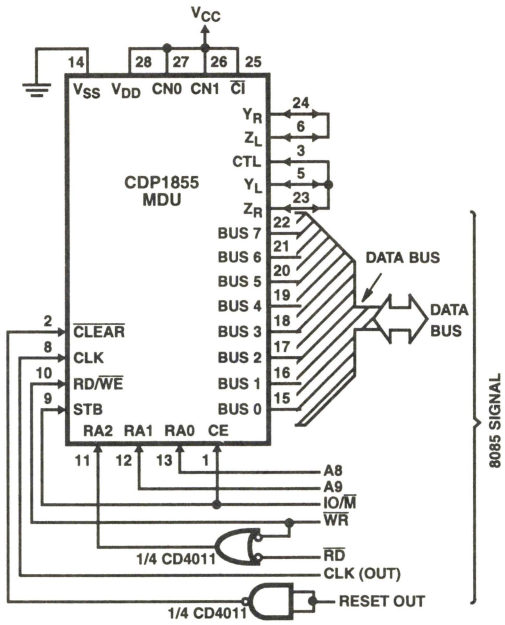


FIGURE 4. INTERFACING THE CDP1855 TO AN 8085 MICROPROCESSOR AS AN I/O DEVICE

Programming Example for Multiplication

For a 24-bit x 24-bit multiply using the system shown in Figure 5, the following is an assembly listing of a program to multiply $201F7C_{16}$ by $723C09_{16}$:

MEMORY LOCATION	OP CODE	LINE NO.	ASSEMBLY LANGUAGE
0000	F830;	0001	LDI 030H
0002	A2;	0002	PLO R2 . . LOAD 30 INTO R2.0
0003	F800;	0003	LDI 00H
0005	B2;	0004	PHI R2 . . LOAD 00 INTO R2.1 (R2=0030)
0006	6758;	0005	OUT 7; DC 058H . . LOAD CONTROL REGISTERS
0008	;	0006	. . SPECIFYING THREE MDU's
0008	;	0007	. . RESET THE Y REGISTER AND
0008	;	0008	. . SEQUENCE COUNTER
0008	6420;	0009	OUT 4; DC 020H . . LOAD MSB OF X REGISTER
000A	;	0010	. . WITH 20
000A	641F;	0011	OUT 4; DC 01FH . . LOAD NEXT MSB OF X REG
000C	;	0012	. . WITH 1F
000C	647C;	0013	OUT 4; DC 07CH . . LOAD LSB OF X REGISTER
000E	;	0014	. . WITH 7C
000E	6572;	0015	OUT 5; DC 072H . . LOAD MSB OF Z REGISTER
0010	;	0016	. . WITH 72

Programming Example for Multiplication

For a 24-bit x 24-bit multiply using the system shown in Figure 5, the following is an assembly listing of a program to multiply $201F7C_{16}$ by $723C09_{16}$: **(Continued)**

MEMORY LOCATION	OP CODE	LINE NO.	ASSEMBLY LANGUAGE
0010	653C;	0017	OUT 5; DC 030H . . LOAD NEXT MSB OF Z REG
0012	;	0018	. . WITH 3C
0012	6509;	0019	OUT 5; DC 09H . . LOAD LSB OF Z REGISTER
0014	;	0020	. . WITH 09
0014	6759;	0021	OUT 7; DC 059H . . LOAD CONTROL REGISTERS
0016	;	0022	. . RESETTING Y REGISTERS
0016	;	0023	. . AND SEQUENCE COUNTERS
0016	;	0024	. . AND STARTING MULTIPLY
0016	;	0025	. . OPERATION
DELAY FOR MULTIPLY TO FINISH			
0016	E2;	0026	SEX R2
0017	6E60;	0027	INP 6; IRX . . MSB OF RESULTS IS STORED
0019	;	0028	. . AT LOCATION 0030
0019	6E60;	0029	INP 6; IRX
001B	6E60;	0030	INP 6; IRX
001D	6D60;	0031	INP 5; IRX
001F	6D60;	0032	INP 5; IRX
0021	6D;	0033	INP 5 . . COMPLETE LOADING RESULT
0022	;	0034	. . INTO MEMORY LOCATIONS
0022	;	0035	. . 0030 TO 0035
0022	;	0036	. . RESULTS = 0E558DBA2B5C
0022	3022;	0037 STOP	BR STOP
0024	;	0038	END
0000			

The result of $201F7C_{16}$ x $723C09_{16}$ is 0E558DBA2B5C = 15760612797276_{10}. It will be stored in memory as follows:

LOC	BYTE
0030	0E
31	55
32	8D
33	BA
34	2B
35	5C

BEFORE MULTIPLY

	MDU1	MDU2	MDU3
REGISTER X	20	1F	7C
REGISTER Y	00	00	00
REGISTER Z	72	3C	09

AFTER MULTIPLY

	MDU1	MDU2	MDU3
REGISTER X	20	1F	7C
REGISTER Y	0E	55	8D
REGISTER Z	BA	2B	5C

Programming Example for Division

MEMORY LOCATION	OP CODE	LINE NO.	ASSEMBLY LANGUAGE	
0000	;	0001	. . Program example for a 16-bit by 8-bit divide using 1 CDP1855 MDU	
0000	;	0002	. . Gives a 16-bit answer with 8-bit remainder	
0000	;	0003		
0000	68C22000;	0004	RLDI R2, 2000H	. . Answer is stored at 2000 hex
0004	;	0005		. . Register 2 points to it
0004	68C33000;	0006	RLDI R3, 3000H	. . Dividend is stored at 3000 hex
0008	;	0007		. . Register 3 points to it
0008	68C44000;	0008	RLDI R4, 4000H	. . Divisor is stored at 4000 hex
000C	;	0009		. . Register 4 points to it
000C	;	0010		
000C	E067F0;	0011	SEX R4; OUT 7; DC OF0H	. . Write to the control register to use
000F	;	0012		. . clock/2; 1MDU; reset sequence
000F	;	0013		. . counter; and no operation
000F	;	0014		
000F	E464;	0015	SEX R4; OUT 4	. . Load the divisor into the X register
0011	;	0016		
0011	E06600;	0017	SEX R0; OUT 6; DC 0	. . Load 0 into the Y register
0014	E365;	0018	SEX R3; OUT 5	. . Load the most significant 8 bits of
0016	;	0019		. . the dividend into the Z register
0016	;	0020		
0016	E067F2;	0021	SEX R0; OUT 7; DC 0F2H	. . Do the first divide, also resets the
0019	;	0022		. . sequence counter
0019	;	0023		
0019	E26D60;	0024	SEX R2; INP 5; IRX	. . Read and store the most significant
001C	;	0025		. . 8 bits of the answer at 2000 hex
001C	;	0026		
001C	E067F0;	0027	SEX R0; OUT 7; DC 0F0H	. . Reset the sequence counter
001F	;	0028		
001F	E365;	0029	SEX R3; OUT 5	. . Load the 8 least significant 8 bits
0021	;	0030		. . of the original dividend into the Z
0021	;	0031		. . register
0021	;	0032		
0021	E067F2;	0033	SEX R0; OUT 7; DC 0F2H	. . Do the second division
0024	;	0034		
0024	E26D60;	0035	SEX R2; INP 5; IRX	. . Read and store the least significant
0027	;	0036		. . 8 bits of the answer at 2001 hex
0027	6E;	0037	INP 6	. . Read and store the remainder at 2002
0028	;	0038		. . hex
0000				

For the divide operation (Figure 5), the formula is:

$$\frac{Y_3Y_2Y_1Z_3Z_2Z_1}{X_3X_2X_1} = Z_3Z_2Z_1 + \frac{Y_3Y_2Y_1}{X_3X_2X_1}$$

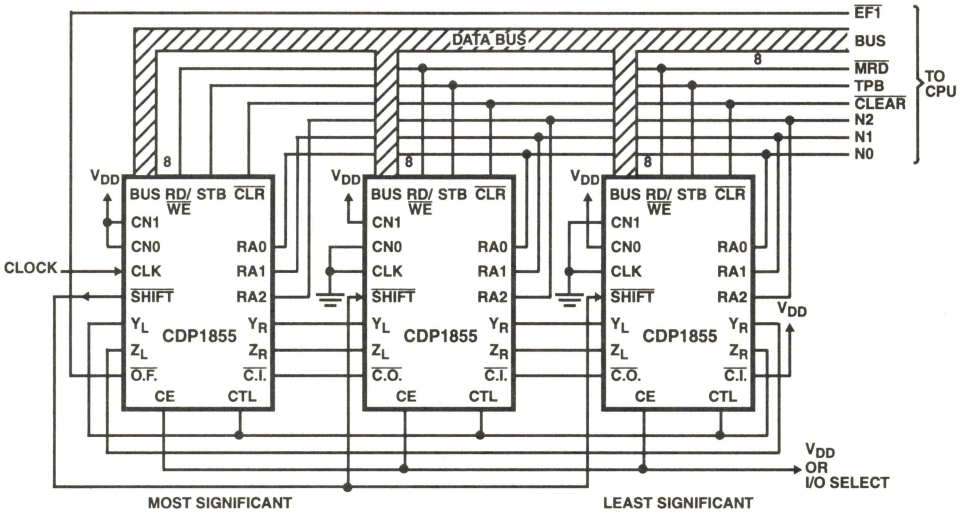


FIGURE 5. CASCADING THREE MDU's (CDP1855) IN AN 1800 SYSTEM WITH MDU's BEING ACCESSED AS I/O PORTS IN PROGRAMMING EXAMPLE

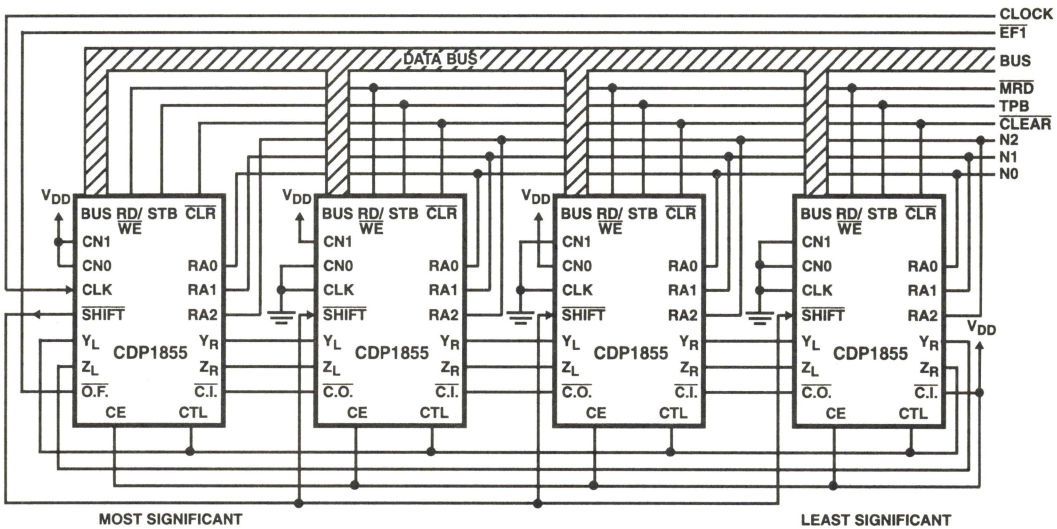


FIGURE 6. CASCADING FOUR MDU's (CDP1855)

Dynamic Electrical Specifications At T_A = -40 to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7V_{DD}, V_{IL} = 0.3V_{DD}, C_L = 100pF (See Figure 7)

(NOTE 1) PARAMETER		V_{DD} (V)	LIMITS						UNITS
			CDP1855			CDP1855C			
			MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX	
OPERATION TIMING									
Maximum Clock Frequency (Note 3)		5	3.2	4	-	3.2	4	-	MHz
		10	6.4	8	-	-	-	-	MHz
Maximum Shift Frequency (1 Device) (Note 4)		5	1.6	2	-	1.6	2	-	MHz
		10	3.2	4	-	-	-	-	MHz
Minimum Clock Width	t_{CLK0} t_{CLK1}	5	-	100	150	-	100	150	ns
		10	-	50	75	-	-	-	ns
Minimum Clock Period	t_{CLK}	5	-	250	312	-	250	312	ns
		10	-	125	156	-	-	-	ns
Clock to Shift Propagation Delay	t_{CSH}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	ns
Minimum C.I. to Shift Setup	t_{SU}	5	-	50	67	-	50	67	ns
		10	-	25	33	-	-	-	ns
C.O. from Shift Propagation Delay	t_{PLH} t_{PHL}	5	-	450	600	-	450	600	ns
		10	-	225	300	-	-	-	ns
Minimum C.I. from Shift Hold	t_H	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Minimum Register Input Setup	t_{SU}	5	-	-20	10	-	-20	10	ns
		10	-	-10	10	-	-	-	ns
Register after Shift Delay	t_{PLH} t_{PHL}	5	-	400	600	-	400	600	ns
		10	-	200	300	-	-	-	ns
Minimum Register after Shift Hold	t_H	5	-	50	100	-	50	100	ns
		10	-	25	50	-	-	-	ns
C.O. from C.I. Propagation Delay	t_{PLH} t_{PHL}	5	-	100	150	-	100	150	ns
		10	-	50	75	-	-	-	ns
Register from C.I. Propagation Delay	t_{PLH} t_{PHL}	5	-	80	120	-	80	120	ns
		10	-	40	60	-	-	-	ns

NOTES:

1. Maximum limits of minimum characteristics are the values above which all devices function.
2. Typical values are for T_A = 25°C and nominal voltages.
3. Clock frequency and pulse width are given for systems using the internal clock option of the CDP1855. Clock frequency equals shift frequency for systems not using the internal clock option.
4. Shift period for cascading of devices is increased by an amount equal to the $\overline{C.I.}$ to $\overline{C.O.}$ Propagation Delay for each device added.

Dynamic Electrical Specifications At T_A = -40 to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7V_{DD}, V_{IL} = 0.3V_{DD}, C_L = 100pF (See Figure 8)

(NOTE 1) PARAMETER		V_{DD} (V)	LIMITS						UNITS
			CDP1855			CDP1855C			
			MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX	
WRITE CYCLE									
Minimum Clear Pulse Width	$t_{\overline{CLR}}$	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Minimum Write Pulse Width	t_{WW}	5	-	150	225	-	150	225	ns
		10	-	75	115	-	-	-	ns
Minimum Data-In-Setup	t_{DSU}	5	-	-75	0	-	-75	0	ns
		10	-	-40	0	-	-	-	ns
Minimum Data-In-Hold	t_{DH}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Minimum Address to Write Setup	t_{ASU}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Minimum Address after Write Hold	t_{AH}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns

NOTES:

1. Maximum limits of minimum characteristics are the values above which all devices function.
2. Typical values are for T_A = 25°C and nominal voltages.

Dynamic Electrical Specifications At T_A = -40 to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7V_{DD}, V_{IL} = 0.3V_{DD}, C_L = 100pF (See Figure 9)

(NOTE 1) PARAMETER		V_{DD} (V)	LIMITS						UNITS
			CDP1855			CDP1855C			
			MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX	
READ CYCLE									
CE to Data Out Active	t_{CDO}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	ns
CE to Data Access	t_{CA}	5	-	300	450	-	300	450	ns
		10	-	150	225	-	-	-	ns
Address to Data Access	t_{AA}	5	-	300	450	-	300	450	ns
		10	-	150	225	-	-	-	ns
Data Out Hold after CE	t_{DOH}	5	50	150	225	50	150	225	ns
		10	25	75	115	-	-	-	ns
Data Out Hold after Read	t_{DOH}	5	50	150	225	50	150	225	ns
		10	25	75	115	-	-	-	ns
Read to Data Out Active	t_{RDO}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	ns
Read to Data Access	t_{RA}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	ns

Dynamic Electrical Specifications At T_A = -40 to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7V_{DD}, V_{IL} = 0.3V_{DD}, C_L = 100pF (See Figure 9) **(Continued)**

(NOTE 1) PARAMETER		V_{DD} (V)	LIMITS						UNITS
			CDP1855			CDP1855C			
			MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX	
Strobe to Data Access	t_{SA}	5	50	200	300	50	200	300	ns
		10	25	100	150	-	-	-	ns
Minimum Strobe Width	t_{SW}	5	-	150	225	-	150	225	ns
		10	-	75	115	-	-	-	ns

NOTES:

1. Maximum limits of minimum characteristics are the values above which all devices function.
2. Typical values are for T_A = 25°C and nominal voltages.

Timing Diagrams

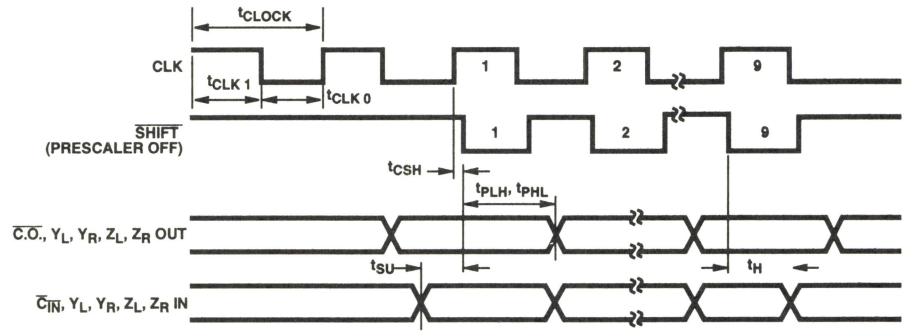


FIGURE 7. OPERATION TIMING DIAGRAM

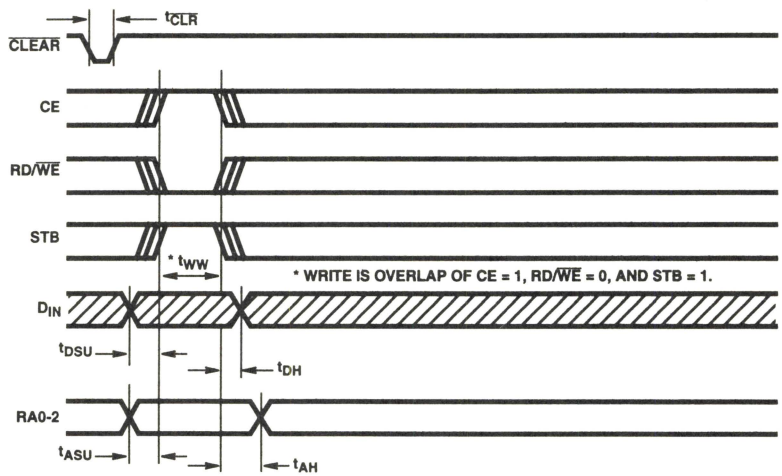


FIGURE 8. WRITE TIMING DIAGRAM

Timing Diagrams (Continued)

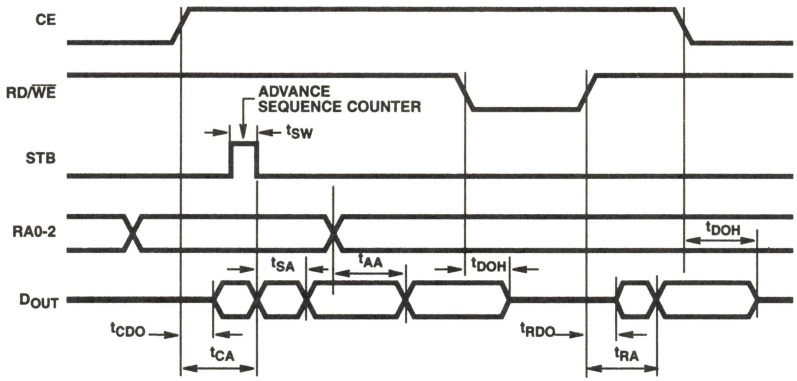


FIGURE 9. READ TIMING DIAGRAM

HARRIS SEMICONDUCTOR

CDP1857C

March 1997

4-Bit Bus Buffer/Separator

Features

- **Provides Easy Connection of I/O to CDP1800-Series Microprocessor Data Bus**
- **Non-Inverting Fully Buffered Data Transfer**

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
CDP1857CE	-40°C to +85°C	PDIP	E16.3
CDP1857CD	-40°C to +85°C	SBDIP	D16.3

TABLE 1. CDP1857 FUNCTION FOR I/O BUS SEPARATOR OPERATION

CS	$\overline{MRD}$	DATA BUS OUT DB0-DB3	DATA OUT DO0-DO3
0	X	High Impedance	High Impedance
1	0	High Impedance	Data Bus
1	1	Data In	High Impedance

Description

The CDP1857C is a 4-bit CMOS non-inverting bus separator designed for use in CDP1800-series microprocessor systems. It can be controlled directly by a 1800-series microprocessor without the use of additional components.

The CDP1857 is designed for use as a bus buffer or separator between the 1800-series microprocessor data bus and I/O devices. It provides a chip-select (CS) input signal which, when high (1), enables the bus-separator three-state output drivers. The direction of data flow, when enabled, is controlled by the $\overline{MRD}$ input signal.

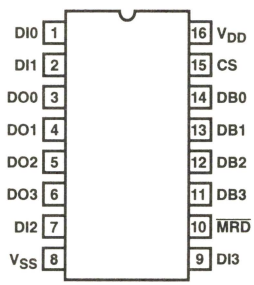
In the CDP1857, when $\overline{MRD}$ = 1, it enables the three-state bus drivers (DB0-DB3) and transfers data from the DATA-IN lines onto the data bus. When $\overline{MRD}$ = 0, it disables the three-state bus drivers (DB0-DB3) and enables the three-state data output drivers (DO0-DO3), thus, transferring data from the data bus to the DATA-OUT terminals.

The CDP1857 can be used as a bidirectional bus buffer by connecting the corresponding DI and DO terminals (Figure 1). The $\overline{MRD}$ output signal from the 1800-series microprocessor has the correct polarity to control the CDP1857 when it is used as I/O bus buffer/separator. Therefore, the 1800-series microprocessor $\overline{MRD}$ signal can be connected directly to the $\overline{MRD}$ input of CDP1857. See Function Table 1 for use of the CDP1857 as an I/O bus buffer/separator.

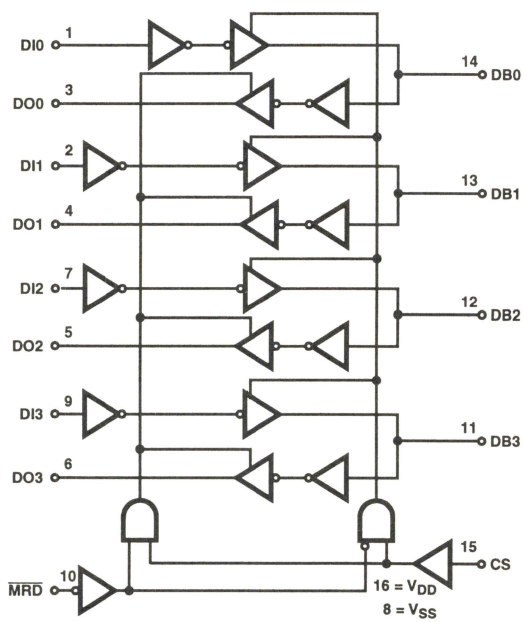
The CDP1857C is supplied in 16-lead hermetic, dual-in-line ceramic packages (D suffix), and in 16-lead plastic packages (E suffix).

Pinout

16 LEAD DIP
TOP VIEW



Functional Diagram For CDP1857



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1192.2**

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal) ..... -0.5V to +7V
Input Voltage Range, All Inputs ..... -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input ..... ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	85	N/A
SBDIP Package	85	22

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type D ..... -55°C to +125°C
Package Type E ..... -40°C to +85°C
Storage Temperature Range (T_{STG}) ..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At distance 1/16 ±1/32 In. (1.59 ± 0.79mm)
from case for 10s max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications

At T_A = -40°C to +85°C, Except as Noted:

PARAMETER	SYMBOL	CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	UNITS
Quiescent Device Current	I_{DD}	-	0, 5	5	-	5	50	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	-	mA
Output Voltage Low-Level (Note 3)	V_{OL}	-	0, 5	5	-	0	0.1	V
Output Voltage High-Level (Note 3)	V_{OH}	-	0, 5	5	4.9	5	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	-	1	µA
Operating Current (Note 2)	I_{DD1}	0, 5	0, 5	5	-	50	100	µA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	pF

NOTES:

1. Typical values are for T_A =+25°C and nominal voltage.
2. Operating current measured in a CDP1802 system at 3.2MHz with outputs floating.
3. $I_{OL} = I_{OH} = 1\mu A$.

Dynamic Electrical Specifications

At T_A = -40°C to +85°C, V_{DD} = 5V ±5%, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, t_R, t_F = 20ns, C_L = 100pF

PARAMETER	SYMBOL	V_{DD} (V)	(NOTE 1) TYP	MAX	UNITS
Propagation Delay Time:					
$\overline{MRD}$ or CS to DO	t_{ED}	5	150	225	ns
$\overline{MRD}$ or CS to DB	t_{EB}	5	150	225	ns
DI to DB	t_{IB}	5	100	150	ns
DB to DO	t_{BO}	5	100	150	ns

NOTE:

1. Typical values are for T_A = 25°C and nominal voltages.

Recommended Operating Conditions At T_A = Full Package Temperature Range.For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	MIN	MAX	UNITS
Supply-Voltage Range	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V

Timing Diagrams

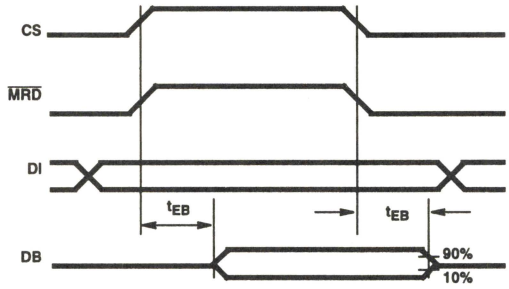


FIGURE 1A. ENABLE TO DB TIME

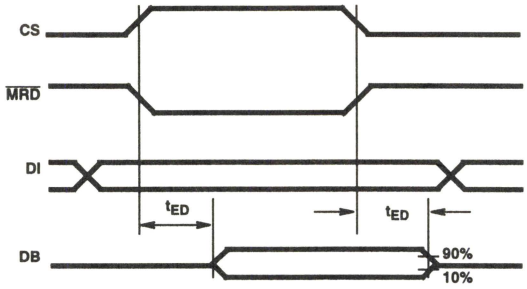


FIGURE 1B. ENABLE TO DO TIME

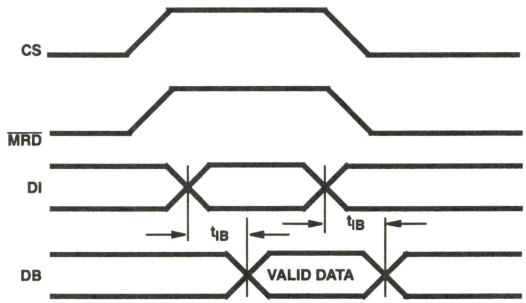


FIGURE 1C. DI TO DB TIME

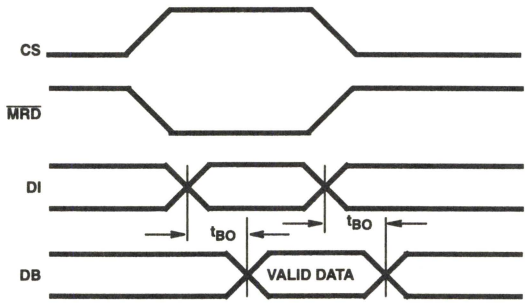


FIGURE 1D. DB TO DO TIME

FIGURE 1. TIMING DIAGRAMS FOR CDP1857C

Typical Applications

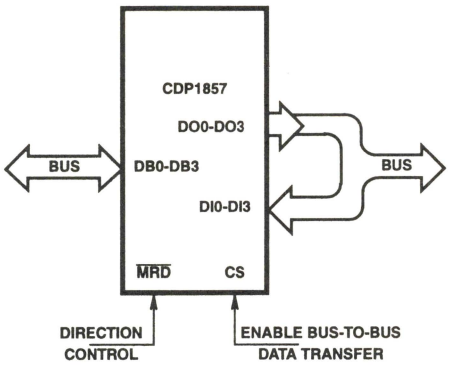


FIGURE 2. CDP1857 BIDIRECTIONAL BUS BUFFER OPERATION

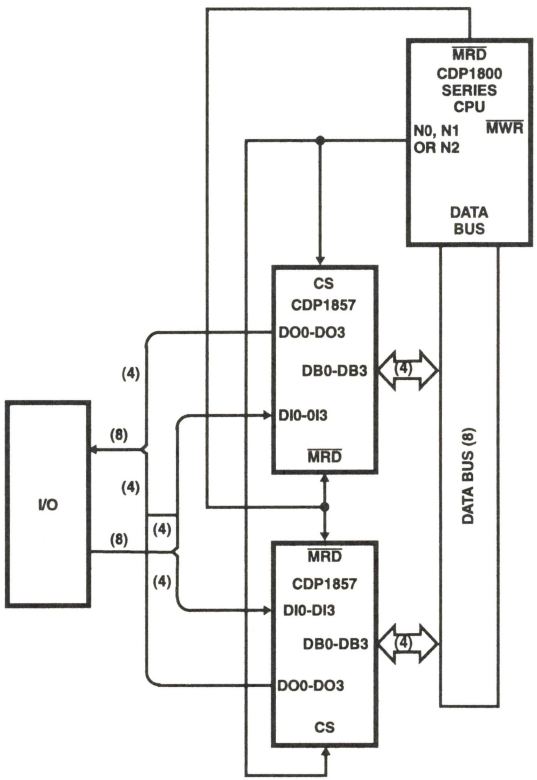


FIGURE 3. CDP1857 BUS SEPARATOR OPERATION

HARRIS SEMICONDUCTOR

CDP1871A, CDP1871AC

REFERENCE APP NOTE 7374

August 1996

CMOS Keyboard Encoder

Features

- Directly Interfaces with CDP1800-Series Microprocessor
- Low Power Dissipation
- Three-State Outputs
- Scans and Generates Code for 53 Key ASCII Keyboard Plus 32 HEX Keys (SPST Mechanical Contact Switches)
- Shift, Control, and Alpha Lock Input
- RC-Controlled Debounce Circuitry
- Single Supply 4V to 10.5V..... (CDP1871A)
  4V to 6.5V..... (CDP1871AC)
- N-Key Lockout

Ordering Information

PACKAGE	TEMP. RANGE	5V	10V	PKG. NO.
PDIP	-40°C to +85°C	CDP1871ACE	CDP1871AE	E40.6
PLCC	-40°C to +85°C	CDP1871ACQ	-	N44.65
SBDIP	-40°C to +85°C	CDP1871ACD	CDP1871AD	D40.6
Burn-In		CDP1871ACDX	-	D40.6

Description

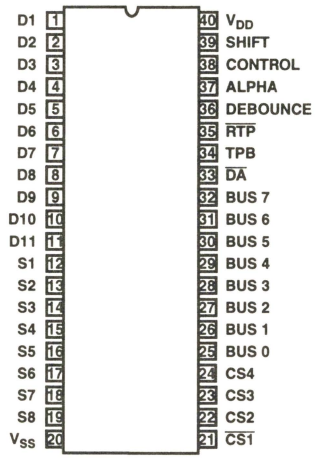
The CDP1871A is a keyboard encoder designed to directly interface between a CDP1800-series microprocessor and a mechanical keyboard array, providing up to 53 ASCII coded keys and 32 HEX coded keys, as shown in the system diagram (Figure 1).

The keyboard may consist of simple single-pole single-throw (SPST) mechanical switches. Inputs are provided for alpha-lock, control, and shift functions, allowing 160 unique codes. An external R-C input is available for user-selectable debounce times. The N-key lock-out feature prevents unwanted key codes if two or more keys are pressed simultaneously.

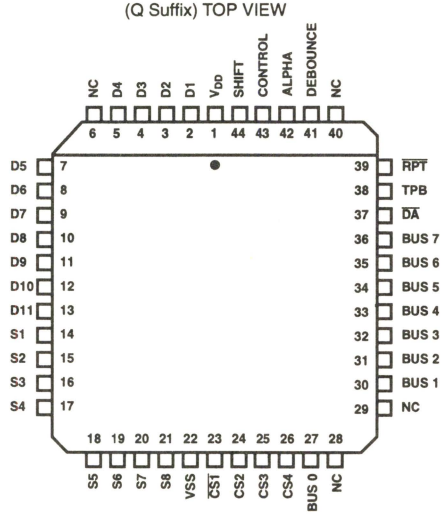
The CDP1871A and CDP1871AC are functionally identical. They differ in that the CDP1871A has a recommended operating voltage range of 4V to 10.5V, and the CDP1871AC has a recommended operating voltage range 4V to 6.5V. These types are supplied in 40 lead dual-in-line ceramic packages (D suffix), and 40 lead dual-in-line plastic packages (E suffix), and 44 lead plastic chip-carrier packages (Q suffix).

Pinouts

40 LEAD PDIP, CERDIP
TOP VIEW



44 LEAD PLCC
(Q Suffix) TOP VIEW



File Number **1374.2**

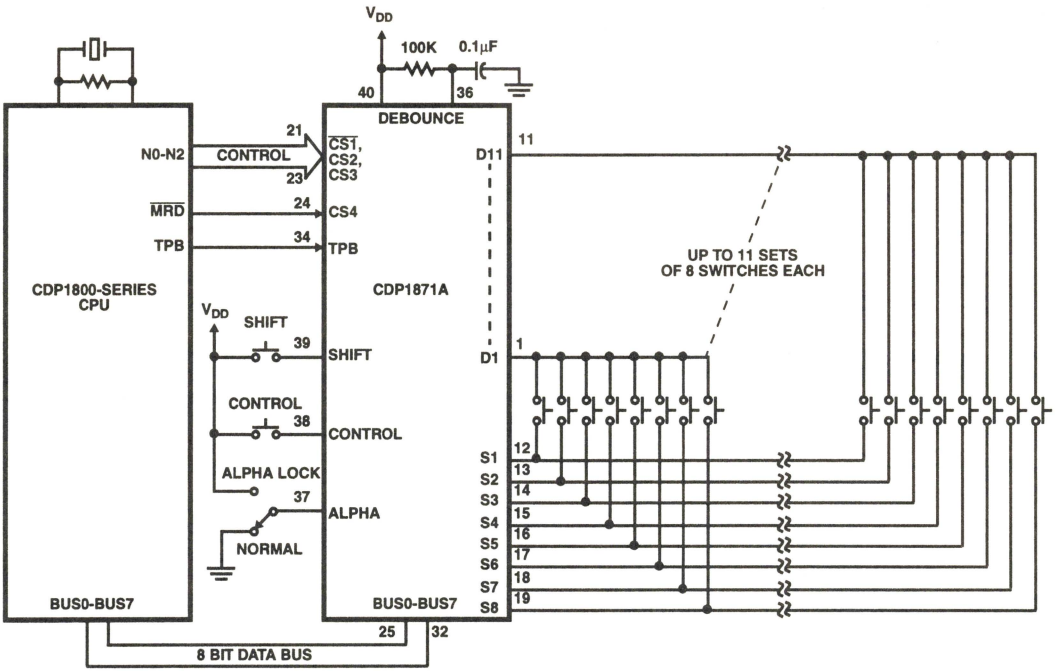


FIGURE 1. TYPICAL CDP1800 SERIES MICROPROCESSOR SYSTEM USING THE CDP1871A

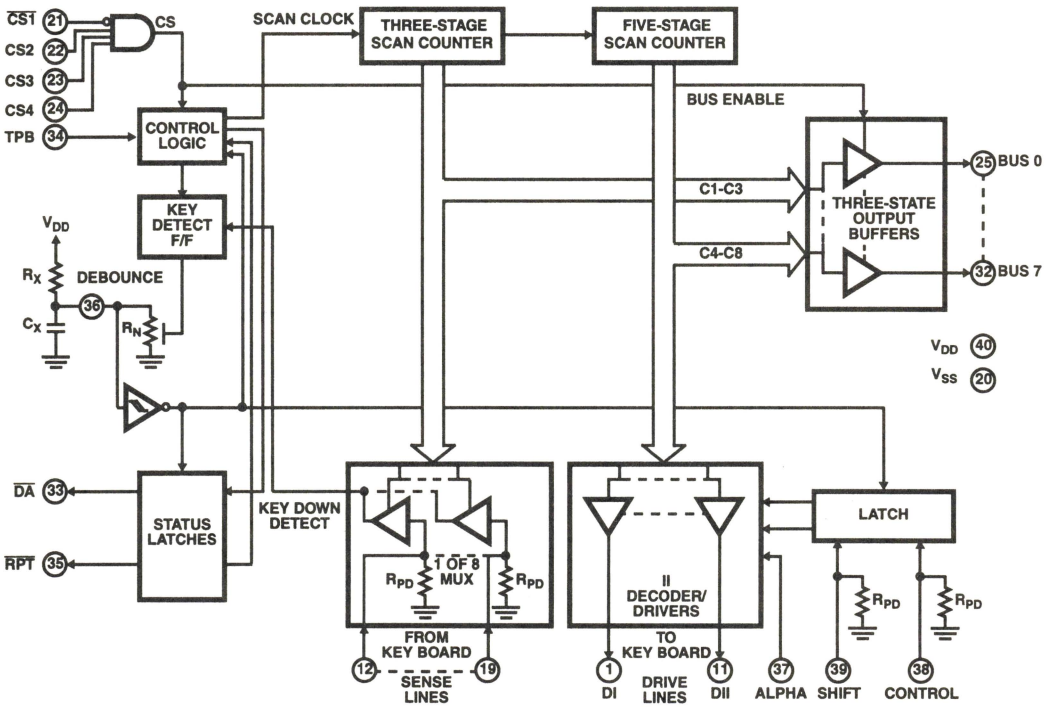


FIGURE 2. CDP1871A BLOCK DIAGRAM

Absolute Maximum Ratings

(All Voltages Referenced to V_{SS} Terminal)
CDP1871A. . . . . -0.5V to +11V
CDP1871AC . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, any One Input . . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	60	N/A
PLCC Package	50	N/A
SBDIP Package	60	18

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type D . . . . . -55°C to +125°C
Package Type E and Q . . . . . -40°C to +85°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ± 1/32 In. (1.59 ± 0.79mm)
from case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

At T_A = -40 to +85°C. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER		V_{DD} (V)	LIMITS				UNITS
			CDP1871AD, CDP1871AE		CDP1871ACD, CDP1871ACE		
			MIN	MAX	MIN	MAX	
Supply Voltage Range			4	10.5	4	6.5	V
Recommended Input Voltage Range			V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Clock Input Frequency, TPB (Keyboard Capacitance = 200 pF)	f_{CL}	5	DC	0.4	DC	0.4	MHz
		10	DC	0.8	-	-	MHz

NOTE:
1. Printed-circuit board mount: 57mm x 57mm minimum area x 1.6mm thick G10 epoxy glass, or equivalent.

Static Electrical Specifications

At T_A = -40 to +85°C, Unless Otherwise Specified

PARAMETER		CONDITIONS			LIMITS						
					CDP1871AD CDP1871AE			CDP1871ACD CDP1871ACE			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE1) TYP	MAX	UNITS
Quiescent Device Current	I_{DD}	-	0.5	5	-	0.1	50	-	1	200	µA
		-	0, 10	10	-	1	200	-	-	-	µA
Output Low Drive (Sink) Current (Except Debounce and D1-D11)	I_{OL}	0.4	0, 5	5	0.5	1	-	0.5	1	-	mA
		0.5	0, 10	10	1	2	-	-	-	-	mA
Debounce	I_{OL}	0.4	0, 5	5	0.75	1.5	-	0.75	1.5	-	mA
		0.5	0, 10	10	1	2	-	-	-	-	mA
D1-D11	I_{OL}	0.4	0, 5	5	0.05	0.1	-	0.05	0.1	-	mA
		0.5	0, 10	10	0.1	0.2	-	-	-	-	mA

Static Electrical Specifications At T_A = -40 to +85°C, Unless Otherwise Specified **(Continued)**

PARAMETER		CONDITIONS			LIMITS						UNITS
					CDP1871AD CDP1871AE			CDP1871ACD CDP1871ACE			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE1) TYP	MAX	
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-0.3	-0.6	-	-0.3	-0.6	-	mA
		9.5	0, 10	10	-0.75	-1.5	-	-	-	-	mA
Input Low Voltage (Except Debounce)	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		1, 9	-	10	-	-	3	-	-	-	V
Input High Voltage (Except Debounce)	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
		1, 9	-	10	7	-	-	-	-	-	V
Debounce Schmitt Trigger Input Voltage	V_D	0.4	-	5	2.0	3.3	4.0	2.0	3.3	4.0	V
Positive Trigger Voltage		0.5	-	10	4.0	6.3	8.0	-	-	-	V
Negative Trigger Voltage	V_N	0.4	-	5	0.8	1.8	3.0	0.8	1.8	3.0	V
		0.5	-	10	1.9	4.0	6.0	-	-	-	V
Hysteresis	V_H	0.4	0, 5	5	0.3	1.6	2.6	0.3	1.6	2.6	V
		0.5	0, 10	10	0.7	2.3	4.7	-	-	-	V
Output Voltage Low Level	V_{OL}	-	0, 5	5	-	0	0.05	-	0	0.05	V
		-	0, 10	10	-	0	0.05	-	-	-	V
Output Voltage High Level	V_{OH}	-	0, 5	5	4.95	5	-	4.95	5	-	V
		-	0, 10	10	9.95	10	-	-	-	-	V
Input Leakage Current (Except S1-S8, Shift, Control)	I_{IN}	-	0, 5	5	-	0.01	1	-	0.01	1	µA
		-	0, 10	10	-	0.01	1	-	-	-	µA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	0.01	1	-	0.02	2	µA
		0, 10	0, 10	10	-	0.02	2	-	-	-	µA
Pull-Down Resistor Value (S1-S8, Shift, Control)	R_{PD}	-	-	-	7	14	24	7	14	24	kΩ
Operating Current (All Outputs Unloaded)											
f_{CL} = 0.4MHz	I_{OPER}	0.5, 4.5	0, 5	5	-	0.6	-	-	0.6	-	mA
f_{CL} = 0.8MHz		1, 9	0, 10	10	-	2.7	-	-	-	-	mA

NOTE:

1. Typical values are for T_A = +25°C and nominal V_{DD}.

Functional Description of CDP1871A Terminals

D1 - D11 (Outputs):

Drive lines for the 11 x 8 keyboard switch matrix. These outputs are connected through the external switch matrix to the sense lines (S1 - S8).

S1 - S8 (Inputs):

Sense lines for the 11 x 8 keyboard maxtrix. These inputs have internal pull-down resistors and are driven high by appropriate drive line when a keyboard switch is closed.

$\overline{CS1}$, CS2, CS3, CS4 (Inputs):

Chip select inputs, which are used to enable the three-state data bus outputs (BUS 0 - BUS 7) and to enable the resetting of the status flag ($\overline{DA}$), which occurs on the low-to-high transition of TPB. These four inputs are normally connected to the N-lines (N0-N2) and $\overline{MRD}$ output of the CDP1800-series microprocessor. (Table 2)

BUS 0 - BUS 7 (Outputs):

Three-state data bus outputs which provide the ASCII and HEX codes of the detected keys. The outputs are normally connected to the BUS 0 - BUS 7 terminals of the CDP1800-series microprocessor.

$\overline{DA}$ (Output):

The data available output flag which is set low when a valid key closure is detected. It is reset high by the low-to-high transition of TPB when data is read from the CDP1871A. This output is normally connected to a flag input ($\overline{EF1}$ - $\overline{EF4}$) of the CDP1800-series microprocessor.

TPB (Input):

The input clock used to drive the scan generator and reset the status flag ($\overline{DA}$). This input is normally connected to the TPB output of the CDP1800-series microprocessor.

$\overline{RPT}$ (Output):

The repeat output flag which is used to indicate that a key is still closed after data has been read from the CDP1871A ($\overline{DA}$ = high). It remains low as long as the key is closed and is used for an autorepeat function, under CPU control. This output is normally connected to a flag input ($\overline{EF1}$ - $\overline{EF4}$) of the CDP1800-series microprocessor.

DEBOUNCE (Input):

This input is connected to the junction of an external resistor to V_{DD} and capacitor to V_{SS}. It provides a debounce time delay ($t \cong RC$) after the release of a key. If a debounce is not desired, the external pull-up resistor is still required.

ALPHA, SHIFT, CONTROL (Inputs):

A high on the SHIFT or CONTROL inputs will be internally latched (after the debounce time) and the drive and sense line decoding will be modified as shown in Table 3. They are normally connected to the keyboard, but produce no code by themselves. The SHIFT and CONTROL inputs have internal pull-down resistors to simplify use with momentary contact switches. The ALPHA input is not latched and is designed for a standard SPDT switch to provide an alpha-lock function. When ALPHA = 1 the drive and sense line decoding will be modified as shown in Table 3.

V_{DD}, V_{SS}:

V_{DD} is the positive supply voltage input. V_{SS} is the most negative supply voltage terminal and is normal connected to ground. All outputs swing from V_{SS} to V_{DD}. The recommended input voltage swing is from V_{SS} to V_{DD}.

TABLE 1. SWITCH INPUT FUNCTIONS

CONTROL	SHIFT	ALPHA	KEY FUNCTION
0	0	0	Normal
1	X	X	Control
0	1	X	Shift
0	0	1	Alpha

NOTE: X = Don't Care

TABLE 2. VALID N-LINE CONNECTIONS

CPU	CDP1871A SIGNAL				CPU INPUT INSTRUCTION
	CS4	CS3	CS2	$\overline{CS1}$	
CDP1800- Series Signal	$\overline{MRD}$	N2	N0	N1	INP5
	$\overline{MRD}$	N0	N1	N2	INP3
	$\overline{MRD}$	N2	N1	N0	INP6

TABLE 3. DRIVE AND SENSE LINE KEYBOARD CONNECTIONS (NOTE 2)

SENSE LINES	DRIVE LINES															
	D_1		D_2		D_3		D_4		D_5		D_6		D_7	D_8	D_9	D_{10}	D_{11}
S_1	SP	0	(	8	‘	@	H	H	P	P	X	X	Space	80_{16}	88_{16}	90_{16}	98_{16}
	0		8		@	NUL	h	BS	p	DLE	x	CAN					
S_2	!	1	)	9	A	A	I	I	Q	Q	Y	Y		81_{16}	89_{16}	91_{16}	99_{16}
	1		9		a	SOH	i	HT	q	DC1	y	EM					
S_3	“	2	*	:	B	B	J	J	R	R	Z	Z	Line Feed	82_{16}	$8A_{16}$	92_{16}	$9A_{16}$
	2		:		b	STX	j	LF	r	DC2	z	SUB					
S_4	#	3	+	;	C	C	K	K	S	S	{	[	Escape	83_{16}	$8B_{16}$	93_{16}	$9B_{16}$
	3		;		c	ETX	k	VT	s	DC3	[	ESC					
S_5	$	4	<	,	D	D	L	L	T	T	|	\		84_{16}	$8C_{16}$	94_{16}	$9C_{16}$
	4		,		d	EOT	l	FF	t	DC4	\	FS					
S_6	%	5	=	-	E	E	M	M	U	U	}	]	Carriage Return	85_{16}	$8D_{16}$	95_{16}	$9D_{16}$
	5		-		e	ENQ	m	CR	u	NAK	]	GS					
S_7	&	6	>	.	F	F	N	N	V	V	~	↑		86_{16}	$8E_{16}$	96_{16}	$9E_{16}$
	6		.		f	ACK	n	SO	v	SYN	↑	RS					
S_8	‘	7	?	/	G	G	O	O	W	W	Del	-	Delete	87_{16}	$8F_{16}$	97_{16}	$9F_{16}$
	7		/		g	BEL	o	SI	W	ETB	-	US					

KEY:

SHIFT (Note 1)	ALPHA (Note 1)
NORMAL	CONTROL (Note 1)

NOTES:

1. CONTROL overrides SHIFT and ALPHA = No Response
2. Showing ASCII outputs for all combinations with and without SHIFT, ALPHA LOCK and CONTROL.
3. Drive lines 8, 9, 10 and 11 generate non-ASCII hex values which can be used for special codes.

TABLE 4. HEXIDECIMAL VALUES OF ASCII CHARACTERS

						MSD							
					b7 →	0	0	0	0	1	1	1	1
					b6 →	0	0	1	1	0	0	1	1
BITS					b5 →	0	1	0	1	0	1	0	1
	b4	b3	b2	b1	HEX ↓	0	1	2	3	4	5	6	7
LSD	0	0	0	0	0	NUL	DLE	SP	0	@	P	\	p
	0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
	0	0	1	0	2	STX	DC2	"	2	B	R	b	r
	0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
	0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
	0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
	0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
	0	1	1	1	7	BEL	ETB	/	7	G	W	g	w
	1	0	0	0	8	BS	CAN	(	8	H	X	h	x
	1	0	0	1	9	HT	EM	)	9	I	Y	i	y
	1	0	1	0	A	LF	SUB	*	:	J	Z	j	z
	1	0	1	1	B	VT	ESC	+	;	K	[	k	{
	1	1	0	0	C	FF	FS	,	<	L	\	l	|
	1	1	0	1	D	CR	GS	-	=	M	]	m	}
	1	1	1	0	E	SO	RS	.	>	N	↑	n	~
	1	1	1	1	F	SI	US	/	?	O	-	o	DEL

Operation

The CDP1871A is made up of two major sections: the counter/scan-selection logic and the control logic (Figure 2). The counter and scan-selection logic scans the keyboard array using the drive lines (D1-D11) and the sense lines (S1-S8). The outputs of the internal 5-stage scancounter are conditionally encoded by the ALPHA, SHIFT, and CONTROL inputs (Table 1, Table 3) and are used to drive the D1-D11 output lines high one at a time. Each D1-D11 output may drive up to eight keys, which are sampled by the sense line inputs (S1-S8). The S1-S8 inputs are enabled by the internal 3-stage scancounter.

The control logic interfaces with the CDP1800-series I/O and timing signals to establish timing and status conditions for the CDP1871A.

The TPB input clocks the scancounters and is also used to reset the Data Available output ($\overline{DA}$). When a valid keydown condition is detected on a sense line, the control logic inhibits the clock to the scancounters on the next low-to-high transition of TPB and the $\overline{DA}$ output is set low. The scancounter outputs (C1 - C8) represent the ASCII and HEX key codes and are used to drive the BUS 0 - BUS 7 outputs, which interface directly to the CDP1800-Series data bus. The BUS 0 - BUS 7 outputs, which are normally three-stated, are enabled by decoding the CS inputs during a CPU input instruction (Table 2). The low-to-high transition of TPB during the input instruction resets the $\overline{DA}$ output high. Once the $\overline{DA}$ output has been reset, it cannot go low again until the present key is released and a new keydown condition is detected. (This prevents unwanted repeated keycode outputs which may be caused by fast software routines).

After the depressed key is released and the debounce delay (determined by RX, CX) has occurred, the scan clock inhibit is removed, allowing the scancounters to advance on the following high-to-low transitions of TPB. This provides an N-key lockout feature, which prevents the entry of erroneous codes when two or more keys are pressed simultaneously. The first key pressed in the scanning order is recognized, while all other keys pressed are ignored until the first key is released

and read by the CPU, at which time the next key pressed in the scanning order is detected. If the first key remains closed after the CPU reads the data and resets the $\overline{DA}$ output, on the low-to-high transition of TPB, an auxiliary signal ($\overline{RPT}$) is generated and is available to the CPU to indicate an auto-repeat condition. The $\overline{RPT}$ output is reset high at the end of the debounce delay after the depressed key is released.

The DEBOUNCE input provides a terminal connection for an external user-selected RC circuit to eliminate false detection of a keydown condition caused by keyboard noise. The operation of the DEBOUNCE circuit is shown in Figure 2 (Pin 36). When a valid keydown is detected, the on-chip active-resistor device (R_N) is enabled and the external capacitor (C_X) is discharged, providing a key closure debounce time $\cong R_N C_X$. This discharge is sensed by the Schmitt-trigger inverter, which clocks the $\overline{DA}$ flip-flop (latching the $\overline{DA}$ output low and inhibiting the scan clock). (The $\overline{DA}$ F/F is reset by the low-to-high transition of TPB when the CS inputs are enabled). When a valid key-release is detected RN is disabled and C_X begins to charge through the external resistor (R_X), providing a key-release debounce time $\cong R_X C_X$. This charge time is again sensed by the Schmitt-trigger inverter, enabling the scan clock to continue on the next high-to-low transitions of TPB, after the current keycode data is read by the CPU.

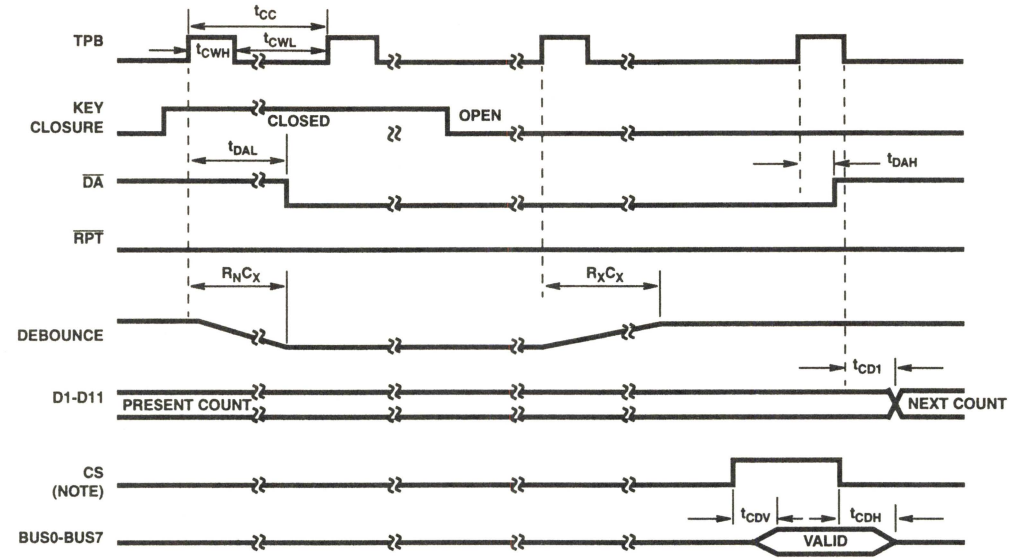
Dynamic Electrical Specifications

At T_A = -40 to +85°C, V_{DD} ±5%, Unless Otherwise Specified

PARAMETER		V_{DD} (V)	LIMITS						UNITS
			CDP1871AD, CDP1871AE			CDP1871ACD, CDP1871ACE			
			MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Clock Cycle Time	t_{CC}	5	-	-	-	-	-	-	Note 2
		10	-	-	-	-	-	-	Note 2
Clock Pulse Width High	t_{CWH}	5	100	40	-	100	40	-	ns
		10	50	20	-	-	-	-	ns
Data Available Valid Delay	t_{DAL}	5	-	260	500	-	260	500	ns
		10	-	130	250	-	-	-	ns
Data Available Invalid Delay	t_{DAH}	5	-	70	150	-	70	150	ns
		10	-	35	75	-	-	-	ns
Scan Count Delay (Non-Repeat)	t_{CD1}	5	-	850	1900	-	850	1900	ns
		10	-	425	950	-	-	-	ns
Data Out Valid Delay	t_{CDV}	5	-	120	250	-	120	250	ns
		10	-	60	125	-	-	-	ns
Data Out Hold Time	t_{CDH}	5	-	100	200	-	100	200	ns
		10	-	50	100	-	-	-	ns
Repeat Valid Delay	t_{RPL}	5	-	150	400	-	150	400	ns
		10	-	75	200	-	-	-	ns
Repeat Invalid Delay	t_{RPH}	5	-	350	700	-	350	700	ns
		10	-	170	350	-	-	-	ns

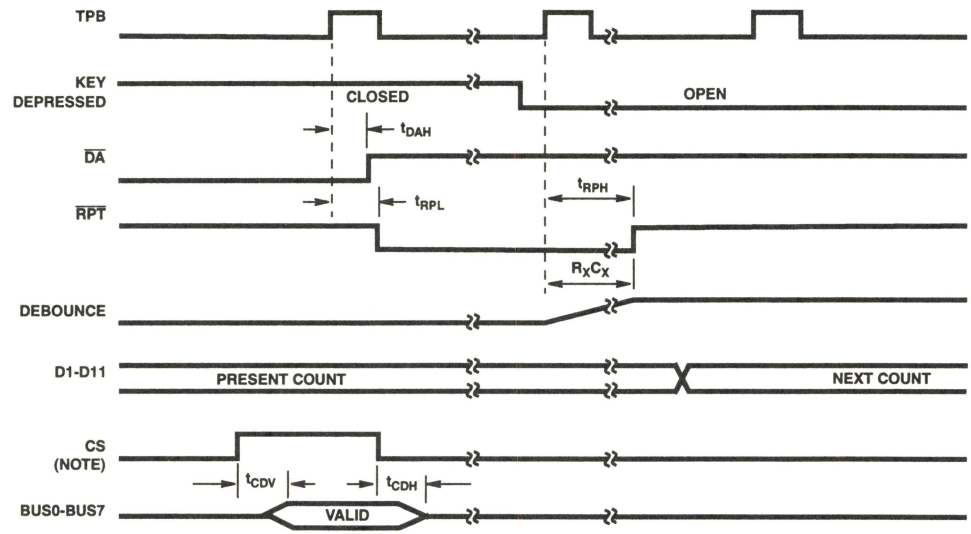
NOTES:

1. Typical values are for T_A = +25°C and nominal V_{DD}.
2. $t_{CC} = t_{CWH} + t_{CWL}$
   $t_{CWL} = t_{CD1} + KC$
   k = 0.9ns per pF
   c = Keyboard capacitance (pF)



NOTE: CS = $\overline{CS1}$ • CS2 • CS3 • CS4
$\overline{CS1}$, CS2, CS3 = (CPU N-LINES)
CS4 ($\overline{MRD}$) is High for CPU Input Instruction

FIGURE 3. CDP1871A DYNAMIC TIMING DIAGRAM (NON-REPEAT)



NOTE: CS = $\overline{CS1}$ • CS2 • CS3 • CS4
$\overline{CS1}$, CS2, CS3 = (CPU N-LINES)
CS4 ($\overline{MRD}$) is High for CPU Input Instruction

FIGURE 4. FIGURE 4. CDP1871A DYNAMIC TIMING DIAGRAM (REPEAT)

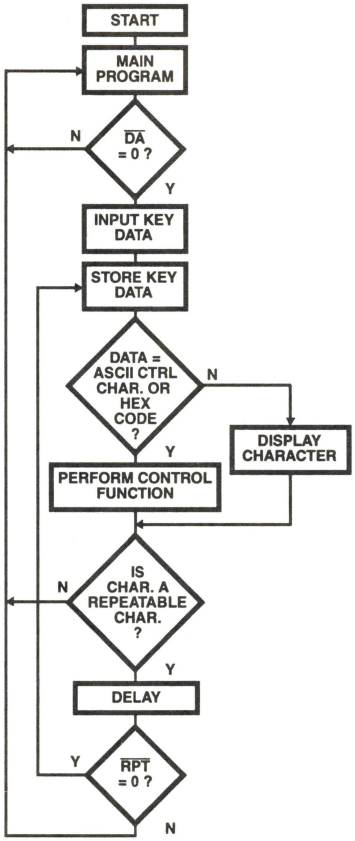


FIGURE 5. TYPICAL SYSTEM SOFTWARE FLOWCHART FOR CDP1871A, CDP1871AC

CDP1872C, CDP1874C, CDP1875C

March 1997

High-Speed 8-Bit Input and Output Ports

Features

- Parallel 8-Bit Input/Output Register with Buffered Outputs
- High-Speed Data-In to Data-Out 85ns (Max) at V_{DD} = 5V
- Flexible Applications In Microprocessor Systems as Buffers and Latches
- High Order Address-Latch Capability in CDP1800-Series Microprocessor Systems
- Output Sink Current = 5mA (Min) at V_{DD} = 5V
- Three-State Output - CDP1872C and CDP1874C

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
CDP1872CE	-40°C to +85°C	PDIP	E22.4
CDP1874CE	-40°C to +85°C	PDIP	E22.4
CDP1875CE	-40°C to +85°C	PDIP	E22.4

Description

The CDP1872C, CDP1874C and CDP1875C devices are high-speed 8-bit parallel input and output ports designed for use in the CDP1800 microprocessor system and for general use in other microprocessor systems. The CDP1872C and CDP1874C are 8-bit input ports; the CDP1875C is an 8-bit output port.

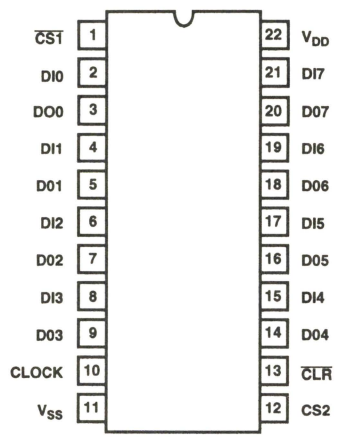
These devices have flexible capabilities as buffers and data latches and are reset by $\overline{CLR}$ input when the data strobe is not active.

The CDP1872C and CDP1874C are functionally identical except for device selects.The CDP1872C has one active low and one active high select; the CDP1874C has two active high device selects. These devices also feature Three-state outputs when deselected. Data is strobed into the register on the leading edge of the CLOCK and latched on the trailing edge of the CLOCK.

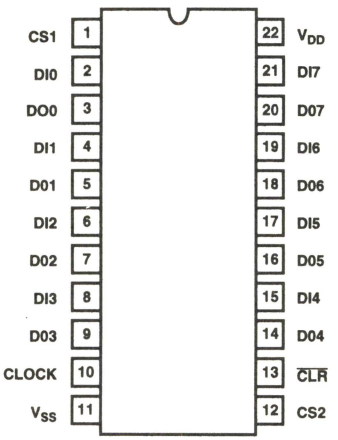
The CDP1875C is an output port with data latched into the registers when the device selects are active. There are two active high and one active low selects. The output buffers are enabled at all times.

Pinouts

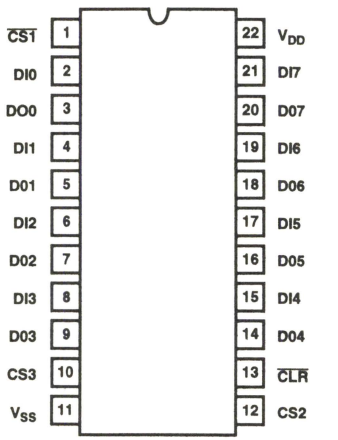
CDP1872C INPUT PORT (PDIP) TOP VIEW



CDP1874C INPUT PORT (PDIP) TOP VIEW



CDP1875C OUTPUT PORT (PDIP) TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1255.2**

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD}) . . . . . -0.5V to +7V
(Voltage referenced to V_{SS} Terminal)
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA

Thermal Information

Thermal Resistance (Typical) θ_{JA} (^{o}C/W)
PDIP Package 75
Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type E . . . . . -40°C to +85°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ± 1/32 In. (1.59 ± 0.79mm)
from case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

At T_A = -40 to +85°C. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS ALL TYPES	UNITS
DC Operating-Voltage Range	4 to 6.5	V
Input Voltage Range	V_{SS} to V_{DD}	V

Static Electrical Specifications

At T_A = -40 to +85°C, V_{DD} ±5%, Unless Otherwise Specified.

PARAMETER		TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{IN} (V)	TEST CONDITIONS V_{DD} (V)	LIMITS ALL TYPES MIN	LIMITS ALL TYPES (NOTE 1) TYP	LIMITS ALL TYPES MAX	UNITS
Quiescent Device Current	I_{DD}	-	0, 5	5	-	25	50	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	5	10	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-4	-7	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	V
Output Voltage High-Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	V
Input Leakage Current	I_{IN}	-	0, 5	5	-	-	±1	µA
Three-State Output Leakage Current (Note 3)	I_{OUT}	0, 5	0, 5	5	-	-	±5	µA
Input Capacitance	C_{IN}	-	-	-	-	15	-	pF
Output Capacitance (Note 3)	C_{OUT}	-	-	-	-	15	-	pF

NOTES:

1. Typical values are for T_A = +25°C and nominal V_{DD} ±5%.
2. $I_{OL} = I_{OH}$ = 1µA
3. For CDP1872C and CDP1874C only.

Logic Diagrams

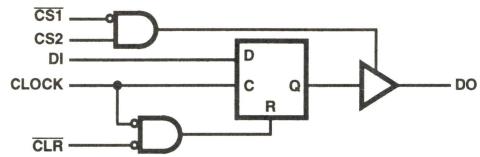


FIGURE 1. EQUIVALENT LOGIC DIAGRAM (1 OF 8 LATCHES SHOWN) FOR CDP1872C

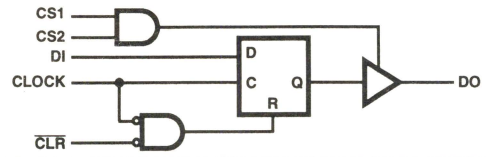


FIGURE 2. EQUIVALENT LOGIC DIAGRAM (1 OF 8 LATCHES SHOWN) for CDP1874C

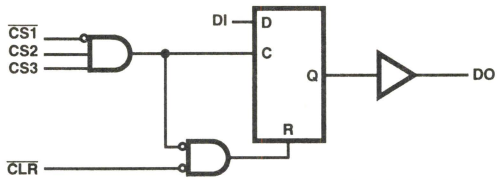


FIGURE 3. EQUIVALENT LOGIC DIAGRAM (1 OF 8 LATCHES SHOWN) FOR CDP1875C

Dynamic Electrical Specifications At $T_A = 25^oC$, V_{DD} 5V, t_R, t_F = 10ns, $V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$, C_L = 150pF

PARAMETER		LIMITS CDP1872C, CDP1874C MIN	(NOTE 1) TYP	(NOTE 2) MAX	UNITS
INPUT PORT (FIGURE 4)					
Output Enable	t_{EN}	-	45	90	ns
Output Disable	t_{DIS}	-	45	90	ns
Clock to Data Out	t_{CLO}	-	45	90	ns
$\overline{Clear}$ to Output	t_{CRO}	-	80	160	ns
Data In to Data Out	t_{DIO}	-	50	85	ns
Minimum Data Setup Time	t_{DSU}	-	10	30	ns
Data Hold Time	t_{DH}	-	10	30	ns
Minimum Clock Pulse Width	t_{CL}	-	30	60	ns
Minimum $\overline{Clear}$ Pulse Width	t_{CR}	-	30	60	ns

NOTES:
1. Typical values are for $T_A = +25^oC$ and V_{DD} ±5%.
2. Maximum values are for $T_A = +85^oC$ and V_{DD} ±5%

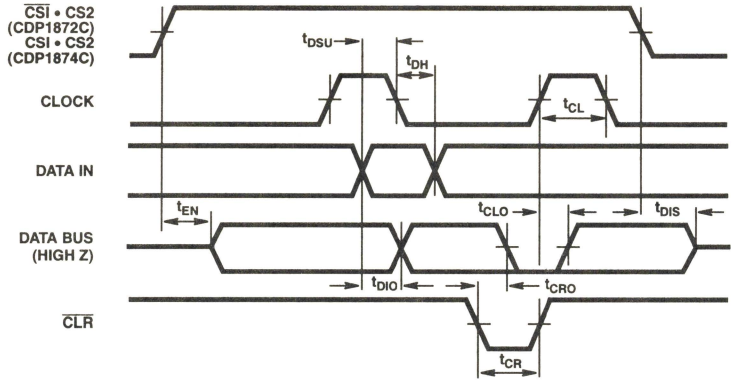


FIGURE 4. TIMING WAVEFORMS FOR CDP1872C AND CDP1874C (INPUT-PORT TYPES)

Dynamic Electrical Specifications At $T_A = 25^oC$, V_{DD} 5V, t_R, t_F = 10ns, $V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$, C_L = 150pF

PARAMETER		LIMITS CDP1875C MIN	(NOTE 1) TYP	(NOTE 2) MAX	UNITS
OUTPUT PORT (FIGURE 5)					
Clock to Data Out	t_{CLO}	-	50	100	ns
$\overline{Clear}$ to Output	t_{CRO}	-	80	160	ns
Data In to Data Out	t_{DIO}	-	50	85	ns
Minimum Data Setup Time	t_{DS}	-	10	30	ns
Data Hold Time	t_{DH}	-	10	30	ns
Minimum $\overline{Clear}$ Pulse Width	t_{CR}	-	30	60	ns

NOTES:

1. Typical values are for $T_A = +25^oC$ and V_{DD} ±5%.
2. Maximum values are for $T_A = +85^oC$ and V_{DD} ±5%

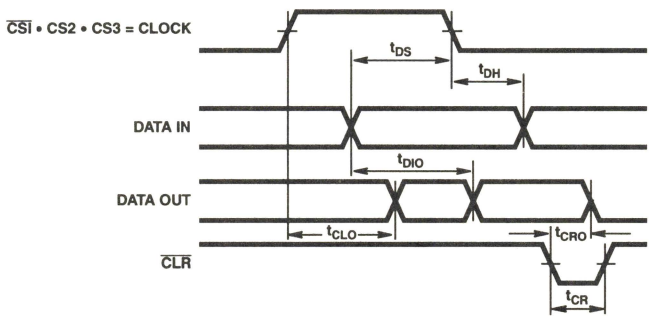


FIGURE 5. TIMING WAVEFORMS FOR CDP1875C (OUTPUT PORT)

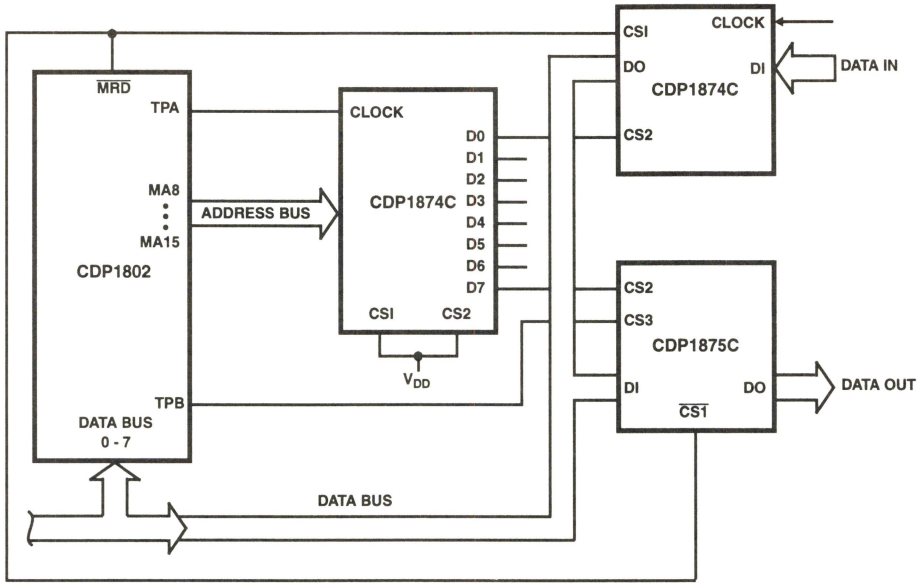


FIGURE 6. CDP1874C USED AS AN INPUT PORT AND ADDRESS LATCH WITH CDP1875C USED AS AN OUTPUT PORT

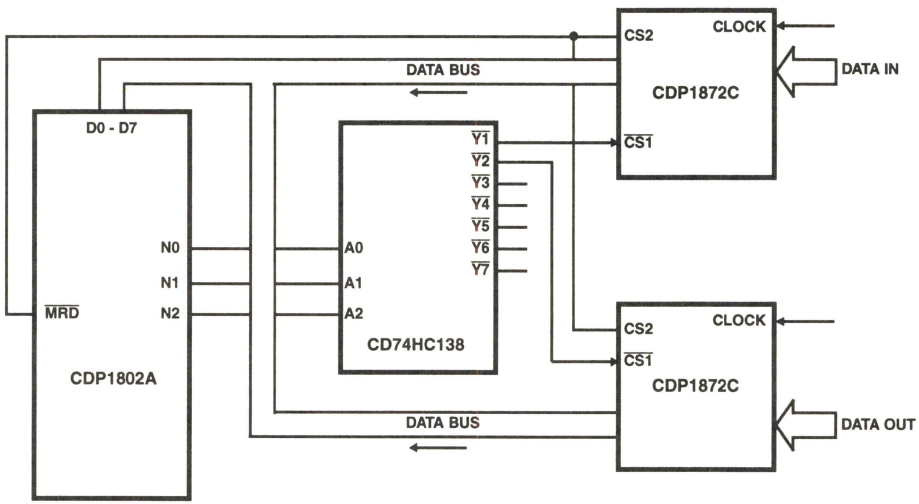


FIGURE 7. CDP1872C USED AS AN INPUT PORT AND SELECTED BY CD74HC138

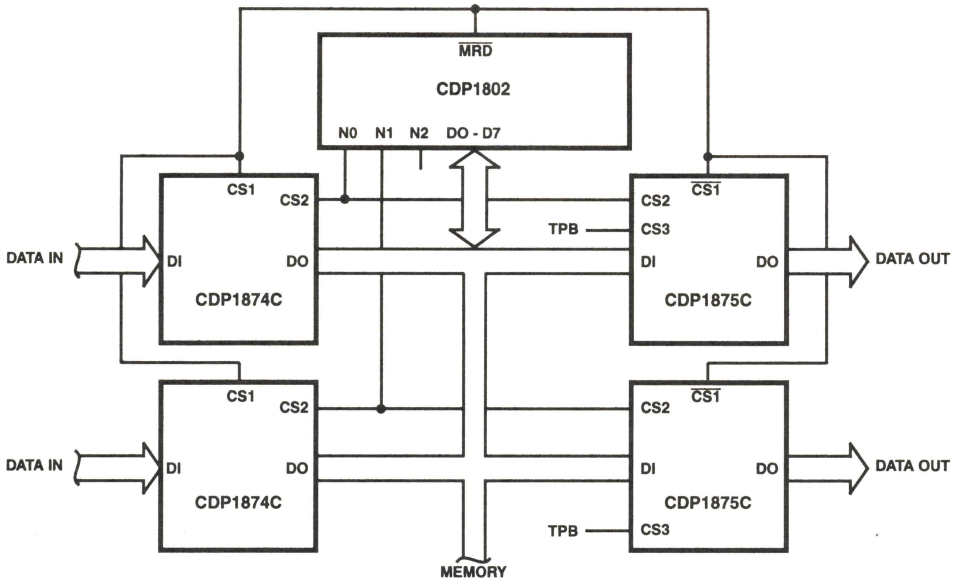


FIGURE 8. CDP1874C AND CDP1875C USED AS INPUT/OUTPUT BUFFERS

HARRIS SEMICONDUCTOR

CDP1877, CDP1877C

March 1997

Programmable Interrupt Controller (PIC)

Features

- Compatible with CDP1800 Series
- Programmable Long Branch Vector Address and Vector Interval
- 8 Levels of Interrupt Per Chip
- Easily Expandable
- Latched Interrupt Requests
- Hard Wired Interrupt Priorities
- Memory Mapped
- Multiple Chip Select Inputs to Minimize Address Space Requirements

Ordering Information

PACKAGE	TEMP. RANGE	5V	10V	PKG. NO.
PDIP	-40°C to +85°C	CDP1877CE	CDP1877E	E28.6

Description

The CDP1877 and CDP1877C are programmable 8-level interrupt controllers designed for use in CDP1800 series microprocessor systems. They provide added versatility by extending the number of permissible interrupts from 1 to N in increments of 8.

When a high to low transition occurs on any of the PIC interrupt lines ($\overline{IR0}$ to $\overline{IR7}$), it will be latched and, unless the request is masked, it will cause the $\overline{INTERRUPT}$ line on the PIC and consequently the $\overline{INTERRUPT}$ input on the CPU to go low.

The CPU accesses the PIC by having interrupt vector register R(1) loaded with the memory address of the PIC. After the interrupt S3 cycle, this register value will appear at the CPU address bus, causing the CPU to fetch an instruction from the PIC. This fetch cycle clears the interrupt request latch bit to accept a new high-to-low transition, and also causes the PIC to issue a long branch instruction (CO) followed by the preprogrammed vector address written into the PIC's address registers, causing the CPU to branch to the address corresponding to the highest priority active interrupt request.

If no other unmasked interrupts are pending, the $\overline{INTERRUPT}$ output of the PIC will return high. When an interrupt is requested on a masked interrupt line, it will be latched but it will not cause the PIC $\overline{INTERRUPT}$ output to go low. All pending interrupts, masked and unmasked, will be indicated by a "1" in the corresponding bit of the status register. Reading of the status register will clear all pending interrupt request latches.

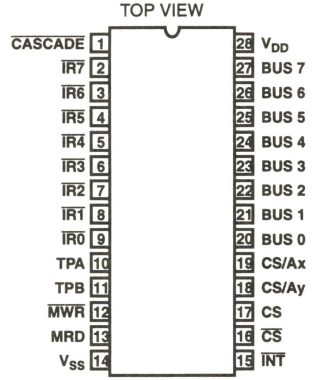
Several PICs can be cascaded together by connecting the $\overline{INTERRUPT}$ output of one chip to the $\overline{CASCADE}$ input of another. Each cascaded PIC provides 8 additional interrupt levels to the system. The number of units cascadable depends on the amount of memory space and the extent of the address decoding in the system.

Interrupts are prioritized in descending order; $\overline{IR7}$ has the highest and $\overline{IR0}$ has the lowest priority.

The CDP1877 and CDP1877C are functionally identical. They differ in that the CDP1877 has a recommended operating voltage range of 4V to 10.5V, and the CDP1877C has a recommended operating voltage range of 4V to 6.5V.

Pinout

CDP1877, CDP1877C (PDIP)
TOP VIEW



Programming Model

PROGRAMMABLE INTERRUPT CONTROLLER (PIC)

BUS 7							BUS 0	
			PAGE REGISTER					WRITE ONLY
A15	A14	A13	A12	A11	A10	A9	A8	
BUS 7							BUS 0	
			CONTROL REGISTER					WRITE ONLY
B7	B6	B5	B4	B3	B2	B1	B0	
BUS 7							BUS 0	
			MASK REGISTER					WRITE ONLY
M7	M6	M5	M4	M3	M2	M1	M0	
BUS 7							BUS 0	
			STATUS REGISTER					READ ONLY
S7	S6	S5	S4	S3	S2	S1	S0	
BUS 7							BUS 0	
			POLLING REGISTER					READ ONLY
P7	P6	P5	P4	P3	P2	P1	P0	

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 1319.2

Absolute Maximum Ratings

DC Supply-Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1877 . . . . . -0.5V to +11V
CDP1877C . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W)
PDIP Package 55
Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type E . . . . . -40°C to +85°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ± 1/32 In. (1.59 ± 0.79mm)
from case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications At T_A = -40 to +85°C, V_{DD} ±5%, Unless Otherwise Specified

PARAMETER		CONDITIONS			LIMITS						UNITS
					CDP1877			CDP1877C			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE1) TYP	MAX	MIN	(NOTE1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	0.01	50	-	0.02	200	µA
		-	0, 10	10	-	1	200	-	-	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	-	1.6	3.2	-	mA
		0.5	0, 10	10	2.6	5.2	-	-	-	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	-	-1.15	-2.3	-	mA
		9.5	0, 10	10	-2.6	-5.2	-	-	-	-	mA
Output Voltage Low Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 9.5	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	-	±1	-	-	±1	µA
			0, 10	10	-	-	±2	-	-	-	µA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	$\pm 10^{-4}$	±1	-	$\pm 10^{-4}$	±1	µA
		0, 10	0, 10	10	-	$\pm 10^{-4}$	±10	-	-	-	µA
Operating Device Current (Note 3)	I_{OPER}	-	-	5	-	0.5	1.0	-	0.5	1.0	mA
		-	-	10	-	1.9	3.0	-	-	-	mA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = +25°C and nominal V_{DD}.
2. $I_{OL} = I_{OH}$ = 1µA
3. Operating current is measured under worst-case conditions in a 3.2MHz CDP1802A system, one PIC access per instruction cycle.

Operating Conditions At T_A = Full package temperature range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS				UNITS
	CDP1877		CDP1877C		
	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

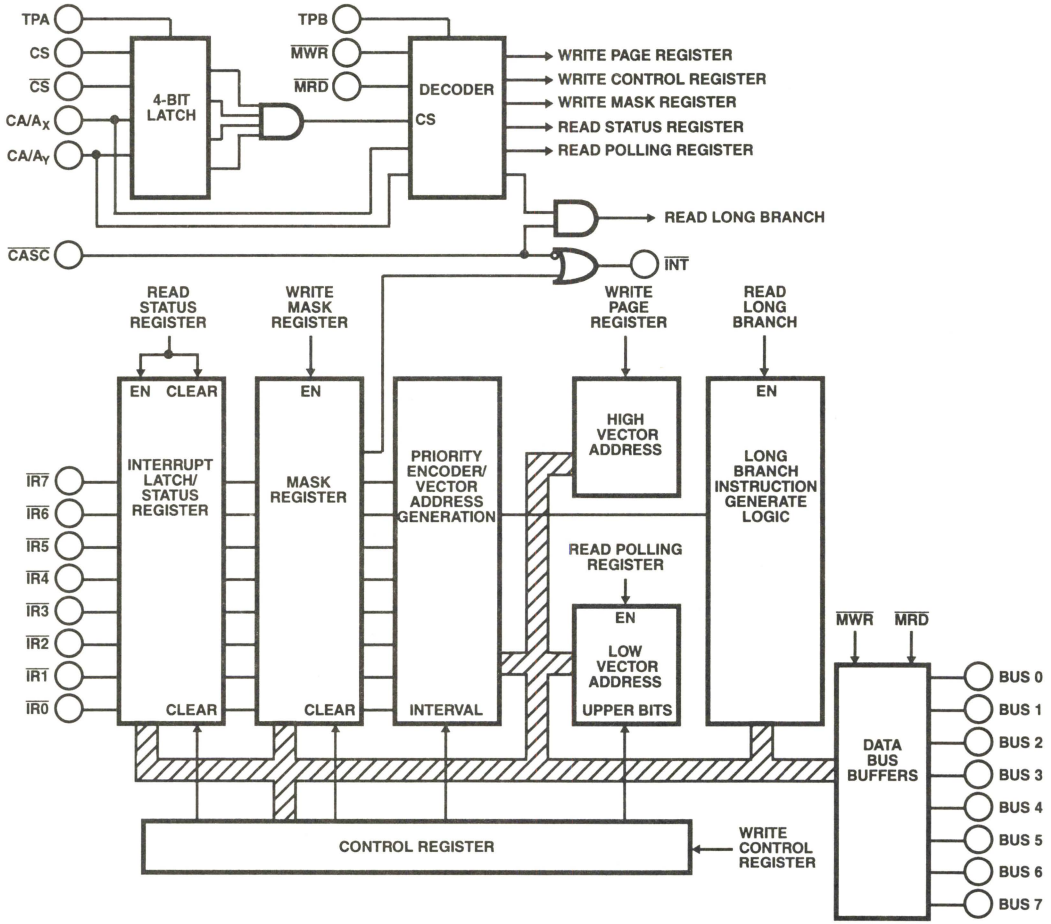


FIGURE 1. FUNCTIONAL DIAGRAM FOR CDP1877

Functional Definitions for CDP1877 and CDP1877C Terminals

TERMINAL	USAGE	TYPE
V_{DD} - V_{SS}	Power	
BUS0 - BUS7	Data Bus - Communicates Information to and from CPU	Bidirectional
$\overline{IR0}$ - $\overline{IR7}$	Interrupt Request Lines	Input
$\overline{INTERRUPT}$	Interrupt to CPU	Output
$\overline{MRD}$, $\overline{MWR}$	Read/Write Controls from CPU	Input
TPA, TPB	Timing Pulses from CPU	Input
CS, $\overline{CS}$	Chip Selects, Enable Chip if Valid during TPA	Input
CS/A_X, CS/A_Y	Used as a Chip Select during TPA and as a Register Address During Read/Write Operations	Input
$\overline{CASCADE}$	Used for Cascading Several PIC Units. The $\overline{INTERRUPT}$ Output from a Higher Priority PIC can be Tied to this Input, or the Input can be Tied to V_{DD} if Cascading is Not Used.	Input

PIC Programming Model

INTERNAL REGISTERS

The PIC has three write-only programmable registers and two read-only registers.

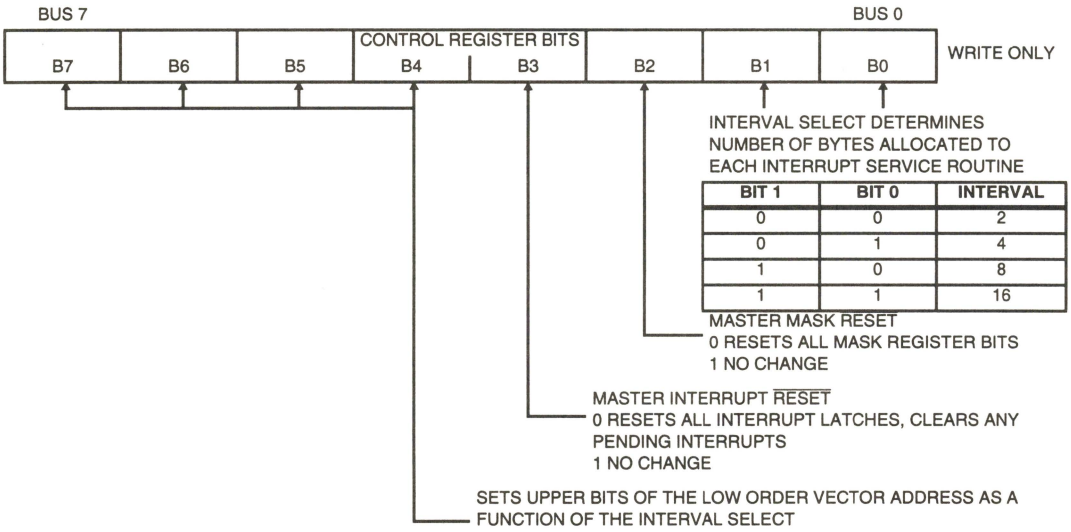
Page Register

This write only register contains the high order vector address the device will issue in response to an interrupt request. This high-order address will be the same for any of the 8 possible interrupt requests; thus, interrupt vectoring differs only in location within a specified page.



Control Register

The upper nibble of this write-only register contains the low order vector address the device will issue in response to an interrupt request. The lower nibble is used for a master interrupt reset, master mask reset and for interval select.



The Low Order Vector Address will be set according to the table below:

INTERVAL SELECTED NO. OF BYTES	LOW ADDRESS BITS			
	BIT B7	BIT B6	BIT B5	BIT B4
2	SETS A7	SETS A6	SETS A5	SET A4
4	SETS A7	SETS A6	SETS A5	X
8	SETS A7	SETS A6	X	X
16	SETS A7	X	X	X

NOTES:

1. X = Don't Care
2. All Don't Care addresses and addresses A0-A3 are determined by interrupt request.

Mask Register

A "1" written into any location in this write only register will mask the corresponding interrupt request line. All interrupt inputs (except $\overline{\text{CASCADE}}$) are maskable.

BUS 7			MASK REGISTER BITS				BUS 0	
M7	M6	M5	M4	M3	M2	M1	M0	WRITE ONLY

Status Register

In this read only register a "1" will be present in the corresponding bit location for every masked or unmasked pending interrupt.

BUS 7			STATUS REGISTER BITS				BUS 0	
S7	S6	S5	S4	S3	S2	S1	S0	READ ONLY

Polling Register

This read only register provides the low order vector address and is used to identify the source of interrupt if a polling technique, rather than interrupt servicing, is used.

BUS 7			POLLING REGISTER BITS				BUS 0	
P7	P6	P5	P4	P3	P2	P1	P0	READ ONLY

RESPONSE TO INTERRUPT (AFTER S3 CYCLE)

The PIC's response to interrogation by the CPU is always 3 bytes long, placed on the data bus in consecutive bytes in the following format:

First (Instruction) Byte:

LONG BRANCH INSTRUCTION - CO (Hex)

BUS 7							BUS 0
1	1	0	0	0	0	0	0

Second (High-Order Address) Byte

This byte is the High-Order vector Address that was written into the PIC's Page Register by the user. The PIC does not alter this value in any way.

High-Order Vector Address

BUS 7							BUS 0
A15	A14	A13	A12	A11	A10	A9	A8

Third (Low-Order Address) Bytes

INTERVAL 2

BUS 7							BUS 0
A7	A6	A5	A4	I2	I1	I0	0

INTERVAL 4

BUS 7							BUS 0
A7	A6	A5	I2	I1	I0	0	0

INTERVAL 8

BUS 7							BUS 0
A7	A6	I2	I1	I0	0	0	0

INTERVAL 16

BUS 7							BUS 0
A7	I2	I1	I0	0	0	0	0

Indicates active interrupt input number (binary 0 to 7).

Bits indicated by A_X (x = 4 to 7) are the same as programmed into the control register. All other bits are generated by the PIC.

REGISTER ADDRESSES

In order to read/write or obtain an interrupt vector from any PIC in the system, all chip selects (CS/A_X, CS/A_Y, CS, $\overline{CS}$) must be valid during TPA.

CS/A_X and CS/A_Y are multiplexed addresses; both must be high during TPA, and set according to this table during TPB to access the proper register.

CS/A_X	CS/A_Y	$\overline{RD}$	$\overline{WR}$	ACTION TAKEN
1	0	0	1	READ Long Branch instruction and vector for highest priority unmasked interrupt pending.
1	0	1	0	WRITE to Page Register
0	1	1	0	WRITE to Control Register
0	0	0	1	READ Status Register
0	0	1	0	WRITE to Mask Register
0	1	0	1	READ Polling Register (Used to identify INTERRUPT source if Polling technique rather than INTERRUPT service is used.)
1	1	X	X	Unused condition

PIC Application Examples

Example 1 - Single PIC Application

Figure 2 shows all the connections required between CPU and PIC to handle eight levels of interrupt control.

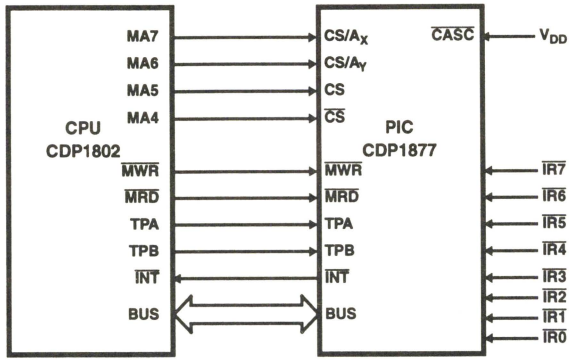


FIGURE 2. PIC AND CPU CONNECTION DIAGRAM

Programming

Programming the PIC consists of the following steps:

1. Disable interrupt at CPU
2. Reset Master Interrupt Bit, B3, of Control Register.
3. Write a "1" into the Interrupt Input bit location of the Mask Register, if masking is desired.
4. Write the High-Order Address byte into the Page Register.
5. Write the Low-Order Address and the vector interval into the Control Register.
6. Program R(1) of the CPU to point to the PIC so that the Long Branch instruction can be read from the PIC during the Interrupt Service routine.

Values for Example 1 with LOCATION 84E0 arbitrarily chosen as the Vector Address with interval of eight bytes, $\overline{IR4}$ pending, is shown in Table 1.

In deriving the above addresses, all Don't Care bits are assumed to be 0.

When an INTERRUPT ($\overline{IR4}$) is received by the CPU, it will address the PIC and will branch to the interrupt service routine.

The three bytes generated by the PIC will be:

1st Byte = $C0_H$
2nd Byte = 84_H
3rd Byte = $E0_H$

TABLE 1. REGISTER ADDRESS VALUES

REGISTER	REGISTER ADDRESS	OPERATION	DATA BYTE
MASK	E000H	WRITE	00_H
CONTROL	E040H	WRITE	CE_H
PAGE	E080H	WRITE	84_H
STATUS	E000H	READ	10_H
POLLING	E040H	READ	$E0_H$
R(1) (IN CPU)	E080H	-	-

Example 2 - Multi-PIC Application

Figure 3 shows all the connections required between CPU and PIC's to handle sixteen levels of interrupt control.

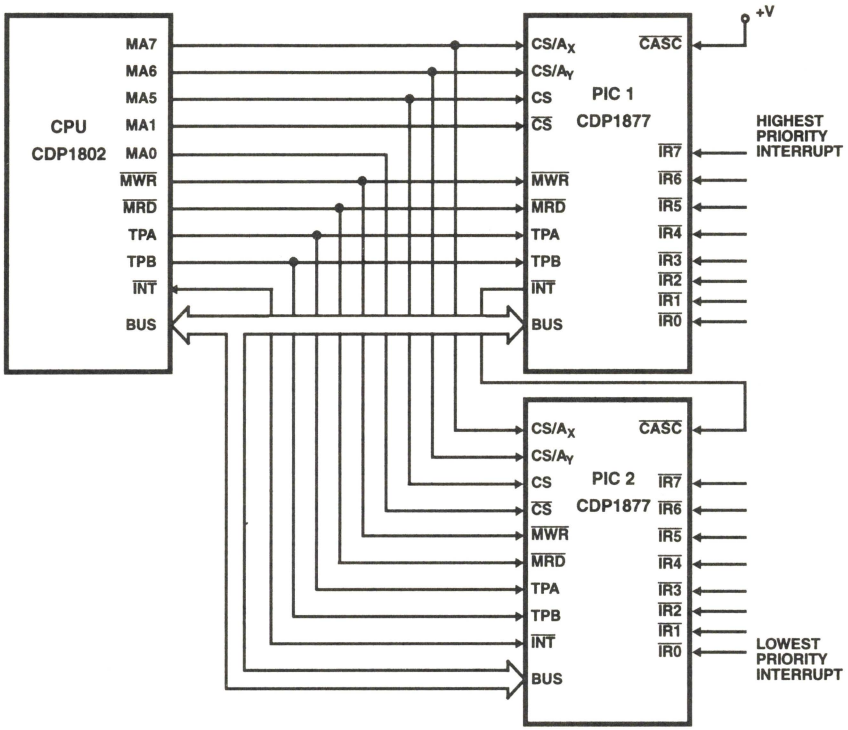


FIGURE 3. PICs AND CPU CONNECTION DIAGRAM

Register Address Assignments

The low-byte register address for any WRITE or READ operation is the same as shown in Table 1.

The High-Byte register differs for each PIC because of the linear addressing technique shown in the example:
PIC 1 = 111XXX01 ($E1_H$ for X = 0)
PIC 2 = 111XXX10 ($E2_H$ for X = 0)

The R(1) vector address is unchanged. This address will select both PICs simultaneously (R(1). 1 = 111XXX00 = $E0_H$). Internal CDP1877 logic controls which PIC will respond when an interrupt request is serviced.

Additional PIC Application Comments

The interval select options provide significant flexibility for interrupt routine memory allocations:

- The 2-byte interval allows one to dedicate a full page to interrupt servicing, with variable space between routines, by specifying indirect vectoring with 2-byte short branch instructions on the current page.
- The 4-byte interval allows for a 3-byte long branch to any location in memory where the interrupt service routine is located. The branch can be preceded by a Save Instruction to save previous contents of X and P on the stack.
- The 8-byte and 16-byte intervals allow enough space to perform a service routine without indirect vectoring. The amount of interval memory can be increased even further if all 8 INTERRUPTS are not required. Thus a 4-level interrupt system could use alternate $\overline{IR}$ Inputs, and expand the interval to 16 and 32 bytes, respectively.
- The 4 Chip Selects allow one to conserve total allotted memory space to the PIC. For one chip, a total of 4 address lines could be used to select the device, mapping it into as little as 4-K of memory space. Note that this selection technique is the only one that allows the PIC to work properly in the system: I/O mapping cannot be used because the PIC must work within the CDP1800 interrupt structure to define the vector address. Decoded signals also will not work because the chip selects must be valid on the trailing edge of TPA.

Dynamic Electrical Specifications At T_A = -40 to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7V_{DD}, V_{IL} = 0.3V_{DD}, C_L = 50pF

PARAMETER		V_{DD} (V)	LIMITS						UNITS
			CDP1877			CDP1877C			
			MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Address to TPA Setup Time	t_{AS}	5	60	-	-	60	-	-	ns
		10	40	-	-	-	-	-	ns
Address to TPA Hold Time	t_{AH}	5	60	-	-	60	-	-	ns
		10	40	-	-	-	-	-	ns
Data Valid after TPB	t_{DTPB}	5	370	-	-	370	-	-	ns
		10	210	310	-	-	-	-	ns
Data Hold Time from Write	t_{HW}	5	30	-	-	30	-	-	ns
		10	40	-	-	-	-	-	ns
Address to Valid Data Access Time	t_{DR}	5	-	340	490	-	340	490	ns
		10	-	125	230	-	-	-	ns
Data Setup Time to Write	t_{DSU}	5	0	-	-	0	-	-	ns
		10	0	-	-	-	-	-	ns
Address Hold from TPB	t_{HTPB}	5	80	-	-	80	-	-	ns
		10	40	-	-	-	-	-	ns
Minimum $\overline{MWR}$ Pulse Width	t_{MWR}	5	130	-	-	130	-	-	ns
		10	60	-	-	-	-	-	ns
Minimum $\overline{IR}$ Pulse Width	t_{IRX}	5	130	-	-	130	-	-	ns
		10	60	-	-	-	-	-	ns

NOTE:

1. Typical values are for T_A = 25°C and V_{DD} ±5%.

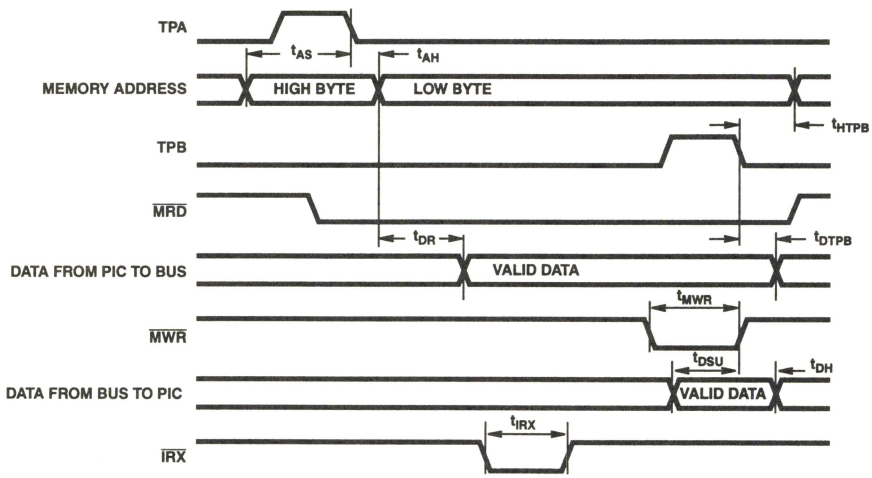


FIGURE 4. TIMING WAVEFORMS FOR CDP1877

CDP1878C

March 1997

CMOS Dual Counter-Timer

Features

- Compatible with General Purpose and CDP1800 Series Microprocessor Systems
- Two 16-Bit Down Counters and Two 8-Bit Control Registers
- 5 Modes Including a Versatile Variable-Duty Cycle Mode
- Programmable Gate-Level Select
- Two-Complemented Output Pins for Each Counter-Timer
- Software-Controlled Interrupt Output
- Addressable in Memory Space or CDP1800-Series I/O Space

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
CDP1878CE	-40°C to +85°C	PDIP	E28.6
CDP1878CD	-40°C to +85°C	SBDIP	N28.6

Description

The CDP1878C is a dual counter-timer consisting of two 16-bit programmable down counters that are independently controlled by separate control registers. The value in the registers determine the mode of operation and control functions. Counters and registers are directly addressable in memory space by any general industry type microprocessors, in addition to input/output mapping with the CDP1800 series microprocessors.

Each counter-timer can be configured in five modes with the additional flexibility of gate-level control. The control registers in addition to mode formatting, allow software start and stop, interrupt enable, and an optional read control that allows a stable readout from the counters. Each counter-timer has software control of a common interrupt output with an interrupt status register indicating which counter-timer has timed out.

In addition to the interrupt output, true and complemented outputs are provided for each counter-timer for control of peripheral devices.

This type is supplied in 28-lead dual-in-line ceramic packages (D suffix), and 28-lead dual-in-line plastic packages (E suffix).

Pinout

CDP1878C
(DIP)
TOP VIEW

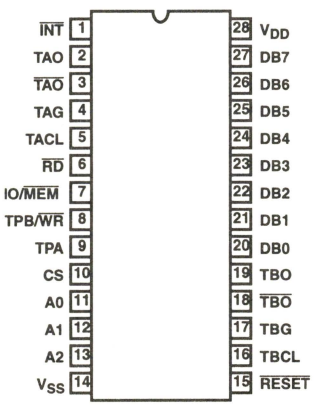


TABLE 1. MODE DESCRIPTION

MODE	FUNCTION	APPLICATION
1 Timeout	Outputs change when clock decrements counter to "0"	Event counter
2 Timeout Strobe	One clockwide output pulse when clock decrements counter to "0"	Trigger pulse
3 Gate-Controlled One Shot	Outputs change when clock decrements counter to "0". Retriggerable	Time-delay generation
4 Rate Generator	Repetitive clockwide output pulse	Time-base generator
5 Variable-Duty Cycle	Repetitive output with programmed duty cycle	Motor control

4 CMOS PERIPHERALS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 1341.2

Absolute Maximum Ratings

DC Supply-Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1878C ..... -0.5V to +7V
Input Voltage Range, All Inputs ..... -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input ..... ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	55	N/A
SBDIP Package	50	12

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type D ..... -55°C to +125°C
Package Type E ..... -40°C to +85°C
Storage Temperature Range (T_{STG}) ..... -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ± 1/32 In. (1.59 ± 0.79mm)
from case for 10s max ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	SYMBOL	MIN	MAX	UNITS
DC Operating Voltage Range		4	6.5	V
Input Voltage Range		V_{SS}	V_{DD}	V
Maximum Clock Input Rise or Fall Time	t_R, t_F	-	5	µs
Minimum Clock Pulse Width	t_{WL}, t_{WH}	200	-	ns
Maximum Clock Input Frequency	f_{CL}	DC	1	MHz

Static Electrical Specifications

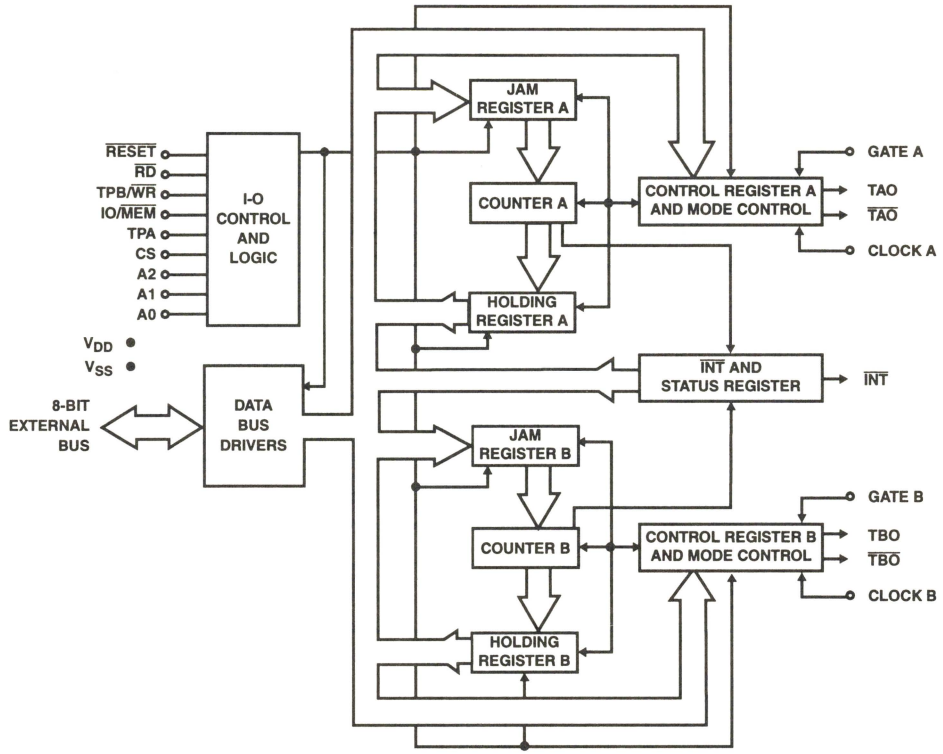
At T_A = -40°C to +85°C, V_{DD} ± 5% Except as noted:

PARAMETER	SYMBOL	CONDITIONS			LIMITS			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	0.02	200	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	V
Output Voltage High-Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	V
Input High Voltage	V_{IH}	0.5, 9.5	-	5	3.5	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	-	±1	µA
Operating Current (Note 3)	I_{DD1}	-	0, 5	5	-	1.5	3	mA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	pF

NOTES:

1. Typical values are for T_A = +25°C and nominal V_{DD}.
2. I_{OL} = I_{OH} = 1µA
3. Operating current measured at 200kHz for V_{DD} = 5V, with open outputs (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2MHz).

Functional Diagram



FUNCTIONAL DEFINITIONS FOR CDP1878C TERMINALS

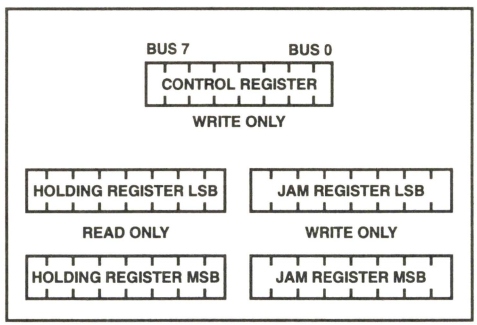
TERMINAL	USAGE
V_{DD} - V_{SS}	Power
DB0-DB7	Data to and from device
TPB/$\overline{WR}$, $\overline{RD}$	Directional Control Signals
A0, A1, A2	Addresses that select counters or registers
TACL, TBCL	Clocks used to decrement counters
TAG, TBG	Gate inputs that control counters

TERMINAL	USAGE
TAO, $\overline{TAO}$	Complemented outputs of Timer A
TBO, $\overline{TBO}$	Complemented outputs of Timer B
TPA	Used with CDP1800-series processors, tied high otherwise
CS	Active high input that enables device
$\overline{INT}$	Low when counter is "0"
$\overline{RESET}$	When active, TAO, TBO are low, $\overline{TAO}$, $\overline{TBO}$ are high. Interrupt status register is cleared.
IO/$\overline{MEM}$	Tied high in CDP1800 input/output mode, otherwise tied low

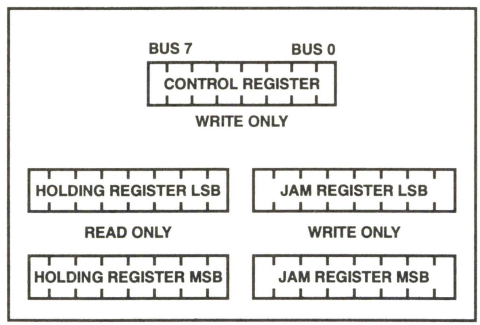
REGISTER TRUTH TABLE

ADDRESS			ACTIVE		REGISTER COUNTER
A2	A1	A0	TPB/$\overline{WR}$	$\overline{RD}$	
1	1	0	X		Write Counter A MSB
1	1	0		X	Read Counter A MSB
0	1	0	X		Write Counter A LSB
0	1	0		X	Read Counter A LSB
1	0	0	X		Control Register A
1	1	1	X		Write Counter B MSB
1	1	1		X	Read Counter B MSB
0	1	1	X		Write Counter B LSB
0	1	1		X	Read Counter B LSB
1	0	1	X		Control Register B
1	0	0		X	Interrupt Status Register
1	0	1		X	
0	0	0			Not Used
0	0	1			Not Used

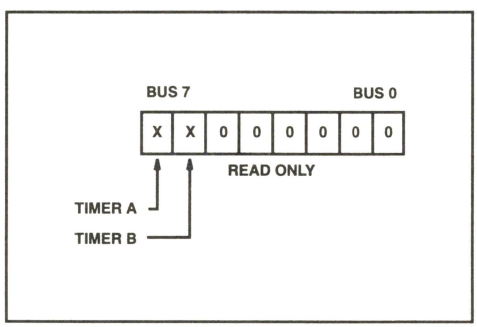
Programming Model



COUNTER A REGISTERS



COUNTER B REGISTERS



INTERRUPT STATUS REGISTER

Functional Description

The dual counter-timer consists of two programmable 16-bit down counters, separately addressable and controlled by two independent 8-bit control registers. The word in the control register determines the mode and type of operation that the counter-timer performs. Writing to or reading from a counter or register is enabled by selective addressing during a write or read cycle. The data is placed on the data bus by the microprocessor during the write cycle or read from the counter during the read cycle. Data to and from the counters and to the control registers is in binary format.

Each counter-timer consists of three parts. The first is the counter itself, a 16-bit down counter that is decremented on the trailing edge of the clock input. The second is the jam register that receives the data when the counter is written to. The word in the control register determines when the jam register value is placed into the counter. The third part is the holding register that places the counter value on the data bus when the counter is read.

When the counter has decremented to zero, three events occur. The first involves the common interrupt output pin that, if enabled, becomes active low. The second is the setting of a bit in the interrupt status register. This register can be read to determine which counter-timer has timed out. The third event is the logic change of the complemented output pins.

In addition to the clock input used to decrement the counter, a gate input is available to enable or initiate operation. The counter-timers are independent and can have different mode operations.

Write Operation

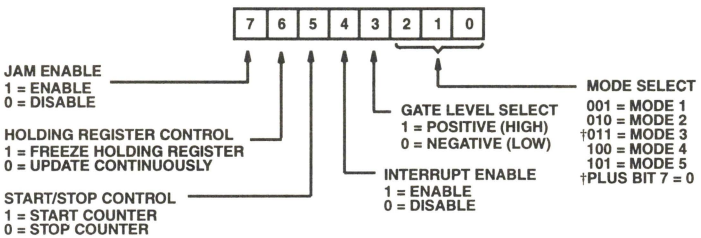
The counters and registers are separately addressable and are programmed via the data bus when the chip is selected with the TPB/$\overline{WR}$ pin active. Normal sequencing requires that the counter jam register be loaded first with the required value (most significant and least significant byte in any order), and then the control register be accessed and loaded with the control word. The trailing edge of the TPB/$\overline{WR}$ pulse will latch the control word into the control register. The trailing edge of the first clock to occur with gate valid will cause the counter to be jammed with its initial value. The counter will decrement on the trailing edge of succeeding clocks as long as the gate is valid, until it reaches zero. The output levels will then change, and if enabled, the interrupt output will become active and the appropriate timer bit will be set in the interrupt status register. The interrupt output and the interrupt status register can be cleared (to their inactive state) by addressing the control register with the TPB/$\overline{WR}$ line active For example, if counter A times out, control register A must be accessed to reset the interrupt output high and reset the timer A bit in the status register low. Timer B bit in the status register will be unaffected.

Read Operation

Each counter has a holding register that is continuously being updated by the counter and is accessed when the counter is addressed during read cycles. Counter reads are accomplished by halting the holding register and then reading it, or by reading the holding register directly. If the holding register is read directly, data will appear on the bus if the counters are addressed with the $\overline{RD}$ line active. However, if the clock decrements the counter between the two read operations (most and least significant byte), an inaccurate value will be read. To preclude this from happening, writing a "1" into bit 6 of the control register and then addressing and reading the counter will result in a stable reading. This operation prevents the holding register from being updated by the counter and does not affect the counter's operation.

The interrupt status register is read by addressing either control register with the $\overline{RD}$ line active. A "1" in bit 7 indicates Timer A has timed out and a "1" in bit 6 indicates Timer B has timed out. Bits 0-5 are zeros.

Control Register



Bits 0, 1 and 2

Mode Selects - See Mode Timing Diagrams (Figures 1, 2, 3, 4, and 5).

Note: When selecting a mode, the timer outputs TAO and TBO are set low, and $\overline{TAO}$ and $\overline{TBO}$ are set high. If bits 0, 1 and 2 are all zero's when the control register is loaded, no mode is selected, and the counter-timer outputs are unaffected. Issuing mode 6 will cause an indeterminate condition of the counter, issuing mode 7 is equivalent to issuing mode 5.

	BIT 7	BIT 2	BIT 1	BIT 0
Mode 1 - Timeout	-	0	0	1
Mode 2 - Timeout Strobe	-	0	1	0
Mode 3 - Gate Controlled One Shot	0	0	1	1
Mode 4 - Rate Generator	-	1	0	0
Mode 5 - Variable-Duty Cycle	-	1	0	1
No Mode selected. Counter outputs unaffected	-	0	0	0

Bit 3 - Gate Level Select - All modes require an enabling signal on the gate to allow counter operation. This enabling signal is either a level or a pulse (edge). Positive gate level or edge enabling is selected by writing a "1" into this bit and negative (low) enabling is selected when bit 3 is "0".

Bit 4 - Interrupt Enable - Setting this bit to "1" enables the $\overline{INT}$ output, and setting it to "0" disables it. When reset, the $\overline{INT}$ output is at a high level. If the interrupt enable bit in the control register is enabled and the counter decrements to zero, the $\overline{INT}$ output will go low and will not return high until the counter-timer is reset or the selected control register is written to. Example: If timer B times out, control register B must be accessed to reset the $\overline{INT}$ output high. If the interrupt enable bit is set to "0", the counter's timeout will have no effect on the $\overline{INT}$ output.

In mode 5, the variable-duty cycle mode, the $\overline{INT}$ pin will become active low when the MSB in the counter has decremented to zero.

Bit 5 - Start/Stop Control - This bit controls the clock input to the counter and must be set to "1" to enable it. Writing a "0" into this location will halt operation of the counter. Operation will not resume until the bit is set to "1".

Bit 6 - Holding Register Control - Since the counter may be decrementing during a read cycle, writing a "1" into this location will hold a stable value in the hold register for subsequent read operations. Rewriting a "1" into bit 6 will cause an update in the holding register on the next trailing clock edge. If this location contains a "0", the holding register will be updated continuously by the value in the counter.

Bit 7 - Jam Enable - When this bit is set to "1 "during a write to the control register, the 16-bit value in the jam register will be available to the counter; TAO and TBO are reset low and $\overline{TAO}$ and $\overline{TBO}$ are set high. On the trailing edge of the first input clock signal with the gate valid this value will be latched in the counter, the counter outputs TAO and TBO will be set high and the $\overline{TAO}$ and $\overline{TBO}$ will be reset low. Setting bit 7 to "0" will leave the counter value unaffected. This location should be set to "0" any time a write to the control register must be performed without changing the present counter value. If the value in the jam register has not been changed, writing a "1" into bit 7 of the control register with zeros in bits 0,1, and 2 (mode select) will reload the counter with the old value and leave the mode unchanged. If the value in the jam register is changed, then the next write to the control register (with bit 7 a "1") must include a valid mode select (i.e., at least 1 of the bits 0,1, or 2 must be a "1").

In mode 3, the hardware start is enabled by writing a "0" into bit 7. If a "1" is written to bit 7, the timeout will start immediately and mode 3 will resemble mode 1.

Mode Descriptions

	MODE	CONTROL REGISTER	GATE CONTROL
1	Timeout	X X X X X 0 0 1 BUS 7 BUS 0	Selectable High or Low Level Enables Operation

Mode 1

After the count is loaded into the jam register and the control register is written to with the jam-enable bit high on the trailing edge of the first clock after the gate is valid, TXO goes high and $\overline{TXO}$ goes low. The input clock decrements the counter as long as the gate remains valid. When it reaches zero TXO goes low and $\overline{TXO}$ goes high, and if enabled, the interrupt output is set low. Writing to the counter while it is decrementing has no effect on the counter value unless the control register is subsequently written to with the jam-enable bit high. After timeout the counter remains at FFFF unless reloaded.

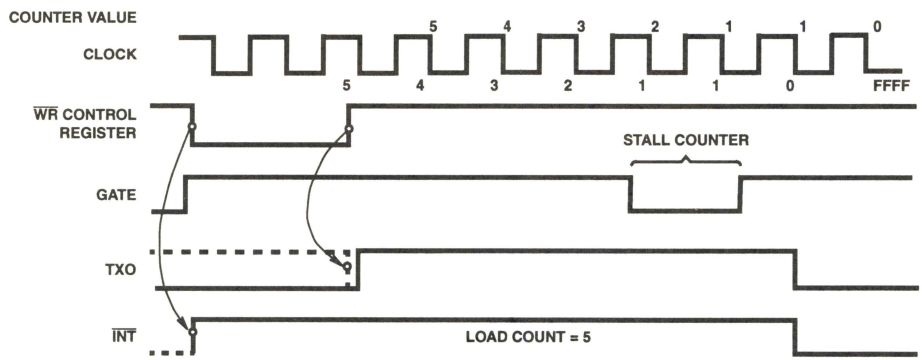


FIGURE 1. TIMEOUT (MODE 1) TIMING WAVEFORMS

MODE		CONTROL REGISTER	GATE CONTROL
2	Timeout Strobe	X X X X X 0 1 0 BUS 7 BUS 0	Selectable High or Low Level Enables Operation

Mode 2

Operation of this mode is the same as mode 1, except the outputs will change for one clock period only and then return to the condition of TXO high and $\overline{TXO}$ low, and the counter is reloaded

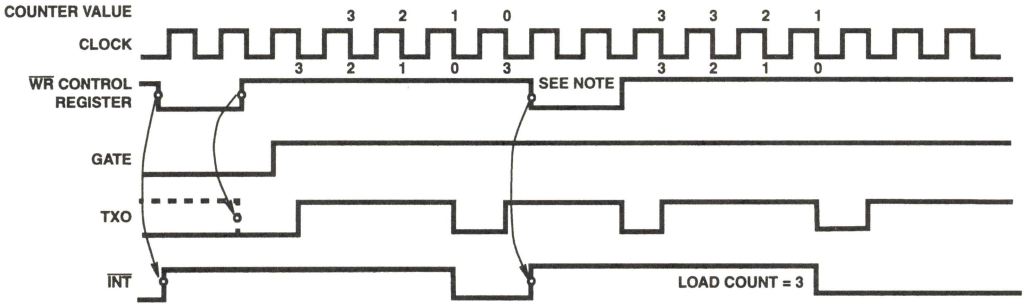


FIGURE 2. TIMEOUT STROBE (MODE 2) TIMING WAVEFORMS

NOTE: Write to control register with mode selects = 0

MODE		CONTROL REGISTER	GATE CONTROL
3	Gate Controlled One-Shot	0 X X X X 0 1 1 BUS 7 BUS 0	Selectable Positive or Negative Going Edge Initiates Operation

Mode 3

After the jam register is loaded with the required value, the gate edge will initiate this mode. TXO will be set high, and $\overline{TXO}$ will be set low. The clock will decrement the counter. When zero is reached, TXO will go low and $\overline{TXO}$ will be high, and the interrupt output will be set low. The counter is retriggerable: While the counter is decrementing, a gate edge or write to the control register with the jam-enable bit high, will load the counter with the jam register value and restart the one-shot operation.

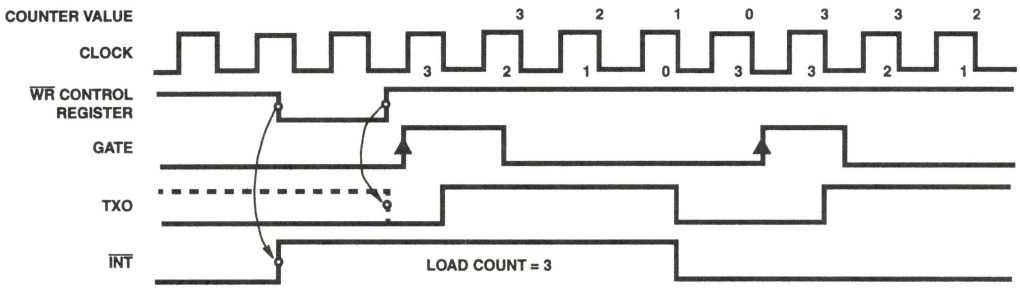


FIGURE 3. GATE CONTROLLED ONE-SHOT (MODE 3) TIMING WAVEFORMS

MODE		CONTROL REGISTER	GATE CONTROL
4	Rate Generator	X X X X X 1 0 0 BUS 7 BUS 0	Selectable High or Low Level Enables Operation

Mode 4

A repetitive clock-wide output pulse will be output, with the time between pulses equal to the counter's value, (trailing edge to leading edge). This model is software started with a write to the control register if the gate level is valid. If the counter is written to while decrementing, the new value will not affect the counter's operation until the present timeout has concluded, unless the control register is written to with the jam-enable bit high. If the gate input (TAG or TBG) is used to start this mode, the first cycle following the gate going true is indeterminate.

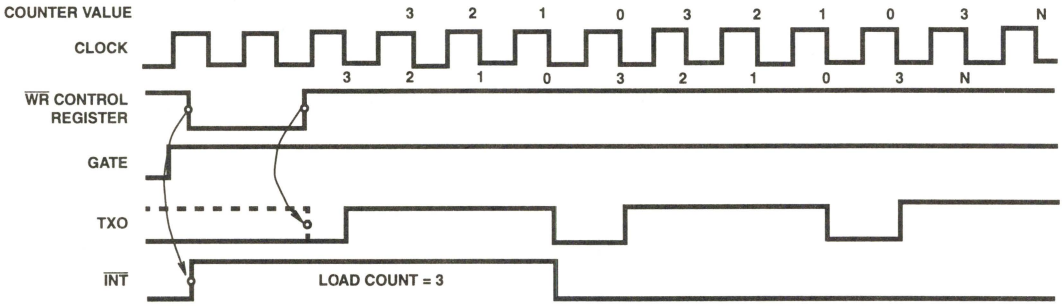


FIGURE 4. RATE GENERATORS (MODE 4) TIMING WAVEFORMS

MODE		CONTROL REGISTER	GATE CONTROL
5	Variable Duty Cycle	X X X X X 1 0 1 BUS 7 BUS 0	Selectable High or Low Level Enables Operation

Mode 5

After the mode is initiated, the outputs will remain at one level until the clock decrements the least significant byte of the counter to N+1. The outputs will then change level and the counter decrements the most significant byte to N+1. The process will then repeat, resulting in a repetitive output with a duty cycle directly controlled by the value in the counter. The output period will be equal to LSB+MSB+2.

The interrupt output will become active after the MSB is loaded into the counter and decrements to zero.

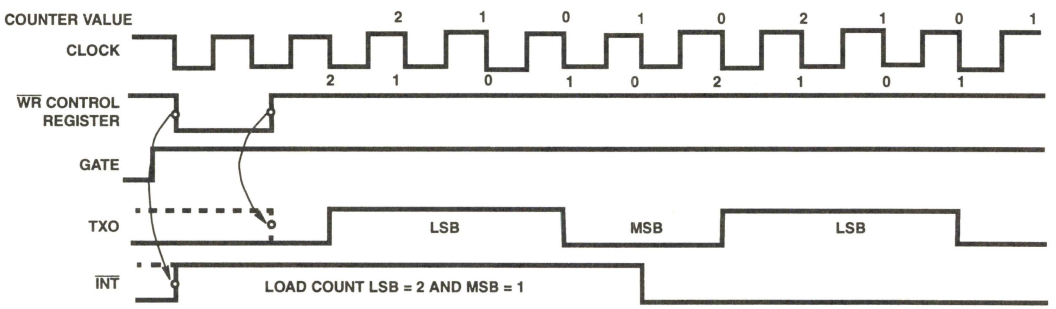


FIGURE 5. VARIABLE-DUTY CYCLE (MODE 5) TIMING WAVEFORMS

NOTE: In order to avoid unwanted starts when selecting mode 3 or 4, the gate signal must be set to the opposite level that will be programmed.

Setting the Control Register

The following will illustrate a counter write and subsequent reads that places stable, accurate values on the data bus from the counter-timer.

The counter is addressed and the required values are loaded with a write operation. The control register is addressed next and loaded with B9H.

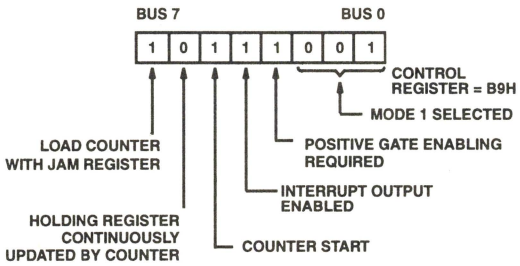


FIGURE 6.

The counter will now decrement with each input clock pulse while the gate is valid. Assuming the counter has not decremented to zero and its value is to be read without affecting the counter's operation, a write to the control register is performed. 78H is loaded into the control register.

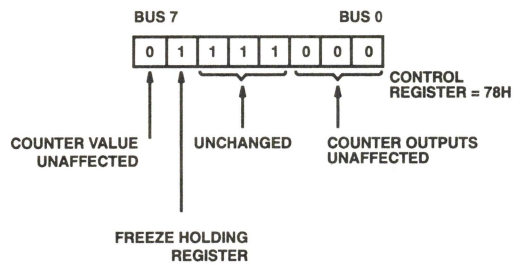


FIGURE 7.

The counter is addressed and read operations are performed.

Function Pin Description

DB7 - DB0 - 8-bit bidirectional bus used to transfer binary information between the microprocessor and the dual counter-timer.

V_{DD}, V_{SS} - Power and ground for device.

A0, A1, and A2 - Addresses used to select counters or registers.

TPB/$\overline{WR}$, $\overline{RD}$ - Directional signals that determine whether data will be placed on the bus from a counter or the interrupt status register ($\overline{RD}$ active) (memory mapped), or data on the bus will be placed into a counter or control register (TPB/$\overline{WR}$ active). The following connections are required between the microprocessor and the counter-timer in the CDP1800-series input/output mapping mode.

MICROPROCESSOR	COUNTER-TIMER
$\overline{MRD}$	$\overline{RD}$
TPB	TPB/$\overline{WR}$
TPA	TPA
N Lines	Address Lines

and IO/$\overline{MEM}$ to V_{DD}

During an output instruction, data from the memory is strobed into the counter-timer during TPB when $\overline{RD}$ is active, and latched on TPB's trailing edge. Data is read from the counter-timer when $\overline{RD}$ is not active between the trailing edges of TPA and TPB. See Figures 11, 12, and 13.

TACL, TBCL - Clocks used to decrement the counter.

TAG, TBG - Gate inputs used to control counter.

TAO, $\overline{TAO}$ - Complemented outputs of Timer A.

TBO, TBO - Complemented outputs of Timer B.

INT - Common interrupt output. Active when counter decrements to zero.

RESET - Active low signal that resets counter outputs (TAO, TBO low, $\overline{TAO}$, $\overline{TBO}$ high). The interrupt output is set high and the status register is cleared.

IO/MEM - Tied high in CDP1800-series input/output mode, otherwise tied low.

TPA - Tied to TPA of the CDP1800-series microprocessors. During memory mapping, it is used to latch the high order address bit for the chip select. In the CDP1800 input/output mode, it is used to gate the N lines. When the counter-timer is used with other microprocessors, or when the high order address of the CDP1800-series microprocessors is externally latched, it is connected to V_{DD}.

CS - An active high signal that enables the device.

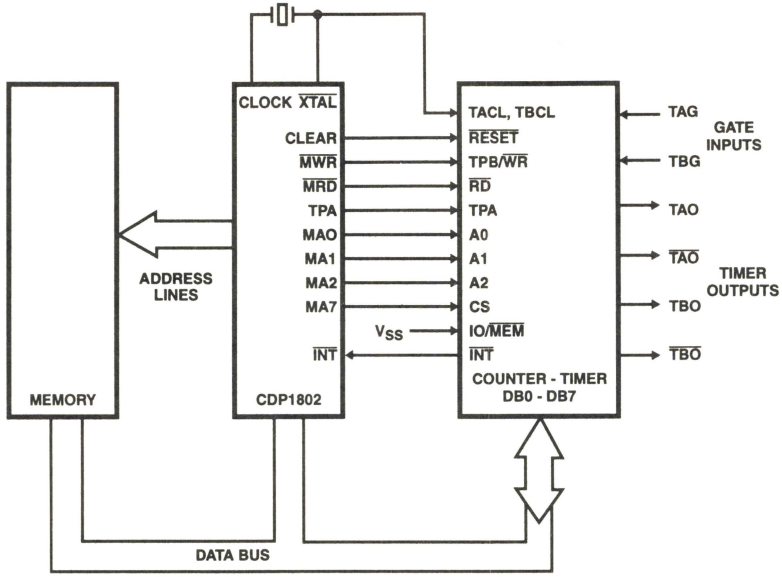


FIGURE 8. TYPICAL CDP1802 MEMORY-MAPPED SYSTEM

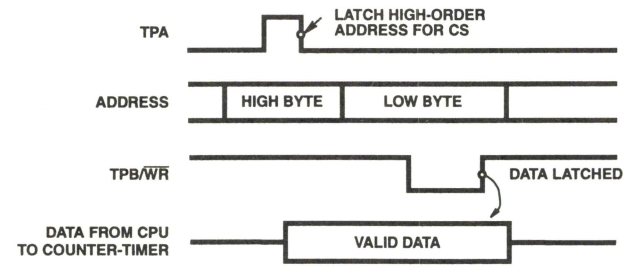


FIGURE 9. CDP1800-SERIES MEMORY-MAPPING WRITE CYCLE TIMING WAVEFORMS

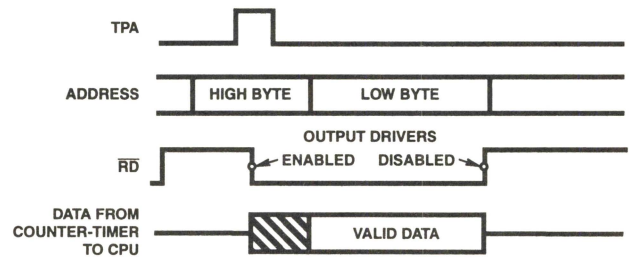


FIGURE 10. CDP1800-SERIES MEMORY-MAPPING READ CYCLE TIMING WAVEFORMS

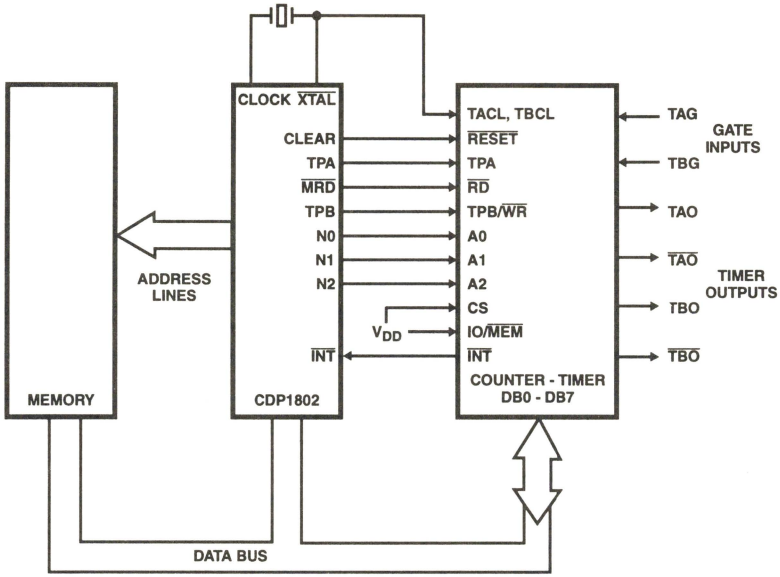


FIGURE 11. TYPICAL CDP1802 INPUT/OUTPUT-MAPPED SYSTEM

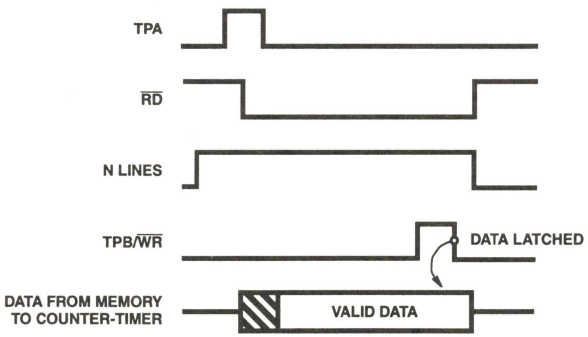


FIGURE 12. CDP1800-SERIES INPUT/OUTPUT-MAPPING TIMING WAVEFORMS WITH OUTPUT INSTRUCTION

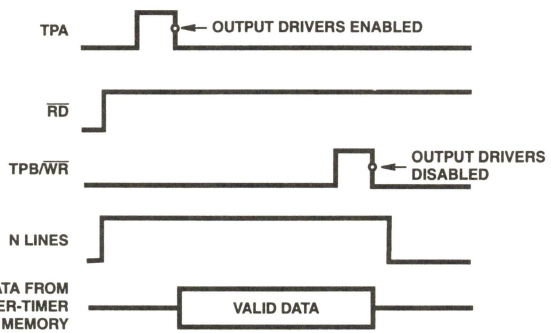


FIGURE 13. CDP1800-SERIES INPUT/OUTPUT-MAPPING TIMING WAVEFORMS WITH INPUT INSTRUCTION

Dynamic Electrical Specifications at T_A = -40 to +85°C, V_{DD} = 5V ± 5%, Input t_R, t_F = 10ns, C_L = 50pF and 1 TTL Load

PARAMETER	SYMBOL	(NOTE 1) MIN	(NOTE 2) TYP	MAX	UNITS
READ CYCLE TIMES (See Figure 14)					
Data Access from Address	t_{DA}	-	350	-	ns
$\overline{\text{Read}}$ Pulse Width	t_{RD}	400	-	-	ns
Data Access from $\overline{\text{Read}}$	t_{DR}	-	250	-	ns
Address Hold after $\overline{\text{Read}}$	t_{RH}	0	-	-	ns
Output Hold after $\overline{\text{Read}}$	t_{DH}	50	-	-	ns
Chip Select Setup to TPA	t_{CS}	50	-	-	ns

NOTES:

1. Time required be a limit device to allow for the indicated function.
2. Typical values are for T_A = 25°C and nominal V_{DD}.

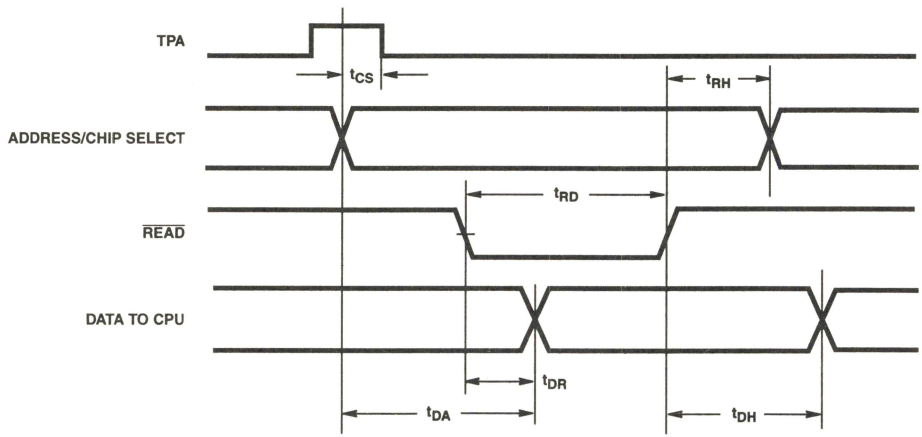


FIGURE 14. READ CYCLE TIMING WAVEFORMS

Dynamic Electrical Specifications at T_A = -40 to +85°C, V_{DD} = 5V ± 5%, Input t_R, t_F = 10ns, C_L = 50pF and 1 TTL Load

PARAMETER	SYMBOL	(NOTE 1) MIN	(NOTE 2) TYP	MAX	UNITS
WRITE CYCLE TIMES (See Figure 15)					
Address Setup to $\overline{\text{Write}}$	t_{AS}	150	-	-	ns
$\overline{\text{Write}}$ Pulse Width	t_{WR}	150	-	-	ns
Data Setup to $\overline{\text{Write}}$	t_{DS}	200	-	-	ns
Address Hold after $\overline{\text{Write}}$	t_{AH}	50	-	-	ns
Data Hold after $\overline{\text{Write}}$	t_{WH}	50	-	-	ns
Chip Select Setup to TPA	t_{CS}	50	-	-	ns

NOTES:

1. Time required by a limit device to allow for the indicated function.
2. Typical values are for T_A = 25°C and nominal V_{DD}.

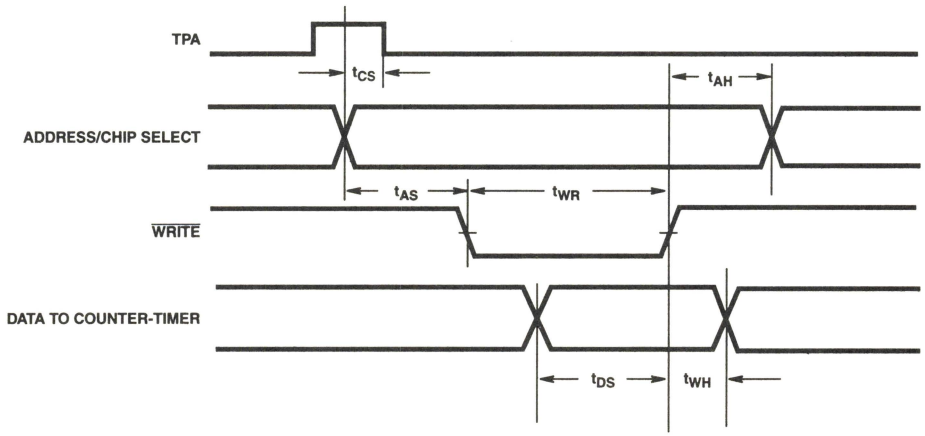


FIGURE 15. WRITE CYCLE TIMING WAVEFORMS

HARRIS SEMICONDUCTOR

CDP1879, CDP1879C-1

March 1997

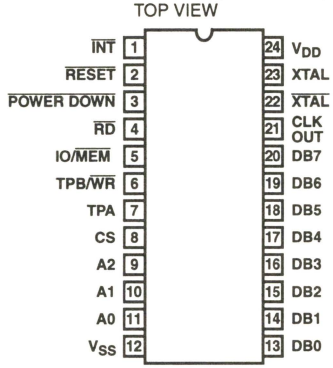
CMOS Real-Time Clock

Features

- CPU Interface for Use with General-Purpose Microprocessors
- Time Of Day/Calendar
- Reads Seconds, Minutes, Hours
- Reads Day of Month and Month
- Alarm Circuit With Seconds, Minutes or Hours Operation
- Power Down Mode
- Separate Clock Output Selects 1 of 15 Square Wave Signals
- Interrupt Output Activated By Clock Output and/or Alarm Circuit
- Date Integrity Sampling for Clock Rollover Eliminated
- On-Board Oscillator:
  - Crystal Operation CDP1879 at 10V. . . . . 4.19MHz, 2.09MHz or 1.048MHz
  - Crystal Operation CDP1879C-1 at 5V. . . . . 4.19MHz, 2.09MHz or 1.048MHz or 32kHz
  - External Clock Operation at 10V or 5V. . . . 4.19MHz, 2.09MHz, 1.048MHz or 32kHz
- Addressable in Memory Space or CDP1800 Series I/O Mode
- Low Standby (Timekeeping) Voltage with External Clock
- Related Literature
  - AN7275, Guide to the Use of CD1879 and CDP1879C1 Real Time Clock

Pinout

CDP1879, CDP1879C-1 (PDIP, SBDIP)
TOP VIEW



Description

The CDP1879 real-time clock supplies time and calendar information from seconds to months in BCD format. It consists of 5 separately addressable and programmable counters that divide down an oscillator input. The clock input can have any one of 4 possible frequencies, allowing flexibility in the choice of crystal or external clock sources. Using an external 32kHz clock source, timekeeping can be performed down to 2.5V (see Standby (Timekeeping) Voltage Operation).

The device can be memory-mapped for use with any general-purpose microprocessor and has the additional capability of operating in the CDP1800 series input/output mode.

The real-time clock functions as a time-of-day/calendar with an alarm capability that can be set for combinations of seconds, minutes or hours. Alarm time is configured by loading alarm latches that activate an interrupt output through a comparator when the counter and alarm latch values are equal.

Fifteen selectable square-wave signals are available as a separate clock output signal and can also activate the interrupt output. A status register is available to indicate the interrupt source. The value in an 8 bit control register determines the operational characteristics of the device, by selecting the prescaler divisor and the clock output, and controls the load and alarm functions.

A transparent "freeze" circuit preclude clock rollover during counter and latch access times to assure stable and accurate values in the counters and alarm latches.

The CDP1879 is functionally identical to the CDP1879C-1. The CDP1879 has a recommended operating voltage range of 4V to 10.5V, and the CDP1879C-1 has a recommended operating voltage range of 4V to 6.5V. The CDP1879 and the CDP1879C-1 are supplied in 24 lead hermetic dual-in-line side-brazed ceramic packages (D suffix) and 24 lead dual-in-line plastic packages (E suffix).

Ordering Information

PACKAGE	TEMP RANGE	5V	10V	PKG. NO.
PDIP	-40°C to +85°C	CDP1879CE1	CDP1879E	E24.6
SBDIP	-40°C to +85°C	CDP1879CD1	-	D24.6
Burn-In		CDP1879CD1X	-	D24.6

CDP1879 Modes of Operation

OPERATION	FUNCTION
Read	1. Seconds, minutes, hours, date and month counters 2. Status register to identify interrupt source
Write	1. Control register to set device operation 2. Seconds, minutes, hours, date and month counters 3. Alarm latches for alarm time
Power Down	1. Three-state interrupt output with active alarm or clock out circuitry for wake-up control 2. Data bus and address inputs are "DON'T CARE"
Interrupt	1. Clock out as source 2. Alarm time as source 3. Either interrupt can occur during normal or power down mode

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1360.2**

Absolute Maximum Ratings

DC Supply Voltage Range, V_{DD}
(Voltage referenced to V_{SS} Terminal)
CDP1879 ..... -0.5V to +11V
CDP1879C-1 ..... -0.5V to +7V
Input Voltage Range, All Inputs ..... -0.5 to V_{DD} +0.5V
DC Input Current, Any One Input ..... ±10mA
Device Dissipation Per Output Transistor 40mW
For T_A = Full Package Temperature Range
(All Package Types)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	60	N/A
SBDIP Package	50	12

Operating Temperature Range (T_A)
Package Type D, H ..... -55°C to +125°C
Package Type E ..... -40°C to +85°C
Storage Temperature Range (T_{STG}) ..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ±1/32 in. (1.59 ± 0.79mm) From Case for 10s Max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions at T_A = Full Package-Temperature Range, Unless Otherwise specified. For maximum reliability, operating conditions should be selected so that operation Is always within the following ranges:

PARAMETER	LIMITS				UNITS
	CDP1879		CDPI879C-1		
	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
DC Standby (Timekeeping) Voltage (Note 1), V_{STBY}					
T_A = -40°C to +85°C (Note 2)	3	-	3	-	V
T_A = 0° to +70°C	2.5	-	2.5		V
Clock Input Rise or Fall Time, t_R, t_F					
V_{DD} = 5V	-	10	-	10	µs
V_{DD} = 10V	-	1	-	-	µs

NOTES:

1. Timekeeping function only, no READ/WRITE accesses, 32kHz external frequency source only, no crystal operation.
2. See Standby (Timekeeping) Voltage Operation.

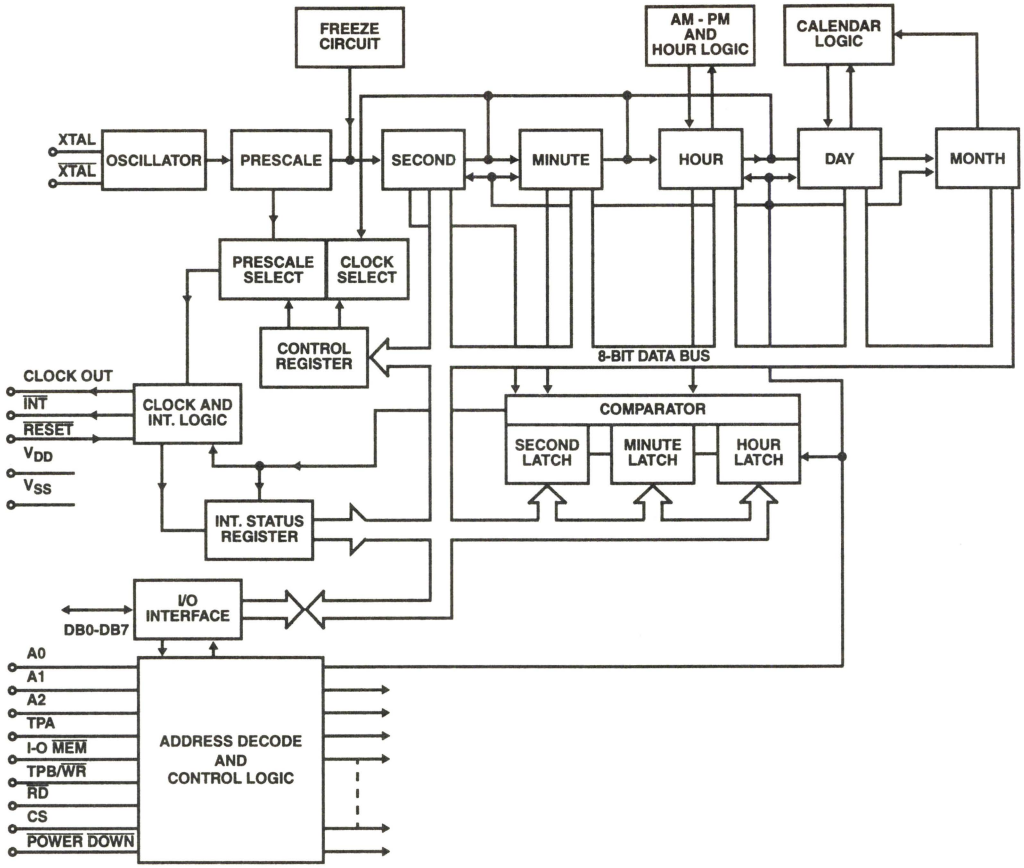


FIGURE 1. REAL-TIME CLOCK FUNCTIONAL DIAGRAM

TABLE 1.

CONTROL REGISTER BIT ASSIGNMENT	
Bit 1, 0	
Frequency 00	32768Hz
Select 01	1.048576MHz
10	2.097152MHz
11	4.194304MHz
Bit 2	
Start/Stop	1 = Start
	0 = Stop
Bit 3	
Counter/Latch Control	
"0" = Write to Counter and disable alarm	
"1" = Write to and enable alarm Clock Select	
Bit 7, 6, 5, 4	
0000 - disableμs	1000 - 62.5ms
0001 - 488.2μs	1001 - 125ms
0010 - 976.5μs	1010 - 250ms
0011 - 1953.1μs	1011 - 500ms
0100 - 3906.2μs	1100 - sec.
0101 - 7812.5μs	1101 - min.
0110 - 15.625ms	1110 - hour
0111 - 31.25ms	1111 - day

TABLE 2.

ADDRESSES	A2	A1	A0
Latch, Counter Seconds	0	1	0
Latch, Counter Minutes	0	1	1
Latch, Counter Hours	1	0	0
Counter, Day	1	0	1
Counter, Month	1	1	0
Control, Register	1	1	1
Status Register	1	1	1
MSB of Hours Counters (Bit 7) is an AM-PM Bit. 0 = AM; 1 = PM			
Bit 6 of Hours Counter Controls 12/24 hr. 1 = 12 Hr: 0 = 24 Hr.			
Status Register: Bit 7 MSB = Alarm Interrupt Source: Bit 6 = Clock.			
MSB of Month Counter (Bit 7) is a Leap Year Bit 0 = No, 1 = Yes.			

Static Electrical Specifications at T_A -40°C to +85°C V_{DD} ± 5%, Unless Otherwise Specified

PARAMETER		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS CDP1879 MIN	LIMITS CDP1879 (NOTE 1) TYP	LIMITS CDP1879 MAX	LIMITS CDPI879C-1 MIN	LIMITS CDPI879C-1 (NOTE 1) TYP	LIMITS CDPI879C-1 MAX	UNITS
Quiescent Device Current	I_{DD}		0, 5	5	-	0.01	50	-	0.02	200	µA
			0, 10	10	-	1	200	-	-	-	
Output Low Drive (Sink) Current, Data Bus and $\overline{INT}$	I_{OL}	0.4	0, 5	5	1.8	4	-	-	-	-	mA
		0.5	0,10	10	3.6	7	-	-	-	-	
Output High Drive (Source) Current, Data Bus and $\overline{INT}$	I_{OH}	4.6	0, 5	5	-1.1	-2.3	-	-1.1	-2.3	-	
		9.5	0,10	10	-2.6	-4.4	-	-	-	-	
Output Low Drive (Sink) Current, Clock Out	I_{OL}	0.4	0, 5	5	0.6	1.4	-	0.6	1.4	-	
		0.5	0,10	10	1.2	3	-	-	-	-	
Output High Drive (Source) Current, Clock Out	I_{OH}	4.6	0, 5	5	-1.1	-2.3	-	-1.1	-2.3	-	
		9.5	0,10	10	-2.6	-4.4	-	-	-	-	
Output Low Drive (Sink) Current, $\overline{XTAL}$ Out	I_{OL}	0.4	0, 5	5	0.2	0.9	-	0.2	0.9	-	
		0.5	0,10	10	0.4	2	-	-	-	-	
Output High Drive (Source) Current, $\overline{XTAL}$ Out	I_{OH}	4.6	0, 5	5	-0.15	-0.4	-	-0.15	-0.4	-	
		9.5	0,10	10	-0.3	-0.7	-	-	-	-	
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0,10	10	-	0	0.1	-	-	-	
Output Voltage High Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	
		-	0, 10	10	9.9	10	-	-	-	-	
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	
		0.5, 9.5	-	10	-	-	3	-	-	-	
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	
		0.5, 9.5	-	10	7	-	-	-	-	-	
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	-	±1	-	-	±1	µA
			0, 10	10	-	-	±2	-	-	-	
Three-State Output Leakage Current	I_{OUT}	0, 5	0,5	5	-	-	±1	-	-	±1	
		0,10	0,10	10	-	-	±1	-	-	-	
Operating Current (Note 3)											
External Clock	32kHz	-	-	5	-	0.01	0.15	-	0.01	0.15	mA
External Clock	1MHz	-	-	5	-	0.2	1	-	0.2	1	
External Clock	2MHz	-	-	5	-	0.35	1.5	-	0.35	1.5	
External Clock	4MHz	-	-	5	-	0.7	2	-	0.7	2	
External Clock	32kHz	-	-	10	-	0.03	0.25	-	-	-	
External Clock	1MHz	-	-	10	-	0.4	2	-	-	-	
External Clock	2MHz	-	-	10	-	0.8	3	-	-	-	
External Clock	4MHz	-	-	10	-	1.6	4.5	-	-		
XTAL Oscillator (Note 4)	32kHz	-	-	5	-	0.1	0.25	-	0.1	0.25	
XTAL Oscillator (Note 4)	1MHz	-	-	5	-	0.3	0.5	-	0.3	0.5	
XTAL Oscillator (Note 4)	2MHz	-	-	5	-	0.4	0.6	-	0.4	0.6	
XTAL Oscillator (Note 4)	4MHz	-	-	5	-	0.6	0.8	-	0.6	0.8	
XTAL Oscillator (Note 4)	1MHz	-	-	10	-	1.6	3	-	-	-	
XTAL Oscillator (Note 4)	2MHz	-	-	10	-	1.8	3.5	-	-	-	
XTAL Oscillator (Note 4)	4MHz	-	-	10	-	2	5	-	-	-	

Static Electrical Specifications at T_A -40°C to +85°C V_{DD} ± 5%, Unless Otherwise Specified **(Continued)**

PARAMETER		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS CDP1879 MIN	LIMITS CDP1879 (NOTE 1) TYP	LIMITS CDP1879 MAX	LIMITS CDPI879C-1 MIN	LIMITS CDPI879C-1 (NOTE 1) TYP	LIMITS CDPI879C-1 MAX	UNITS
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	
Maximum Clock Rise and Fall Times	t_R, t_F	-	-	5	-	-	10	-	-	10	µs
		-	-	10	-	-	1	-	-	-	

NOTES:

1. Typical values are for T_A = 25°C and nominal V_{DD}.
2. $I_{OL} = I_{OH}$ = 1µA.
3. Operating current measured with clockout = 488.2µs and no load.
4. See Table 3 and Figure 6 for oscillator circuit information.

Programming Model

WRITE AND READ REGISTERS

BCD FORMAT

DB7 DB0

TENS 0-5	UNITS 0-9

SECONDS COUNTER (00-59)

DB7 DB0

TENS 0-5	UNITS 0-9

MINUTES COUNTER (00-59)

DB7 DB6 DB0

X	X	TENS 0-2	UNITS 0-9

HOURS COUNTER (01 - 12 OR 00-23)
DB7 0=AM, 1=PM
DB6 0=24 HR, 1=12 HR

DB7 DB0

TENS 0-3	UNITS 0-9

DAY OF MONTH COUNTER
(01-28, 29, 30, 31)

DB7 DB0

X	TENS 0 OR 1	UNITS 0-9

MONTH COUNTER
(JAN=1 DEC=12)
DB7 0=NO LEAP YEAR
1=LEAP YEAR

WRITE ONLY REGISTERS

DB7 DB0

7	6	5	4	3	2	1	0

CONTROL REGISTER

DB0-DB1 - FREQUENCY SELECT
DB2 - START/STOP
DB3 - COUNTER/ALARM LATCH CONTROL
DB4-DB7 - CLOCK OUTPUT SELECT

DB7 DB0

TENS 0-5	UNITS 0-9

SECONDS ALARM LATCH (00-59)

DB7 DB0

TENS 0-5	UNITS 0-9

MINUTES ALARM LATCH (00-59)

DB7 DB6 DB0

X	X	TENS 0-2	UNITS 0-9

HOURS ALARM LATCH (01-12 OR 00-23
12 HR, DB7=0 AM, 1=PM
24 HR, DB7=X

READ ONLY REGISTER

DB7 DB6 DB0

X	X	0	0	0	0	0	0

INTERRUPT STATUS REGISTER
DB7=1 ALARM CIRCUIT ACTIVATED $\overline{INT}$.
DB6=1 CLOCK OUTPUT ACTIVATED $\overline{INT}$.

REGISTER TRUTH TABLE

ADDRESS			ACTIVE SIGNAL		BIT 3 CONTROL REGISTER	REGISTER OPERATION
A2	A1	AO	TPB/$\overline{WR}$	$\overline{RD}$		
0	1	0	X	-	0	Write Seconds Counter
0	1	0	-	X	0	Read Seconds Counter
0	1	1	X	-	0	Write Minutes Counter
0	1	1	-	X	0	Read Minutes Counter
1	0	0	X	-	0	Write Hours Counter
1	0	0	-	X	0	Read Hours Counter
1	0	1	X	-	0	Write Date Counter
1	0	1	-	X	0	Read Date Counter
1	1	0	X	-	0	Write Month Counter
1	1	0	-	X	0	Read Month Counter
0	1	0	X	-	1	Write Seconds Alarm Latch
0	1	1	X	-	1	Write Minutes Alarm Latch
1	0	0	X	-	1	Write Hours Alarm Latch
1	1	1	X	-	-	Write Control Register
1	1	1	-	X	-	Read Int. Status Register

General Operation

The real-time clock contains seconds, minutes, and hours, date and month counters that hold time of day/calendar information (see Figure 2). The frequency of an intrinsic oscillator is divided down to supply a once-a-second signal to the counter series string. The counters are separately addressable and can be written to or read from.

The real-time clock contains seconds, minutes and hour write-only alarm latches that store the alarm time (see Figure 3). When the value of the alarm latches and counters are equal, the interrupt output is activated. The interrupt output can also be activated by a clock output transition. The clock output is derived from the prescaler and counters and can be one of 15 square-wave signals. The value in the read-only interrupt status register identifies the interrupt source.

Operational control of the real-time clock is determined by the byte in a write-only control register. The 8-bit value in this register determines the correct divisor for the prescaler, a data direction and alarm enable bit, clock output select, and start/stop control (see Figure 4).

Data transfer and addressing are accomplished in two modes of operation, memory mapping and I/O mapping using the CDP1800-series microprocessors. The mode is selected by the level on an input pin. (IO/$\overline{MEM}$). Memory mapping implies use of the address lines as chip selects and address inputs during linear selection or partial or full decoding methods. I/O mapping with the CDP1800-series microprocessors involves use of the N line outputs in conjunction with input and output instructions to transfer data to and from memory.

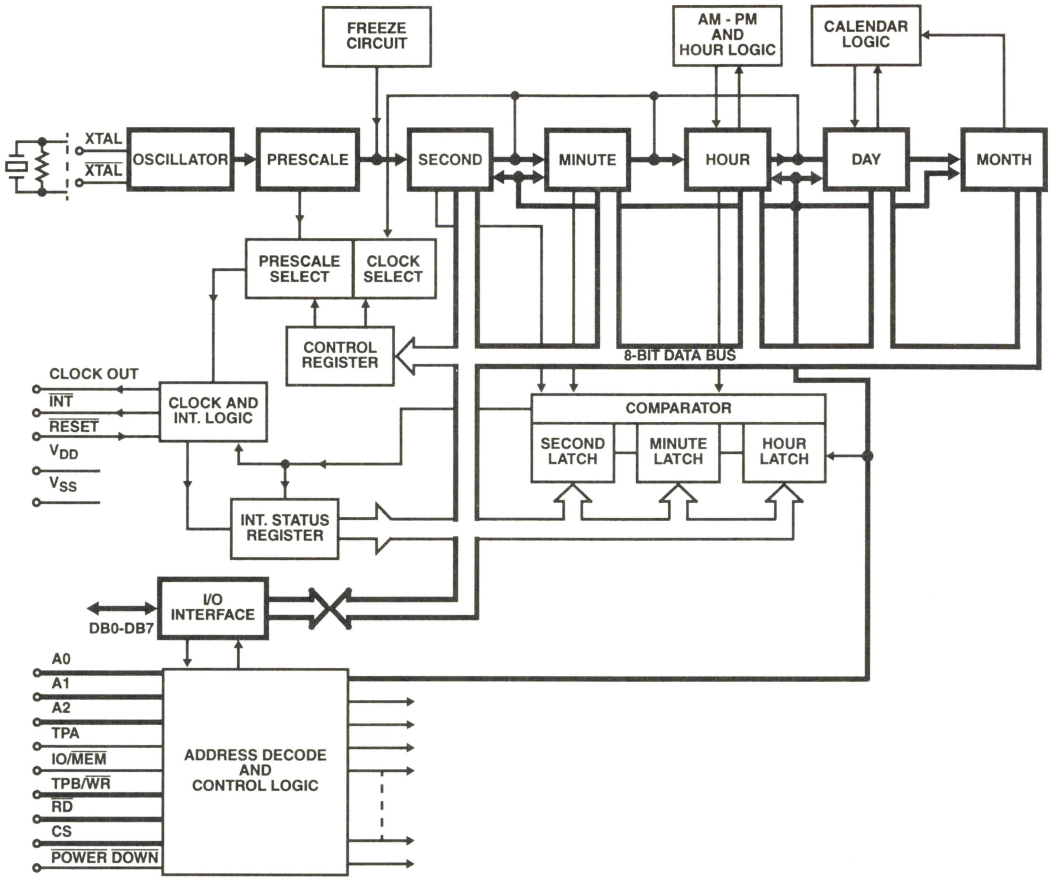


FIGURE 2. FUNCTIONAL DIAGRAM - TIME COUNTERS HIGHLIGHTED

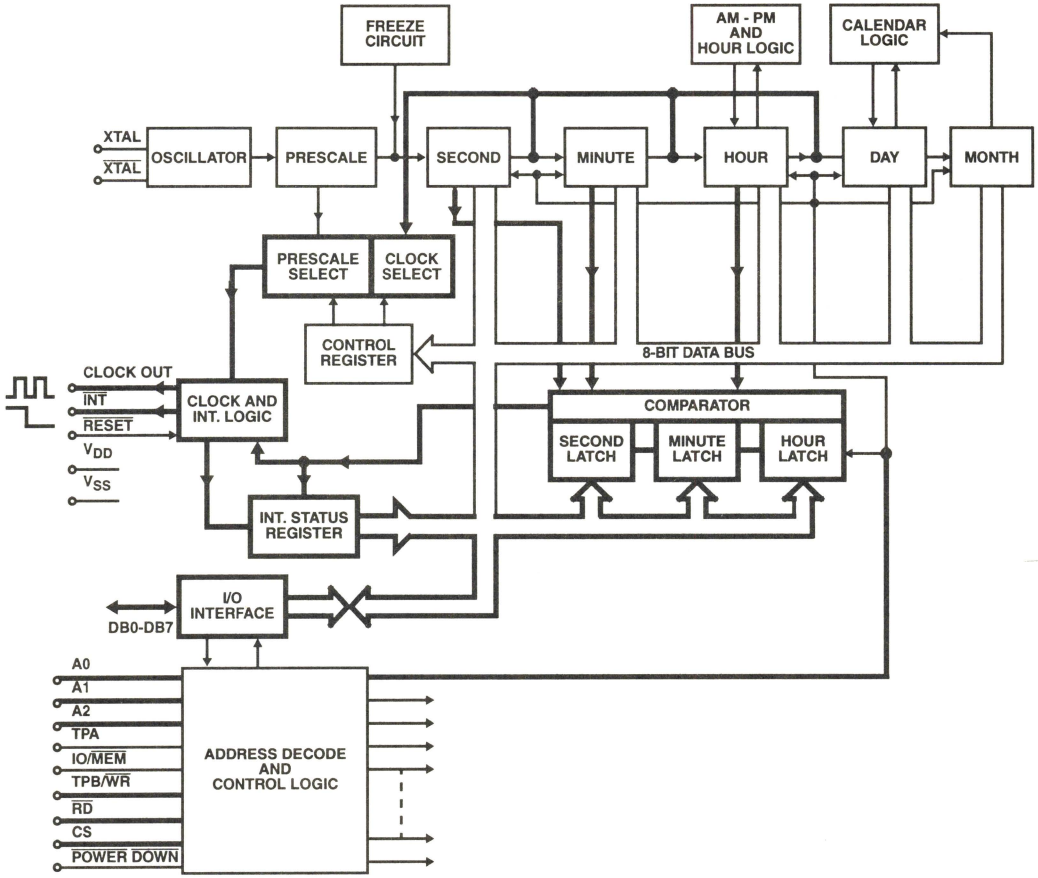


FIGURE 3. FUNCTIONAL DIAGRAM - ALARM CIRCUIT, CLOCK OUTPUT, INTERRUPT, AND STATUS REGISTERS HIGHLIGHTED

Operational Sequence

Power is applied and the real-time clock is reset. This sets the interrupt output pin high. After the CS pin is set high and with address 7 on the address input lines, the control register is loaded via the data bus to configure the clock.

With selective addressing, the seconds through month counters are then written to and loaded to set the current time. The real-time clock will now hold the current "wall clock" time, with an accuracy determined by the crystal or external clock used. If the alarm function is desired, the control register is accessed and loaded again. This new byte will allow subsequent time data to be entered into the seconds, minutes and hours alarm latches. This sequence is also used when selecting one of the 15 available clock-out signals.

If the alarm function was selected, the interrupt output pin will be set low when the values in the seconds, minutes and hour alarm latches match those in the seconds, minutes and hour counters.

If one of the 15 sub second-to-day clock outputs is selected by the byte in the control register, the clock output pin toggles at that frequency (50% duty cycle) The interrupt output will also be set low on the first clock out negative transition. The interrupt source (alarm or clock out) can be determined by reading the interrupt status register. The clock output can be deselected by placing zero in the upper nibble of the control register if the alarm function is selected as the only interrupt source.

Counters

The counter section consists of an on-board oscillator, a prescaler and 5 counters that hold the time of day/calendar information (see Figure 2).

1 of 4 possible external crystals determine the frequency of the on-board oscillator (32,768Hz, 1.048576MHz, 2.097152MHz, 4.194304MHz). The oscillator output is divided down by a pres-

caler that supplies a once-a-second pulse to the counters. The seconds counter divide the pulse by 60 and its output clocks the minute counter every 60 seconds Further division by the minutes, hours, day of month and month counters result in 5 counters holding data that reflect the time/calendar from seconds to months. The counters are addressed separately and BCD data is transferred to and from via the data bus. The most significant bit of the hours counter (Bit 7) is user programmed to indicate AM or PM and will be inverted every 12th hour. (0=AM, 1=PM). Bit 6 of the hours counter is user programmed to enable the hours counter for 12 or 24 hour operation. (0=24,1=12). If 24-hour operation is selected, the AM-PM bit is "don't care", but still toggles every 12th hour. Writing to the seconds counter resets the last 7 stages of the prescaler, allowing time accuracy to approximately 1/100 of a second.

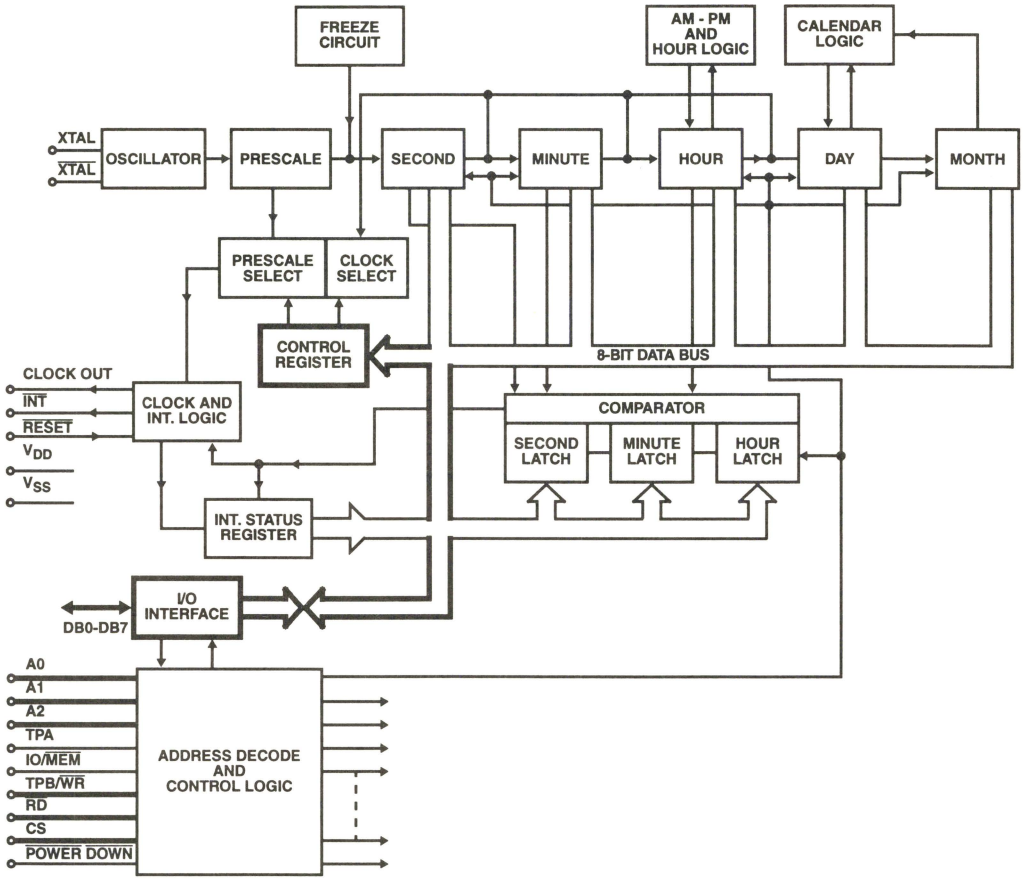


FIGURE 4. FUNCTIONAL DIAGRAM - CONTROL REGISTER HIGHLIGHTED

The most significant bit of the month counter is a Leap Year bit. If it is set to "1", the counter will count to February 29, then roll to March 1. If set to "0" it will go to March 1st after February 28th.

Alarm And Interrupt Status Register

The alarm circuit consists of 1) seconds, minutes and hour alarm latches that hold the alarm time, 2) the outputs of the seconds, minutes and hour counters, and 3) a comparator that drives an interrupt output. The comparator senses the counter and alarm latch values and activates the interrupt output (active low) when they are equal (see Figure 3).

The write-only alarm latches have the same addresses as their comparable counters. Bit 3 in the control register determines data direction to the latches or counters and alarm enabling. For example, during a write cycle, if bit-3 in the control register is a "1", addressing the seconds counter or alarm latch will load the seconds alarm latch from the data bus and will enable the alarm function. Conversely, if bit-3 in the control register is a "0", addressing the seconds counter or alarm latch during a write cycle will place the value on the data bus into the seconds counter and will disable the alarm function. The interrupt output can be activated by the alarm circuit or the clock output. When an interrupt occurs, the

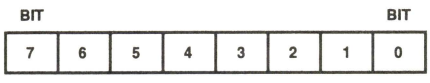
upper two bits of the interrupt status register identify the interrupt source. The interrupt status register has the same address as the control register. Addressing the interrupt status register with the $\overline{RD}$ line active will place these register bits on the data bus. Bits 0-5 are held low. A "1" in bit-6 represents a clock output transition as the interrupt source. A "1" in bit-7 will identify the alarm circuit as the interrupt source.

Activating the reset pin (active low) resets the hour latch to "30" which prevents a match between alarm and time registers during an initialization procedure. Activating the reset pin or writing to the control register resets the interrupt output (high) and clears the interrupt status register

Clock Output

One of 15 counter and prescaler overflows can be selected as a 50% duty cycle output signal that is available at the "clock out" pin. The frequency is selected by the upper nibble in the control register. For example, selecting a one-second clock output will result in a repetitive signal that will be high for 500ms and low for the same period. The high-to-low transition of the output signal will set the clock bit in the status register and activate the interrupt output. The level of the "clock out" signal is derived from the value in the counter. Example - if hours clock is selected and the minutes counter holds 4 minutes, the clock out will be low for 26 minutes and high for 30 minutes Thereafter, the clock out will toggle at a 50% duty cycle rate (see Table 1 and Figure 3).

CONTROL REGISTER (SEE TABLE 1 AND FIGURE 4)



CONTROL REGISTER BYTE

The 8-bit value in the control register determines the following:

1. **Bit 0 and 1 - Frequency Select** - Since there are one of 4 possible crystals the oscillator in the real-time clock can operate with, these bit levels determine the prescaler divisor so that an accurate one second pulse is supplied to the counter series string.

BIT 1	BIT 0	FREQUENCY
0	0	32,768Hz
0	1	1.048576MHz
1	0	2.097152MHz
1	1	4.194304MHz

2. **Bit 2 - Start-Stop Control** - Counter enabling is controlled by the value at this location. A "1" will allow the counters to function and a "0" in this location will disable the counters.

3 **Bit 3 - Counter/Latch Control** - The level at this location controls two functions. It is required since the counters and alarm latches have the same addresses.

   1) A "0" in bit-3 will direct subsequent data to or from the counter selected and the alarm function will be disabled.

   2) A "1" in bit-3 will direct subsequent data to or from the alarm latch and will enable the alarm.

4. **Bits 4 to 7 - Clock Select** - These bits select one of 15 square-wave signals that will be present at the "clock-out" pin. If bit-4 to bit-7 are zero's, the clock output pin will be high. If a clock is selected, the first high-to-low clock out transition will activate the interrupt pin (active low) and place a "1" in bit-6 of the status register. Writing to the control register or activating the reset pin will set the interrupt pin high and reset the interrupt status register.

Normal operation requires the control register to be written to and loaded first with a control word. However, subsequent writing to a counter if a "clock out" is selected may cause an interrupt out signal. Therefore, "clock-out" should be deselected by writing zero's into bit-4 through bit-7 if the interrupt is used. When the counters are loaded, the control register is again written to with the value in the upper nibble selecting the "clock out" signal. See Table 1.

Read And Write Signals

When the IO/$\overline{MEM}$ pin is low, the real-time clock is enabled for memory mapped operation. Data on the bus is placed in, or read from a counter, alarm latch or register by 1) placing the CS pin high, 2) selective addressing, 3) placing the TPB/$\overline{WR}$ pin low during a write cycle with the $\overline{RD}$ pin high or 4) setting the $\overline{RD}$ pin low during a read cycle with this TPB/$\overline{WR}$ pin high.

The I/O mapping mode used with the CDP1800 series microprocessor is selected by setting the IO/$\overline{MEM}$ pin high. The TPB/$\overline{WR}$ pin on the real-time clock is connected to the TPB output pin of the microprocessor. Data on that bus is written to or read from the counters, latches and registers by 1) placing the CS pin high, 2) selective addressing utilizing the microprocessor N lines and I/O instructions, 3) placing the TPB/$\overline{WR}$ pin high with the $\overline{RD}$ pin low during an output or write operation (data is latched on TPB's trailing edge), 4) setting the $\overline{RD}$ line high during an input or read operation. Data is placed on the bus by the real-time clock between the trailing edges of TPA and TPB.

Freeze Circuit

Since writing to or reading from the counters or alarm latches is performed asynchronously, the once-a-second signal from the prescaler may pulse the counter series string during these operations. This can result in erroneous data. To avoid this occurring, a transparent "freeze" circuit' is incorporated into the real-time clock. This circuit is designed to trap and hold the one-second input clock transition if it occurs during access times. When the operations are completed, it is inserted into the counter series string. To utilize the "freeze" circuit, address "1" (A0 = 1, A1 = 0, A2 = 0) is selected first while performing a write operation. Read or write accesses may now be performed with assurance the data is stable. All operations must be concluded within

250ms of the address "1" access. In memory mapping any dummy write operation after selecting address "1" will set the "freeze" circuit. If using the I/O mode, a 61 output instruction will perform the same function. There is no time restriction on subsequent accesses as long as the read or write operations are preceded by selecting address "1".

Power Down

Power down operation is initiated with a low signal on the "POWER DOWN" input pin. In conjunction with the interrupt output, it is used to supply external control circuits with a 3 level control signal. The operating current is not appreciably reduced during "POWER DOWN" operation. When power down is initiated, any inputs on the address or data bus are ignored. The clock output is set low. The interrupt output is three-stated. If enabled previously, the alarm circuitry is active and will set the interrupt output pin low when alarm time occurs. The interrupt output will also go low if a clock was selected and an internal high-to-low transition occurs during power down. The clock output pin will remain low. If power down is initiated in the middle of a read or write sequence, it will not become activated until the read or write cycle is completed.

Pin Functions

V_{DD}, V_{SS} - Power and ground for device.

DB0 - DB7 - DATA BUS - 8-bit bidirectional bus that transfers BCD data to and from the counters, latches and registers.

A0, A1, A2 - Address inputs that select a counter, latch or register to read from or write to.

TPA - Strobe input used to latch the value on the chip select pin. CS is latched on the trailing edge of TPA. During memory mapping, it is used to latch the high order address bit used for the chip select. When the real-time clock is used with other microprocessors, or when the high order address of the CDP1800 series microprocessor is externally latched, it is connected to V_{DD}. In the input/output mode, it is used to gate the N lines.

IO/MEM - Tied low during memory mapping and high when the input/output mode of the CDP1800 series microprocessor is used.

RD, TPB/WR - Direction Signals - Active signals that determine data direction flow. In the memory mapped mode, data is placed on the bus from the counters or status register when $\overline{RD}$ pin is active.

Data is transferred to a counter, latch or the control register when $\overline{RD}$ is high and TPB/$\overline{WR}$ is active and latched on the trailing edge (low to high) of the TPB/$\overline{WR}$ signal.

In the input/output mode, data is placed on the bus from a counter or status register when RD is not active between the trailing edges of TPA and TPB. Data on the bus is written to a counter, latch, or the control register during TPB when $\overline{RD}$ is active and latched on TPB's trailing edge. The following connections are required between the microprocessor and real-time clock in the CDP1800 series I/O mode.

Microprocessor Real-Time Clock

$\overline{MRD}$	$\overline{RD}$
TPB	TPB/$\overline{WR}$
TPA	TPA
N LINES	ADDRESS LINES
IO/$\overline{MEM}$	V_{DD}

CS - CHIP SELECT - Used to enable or disable the inputs and outputs. TPA is used to strobe and latch a positive level on this pin to enable the device.

XTAL AND XTAL - The frequency of the internal oscillator is determined by the value of the crystal connected to these pins. "XTAL" may be driven directly by an external frequency source.

Clock Out - 1 of 15 square wave frequencies will appear at this pin when selected. During power down, this pin will be placed low, and will be high during normal operation when the clock is deselected.

Power Down - Power Down Control - A low on this pin will place the device in the power down mode.

INT - Interrupt Output - A low on this pin indicates an active alarm time or high-to-low transition of the "clock out" signal.

RESET - A low on this pin clears the status register and places the interrupt output pin high.

Frequency Input Requirements

The Real-Time Clock operates with the following frequency input sources:

1. An external crystal that is used with the on-board oscillator. The oscillator is biased by a large feedback resistor and oscillates at the crystal frequency (see Figure 6, Table 3).
2. An external frequency input that is supplied at the XTAL input. $\overline{XTAL}$ is left open (see Figure 5). A typical external oscillator circuit is shown in Figure 7 in section, "Standby (Timekeeping) Voltage Operation".

TABLE 3. TYPICAL OSCILLATOR CIRCUIT PARAMETERS FOR SUGGESTED OSCILLATOR CIRCUIT, SEE FIGURE 6

PARAMETER	4.197MHz	2.097MHz	1.049MHz	32768Hz (NOTE)	UNITS
R_F	22	22	22	22	MΩ
C_0	39	39	39	39	pF
C_1	5	5	5	5	pF
R_S	-	-	-	200	kΩ
C_L	-	-	-	91	pF
Crystal Impedance	73	200	200	50K (max.)	Ω

NOTE: CDP1879C-1 only.

Design Considerations for Stable Crystal Oscillation

1. Stray capacitances should be minimized for best oscillator performance. Circuit board traces should be kept to a maximum of 1 inch, and there should be no parallel traces.
2. A signal line or power source line must not cross or go near the oscillator circuit line.
3. It is advisable to put a 0.1μF capacitor between V_{DD} and V_{SS} of the CDP1879.

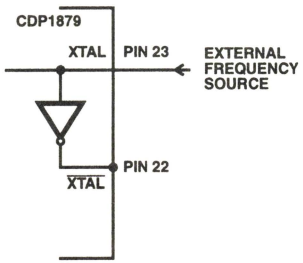


FIGURE 5. CONNECTIONS FOR AN EXTERNAL FREQUENCY SOURCE APPLIED TO REAL-TIME CLOCK

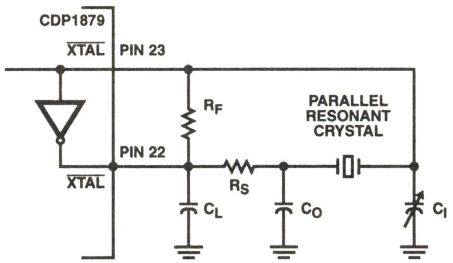


FIGURE 6. SUGGESTED OSCILLATOR CIRCUIT APPLIED TO REAL-TIME CLOCK (SEE TABLE 3)

Standby (Timekeeping) Voltage Operation

When any one of the four specified crystals is used with the on-board oscillator, the Real-Time Clock can operate at a minimum of 4V V_{DD}. However, at 32kHz the clock will run (timekeeping only, no device READ/WRITE accesses) down to 3V at -40°C to +85°C and 2.5V at 0° to +70°C.

To achieve this low voltage operation, an external 32kHz clock source must be supplied at the XTAL input (see Figure 7). The standby requirements for CHIP SELECT/DESELECT are listed in Table 4, and Figure 8 indicates the timing waveforms. Figure 9 illustrates the typical timekeeping curve over the full temperature range.

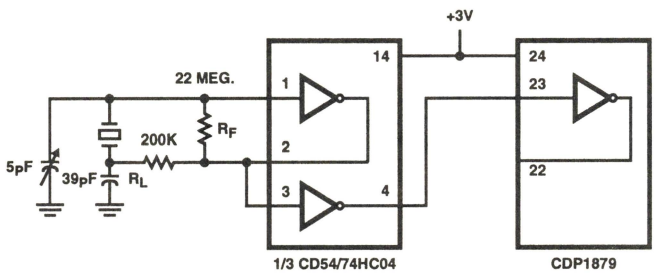
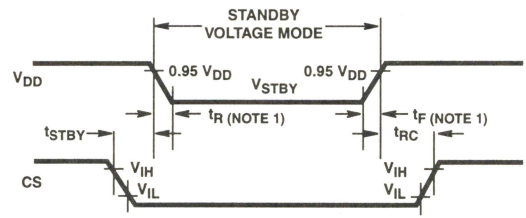


FIGURE 7. TYPICAL EXTERNAL CLOCK-SOURCE CIRCUIT

STANDBY (TIMEKEEPING) CHARACTERISTICS AT FULL TEMPERATURE RANGE

PARAMETER		V_{DD} (V)	V_{STBY} (V)	LIMITS				UNITS
				CDP1879		CDP1879C-1		
				MIN	MAX	MIN	MAX	
Chip Deselect to Standby (Timekeeping) Voltage Time	t_{CSTBY}	5	2.5, 3	2	-	2	-	µs
		10	2.5, 3	1	-	-	-	
Recovery to Normal Operation Time	t_{RC}	5	2.5, 3	2	-	2	-	
		10	2.5, 3	1	-	-	-	



NOTE:

1. t_R, $t_F \geq 1\mu s$

FIGURE 8. STANDBY (TIMEKEEPING) VOLTAGE AND TIMING WAVEFORMS

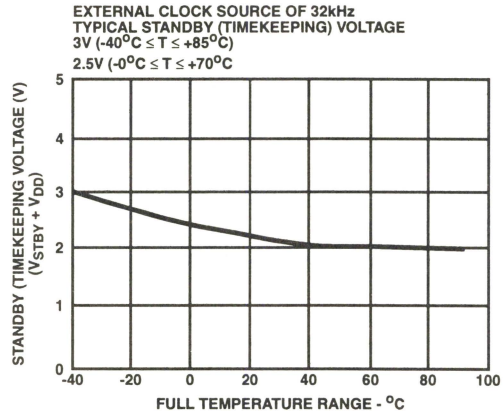


FIGURE 9. TYPICAL STANDBY (TIMEKEEPING) VOLTAGE vs FULL TEMPERATURE RANGE

Applications

A typical application for this real-time clock is as a wake-up control to a CPU to reduce total system power in intermittent-use systems. A hookup diagram illustrating this feature is shown in Figure 10. In this configuration, the alarm and power-down features of the CDP1879 are utilized in the control of the sleep and wake-up states of the CPU. A typical shut-down/start-up sequence for this system could proceed as follows:

1. The CPU has finished a current task and will be inactive for the next six hours.
2. The CPU loads the CDP1879 alarm registers with the desired wake-up time.
3. The CDP1800 Q output is set high, which stops the CPU oscillator (as an alternative, in an NMOS system, power to all components except the clock chip could be shut off).
4. This Q output signal is received by the CDP1879 as a power-down signal.
5. The CDP1879 three-states the interrupt output pin.
6. The CDP1879 eventually times out, and sets an alarm by driving the $\overline{INT}$ output low.
7. The alarm signal resets the CPU (to avoid oscillator start-up problems) and flags the processor for a warm-start routine.
8. The CPU, once into its normal software sequence, writes to the CDP1879 control register to reset the interrupt request.

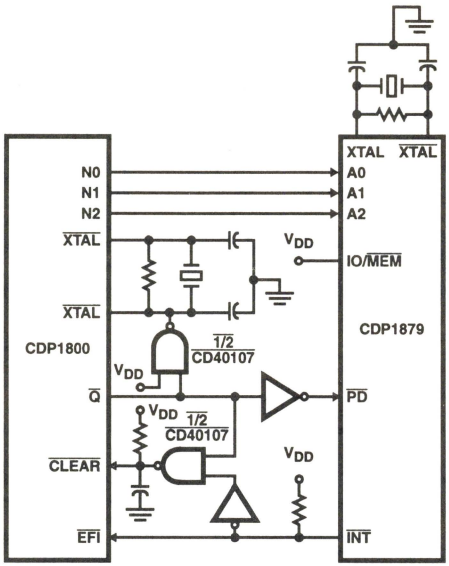


FIGURE 10. CPU WAKE-UP CIRCUIT USING THE CDP1879 REAL-TIME CLOCK

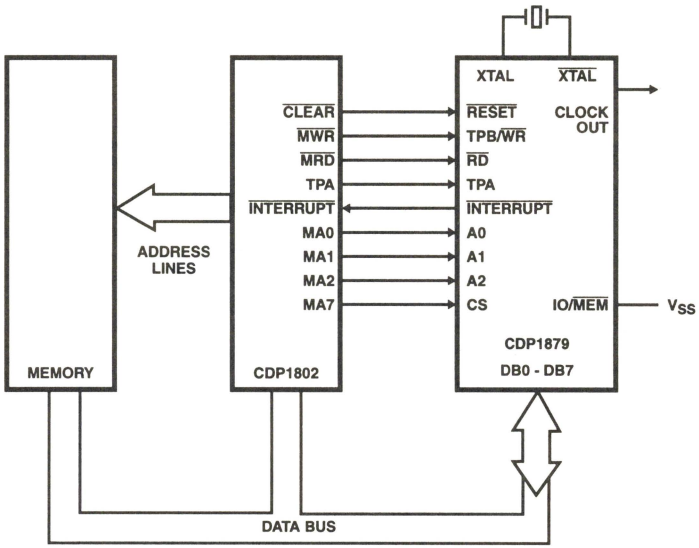


FIGURE 11. TYPICAL CDP1802 MEMORY MAPPED SYSTEM

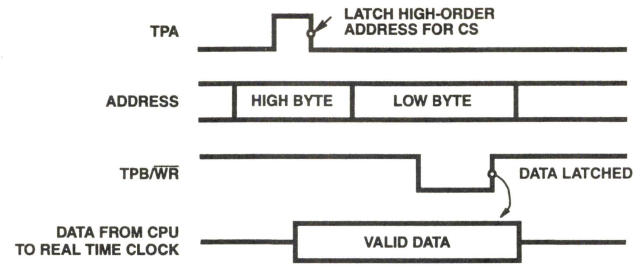


FIGURE 12. CDP1800 SERIES MEMORY MAPPED WRITE CYCLE TIMING WAVEFORMS

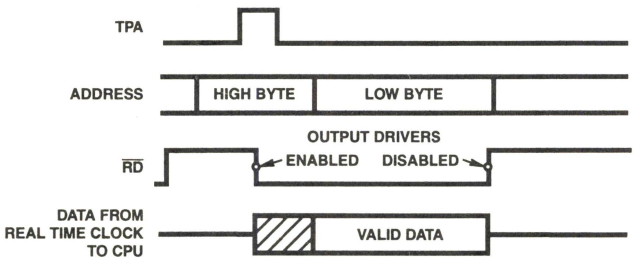


FIGURE 13. CDP1800 SERIES MEMORY MAPPED READ CYCLE TIMING WAVEFORMS

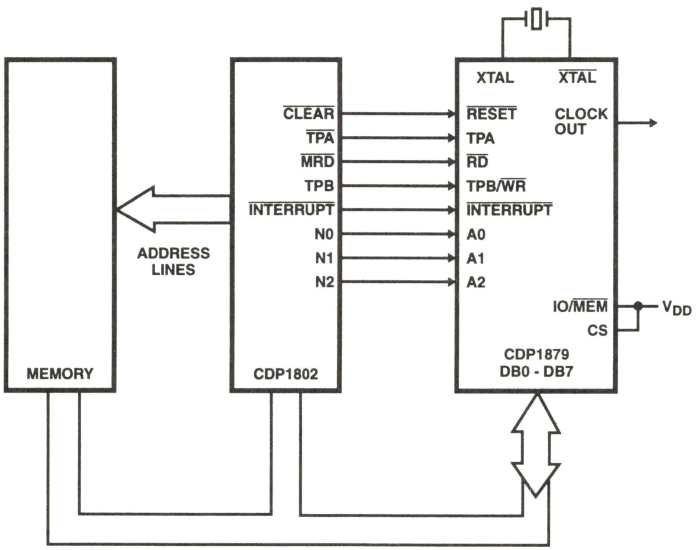


FIGURE 14. TYPICAL CDP1802 INPUT/OUTPUT MAPPED SYSTEM

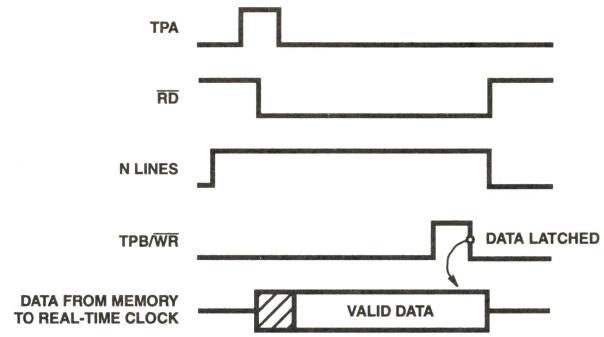


FIGURE 15. CDP1800 SERIES INPUT/OUTPUT MAPPING TIMING WAVEFORMS WITH OUTPUT INSTRUCTION

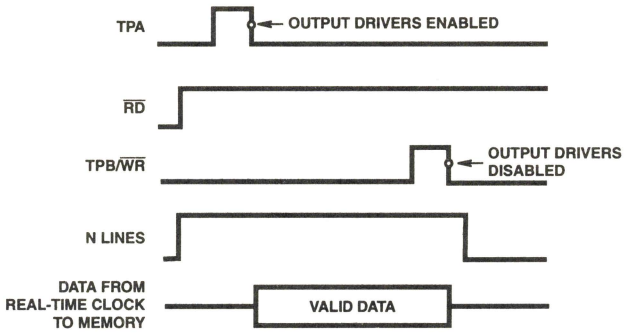


FIGURE 16. CDP1800 SERIES INPUT/OUTPUT MAPPING TIMING WAVEFORMS WITH INPUT INSTRUCTION

Dynamic Electrical Specifications at T_A -40°C to +85°C, Input t_R, t_F = 10ns, C_L = 50pF

PARAMETER		V_{DD} (V)	LIMITS				UNITS
			CDP1879		CDP1879C-1		
			(NOTE 1) MIN	MAX	(NOTE 1) MIN	MAX	
Read Cycle Times (See Figure 17)							
Data Access from Address	t_{DA}	5	-	400	-	400	ns
		10	-	190	-	-	
$\overline{\text{Read}}$ Pulse Width	t_{RD}	5	270	-	270	-	
		10	160	-	-	-	
Data Access from $\overline{\text{Read}}$	t_{DR}	5	-	375	-	375	
		10	-	170	-	-	
Address Hold after $\overline{\text{Read}}$	t_{RH}	5	0	-	0	-	
		10	0	-	-	-	
Output Hold after $\overline{\text{Read}}$	t_{DH}	5	50	230	50	230	
		10	40	130	-	-	
Chip Select Setup to TPA	t_{CS}	5	50	-	50	-	
		10	30	-	-	-	

NOTE:

1. Time required by a limit device to allow for the indicated function.

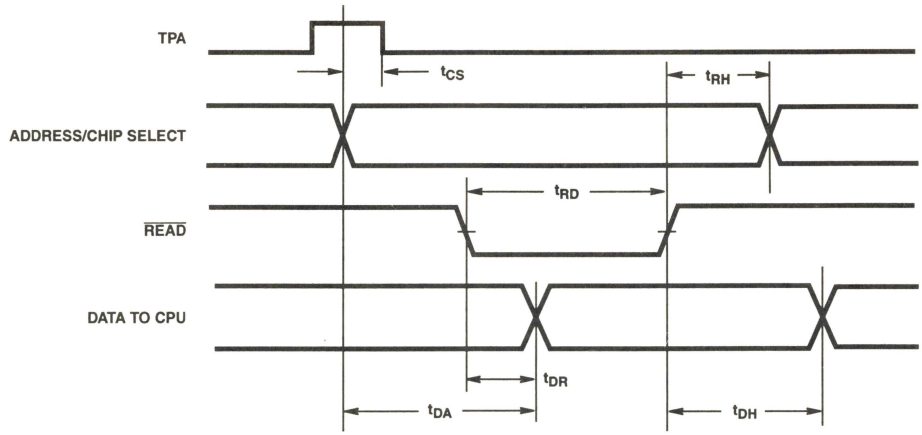


FIGURE 17. READ CYCLE TIMING WAVEFORMS

Dynamic Electrical Specifications at T_A -40°C to +85°C, Input t_R, t_F = 10ns, C_L = 50 pF

PARAMETER		V_{DD} (V)	LIMITS CDP1879 (NOTE 1) MIN	CDP1879 MAX	CDP1879C-1 (NOTE 1) MIN	CDP1879C-1 MAX	UNITS
Write Cycle Times (See Figure 18)							
Address Setup to $\overline{\text{Write}}$	t_{AS}	5	225	-	225	-	ns
		10	110	-	-	-	
$\overline{\text{Write}}$ Pulse Width	t_{WR}	5	150	-	150	-	
		10	70	-	-	-	
Data Setup to $\overline{\text{Write}}$	t_{DS}	5	65	-	65	-	
		10	30	-	-	-	
Address Hold after $\overline{\text{Write}}$	t_{AH}	5	0	-	0	-	
		10	0	-	-	-	
Data Hold after $\overline{\text{Write}}$	t_{WH}	5	150	-	150	-	
		10	80	-	-	-	
Chip Select Setup to TPA	t_{CS}	5	50	-	50	-	
		10	30	-	-	-	

NOTE:

1. Time required by a limit device to allow for the indicated function.

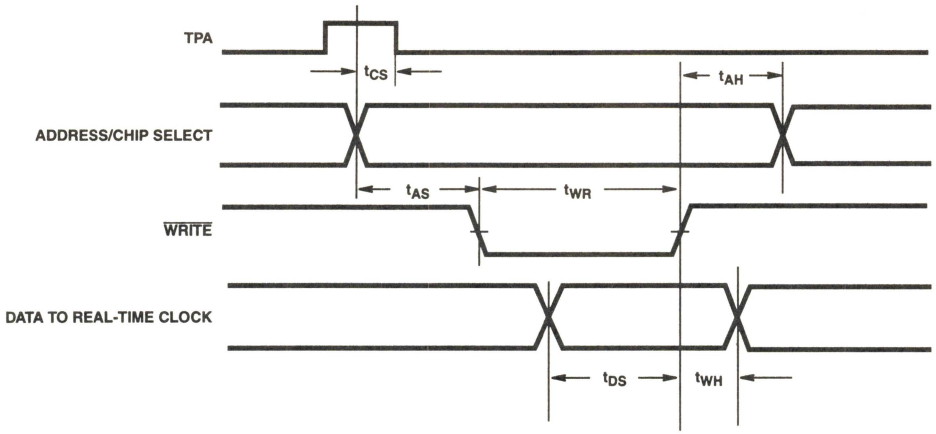


FIGURE 18. WRITE CYCLE TIMING WAVEFORM

HARRIS SEMICONDUCTOR

CDP1881C, CDP1882, CDP1882C

CMOS 6-Bit Latch and Decoder Memory Interfaces

March 1997

Features

- Performs Memory Address Latch and Decoder Functions Multiplexed or Non-Multiplexed
- Decodes Up to 16K Bytes of Memory
- Interfaces Directly with CDP1800-Series Microprocessors at Maximum Clock Frequency
- Can Replace CDP1866 and CDP1867 (Upward Speed and Function Capability)

Ordering Information

PACKAGE	5V	10V	TEMP. RANGE (°C)	PKG. NO.
PDIP	CDP1881CE	-	-40 to +85	E20.3
PDIP	CDP1882CE	-	-40 to +85	E18.3
PDIP Burn-In	CDP1882CEX	-	-40 to +85	E18.3
SBDIP	-	CDP1882D	-40 to +85	D18.3

Description

The CDP1881C, CDP1882 and CDP1882C are CMOS 6-bit memory latch and decoder circuits intended for use in CDP1800 series microprocessor systems. They can interface directly with the multiplexed address bus of this system at maximum clock frequency, and up to four 4K x 8-bit memories to provide a 16K byte memory system. With four 2K x 8-bit memories an 8K byte system can be decoded.

The devices are also compatible with non-multiplexed address bus microprocessors. By connecting the clock input to V_{DD}, the latches are in the data-following mode and the decoded outputs can be used in general purpose memory-system applications.

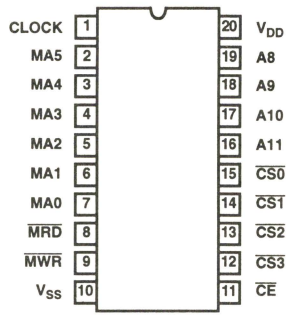
The CDP1881C, CDP1882 and CDP1882C are intended for use with 2K or 4K byte RAMs and are identical except that in the CDP1882 $\overline{MWR}$ and $\overline{MRD}$ are excluded.

The CDP1882 is functionally identical to the CDP1882C. It differs in that the CDP1882 has recommended operating voltage range of 4V to 10.5V and the C version has a recommended operating voltage range of 4V to 6.5V.

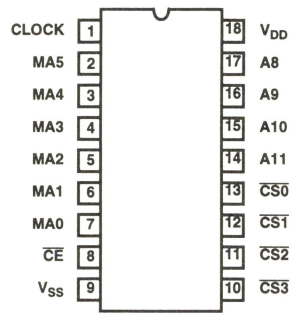
The CDP1881C, CDP1882 and CDP1882C are supplied in 20 lead and 18 lead packages, respectively. The CDP1881C is supplied only in a dual-in-line plastic package (E suffix). The CDP1882 is supplied in dual-in-line, hermetic side-brazed ceramic (D suffix) and in plastic (E suffix) packages.

Pinouts

CDP1881C
(PDIP)
TOP VIEW



CDP1882, CDP1882C
(PDIP, CERDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1367.2**

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1882 . . . . . -0.5V to +11V
CDP1881C and CDP1882C. . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
18 Lead PDIP	85	N/A
20 Lead PDIP	80	N/A
SBDIP Package	85	22

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type D. . . . . -55°C to +125°C
Package Type E. . . . . -40°C to +85°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ±1/32 In. (1.59 ± 0.79mm)
from case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	CDP1882		CDP1881C, CDP1882C		UNITS
	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Static Electrical Specifications

At T_A = -40°C to +85°C, V_{DD} ± 5%, Except as Noted:

PARAMETER	SYMBOL	CONDITIONS			CDP1882			CDP1881C, CDP1882C			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	1	10	-	5	50	µA
		-	0, 10	10	-	10	100	-	-	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	-	1.6	3.2	-	mA
		0.5	0, 10	10	3.2	6.4	-	-	-	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	-	-1.15	-2.3	-	mA
		9.5	0, 10	10	-2.3	-4.6	-	-	-	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High-Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		1, 9	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 9.5	-	5	3.5	-	-	3.5	-	-	V
		1, 9	-	10	7	-	-	-	-	-	V

Static Electrical Specifications At T_A = -40°C to +85°C, V_{DD} ± 5%, Except as Noted: **(Continued)**

PARAMETER	SYMBOL	CONDITIONS			CDP1882			CDP1881C, CDP1882C			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	-	±1	-	-	±1	µA
			0, 10	10	-	-	±2	-	-	-	µA
Operating Current (Note 2)	I_{DD1}	0, 5	0, 5	5	-	-	2	-	-	2	mA
		0, 10	0, 10	10	-	-	4	-	-	-	mA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF
Minimum Data Retention Voltage	V_{DR}	$V_{DD} = V_{DR}$			-	2	2.4	-	2	2.4	V
Data Retention Current	I_{DR}	V_{DD} = 2.4V			-	0.01	1	-	0.5	5	µA

NOTES:

1. Typical values are for T_A = +25°C.
2. $I_{OL} = I_{OH}$ = 1µA.
3. Operating current measured at 200kHz for V_{DD} = 5V and 400kHz for V_{DD} = 10V, with outputs open circuits (equivalent to typical CDP1800 system at 3.2MHz, 5V; and 6.4MHz, 10V).

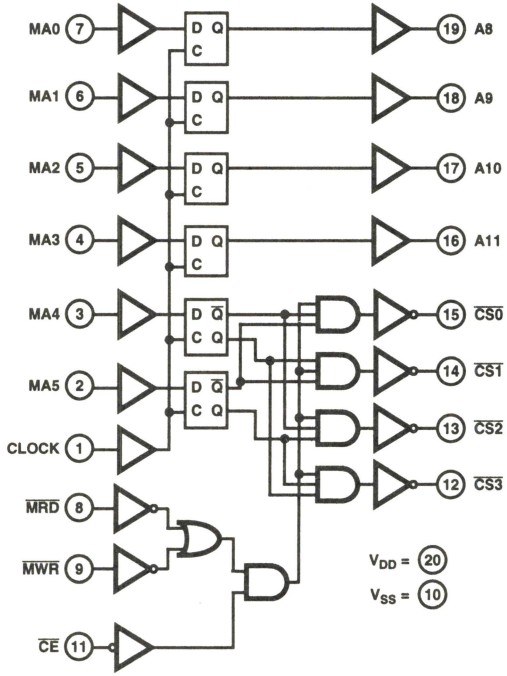


FIGURE 1. FUNCTIONAL DIAGRAM FOR THE CDP1881C

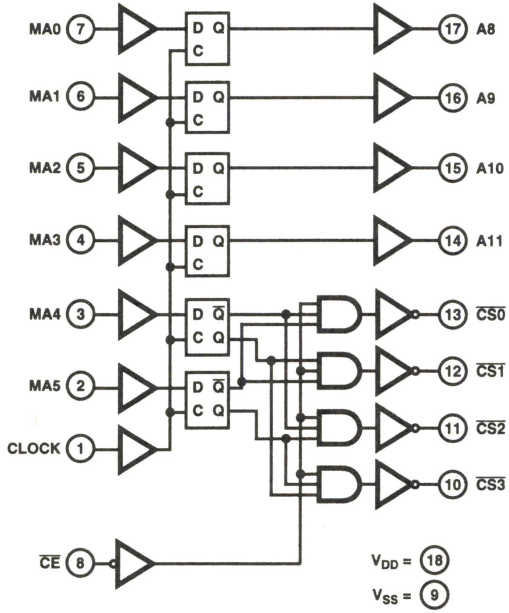


FIGURE 2. FUNCTIONAL DIAGRAM FOR THE CDP1882, CDP1882C

TRUTH TABLE

INPUTS						OUTPUTS			
(NOTE 1) $\overline{MWR}$	(NOTE 1) $\overline{MRD}$	$\overline{CE}$	CLK	MA4	MA5	$\overline{CS0}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
1	1	X	X	X	X	1	1	1	1
X	X	1	X	X	X	1	1	1	1
0	X	0	1	0	0	0	1	1	1
0	X	0	1	1	0	1	0	1	1
0	X	0	1	0	1	1	1	0	1
0	X	0	1	1	1	1	1	1	0
0	X	0	0	X	X	Previous State			
X	0	0	1	0	0	0	1	1	1
X	0	0	1	1	0	1	0	1	1
X	0	0	1	0	1	1	1	0	1
X	0	0	1	1	1	1	1	1	0
X	0	0	0	X	X	Previous State			

NOTE:

1. CDP1881C Only

INPUTS			OUTPUTS
$\overline{CE}$	CLK	MA0, MA1, MA2, MA3	A8, A9, A10, A11
X	1	1	1
X	1	0	0
X	0	X	Previous State

Logic 1 = High, Logic 0 = Low, X = Don't Care

Dynamic Electrical Specifications at T_A = -40°C to +85°C, $V_{DD} \pm 5\%$, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, (See Figure 1)

PARAMETER		V_{DD} (V)	CDP1882			CDP1881C, CDP1882C			UNITS
			MIN	(NOTE 1) TYP	(NOTE 2) MAX	MIN	(NOTE 1) TYP	(NOTE 2) MAX	
Minimum Setup Time	t_{MACL}	5	-	10	35	-	10	35	ns
Memory Address to CLOCK		10	-	8	25	-	-	-	ns
Minimum Hold Time	t_{CLMA}	5	-	8	25	-	8	25	ns
Memory Address After CLOCK		10	-	8	25	-	-	-	ns
Minimum CLOCK Pulse Width	t_{CLCL}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns

Dynamic Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ± 5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, (See Figure 1) **(Continued)**

PARAMETER		V_{DD} (V)	CDP1882 MIN	CDP1882 (NOTE 1) TYP	CDP1882 (NOTE 2) MAX	CDP1881C, CDP1882C MIN	CDP1881C, CDP1882C (NOTE 1) TYP	CDP1881C, CDP1882C (NOTE 2) MAX	UNITS
PROPAGATION DELAY TIMES									
$\overline{\text{Chip Enable}}$ to $\overline{\text{Chip Select}}$	t_{CECS}	5	-	75	150	-	75	150	ns
		10	-	45	100	-	-	-	ns
$\overline{\text{MRD}}$ or $\overline{\text{MRW}}$ to $\overline{\text{Chip Select}}$ (Note 3)	t_{MCS}	5	-	75	150	-	75	150	ns
		10	-	40	100	-	-	-	ns
CLOCK to $\overline{\text{Chip Select}}$	t_{CLCS}	5	-	100	175	-	100	175	ns
		10	-	65	125	-	-	-	ns
CLOCK to Address	t_{CLA}	5	-	100	175	-	100	175	ns
		10	-	65	125	-	-	-	ns
Memory Address to $\overline{\text{Chip Select}}$	t_{MACS}	5	-	100	175	-	100	175	ns
		10	-	75	125	-	-	-	ns
Memory Address to Address	t_{MAA}	5	-	80	125	-	80	125	ns
		10	-	40	60	-	-	-	ns

NOTES:

1. Typical values are for T_A = 25°C.
2. Maximum limits of minimum characteristics are the values above which all devices function.
3. For CDP1881C type only.

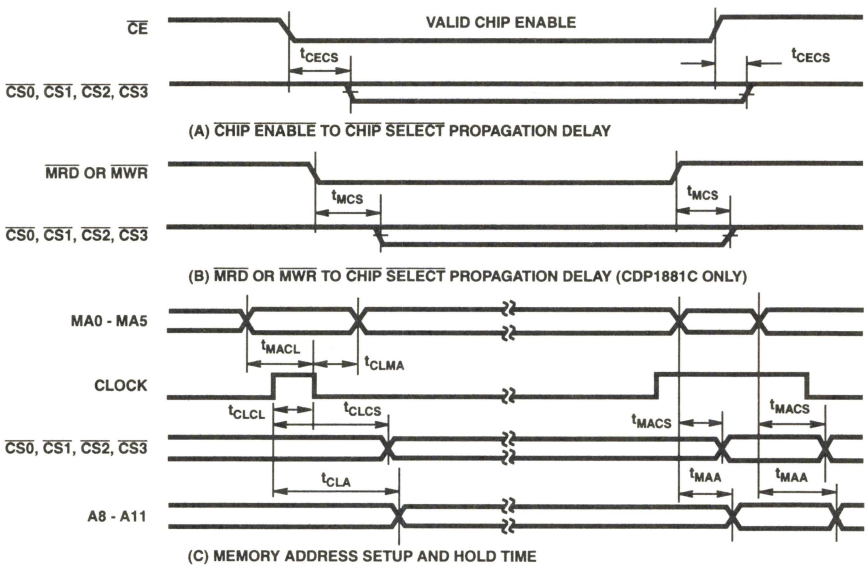


FIGURE 3. TIMING WAVEFORMS

Signal Descriptions/Pin Functions

CLOCK: Latch-Input Control - a high at the clock input will allow data to pass through the latch to the output pin. Data is latched on the high to low transition of the clock input. This input is connected to TPA in CDP1800-series systems.

MA0 - MA3: Address inputs to the high-byte address latches.

MA4 - MA5: High byte address inputs decoded to produce chip selects $\overline{CS0}$ - $\overline{CS3}$.

MRD, MWR: MEMORY READ ($\overline{MRD}$) and MEMORY WRITE ($\overline{MWR}$) signal inputs on the CDP1881C. A low at either input, when the $\overline{CE}$ pin is low, will enable the decoder chip select outputs ($\overline{CS0}$ - $\overline{CS3}$).

CE: CHIP ENABLE input - a low at the $\overline{CE}$ input of CDP1882, CDP1882C will enable the chip select decoder. A low at the $\overline{CE}$ input of CDP1881C, coincident with a low at either $\overline{MRD}$ or $\overline{MRW}$ pin, will enable the chip select decoder. A high on this pin forces $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, and $\overline{CS3}$ to a high (false) state.

A8 - A11: Latched high-byte address outputs.

CS0 - CS3: One of four latched and decoded Chip Select outputs.

V_{DD}, V_{SS}: Power and ground pins, respectively.

Application Information

The CDP1881C, CDP1882, CDP1882C can interface directly with the multiplexed address bus of the CDP1800-series microprocessor family at maximum clock frequency. A single CDP1881C or CDP1882 is capable of decoding up to 16K-bytes of memory.

The CDP1881C is provided with $\overline{MRD}$ and $\overline{MWR}$ inputs for controlling bus contention, and is especially useful for interfacing with RAMs that do not have an output enable function ($\overline{OE}$). Figure 4 shows the CDP1881C in a minimum system configuration which includes the CDP1833 ROM (1K x 8) and two 2K x 8 RAMS. The CDP1881C in this example performs the following functions:

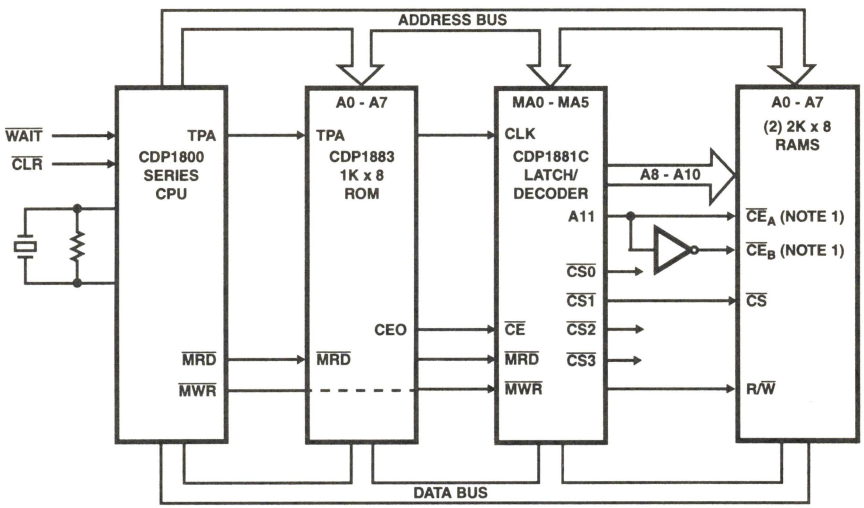
1) Latch and decode high-order address bits for use as chip selects.

2) Gate chip selects with $\overline{MRD}$ and $\overline{MWR}$ to prevent bus contention with the CPU.

3) Latch high-order address bits A8 to A11.

A system using the CDP1882 is shown in Figure 5. The CDP1882 performs the memory address latch and decoder functions. Note that the RAM has an output enable ($\overline{OE}$) pin which eliminates the need for $\overline{MRD}$ and $\overline{MWR}$ inputs on the latch/decoder. Instead, the $\overline{MRD}$ line is connected directly to the RAM output enable ($\overline{OE}$) pin.

In Figure 6 the CDP1882 is used to decode a 16K-byte ROM system consisting of four CDM5332s.



NOTE: $\overline{CE}_A$ = $\overline{CE}$ RAM NUMBER 1
$\overline{CE}_B$ = $\overline{CE}$ RAM NUMBER 2

FIGURE 4. MINIMUM 1800-SERIES USING THE CDP1881C

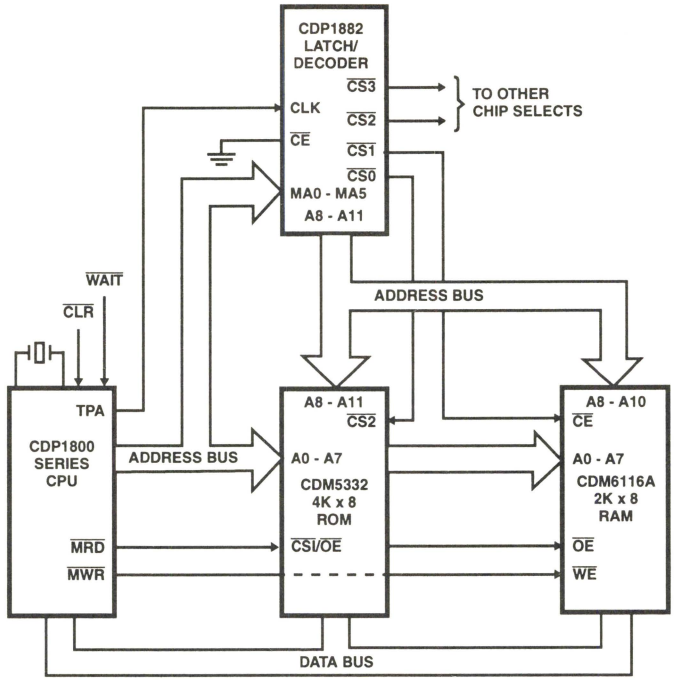


FIGURE 5. CDP1800-SERIES SYSTEM USING THE CDP1882

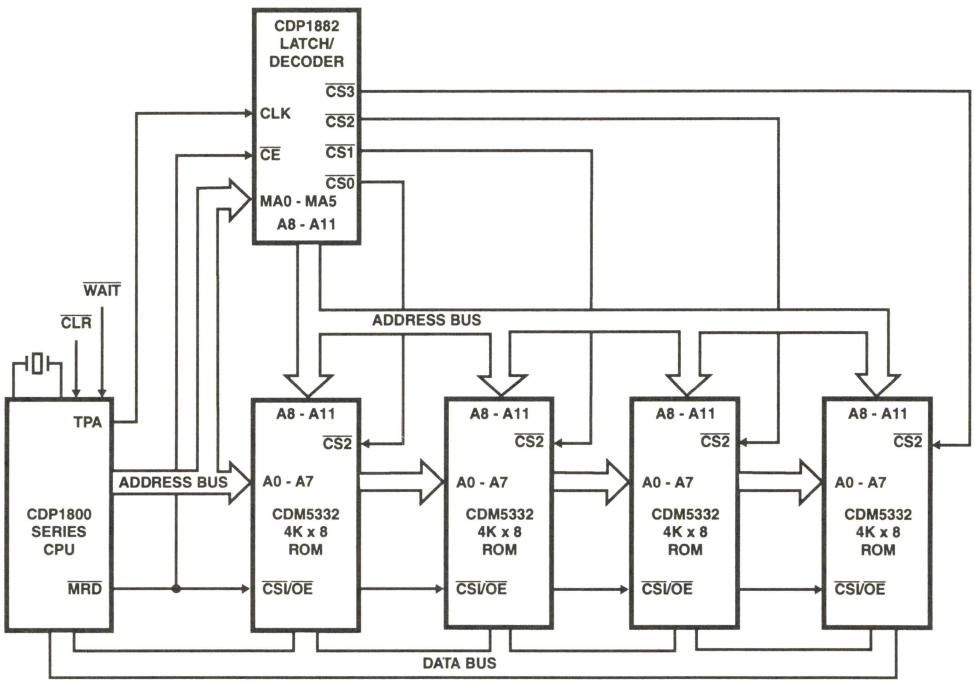


FIGURE 6. 6K-BYTE ROM SYSTEMS USING THE CDP1882

HARRIS SEMICONDUCTOR

CDP1883, CDP1883C

CMOS 7-Bit Latch and Decoder Memory Interfaces

March 1997

Features

- **Performs Memory Address Latch and Decoder Functions Multiplexed or Non-Multiplexed**
- **Interfaces Directly with the CDP1800-Series Microprocessors**
- **Allows Decoding for Systems Up to 32K Bytes**

Ordering Information

5V	10V	TEMP. RANGE	PACKAGE	PKG. NO.
CDP1883CE	CDP1883E	-40°C to +85°C	PDIP	E20.3

Description

The CDP1883 is a CMOS 7-bit memory latch and decoder circuit intended for use in CDP1800-series microprocessor systems. It can serve as a direct interface between the multiplexed address bus of this system and up to four 8K x 8-bit memories to implement a 32K-byte memory system. With four 4K x 8-bit memories, a 16K-byte system can be decoded.

The device is also compatible with non-multiplexed address bus microprocessors. By connecting the clock input to V_{DD}, the latches are in the data-following mode and the decoded outputs can be used in general-purpose memory-system applications.

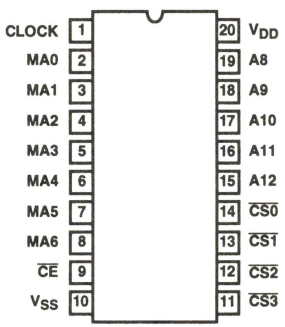
The CDP1833 is compatible with CDP1800-series microprocessors operating at maximum clock frequency.

The CDP1883 and CDP1883C are functionally identical. They differ in that the CDP1883 has a recommended operating voltage range of 4V to 10.5V and the C version has a recommended operating voltage range of 4V to 6.5V.

The CDP1883 and CDP1883C are supplied in 20 lead dual-in-line plastic packages (E Suffix).

Pinout

CDP1883, CDP1883C
(PDIP)
TOP VIEW



4 CMOS PERIPHERALS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

File Number **1507.2**

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1883 . . . . . -0.5V to +11V
CDP1883C. . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W)
PDIP Package 80
Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range 100mW
Operating Temperature Range (T_A)
Package Type E. . . . . -40°C to +85°C
Storage Temperature Range (T_{STG}). . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ±1/32 In. (1.59 ± 0.79mm)
from case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	SYMBOL	CDP1883		CDP1883C		UNITS
		MIN	MAX	MIN	MAX	
DC Operating Voltage Range		4	10.5	4	6.5	V
Input Voltage Range		V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Static Electrical Specifications

At T_A = -40°C to +85°C, V_{DD} ± 5%, Except as Noted:

PARAMETER	SYMBOL	CONDITIONS			CDP1883			CDP1883C			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	1	10	-	5	50	µA
		-	0, 10	10	-	10	100	-	-	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	-	1.6	3.2	-	mA
		0.5	0, 10	10	3.2	6.4	-	-	-	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	-	-1.15	-2.3	-	mA
		9.5	0, 10	10	-2.3	-4.6	-	-	-	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High-Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 9.5	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	-	±1	-	-	±1	µA
			0, 10	10	-	-	±2	-	-	-	µA
Operating Current (Note 3)	I_{DD1}	0, 5	0, 5	5	-	-	2	-	-	2	mA
		0, 10	0, 10	10	-	-	4	-	-	-	mA

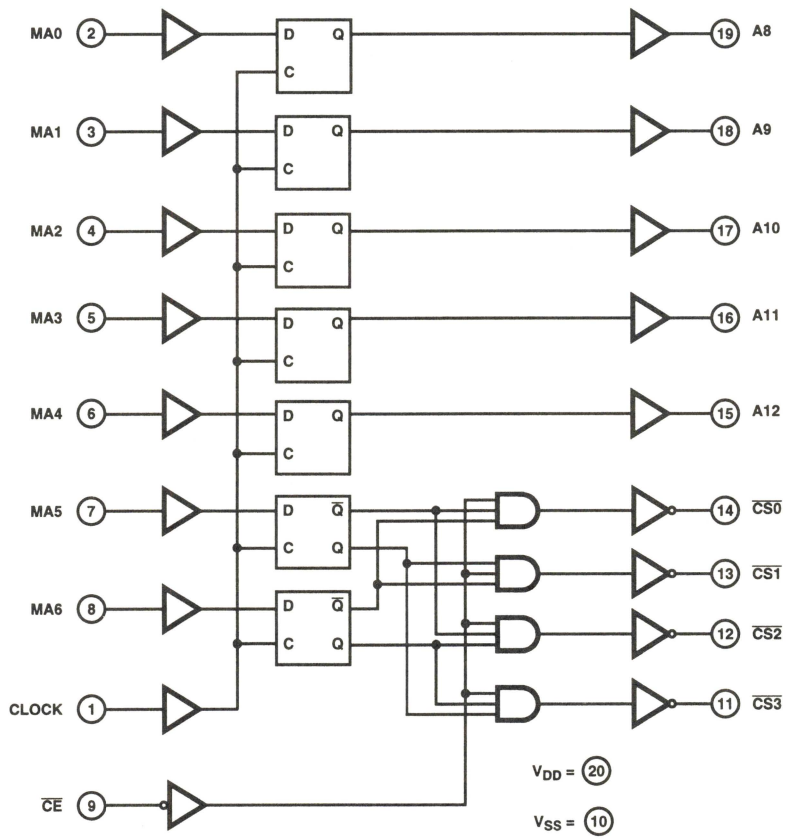
Static Electrical Specifications At T_A = -40°C to +85°C, V_{DD} ± 5%, Except as Noted: **(Continued)**

PARAMETER	SYMBOL	CONDITIONS			CDP1883			CDP1883C			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Minimum Data Retention Voltage	V_{DR}	$V_{DD} = V_{DR}$			-	2	2.4	-	2	2.4	V
Data Retention Current	I_{DR}	V_{DD} = 2.4V			-	0.01	1	-	0.5	5	µA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = +25°C.
2. $I_{OL} = I_{OH}$ = µA
3. Operating current measured at 200kHz for V_{DD} = 5V and 400kHz for V_{DD} = 10V, with outputs open circuit.

Functional Diagram



Signal Descriptions/Pin Functions

CLOCK: Latch Input Control - a high on the clock input will allow data to pass through the latch to the output pin. Data is latched on the high-to-low transition of the clock input. This pin is connected to TPA in CDP1800-series systems and tied to V_{DD} for other applications.

MA0 - MA4: Address inputs to the high-byte address latches.

MA5 - MA6: High byte address inputs decoded to produce chip selects $\overline{CS0}$ - $\overline{CS3}$.

$\overline{CE}$: CHIP ENABLE input - A low on this pin will enable the chip select decoder. A high on this pin forces $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, and $\overline{CS3}$ outputs to a high (false) state.

A8 - A12: Latched high-byte address outputs.

$\overline{CS0}$ - $\overline{CS3}$: One of four latched and decoded Chip Select outputs.

V_{DD}, V_{SS}: Power and ground pins, respectively.

TRUTH TABLE

INPUTS				OUTPUTS			
$\overline{CE}$	CLK	MA5	MA6	$\overline{CS0}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
0	1	0	0	0	1	1	1
0	1	1	0	1	0	1	1
0	1	0	1	1	1	0	1
0	1	1	1	1	1	1	0
0	0	X	X	Previous State			
1	X	X	X	1	1	1	1

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{CE}$	CLK	MA0 - 4	A8 - A12
X	1	1	1
X	1	0	0
X	0	X	Previous State

X = Don't Care

Application Information

The CDP1883 and CDP1883C can be interfaced, without external components, with CDP1800-series microprocessor systems. These microprocessors feature a multiplexed address bus and provide an address latch signal (TPA) that is used as the clock input of the CDP1883. See Figure 2 and Figure 3.

This signal is used to latch 7 bits of the high-order address. The lower five high-order address inputs are latched and held to be used with the eight lower-order address inputs to access an 8K x 8-bit memory. The two upper high-order address inputs are latched and decoded for use as chip selects.

The latched address and decoding functions of the CDP1883 and CDP1883C allow them to operate with 32K-byte memory systems. In addition, smaller memory systems can be configured with 4K x 8-bit or smaller memories, or a mix of memory sizes up to 8K x 8-bit.

Dynamic Electrical Specifications $T_A = -40^oC$ to $+85^oC$, $V_{DD} \pm 5\%$, t_R, $t_F = 20ns$, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100pF$. See Figure 1

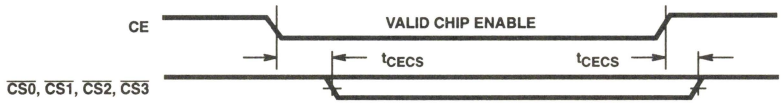
PARAMETER		V_{DD} (V)	CDP1883 MIN	CDP1883 (NOTE 1) TYP	CDP1883 (NOTE 2) MAX	CDP1883C MIN	CDP1883C (NOTE 1) TYP	CDP1883C (NOTE 2) MAX	UNITS
Minimum Setup Time, Memory Address to CLOCK	t_{MACL}	5	-	10	35	-	10	35	ns
		10	-	8	25	-	-	-	ns
Minimum Hold Time, Memory Address After CLOCK	t_{CLMA}	5	-	8	25	-	8	25	ns
		10	-	8	25	-	-	-	ns
Minimum CLOCK Pulse Width	t_{CLCL}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
PROPAGATION DELAY TIMES									
$\overline{Chip\ Enable}$ to $\overline{Chip\ Select}$	t_{CECS}	5	-	75	150	-	75	150	ns
		10	-	45	100	-	-	-	ns
CLOCK to $\overline{Chip\ Select}$	t_{CLCS}	5	-	100	175	-	100	175	ns
		10	-	65	125	-	-	-	ns

Dynamic Electrical Specifications $T_A = -40^oC$ to $+85^oC$, $V_{DD} \pm 5\%$, t_R, $t_F = 20ns$, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100pF$. See Figure 1 **(Continued)**

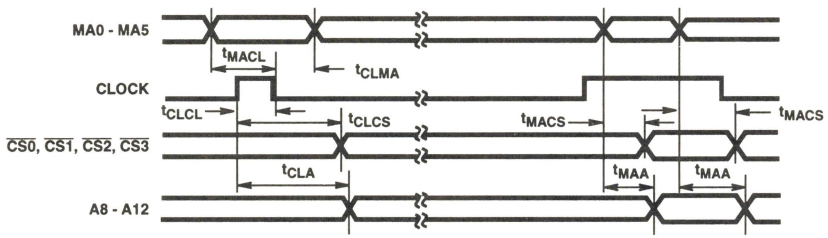
PARAMETER		V_{DD} (V)	CDP1883 MIN	CDP1883 (NOTE 1) TYP	CDP1883 (NOTE 2) MAX	CDP1883C MIN	CDP1883C (NOTE 1) TYP	CDP1883C (NOTE 2) MAX	UNITS
CLOCK to Address	t_{CLA}	5	-	100	175	-	100	175	ns
		10	-	65	125	-	-	-	ns
Memory Address to $\overline{\text{Chip Select}}$	t_{MACS}	5	-	100	175	-	100	175	ns
		10	-	75	125	-	-	-	ns
Memory Address to Address	t_{MAA}	5	-	80	125	-	80	125	ns
		10	-	40	60	-	-	-	ns

NOTES:

1. Typical values are for $T_A = 25^oC$.
2. Maximum limits of minimum characteristics are the values above which all devices function.



(A) $\overline{\text{CHIP ENABLE}}$ TO $\overline{\text{CHIP SELECT}}$ PROPAGATION DELAY



(B) MEMORY ADDRESS SETUP AND HOLD TIME

FIGURE 1. CDP1883 TIMING WAVEFORMS

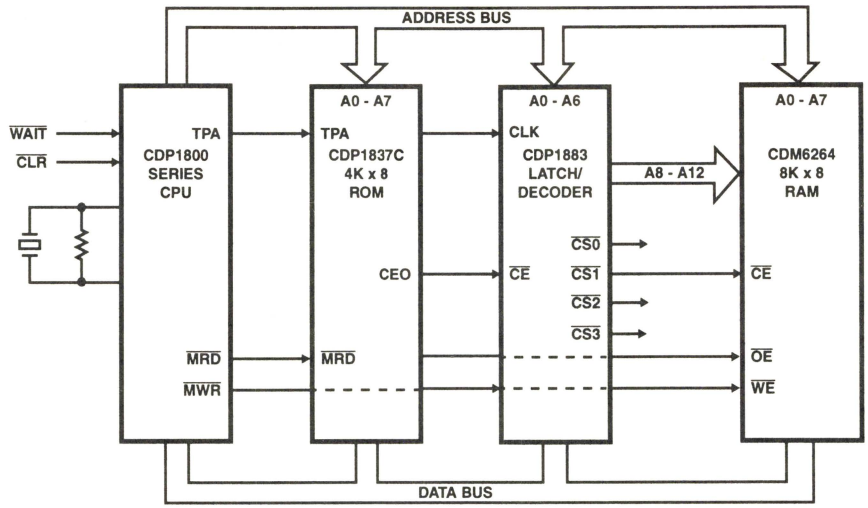


FIGURE 2. MINIMUM CDP1800-SYSTEM USING THE CDP1883 INTERFACE WITH AN 8K X 8-BIT MEMORY

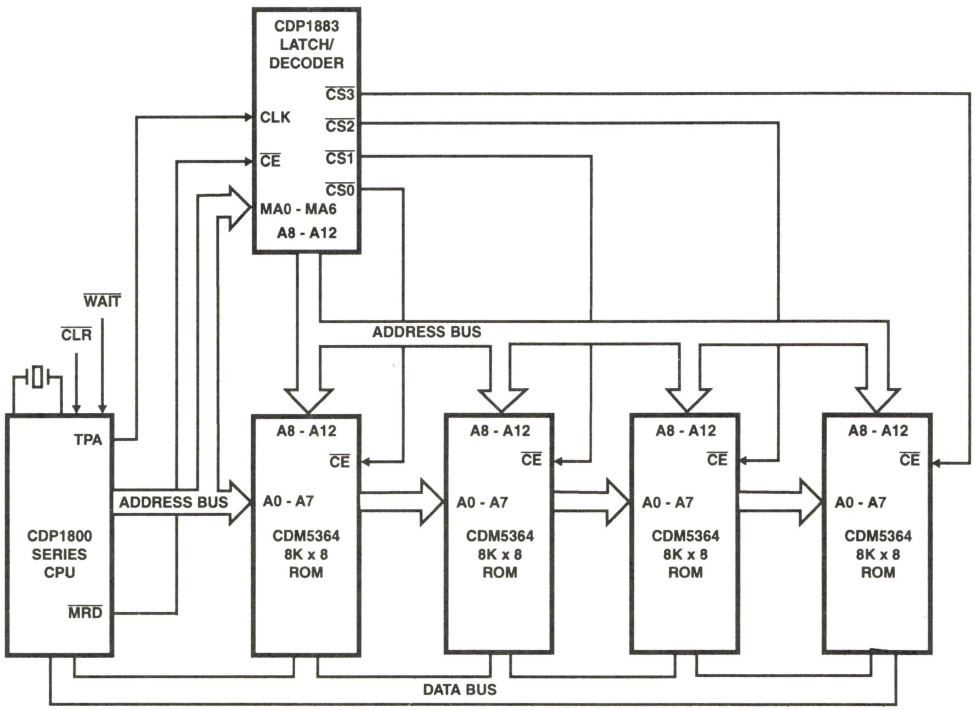


FIGURE 3. 32K-BYTE ROM SYSTEM USING THE CDP1883

ICM7170

April 1997

µP-Compatible, Real-Time Clock

Features

- 8-Bit, µP Bus Compatible
  - Multiplexed or Direct Addressing
- Regulated Oscillator Supply Ensures Frequency Stability and Low Power
- Time From 1/100 Seconds to 99 Years
- Software Selectable 12/24 Hour Format
- Latched Time Data Ensures No Roll Over During Read
- Full Calendar with Automatic Leap Year Correction
- On-Chip Battery Backup Switchover Circuit
- Access Time Less than 300ns
- 4 Programmable Crystal Oscillator Frequencies Over Industrial Temperature Range
- 3 Programmable Crystal Oscillator Frequencies Over Military Temperature Range
- On-Chip Alarm Comparator and RAM
- Interrupts from Alarm and 6 Selectable Periodic Intervals
- Standby Micro-Power Operation: 1.2µA Typical at 3.0V and 32kHz Crystal

Applications

- Portable and Personal Computers
- Data Logging
- Industrial Control Systems
- Point Of Sale

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
ICM7170IPG	-40 to 85	24 Ld PDIP	E24.6
ICM7170IDG	-40 to 85	24 Ld SBDIP	D24.6
ICM7170IBG	-40 to 85	24 Ld SOIC	M24.3
ICM7170MDG	-55 to 125	24 Ld SBDIP	D24.6
ICM7170AIPG	-40 to 85	24 Ld PDIP	E24.6
ICM7170AIDG	-40 to 85	24 Ld SBDIP	D24.6
ICM7170AIBG	-40 to 85	24 Ld SOIC	M24.3
ICM7170AMDG	-55 to 125	24 Ld SBDIP	D24.6

NOTE: "A" Parts Screened to <5µA I_{STBY} at 32kHz.

Description

The ICM7170 real time clock is a microprocessor bus compatible peripheral, fabricated using Harris' silicon gate CMOS LSI process. An 8-bit bidirectional bus is used for the data I/O circuitry. The clock is set or read by accessing the 8 internal separately addressable and programmable counters from $^{1}/_{100}$ seconds to years. The counters are controlled by a pulse train divided down from a crystal oscillator circuit, and the frequency of the crystal is selectable with the on-chip command register. An extremely stable oscillator frequency is achieved through the use of an on-chip regulated power supply.

The device access time (t_{ACC}) of 300ns eliminates the need for wait states or software overhead with most microprocessors. Furthermore, an ALE (Address Latch Enable) input is provided for interfacing to microprocessors with a multiplexed address/data bus. With these two special features, the ICM7170 can be easily interfaced to any available microprocessor.

The ICM7170 generates two types of interrupts, periodic and alarm. The periodic interrupt (100Hz, 10Hz, etc.) can be programmed by the internal interrupt control register to provide 6 different output signals. The alarm interrupt is set by loading an on-chip 51-bit RAM that activates an interrupt output through a comparator. The alarm interrupt occurs when the real time counter and alarm RAM time are equal. A status register is available to indicate the interrupt source.

An on-chip Power Down Detector eliminates the need for external components to support the battery back-up function. When a power down or power failure occurs, internal logic switches the on-chip counters to battery back-up operation. Read/write functions become disabled and operation is limited to time-keeping and interrupt generation, resulting in low power consumption.

Internal latches prevent clock roll-over during a read cycle. Counter data is latched on the chip by reading the 100th-seconds counter and is held indefinitely until the counter is read again, assuring a stable and reliable time value.

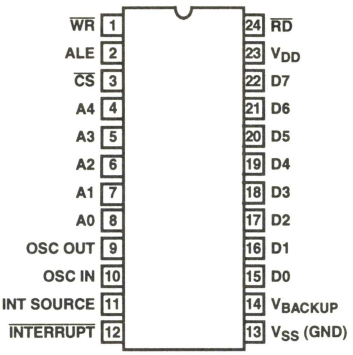
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Copyright © Harris Corporation 1997

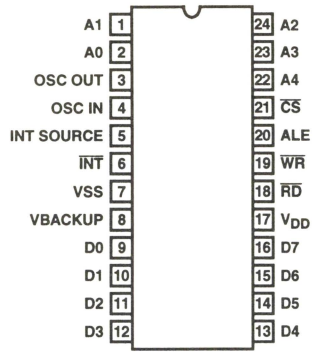
File Number **3019.2**

Pinouts

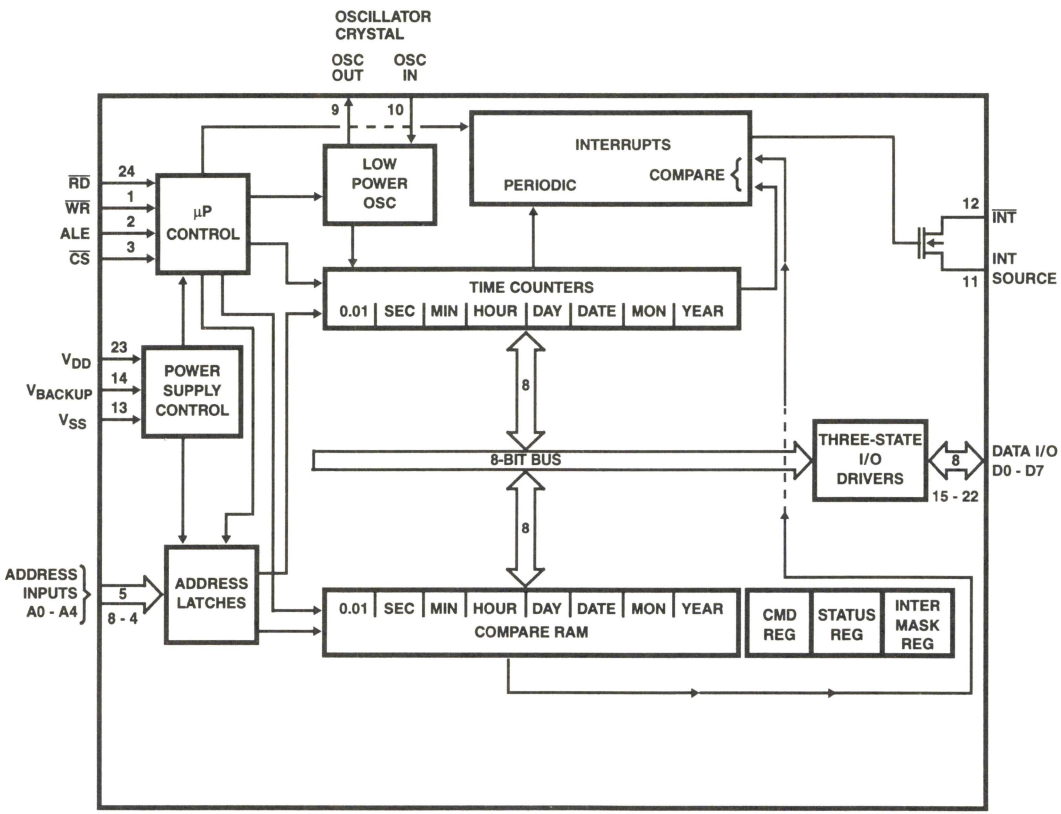
ICM7170
(PDIP, SBDIP)
TOP VIEW



ICM7170
(SOIC)
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Power Dissipation (Note 1) 500mW
Storage Temperature Range . . . . . -65°C to 150°C
Lead Temperature (Soldering 10s) . . . . . 300°C
Input Voltage (Any Terminal) (Note 2) . . . . V_{DD} +0.3V to V_{SS} -0.3V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	65	N/A
SBDIP Package	60	18
SOIC Package	75	N/A

Maximum Junction Temperature
Plastic Package . . . . . 150°C
SBDIP Package . . . . . 175°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

T_A = -40°C to 85°C, V_{DD} +5V ±10%, V_{BACKUP} V_{DD}, V_{SS} = 0V Unless Otherwise Specified
All I_{DD} specifications include all input and output leakages (ICM7170 and ICM7170A)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Supply Range, V_{DD}	F_{OSC} = 32kHz		1.9	-	5.5	V
	F_{OSC} = 1, 2, 4MHz		2.6	-	5.5	V
Standby Current, $I_{STBY(1)}$	F_{OSC} = 32kHz Pins 1 - 8,15 - 22 and 24 = V_{DD}	ICM7170	-	1.2	20.0	µA
	V_{DD} = V_{SS}; V_{BACKUP} = V_{DD} - 3.0V For ICM7170A See General Notes 5	ICM7170A	-	1.2	5.0	µA
Standby Current, I_{STBY}(2)	F_{OSC} = 4MHz Pins 1 - 8,15 - 22 and 24 = V_{DD} V_{DD} = V_{SS}; V_{BACKUP} = V_{DD} - 3.0V		-	20	150	µA
Operating Supply Current, $I_{DD(1)}$	F_{OSC} = 32kHz Read/Write Operation at 100Hz		-	0.3	1.2	mA
Operating Supply Current, $I_{DD(2)}$	F_{OSC} = 32kHz Read/Write Operation at 1MHz		-	1.0	2.0	mA
Input Low Voltage (Except Osc.), V_{IL}	V_{DD} = 5.0V		-	-	0.8	V
Input High Voltage (Except Osc.), V_{IH}	V_{DD} = 5.0V		2.4	-	-	V
Output Low Voltage (Except Osc.), V_{OL}	I_{OL} = 1.6mA		-	-	0.4	V
Output High Voltage Except $\overline{\text{INTERRUPT}}$ (Except Osc.), V_{OH}	I_{OH} = -400µA		2.4	-	-	V
Input Leakage Current, I_{IL}	V_{IN} = V_{DD} or V_{SS}		-10	0.5	+10	µA
Three-State Leakage Current (D0 - D7), I_{OL}(1)	V_O = V_{DD} or V_{SS}		-10	0.5	+10	µA
Backup Battery Voltage, $V_{BATTERY}$	F_{OSC} = 1, 2, 4MHz		2.6	-	V_{DD} - 1.3	V
Backup Battery Voltage, $V_{BATTERY}$	F_{OSC} = 32kHz		1.9	-	V_{DD} - 1.3	V
Leakage Current $\overline{\text{INTERRUPT}}$, I_{OL}(2)	V_O = V_{DD}	INT SOURCE Connected to V_{SS}	-	0.5	10	µA
Capacitance D0 - D7, $C_{I/O}$			-	8	-	pF
Capacitance A0 - A4, $C_{ADDRESS}$			-	6	-	pF

4 CMOS PERIPHERALS

AC Electrical Specifications

T_A = -40°C to 85°C, V_{DD} = +5V ± 10%, V_{BACKUP} = V_{DD}, D0 - D7 Load Capacitance = 150pF, V_{IL} = 0.4V, V_{IH} = 2.8V, Unless Otherwise Specified

PARAMETER	MIN	MAX	UNITS
READ CYCLE TIMING			
READ to DATA Valid, t_{RD}	-	250	ns
ADDRESS Valid to DATA Valid, t_{ACC}	-	300	ns
READ Cycle Time, t_{CYC}	400	-	ns
Read High Time, t_{RH}	150	-	ns
$\overline{RD}$ High to Bus Three-State, t_{RH}	-	25	ns
ADDRESS to READ Set Up Time, t_{AS}	50	-	ns
ADDRESS HOLD Time After READ, t_{AR}	0	-	ns
WRITE CYCLE TIMING			
ADDRESS Valid to WRITE Strobe, t_{AD}	50	-	ns
ADDRESS Hold Time for WRITE, t_{WA}	0	-	ns
WRITE Pulse Width, Low, t_{WL}	100	-	ns
WRITE High Time, t_{WH}	300	-	ns
DATA IN to WRITE Set Up Time, t_{DW}	100	-	ns
DATA IN Hold Time After WRITE, t_{WD}	30	-	ns
WRITE Cycle Time, t_{CYC}	400	-	ns
MULTIPLEXED MODE TIMING			
ALE Pulse Width, High, t_{LL}	50	-	ns
ADDRESS to ALE Set Up Time, t_{AL}	30	-	ns
ADDRESS Hold Time After ALE, t_{LA}	30	-	ns

NOTE:

1. T_A = 25°C.
2. Due to the SCR structure inherent in the CMOS process, connecting any terminal at voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7170 be turned on first.

Timing Diagrams

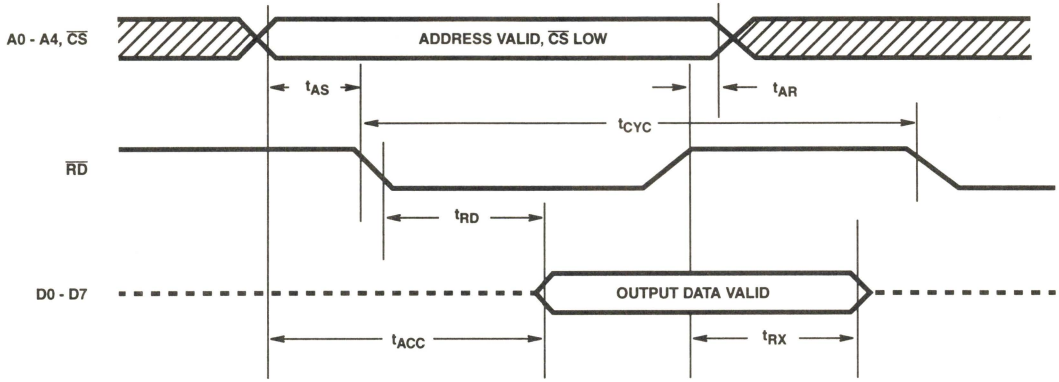


FIGURE 1. READ CYCLE TIMING FOR NON-MULTIPLEXED BUS (ALE = V_{IH}, $\overline{WR}$ = V_{IH}

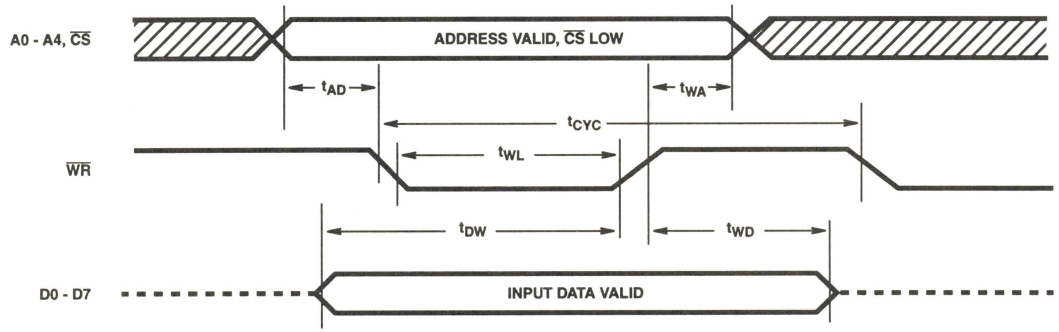


FIGURE 2. WRITE CYCLE TIMING FOR NON-MULTIPLEXED BUS (ALE = V_{IH}, $\overline{RD}$ = V_{IH})

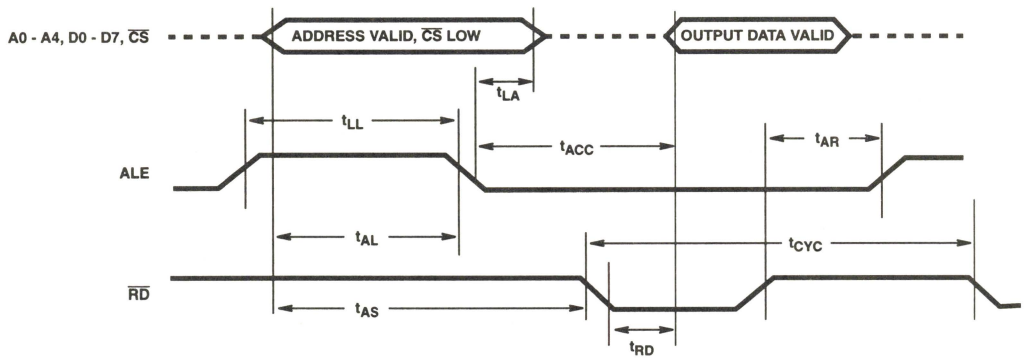


FIGURE 3. READ CYCLE TIMING FOR MULTIPLEXED BUS ($\overline{WR}$ = V_{IH})

Timing Diagrams (Continued)

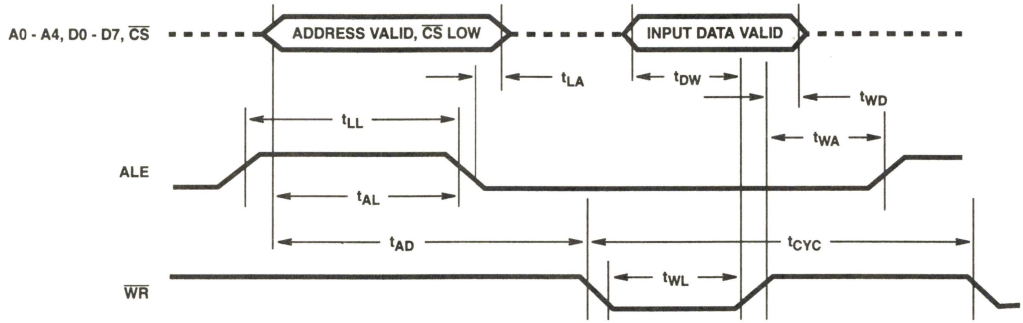


FIGURE 4. WRITE CYCLE TIMING FOR MULTIPLEXED BUS ($\overline{RD}$ = V_{IH})

Pin Descriptions

SIGNAL	PIN NUMBER	SOIC PIN NUMBER	DESCRIPTION
$\overline{WR}$	1	19	$\overline{Write}$ Input
ALE	2	20	Address Latch Enable Input
$\overline{CS}$	3	21	$\overline{Chip\ Select}$ Input
A4-A0	4 - 8	22 - 2	Address Inputs
OSC OUT	9	3	Oscillator Output
OSC IN	10	4	Oscillator Input
INT SOURCE	11	5	Interrupt Source
$\overline{INTERRUPT}$	12	6	$\overline{Interrupt}$ Output
V_{SS} (GND)	13	7	Digital Common
V_{BACKUP}	14	8	Battery Negative Side
D0 - D7	15 - 22	9 - 16	Data I/O
V_{DD}	23	17	Positive Digital Supply
$\overline{RD}$	24	18	$\overline{Read}$ Input

TABLE 1. COMMAND REGISTER FORMAT

COMMAND REGISTER ADDRESS (10001b, 11h) WRITE-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
n/a	n/a	Normal/Test Mode	Interrupt Enable	Run/Stop	12/24 Hour Format	Crystal Frequency	Crystal Frequency

TABLE 2. COMMAND REGISTER BIT ASSIGNMENTS

D5	TEST BIT	D4	INTERRUPT ENABLE	D3	RUN/STOP	D2	24/12 HOUR FORMAT	D1	D0	CRYSTAL FREQUENCY
0	Normal Mode	0	Interrupt disabled	0	Stop	0	12-Hour Mode	0	0	32.768kHz
1	Test Mode	1	Interrupt enable	1	Run	1	24-Hour Mode	0	1	1.048576MHZ
								1	0	2.097152MHz
								1	1	4.194304MHz

TABLE 3. ADDRESS CODES AND FUNCTIONS

ADDRESS						FUNCTION	DATA								VALUE
A4	A3	A2	AI	A0	HEX		D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	00	Counter-1/100 seconds	-								0 - 99
0	0	0	0	1	01	Counter-hours	-	-	-						0 - 23
						12 Hour Mode	†	-	-	-					1 - 12
0	0	0	1	0	02	Counter-minutes	-	-							0 - 59
0	0	0	1	1	03	Counter-seconds	-	-							0 - 59
0	0	1	0	0	04	Counter-month	-	-	-	-					1 - 12
0	0	1	0	1	05	Counter-date	-	-	-						1 - 31
0	0	1	1	0	06	Counter-year	-								0 - 99
0	0	1	1	1	07	Counter-day of week	-	-	-	-	-				0 - 6
0	1	0	0	0	08	RAM-1/100 seconds	M								0 - 99
0	1	0	0	1	09	RAM-hours	-	M	-						0 - 23
						12 Hour Mode	†	M	-	-					1 - 12
0	1	0	1	0	0A	RAM-minutes	M	-	.	.					0 - 59
0	1	0	1	1	0B	RAM-seconds	M	-	.	.					0 - 59
0	1	1	0	0	0C	RAM-month	M	-	-	-					1 - 12
0	1	1	0	1	0D	RAM-date	M	-	-						1 - 31
0	1	1	1	0	0E	RAM-year	M								0 - 99
0	1	1	1	1	0F	RAM-day of week	M	-	-	-	-				0 - 6
1	0	0	0	0	10	Interrupt Status and Mask Register	+								
1	0	0	0	1	11	Command register	-	-							

NOTES:

Addresses 10010 to 11111 (12h to 1Fh) are unused.
'+' Unused bit for interrupt Mask Register, MSB bit for interrupt Status Register.
'-' Indicates unused bits.
'†' AM/PM indicator bit in 12 hour format Logic "0" indicates AM, logic "1" indicates PM.
'M' Alarm compare for particular counter will be enabled if bit is set to logic "0".

TABLE 4. INTERRUPT AND STATUS REGISTERS FORMAT

INTERRUPT MASK REGISTER ADDRESS (10000b, 10h) WRITE-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
NOT USED	DAY	HOUR	MIN	SEC	1/10 SEC	1/100 SEC	ALARM
	← Periodic Interrupt Mask Bits →						Alarm/Compare Mask Bit
INTERRUPT STATUS REGISTER ADDRESS (10000b, 10h) READ-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
GLOBAL INTERRUPT	DAY	HOUR	MIN	SEC	1/10 SEC	1/100 SEC	ALARM
Periodic and Alarm Flags	← Periodic Interrupt Flags →						Alarm Compare Flag

Detailed Description

Oscillator

The ICM7170 has an onboard CMOS Pierce oscillator with an internally regulated voltage supply for maximum accuracy, stability, and low power consumption. It operates at any of four popular crystal frequencies: 32.768kHz, 1.046576MHz, 2.097152MHz, and 4.194304MHz (Note 1). The crystal should be designed for the parallel resonant mode of oscillation. In addition to the crystal, 2 or 3 load capacitors are required, depending on the circuit topology used.

The oscillator output is divided down to 4000Hz by one of four divider ratios, determined by the two frequency selection bits in the Command Register (D0 and D1 at address 11H). This 4000Hz is then divided down to 100Hz, which is used as the clock for the counters.

Time and calendar information is provided by 8 consecutive, programmable counters: 100ths of, seconds, minutes, hours, day of week, date, month, and year. The data is in binary format with 8 bits per digit. See Table 3 for address information. Any unused bits are held to a logic "0" during a read and ignored during a write operation.

NOTE:

1. 4.94304MHz is not available over military temperature range.

Alarm Compare RAM

On the chip are 51 bits of Alarm Compare RAM grouped into words of different lengths. These are used to store the time, ranging from 10ths of seconds to years, for comparison to the real-time counters. Each counter has a corresponding RAM word. In the Alarm Mode an interrupt is generated when the current time is equal to the alarm time. The RAM contents are compared to the counters on a word by word basis. If a comparison to a particular counter is unnecessary, then the appropriate 'M' bit in Compare RAM should be set to logic "1".

The 'M' bit, referring to Mask bit, causes a particular RAM word to be masked off or ignored during a compare. Table 3 shows addresses and Mask bit information.

Periodic Interrupts

The interrupt output can be programmed for 6 periodic signals: 100Hz, 10Hz, once per second, once per minute, once per hour, or once per day. The 100Hz and 10Hz interrupts have instantaneous errors of ±2.5% and ±0.15% respectively. This is because non-integer divider circuitry is used to generate these signals from the crystal frequency, which is a power of 2. The time average of these errors over a 1 second period, however, is zero. Consequently, the 100Hz or 10Hz interrupts are not suitable as an aid in tuning the oscillator; the 1 second interrupt must be used instead.

See General, Note 6.

The periodic interrupts can occur concurrently and in addition to alarm interrupts. The periodic interrupts are controlled by bits in the interrupt mask register, and are enabled by setting the appropriate bit to a "1" as shown in Table 4. Bits D1 through D6 in the mask register, in conjunction with bits D1 through D6 of the status register, control the generation of interrupts according to Figure 5.

The interrupt status register, when read, indicates the cause of the interrupt and resets itself on the rising edge of the RD signal. When any of the counters having a corresponding bit in the status register increments, that bit is set to a "1" regardless of whether the corresponding bit in the interrupt mask register is set or not.

Consequently, when the status register is read it will always indicate which counters have increments and if an alarm compare occurred, since the last time it was read. This requires some special software considerations. If a slow interrupt is enabled (i.e. hourly or daily), the program must always check the slowest interrupt that has been enabled first, because all the other lower order bits in the status register will be set to "1" as well.

Bit D7 is the global interrupt bit, and when set to a "1", indicates that the ICM7170 did indeed generate a hardware interrupt. This is useful when other interrupting devices in addition to the ICM7170 are attached to the system microprocessor, and all devices must be polled to determine which one generated the interrupt.

See General Notes, Note 6.

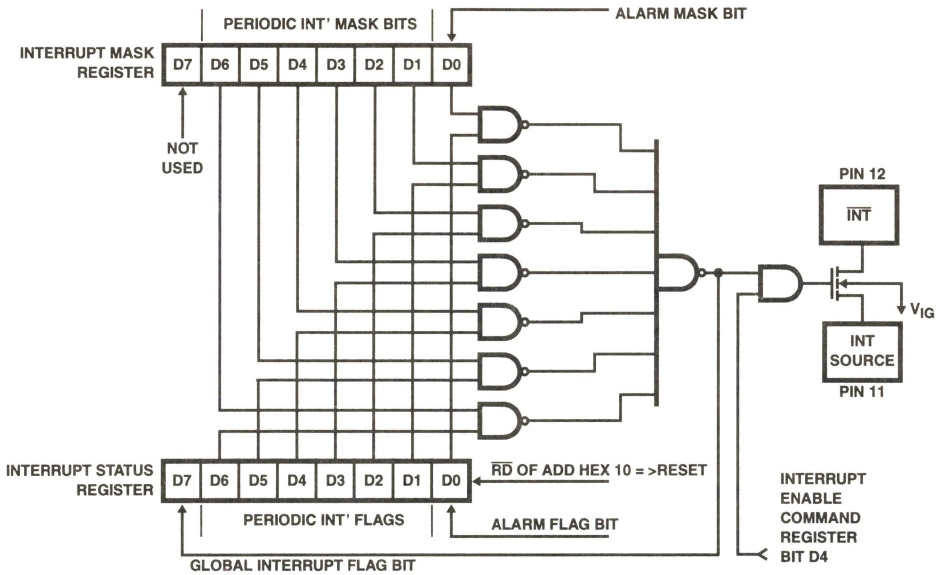


FIGURE 5. INTERRUPT OUTPUT CIRCUIT

Interrupt Operation

The Interrupt Output N-channel MOSFET (Figure 4) is enabled whenever both the Interrupt Enable bit (D4 of the Command Register) and a mask bit (D0 - D6 of the Interrupt Mask Register) are set. The transistor is turned ON when a flag bit is set that corresponds to one of the set mask bits. This also sets the Global Interrupt Flag Bit (D7 of the Interrupt Status Register). It is turned OFF when the Interrupt Status Register is read. An interrupt can occur in both the operational and standby modes of operation.

Since system power is usually applied between V_{DD} and V_{SS}, the user can connect the Interrupt Source (pin 11) to V_{SS}. This allows the Interrupt Output to turn on only while system powers applied and will not be pulled to V_{SS} during standby operation. If interrupts are required only during standby operation, then the interrupt source pin should be connected to the battery's negative side (V_{BACKUP}). In this configuration, for example, the interrupt could be used to turn on power for a cold boot.

Power Down Detector

The ICM7170 contains an on-chip power down detector that eliminates the need for external components to support the battery-backup switchover function, as shown in Figure 6. Whenever the voltage from the V_{SS} pin to the V_{BACKUP} pin is less than approximately 1.0V (the V_{TH} of the N-channel MOSFET), the data bus I/O buffers in the ICM7170 are automatically disabled and the chip cannot be read or written to. This prevents random data from the microprocessor being written to the clock registers as the power supply is going down.

Actual switchover to battery operation occurs when the voltage on the V_{BACKUP} pin is within ±50mV of V_{SS}. This switchover uncertainty is due to the offset voltage of the CMOS comparator that is used to sense the battery voltage. During battery backup, device operation is limited to timekeeping and interrupt generation only, thus achieving micro- power current drain. If an external battery-backup switch-over circuit is being used with the ICM7170, or if standby battery operation is not required, the V_{BACKUP} pin should be pulled up to V_{DD} through a 2K resistor.

Time Synchronization

Time synchronization is achieved through bit D3 of the Command Register, which is used to enable or disable the 100Hz clock from the counters. A logic "1" allows the counters to function and a logic "0" disables the counters. To accurately set the time, a logic "0" should be written into D3 and then the desired times entered into the appropriate counters. The clock is then started at the proper time by writing a logic "1" into D3 of the Command Register.

Latched Data

To prevent ambiguity while the processor is gathering data from the registers, the ICM7170 incorporates data latches and a transparent transition delay circuit.

By accessing the 100ths of seconds counter an internal store signal is generated and data from all the counters is transferred into a 36-bit latch. A transition delay circuit will delay a 100Hz transition during a READ cycle. The data stored by the latches is then available for further processing until the 100ths of seconds counter is read again. If a $\overline{RD}$ signal is wider than 0.01s, 100Hz counts will be ignored.

Control Lines

The $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ signals are active low inputs. Data is placed on the bus from counters or registers when $\overline{RD}$ is a logic "0". Data is transferred to counters or registers when $\overline{WR}$ is a logic "0". $\overline{RD}$ and $\overline{WR}$ must be accompanied by a

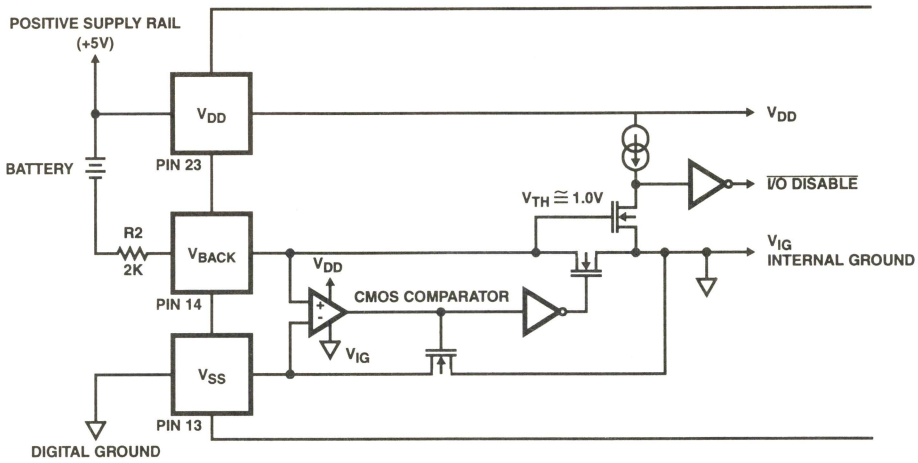


FIGURE 6. SIMPLIFIED ICM7170 BATTERY BACKUP CIRCUIT

logical "0" $\overline{CS}$ as shown in Figures 2 and 3. The ICM7170 will also work satisfactorily with $\overline{CS}$ grounded. In this mode, access to the ICM7170 is controlled by $\overline{RD}$ and $\overline{WR}$ only.

With the ALE (Address Latch Enable) input, the ICM7170 can be interfaced directly to microprocessors that use a multiplexed address/data bus by connecting the address lines A0 - A4 to the data lines D0 - D4. To address the chip, the address is placed on the bus and ALE is strobed. On the falling edge, the address and $\overline{CS}$ information is read into the address latch and buffer. $\overline{RD}$ and $\overline{WR}$ are used in the same way as on a non-multiplexed bus. If a non-multiplexed bus is used, ALE should be connected to V_{DD}.

Test Mode

The test mode is entered by setting D5 of the Command Register to a logic "1". This connects the 100Hz counter directly to the oscillator's output.

Oscillator Considerations

Load Design: A new oscillator load configuration, shown in Figure 7, has been found that eliminates start-up problems sometimes encountered with 32kHz tuning fork crystals.

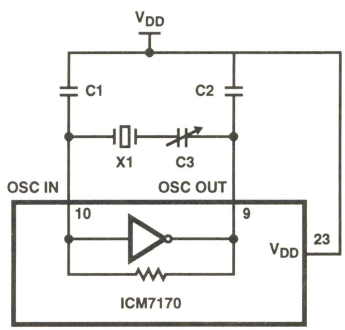


FIGURE 7. NEW OSCILLATOR CONFIGURATION

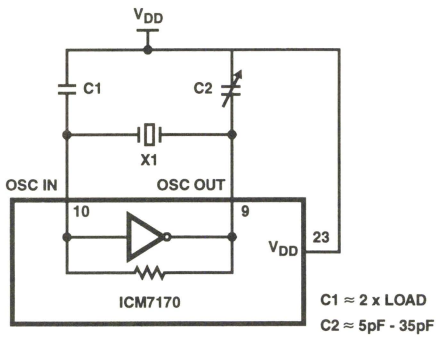


FIGURE 8. ORIGINAL OSCILLATOR CONFIGURATION

Two conditions must be met for best oscillator performance: the capacitive load must be matched to both the inverter and crystal to provide the ideal conditions for oscillation, and the resonant frequency of the oscillator must be adjustable to the desired frequency. In the original design (Figure 8), these two goals were often at odds with each other; either the oscillator was trimmed to frequency by detuning the load circuit, or stability was increased at the expense of absolute frequency accuracy.

The new load configuration (Figure 6) allows these two conditions to be met independently. The two load capacitors, C1 and C2, provide a fixed load to the oscillator and crystal. C3 adjusts the frequency that the circuit resonates at by reducing the effective value of the crystal's motional capacitance, C0. This minute adjustment does not appreciably change the load of the overall system, therefore, stability is no longer affected by tuning. Typical values for these capacitors are shown in Table 5. C1 and C2 must always be greater than twice the crystal's recommended load capacitance in order for C3 to be able to trim the frequency. Some experimentation may be necessary to determine the ideal values of C1 and C2 for a particular crystal.

TABLE 5. TYPICAL LOAD CAPACITOR VALUES

CRYSTAL FREQUENCY	LOAD CAPS (C1, C2)	TRIMMER CAP (C3)
32kHz	33pF	5 - 50pF
1MHz	33pF	5 - 50pF
2MHz	25pF	5 - 50pF
4MHz	22pF	5 - 100pF

This three capacitor tuning method will be more stable than the original design and is mandatory for 32kHz tuning fork crystals: without it they may leap into an overtone mode when power is initially applied.

The original two-capacitor circuit (Figure 8) will continue to work as well as it always has, and may continue to be used in applications where cost or space is a critical consideration. It is also easier to tune to frequency since one end of the trimmer capacitor is fixed at the AC ground of the circuit (V_{DD}), minimizing the disturbance cause by contact between the adjustment tool and the trimmer capacitor. Note that in both configurations the load capacitors are connected between the oscillator pins and V_{DD} - do not use V_{SS} as an AC ground.

Layout: Due to the extremely low current (and therefore high impedance) design of the ICM7170s oscillator, special attention must be given to the layout of this section. Stray capacitance should be minimized. Keep the oscillator traces on a single layer of the PCB. Avoid putting a ground plane above or below this layer. The traces between the crystal, the capacitors, and the ICM7170 OSC pins should be as short as possible. Completely surround the oscillator components with a thick trace of V_{DD} to minimize coupling with any digital signals. The final assembly must be free from contaminants such as solder flux, moisture, or any other potential sources of leakage. A good solder mask will help keep the traces free of moisture and contamination over time.

Oscillator Tuning

Trimming the oscillator should be done indirectly. Direct monitoring of the oscillator frequency by probing OSC IN or OSC OUT is not accurate due to the capacitive loading of most probes. One way to accurately trim the ICM7170 is by turning on the 1 second periodic interrupt and trimming the oscillator until the interrupt period is exactly one second. This can be done as follows:

1. Turn on the system. Write a 00H to the Interrupt Mask Register (location 10H) to clear all interrupts.
2. Set the Command Register (location 11H) for the appropriate crystal frequency, set the Interrupt Enable and Run/Stop bits to 1, and set the Test bit to 0.
3. Write a 08H to the Interrupt Mask Register to turn on the 1s interrupt.
4. Write an interrupt handler to read the Interrupt Status Register after every interrupt. This resets the interrupt and allows it to be set again. A software loop that reads the Interrupt Status Register several times each second will accomplish this also.
5. Connect a precision period counter capable of measuring 1s within the accuracy desired to the interrupt output. If the interrupt is configured as active low, trigger on the falling edge. If the interrupt is active high, trigger on the rising edge. Be sure to measure the period between when the transistor turns ON, and when the transistor turns ON a second later.
6. Adjust C3 (C2 for the two-capacitor load configuration) for an interrupt period of exactly 1.000000 seconds.

Application Notes

Digital Input Termination During Backup

To ensure low current drain during battery backup operation, none of the digital inputs to the ICM7170 should be allowed to float. This keeps the input logic gates out of their transition region, and prevents crossover current from flowing which will shorten battery life. The address, data, $\overline{CS}$, and ALE pins should be pulled to either V_{DD} or V_{SS}, and the $\overline{RD}$ and $\overline{WR}$ inputs should be pulled to V_{DD}. This is necessary whether the internal battery switchover circuit is used or not.

IBM/PC Evaluation Circuit

Figure 9 shows the schematic of a board that has been designed to plug into an IBM PC/XT (Note 1) or compatible computer. In this example $\overline{CS}$ is permanently tied low and access to the chip is controlled by the $\overline{RD}$ and $\overline{WR}$ pins. These signals are generated by U1, which gates the IBM's $\overline{IOR}$ and $\overline{IOW}$ with a device select signal from U3, which is functioning as an I/O block address decoder. DS1 selects the interrupt priority.

U5 is used to isolate the ICM7170 from the PC databus for test purposes. It is only required on heavily-loaded TTL databuses - the ICM7170 can drive most TTL and CMOS databuses directly.

Since the IBM PC/XT (Note 1) requires a positive interrupt transition, the ICM7170s interrupt output transistor has been configured as a source follower. As a source follower, the interrupt output signal will swing between 0V and 2.5V. When trimming the oscillator, the frequency counter must be triggered on the rising edge of the interrupt signal.

TABLE 6.

BATTERIES	CRYSTALS		
Panasonic	Saronix	32kHz	NTF3238
Rayovac	Statek	32kHz	CX - 1V
	Seiko	2MHz	GT - 38

NOTE:

1. IBM, IBM PC, and IBM XT are trademarks of IBM Corp.

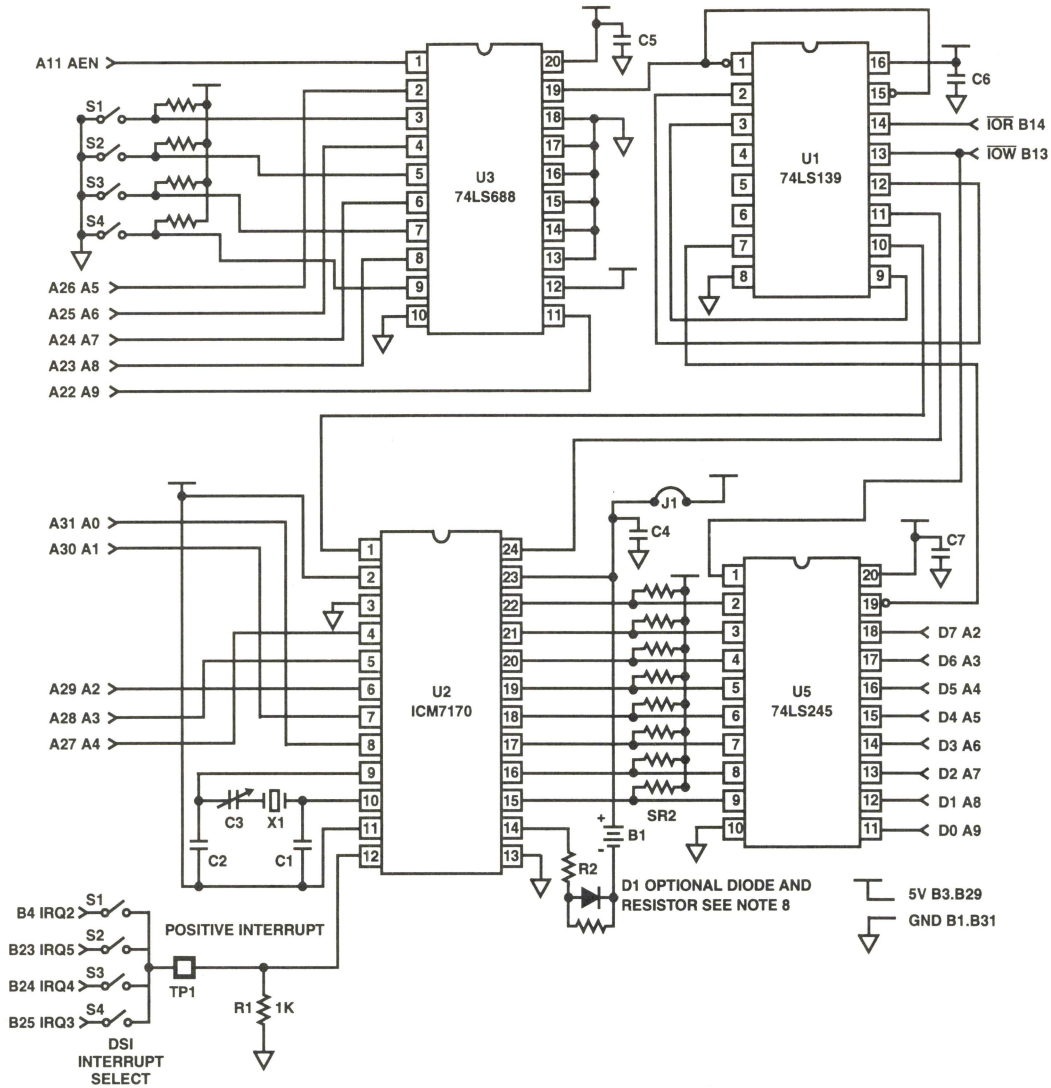


FIGURE 9. IBM PC INTERFACE FOR ICM7170Y

General Notes

1. TIME ACCESS - To update the present time registers (Hex 00 - 07) the $^1/_{100}$ register must be read first. The 7 real time counter registers (Hours, Minutes, Seconds, Month, Date, Day, and Year) data are latched only if the 1/100 second counter register is read. The 1/100 seconds data itself is not latched. The real time data will be held in the latches until the $^1/_{100}$ seconds is read again. See the data sheet section on LATCHED DATA. None of the RAM data is latched since it is static by nature.
2. REGULATED OSCILLATOR - The oscillator's power supply is voltage regulated with respect to V_{DD}. In the 32kHz mode the regulator's amplitude is ΣVtn + Vtp ($\cong$1.8V). In the 1, 2, and 4MHz mode the regulator's amplitude is ΣVtn + Vtn + Vtp ($\cong$2.6V). As a result, signal conditioning is necessary to drive the oscillator with an external signal. In addition, it is also necessary to buffer the oscillator's signal to drive other external clocks because of its reduced amplitude and offset voltage.
3. INTERNAL BATTERY BACKUP - When the ICM7170 is using its own internal battery backup circuitry, no other circuitry interfaced to the ICM7170 should be active during standby operation. When V_{DD} (+5V) is turned off (Standby operation), V_{DD} should equal V_{SS} = 0V. All ICM7170 I/O should also equal V_{SS}. At this time, the V_{BACKUP} pin should be 2.8V to 3.5V below V_{SS} when using a Lithium battery.
4. EXTERNAL BATTERY BACKUP - The ICM7170 may be placed on the same power supply as battery-backed up RAM by keeping the ICM7170 in its operational state and having an external circuit switch between system and backup power for the ICM7170 and the RAM. In this case V_{BACKUP} should be pulled up to V_{DD} through a 2K resistor. Although the ICM7170 is always "on" in this configuration, its current consumption will typically be less than a microamp greater than that of standby operation at the same supply voltage (See Note 9). Proper consideration must be given to disabling the ICM7170s and the RAMs I/O before system power is removed. This is important because many microprocessors can generate spurious write signals when their supply falls below their specified operating voltage limits. NANDing CS (or WR) with a POWERGOOD signal will create a $\overline{CS}$ (or $\overline{WR}$) that is only valid when system power is within specifications. The POWERGOOD signal should be generated by an accurate supply monitor such as the ICL7665 under/over voltage detector. An alternate method of disabling the ICM7170's I/O is to pull V_{BACKUP} down to under a volt above V_{SS} ($V_{SS} < V_{BACKUP} < 1.0V$). This will cause the ICM7170 to internally disable all I/O. Do not allow V_{BACKUP} to equal V_{SS}, since this could cause oscillation of the battery backup comparator (See Figure 6). $V_{BACKUP} = V_{SS} + 0.5V$ will disable the I/O and provide enough overdrive for the comparator.
5. ICM7170A PART - The ICM7170A part is binned at final test for a 32.768kHz maximum current of 5µA. All other specifications remain the same.
6. INTERRUPTS - The Interrupt Status Register (address 10H) always indicates which of the real time counters have been incremented since the last time the register was read. NOTE: This is independent of whether or not any mask bits are set.

   The status register is always reset immediately after it is read. If an interrupt from the ICM7170 has occurred since the last time the status register was read, bit D7 of the register will be set. If the source was an alarm interrupt, bit D0 will also be set. If the interrupt transistor has been turned on, reading the Interrupt Status Register will reset it.

   To enable the periodic interrupt, both the Command Register's Interrupt Enable bit (D4) and at least one bit in the Interrupt Mask Register (D1 - D6) must be set to a 1. The periodic interrupt is triggered when the counter corresponding to a mask bit that has been set is incremented. For example, if you enable the 1 second interrupt when the current value in the 100ths counter is 57, the first interrupt will occur 0.43 seconds later. All subsequent interrupts will be exactly one second apart. The interrupt service routine should then read the Interrupt Status Register to reset the interrupt transistor and, if necessary, determine the cause of the interrupt (periodic, alarm, or non-ICM7170 generated) from the contents of the status register.

   To enable the alarm interrupts, both the Command Register's Interrupt Enable bit (D4) and the Interrupt Mask Register's Alarm bit (D0) must be set to a 1. Each time there is an exact match between the values in the alarm register and the values in the real time counters, bits D0 and D7 of the Interrupt Status Register will be set to a 1 and the N-channel interrupt transistor will be turned on. As with a periodic interrupt, the service routine should then read the Interrupt Status Register to reset the interrupt transistor and, since periodic and alarm interrupts may be simultaneously enabled, determine the cause of the interrupt if necessary.

   Mask bits: The ICM7170 alarm interrupt compares the data in the alarm registers with the data in the real time registers, ignoring any registers with the mask bit set. For example, if the alarm register is set to 11-23-95 (Month-Day-Year), 10:59:00:00 (Hour-Minutes-Seconds-Hundredths), and DAY = XX (XX = masked off), the alarm will generate a single interrupt at 10:59 on November 23,1995. If the alarm register is set to 11-XX-95, 10:XX:00:00, and DAY = 2 (2 = Tuesday); the alarm will generate one interrupt every minute from 10:00-10:59 on every Tuesday in November, 1995.

   NOTE: Masking off the 100ths of a second counter has the same effect as setting it to 00.
7. RESISTOR IN SERIES WITH BATTERY - A 2K resistor (R2) must be placed in series with the battery backup pin of the ICM7170. The UL laboratories have requested the resistor to limit the charging and discharging current to the battery. The resistor also serves the purpose of degenerating parasitic SCR action. This SCR action may occur if an input is applied to the ICM7170, outside of its supply voltage range, while it is in the standby mode.
8. V_{BACKUP} DIODE - Lithium batteries may explode if charged or if discharged at too high a rate. These conditions could occur if the battery was installed backwards or in the case of a gross component failure. A 1N914-type diode placed in series with the battery as shown in Figure 9 will prevent this from occurring. A resistor of 2MΩ or so should parallel the diode to keep the V_{BACKUP} terminal from drifting toward the V_{SS} terminal and shutting off ICM7170 I/O during normal operation.
9. SUPPLY CURRENT - ICM7170 supply current is predominantly a function of oscillator frequency and databus activity. The lower the oscillator frequency, the lower the supply current. When there is little or no activity on the data, address or control lines, the current consumption of the ICM7170 in its operational mode approaches that of the backup mode.

HARRIS SEMICONDUCTOR

82C237

CMOS High Performance Programmable DMA Controller

March 1997

Features

- Fully Compatible with Harris 82C37A
  - 82C237 May be Used in 8MHz and 12.5MHz 82C37A Sockets
- Optimized for 10MHz and 12.5MHz 80C286 Systems
- Special Mode Permits 16-Bit, Zero Wait State DMA Transfers
- High Speed Data Transfers:
  - Up to 6.25MBytes/sec with 12.5MHz Clock in Normal Mode
  - Up to 12.5MBytes/sec with 12.5MHz Clock in 16-Bit Mode
- Compatible with the NMOS 8237A
- Four Independent Maskable Channels with Autoinitialization Capability
- Cascadable to any Number of Channels
- Memory-to-Memory Transfers
- Static CMOS Design Permits Low Power Operation
  - ICCSB = 10μA Maximum
  - ICCOP = 2mA/MHz Maximum
- Fully TTL/CMOS Compatible
- Internal Registers may be Read from Software

Description

The 82C237 is a modified version of the 82C37A. The 82C237 is fully software and pin for pin compatible with the 82C37A but provides an additional mode for 16-bit DMA transfers, as well as enhanced speed. Each channel may be individually programmed for 8-bit or 16-bit data transfers.

The 82C237 controller can improve system performance by allowing external devices to transfer data directly to or from system memory. Memory-to-memory transfer capability is also provided, along with a memory block initialization feature. DMA requests may be generated by either hardware or software, and each channel is independently programmable with a variety of features for flexible operation.

The 82C237 is designed to be used with an external address latch, such as the 82C82, to demultiplex the most significant 8 bits of address. An additional latch is required to temporarily store the most significant 8 bits of data if 16-bit memory-to-memory transfers are desired. The 82C237 can be used with industry standard microprocessors such as 80C286, 80286, 80C86, 80C88, 8086, 8088, 8085, Z80, NSC800, 80186 and others. Multimode programmability allows the user to select from three basic types of DMA services, and reconfiguration under program control is possible even with the clock to the controller stopped. Each channel has a full 64K address and word count range, and may be programmed to autoinitialize these registers following DMA termination (end of process).

Ordering Information

PACKAGE	TEMPERATURE RANGE	8MHz	12.5MHz	PKG. NO.
PDIP	0°C to +70°C	CP82C237	CP82C237-12	E40.6
	-40°C to +85°C	IP82C237	IP82C237-12	E40.6
PLCC	0°C to +70°C	CS82C237	CS82C237-12	N44.65
	-40°C to +85°C	IS82C237	IS82C237-12	N44.65
SBDIP	0°C to +70°C	CD82C237	CD82C237-12	F40.6
	-40°C to +85°C	ID82C237	ID82C237-12	F40.6
	-55°C to +125°C	MD82C237/B	MD82C237-12/B	F40.6
SMD#		5962-9054304MQA	5962-9054305MQA	F40.6
CLCC	-55°C to +125°C	MR82C237/B	MR82C237-12/B	J44.A
SMD#		5962-9054304MXA	5962-9054305MXA	J44.A

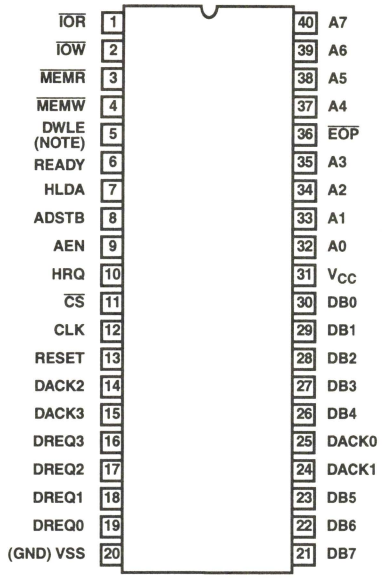
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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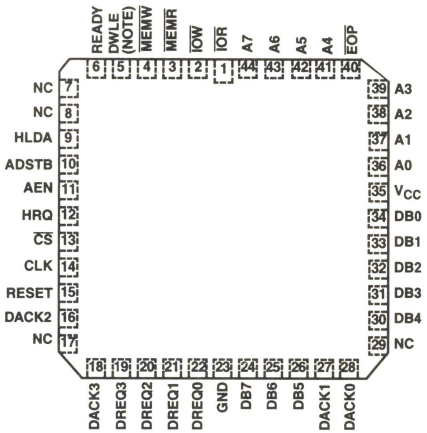
File Number **2965.1**

Pinouts

82C237 (DIP)
TOP VIEW

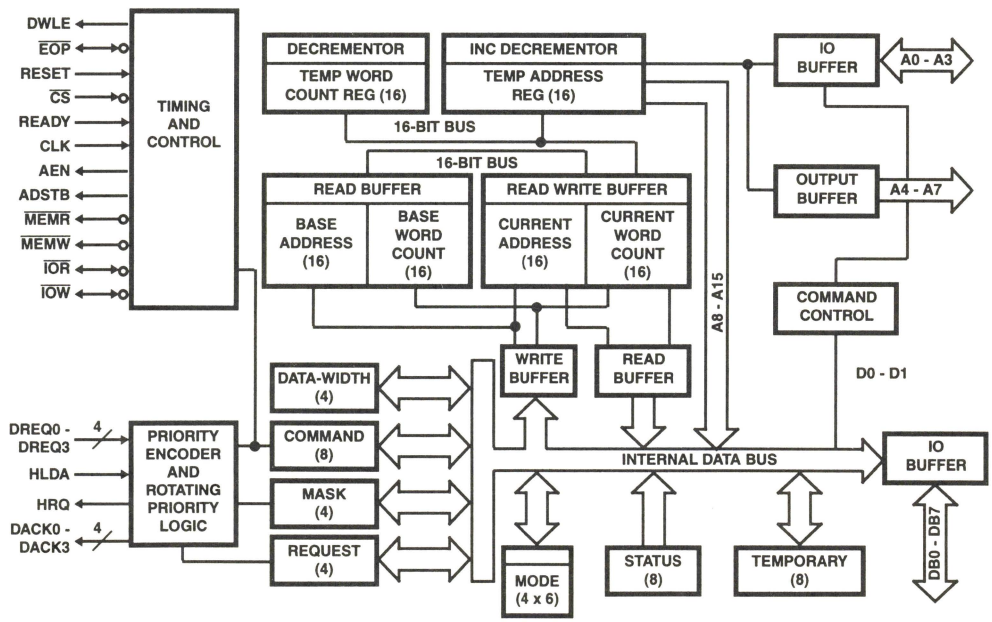


82C237 (CLCC/PLCC)
TOP VIEW



NOTE: See Pin Description.

Block Diagram



Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	31		V_{CC}: is the +5V power supply pin. A 0.1µF capacitor between pins 31 and 20 is recommended for decoupling.
GND	20		Ground
CLK	12	I	CLOCK INPUT: The Clock Input is used to generate the timing signals which control 82C237 operations. This input may be driven from DC to 12.5MHz for the 82C237-12 or from DC to 8MHz for the 82C237. The Clock may be stopped in either state for standby operation.
$\overline{CS}$	11	I	CHIP SELECT: Chip Select is an active low input used to enable the controller onto the data bus for CPU communications.
RESET	13	I	RESET: This is an active high input which clears the Command, Status, Request, and Temporary registers, the First/Last Flip-Flop, and the mode register counter. The Mask register is set to ignore requests. The Data-Width register is set to perform 8-bit transfers on all channels (82C237 only). Following a Reset, the controller is in an idle cycle.
READY	6	I	READY: This signal can be used to extend the memory read and write pulses from the 82C237 to accommodate slow memories or I/O devices. READY must not make transitions during its specified set-up and hold times. See Figure 14 for timing. READY is ignored in verify transfer mode.
HLDA	7	I	HOLD ACKNOWLEDGE: The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses. HLDA is a synchronous input and must not transition during its specified set-up time. There is an implied hold time (HLDA inactive) of TCH from the rising edge of clock, during which time HLDA must not transition.
DREQ0-DREQ3	16-19	I	DMA REQUEST: The DMA Request (DREQ) lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In Fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of a DREQ signal. Polarity of DREQ is programmable. RESET initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active. DREQ will not be recognized while the clock is stopped. Unused DREQ inputs should be pulled High or Low (inactive) and the corresponding mask bit set. In 16-bit Transfer mode (82C237 only), each DREQ channel may be programmed to perform either 8-bit or 16-bit DMA transfers.
DB0-DB7	21-23 26-30	I/O	DATA BUS: The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of a register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the 82C237 control registers. During DMA cycles, the most significant 8-bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory enters the 82C237 on the data bus during the read-from-memory transfer, then during the write-to-memory transfer, the data bus outputs write the data into the new memory location.
$\overline{IOR}$	1	I/O	I/O READ: I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the 82C237 to access data from the peripheral during a DMA Write transfer.
$\overline{IOW}$	2	I/O	I/O WRITE: I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the 82C237. In the Active cycle, it is an output control signal used by the 82C237 to load data to the peripheral during a DMA Read transfer.

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{EOP}$	36	I/O	END OF PROCESS: End of Process ($\overline{EOP}$) is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional $\overline{EOP}$ pin. The 82C237 allows an external signal to terminate an active DMA service by pulling the $\overline{EOP}$ pin low. A pulse is generated by the 82C237 when terminal count (TC) for any channel is reached, except for channel 0 in memory-to-memory mode. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. The $\overline{EOP}$ pin is driven by an open drain transistor on-chip, and requires an external pull-up resistor to V_{CC}. When an $\overline{EOP}$ pulse occurs, whether internally or externally generated, the 82C237 will terminate the service, and if autoinitialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for autoinitialize. In that case, the mask bit remains clear.
A0-A3	32-35	I/O	ADDRESS: The four least significant address lines are bidirectional three-state signals. In the Idle cycle, they are inputs and are used by the 82C237 to address the control register to be loaded or read. In the Active cycle, they are outputs and provide the lower 4-bits of the output address. When in 16-bit mode (82C237 only), and the active channel is a 16-bit channel (as defined by the Data-Width register), then A0 will remain low during the entire transfer (i.e. an even word address will always be generated).
A4-A7	37-40	O	ADDRESS: The four most significant address lines are three-state outputs and provide 4-bits of address. These lines are enabled only during the DMA service.
HRQ	10	O	HOLD REQUEST: The Hold Request (HRQ) output is used to request control of the system bus. When a DREQ occurs and the corresponding mask bit is clear, or a software DMA request is made, the 82C237 issues HRQ. The HLDA signal then informs the controller when access to the system busses is permitted. For stand-alone operation where the 82C237 always controls the busses, HRQ may be tied to HLDA. This will result in one S0 state before the transfer.
DACK0- DACK3	14, 15 24, 25	O	DMA ACKNOWLEDGE: DMA acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. RESET initializes them to active low.
AEN	9	O	ADDRESS ENABLE: Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
ADSTB	8	O	ADDRESS STROBE: This is an active high signal used to control latching of the upper address byte. It will drive directly the strobe input of external transparent octal latches, such as the 82C82. During block operations, ADSTB will only be issued when the upper address byte must be updated, thus speeding operation through elimination of S1 states. ADSTB timing is referenced to the falling edge of the 82C237 clock.
$\overline{MEMR}$	3	O	MEMORY READ: The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer.
$\overline{MEMW}$	4	O	MEMORY WRITE: The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.
DWLE	5	O	DATA-WIDTH, LATCH ENABLE: In normal 8-bit transfer mode (16-bit transfer mode not enabled), this output is always high impedance three-stated. In 16-bit transfer mode (82C237 only), this output serves a dual purpose. During S1 cycles, the DWLE output indicates the data width (0 = 16-bit, 1 = 8-bit) of the active channel. During memory-to-memory transfers, the DWLE output is used to enable an external latch which temporarily stores the 8 most significant bits of data during the read-from-memory transfer. DWLE enables this byte of data onto the data bus during the write-to-memory transfer of a memory-to-memory operation.

Functional Description

The 82C237 is an improved version of the Harris 82C37A DMA controller and is fully software and pin for pin compatible with the 82C37A. All operational and pin descriptions of the 82C37A apply to the 82C237 with additional features noted in the section titled 82C237 Operation.

The 82C237 direct memory access controller is designed to improve the data transfer rate in systems which must transfer data from an I/O device to memory, or move a block of memory to an I/O device. It will also perform memory-to-memory block moves, or fill a block of memory with data from a single location. Operating modes are provided to handle single byte transfers as well as discontinuous data streams, which allows the 82C237 to control data movement with software transparency.

The DMA controller is a state-driven address and control signal generator, which permits data to be transferred directly from an I/O device to memory or vice versa without ever being stored in a temporary register. This can greatly increase the data transfer rate for sequential operations, compared with processor move or repeated string instructions. Memory-to-memory operations require temporary internal storage of the data byte between generation of the source and destination addresses, so memory-to-memory transfers take place at less than half the rate of I/O operations, but still much faster than with central processor techniques. The maximum data transfer rates obtainable with the 82C237 are shown in Figure 1.

The block diagram of the 82C237 is shown on page 2. The timing and control block, priority block, and internal registers are the main components. Figure 2 lists the name and size of the internal registers. The timing and control block derives internal timing from CLK input, and generates external control signals. The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously.

82C237 TRANSFER TYPE	8MHz		12.5MHz		UNIT
	8-BIT	16-BIT	8-BIT	16-BIT	
Compressed	4.00	8.00	6.25	12.5	MByte/sec
Normal I/O	2.67	5.34	4.17	8.34	MByte/sec
Memory-to-Memory	1.00	2.00	1.56	3.12	MByte/sec

FIGURE 1. DMA TRANSFER RATES

DMA Operation

In a system, the 82C237 address and control outputs and data bus pins are basically connected in parallel with the system busses. An external latch is required for the upper address byte. While inactive, the controller's outputs are in a high impedance state. When activated by a DMA request and bus control is relinquished by the host, the 82C237 drives the busses and generates the control signals to perform the data transfer. The operation performed by activating one of the four DMA request inputs has previously been programmed into the controller via the Command, Mode, Address, and Word Count registers.

For example, if a block of data is to be transferred from RAM to an I/O device, the starting address of the data is loaded into the 82C237 Current and Base Address registers for a particular channel, and the length of the block is loaded into the channel's Word Count register. The corresponding Mode register is programmed for a memory-to-I/O operation (read transfer), and various options are selected by the Command register and the other Mode register bits. The channel's mask bit is cleared to enable recognition of a DMA request (DREQ). The DREQ can either be a hardware signal or a software command.

Once initiated, the block DMA transfer will proceed as the controller outputs the data address, simultaneous $\overline{MEMR}$ and $\overline{IOW}$ pulses, and selects an I/O device via the DMA acknowledge (DACK) outputs. The data byte flows directly from the RAM to the I/O device. After each byte is transferred, the address is automatically incremented (or decremented) and the word count is decremented. The operation is then repeated for the next byte. The controller stops transferring data when the Word Count register underflows, or an external $\overline{EOP}$ is applied.

NAME	SIZE	NUMBER
Base Address Registers	16-Bits	4
Base Word Count Registers	16-Bits	4
Current Address Registers	16-Bits	4
Current Word Count Registers	16-Bits	4
Temporary Address Register	16-Bits	1
Temporary Word Count Register	16-Bits	1
Status Register	8-Bits	1
Command Register	8-Bits	1
Temporary Register	8-Bits	1
Mode Registers	6-Bits	4
Mask Register	4-Bits	1
Request Register	4-Bits	1
Data-Width Register (See Note)	4-Bits	1

NOTE: 82C237 only

FIGURE 2. 82C237 INTERNAL REGISTERS

To further understand 82C237 operation, the states generated by each CLK cycle must be considered. The DMA controller operates in two major cycles, active and idle. After being programmed, the controller is normally idle until a DMA request occurs on an unmasked channel, or a software request is given. The 82C237 will then request control of the system busses and enter the active cycle. The active cycle is composed of several internal states, depending on what options have been selected and what type of operation has been requested.

The 82C237 can assume seven separate states, each composed of one full CLK period. State I (SI) is the idle state. It is entered when the 82C237 has no valid DMA requests pending, at the end of a transfer sequence, or when a RESET or Master Clear has occurred. While in SI, the DMA controller is inactive but may be in the Program Condition (being programmed by the processor).

State 0 (S0) is the first state of a DMA service. The 82C237 has requested a hold but the processor has not yet returned an acknowledge. The 82C237 may still be programmed until it has received HLDA from the CPU. An acknowledge from the CPU will signal the DMA transfer may begin. S1, S2, S3, and S4 are the working state of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S3 and S4 in normal transfers by the use of the READY line on the 82C237. For compressed transfers, wait states can be inserted between S2 and S4. See timing Figures 14 and 15.

Note that the data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active at the same time. The data is not read into or driven out of the 82C237 in I/O-to-memory or memory-to-I/O DMA transfers.

Memory-to-memory transfers require a read-from and a write-to memory to complete each transfer. The States, which resemble the normal working states, use two-digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer.

Idle Cycle

When no channel is requesting service, the 82C237 will enter the idle cycle and perform "SI" States. In this cycle, the 82C237 will sample the DREQ lines on the falling edge of every CLK cycle to determine if any channel is requesting a DMA service.

Note that for standby operation where the clock has been stopped, DMA requests will be ignored. The device will respond to $\overline{CS}$ (chip select), in case of an attempt by the microprocessor to write or read the internal registers of the 82C237. When $\overline{CS}$ is low and HLDA is low, the 82C237 enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers.

The 82C237 may be programmed with the clock stopped, provided that HLDA is low and at least one rising CLK edge has occurred after HLDA was driven low, so the controller is in an SI state. Address lines A0-A3 are inputs to the device and select which registers will be read or written. The $\overline{IOR}$ and $\overline{IOW}$ lines are used to select and time the read or write operations. Due to the number and size of the internal registers, an internal flip-flop called the First/Last Flip-Flop is used to generate an additional bit of address. The bit is used to determine the upper or lower byte of the 16-bit Address and Work Count registers. The flip-flop is reset by Master Clear or RESET. Separate software commands can also set or reset this flip-flop.

Special software commands can be executed by the 82C237 in the Program Condition. These commands are decoded as sets of addresses with $\overline{CS}$, $\overline{IOR}$, and $\overline{IOW}$. The commands do not make use of the data bus. Instructions include Set and Clear First/Last Flip-Flop, Master Clear, Clear Mode Register Counter, and Clear Mask Register.

Active Cycle

When the 82C237 is in the Idle cycle, and a software request or an unmasked channel requests a DMA service, the device will issue HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode - In single transfer mode, the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero to FFFFH, a terminal count bit in the status register is set, an $\overline{EOP}$ pulse is generated, and the channel will autoinitialize if this option has been selected. If not programmed to autoinitialize, the mask bit will be set, along with the TC bit and $\overline{EOP}$ pulse.

DREQ must be held active until DACK becomes active. If DREQ is held active throughout the single transfer, HRQ will go inactive and release the bus to the system. It will again go active and, upon receipt of a new HLDA, another single transfer will be performed, unless a higher priority channel takes over. In 8080A, 8085A, 80C88, or 80C86 systems, this will ensure one full machine cycle execution between DMA transfers. Details of timing between the 82C237 and other bus control protocols will depend upon the characteristics of the microprocessor involved.

Block Transfer Mode - In Block Transfer mode, the device is activated by DREQ or software request and continues making transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process ($\overline{EOP}$) is encountered. DREQ need only be held active until DACK becomes active. Again, an Autoinitialization will occur at the end of the service if the channel has been programmed for that option.

Demand Transfer Mode - In Demand Transfer mode the device continues making transfers until a TC or external $\overline{EOP}$ is encountered, or until DREQ goes inactive. Thus, transfer may continue until the I/O device has exhausted its data capacity. After the I/O device has had a chance to catch up, the DMA service is reestablished by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the 82C237 Current Address and Current Word Count registers. Higher priority channels may intervene in the demand process, once DREQ has gone inactive. Only an $\overline{EOP}$ can cause an Autoinitialization at the end of service. $\overline{EOP}$ is generated either by TC or by an external signal.

Cascade Mode - This mode is used to cascade more than one 82C237 for simple system expansion. The HRQ and HLDA signals from the additional 82C237 are connected to the DREQ and DACK signals respectively of a channel for

the initial 82C237. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial 82C237 is used only for prioritizing the additional device, it does not output an address or control signals of its own. These could conflict with the outputs of the active channel in the added device. The initial 82C237 will respond to DREQ and generate DACK but all other outputs except HRQ will be disabled. An external $\overline{EOP}$ will be ignored by the initial device, but will have the usual effect on the added device.

Figure 3 shows two additional devices cascaded with an initial device using two of the initial device's channels. This forms a two-level DMA system. More 82C237s could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

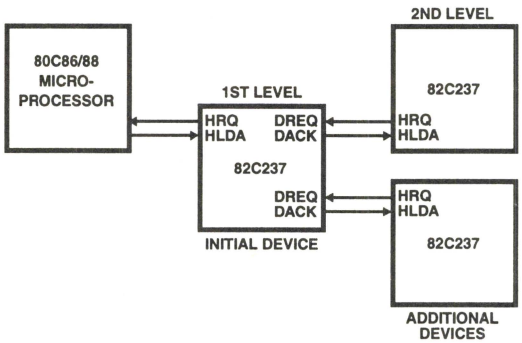


FIGURE 3. CASCADED 82C237s

When programming cascaded controllers, start with the first level device (closest to the microprocessor). After RESET, the DACK outputs are programmed to be active low and are held in the high state. If they are used to drive HLDA directly, the second level device(s) cannot be programmed until DACK polarity is selected as active high on the initial device. Also, the initial device's mask bits function normally on cascaded channels, so they may be used to inhibit second-level services.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{MEMW}$ and $\overline{IOR}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$.

Verify transfers are pseudo-transfers. The 82C237 operates as in Read or Write transfers generating addresses and responding to $\overline{EOP}$, etc., however the memory and I/O control lines all remain inactive. Verify mode is not permitted for memory-to-memory operation. READY is ignored during verify transfers.

Autoinitialize - By setting bit 4 in the Mode register, a channel may be set up as an Autoinitialize channel. During Autoinitialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word Count registers of the channel following $\overline{EOP}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in Autoinitialize mode. Following Autoinitialization, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected, or software request made.

Memory-to-Memory - To perform block moves of data from one memory address space to another with minimum of program effort and time, the 82C237 includes a memory-to-memory transfer feature. Setting bit 0 in the Command register selects channels 0 and 1 to operate as memory-to-memory transfer channels.

The transfer is initiated by setting the software or hardware DREQ for channel 0. The 82C237 requests a DMA service in the normal manner. After HLDA is true, the device, using four-state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the 82C237 internal Temporary register. Another four-state transfer moves the data to memory using the address in channel one's Current Address register and incrementing or decrementing it in the normal manner. The channel 1 Current Word Count is decremented.

When the word count of channel 1 decrements to FFFFH, a TC is generated causing an $\overline{EOP}$ output, terminating the service, and setting the channel 1 TC bit in the Status register. The channel 1 mask bit will also be set, unless the channel 1 mode register is programmed for autoinitialization. Channel 0 word count decrementing to FFFFH will not set the channel 0 TC bit in the status register or generate an $\overline{EOP}$, or set the channel 0 mask bit in this mode. It will cause an autoinitialization of channel 0, if that option has been selected.

If full Autoinitialization for a memory-to-memory operation is desired, the channel 0 and channel 1 word counts must be set to equal values before the transfer begins. Otherwise, if channel 0 underflows before channel 1, it will autoinitialize and set the data source address back to the beginning of the block. If the channel 1 word count underflows before channel 0, the memory-to-memory DMA service will terminate, and channel 1 will autoinitialize but channel 0 will not.

In memory-to-memory mode, Channel 0 may be programmed to retain the same address for all transfers. This allows a single byte to be written to a block of memory. This channel 0 address hold feature is selected by setting bit 1 in the Command register.

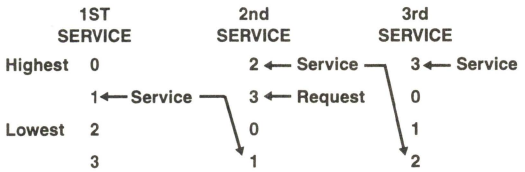
The 82C237 will respond to external $\overline{EOP}$ signals during memory-to-memory transfers, but will only relinquish the system busses after the transfer is complete (i.e. after an S24 state). It should be noted that an external $\overline{EOP}$ cannot cause the channel 0 Address and Word Count registers to

autoinitialize, even if the Mode register is programmed for autoinitialization. An external $\overline{EOP}$ will autoinitialize the channel 1 registers, if so programmed. Data comparators in block search schemes may use the $\overline{EOP}$ input to terminate the service when a match is found. The timing of memory-to-memory transfers in found in Figure 13. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

Priority - The 82C237 has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their numbers. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interfering with the service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly. The next lower channel from the channel serviced has highest priority on the following request. Priority rotates every time control of the system busses is returned to the processor.

Rotating Priority



With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.

Regardless of which priority scheme is chosen, priority is evaluated every time a HLDA is returned to the 82C237.

Compressed Timing - In order to achieve even greater throughput where system characteristics permit, the 82C237 can compress the transfer time to two clock cycles. From Figure 12 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8-A15 need updating (see Address Generation). Timing for compressed transfers is found in Figure 15. $\overline{EOP}$ will output in S2 if compressed timing is selected. Compressed timing is not allowed for memory-to-memory transfers.

Address Generation - In order to reduce pin count, the 82C237 multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are output by the 82C237 directly. Lines A0-A7 should be connected to the address bus. Figure 12 shows the time relationships between CLK, AEN, ADSTB, DB0-DB7 and A0-A7.

During Block and Demand Transfer mode service, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the 82C237 executes S1 states only when updating of A8-A15 in the latch is necessary. This means for long services, S1 states and Address Strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

Programming

The 82C237 will accept programming from the host processor anytime that HLDA is inactive, and at least one rising CLK edge has occurred after HLDA went low. It is the responsibility of the host to assure that programming and HLDA are mutually exclusive.

Note that a problem can occur if a DMA request occurs on an unmasked channel while the 82C237 is being programmed. For instance, the CPU may be starting to reprogram the two byte Address register of channel 1 when channel 1 receives a DMA request. If the 82C237 is enabled (bit 2 in the Command register is 0), and channel 1 is unmasked, a DMA service will occur after only one byte of the Address register has been reprogrammed. This condition can be avoided by disabling the controller (setting bit 2 in the Command register) or masking the channel before programming any of its registers. Once the programming is complete, the controller can be enabled/unmasked.

After power-up it is suggested that all internal locations be loaded with some known value, even if some channels are unused. This will aid in debugging.

Register Description

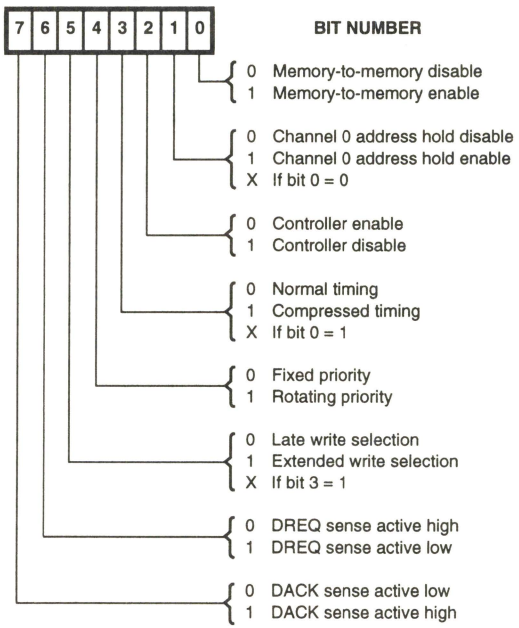
Current Address Register - Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented by one after each transfer and the values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. See Figure 6 for programming information. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an $\overline{EOP}$. In memory-to-memory mode, the channel 0 Current Address register can be prevented from incrementing or decrementing by setting the address hold bit in the Command register.

Current Word Count Register - Each channel has a 16-Bit Current Word Count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. See Figure 6 for programming information. Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialization can occur only when an $\overline{EOP}$ occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC.

Base Address and Base Word Count Registers - Each Channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. See Figure 6 for programming information. These registers cannot be read by the microprocessor.

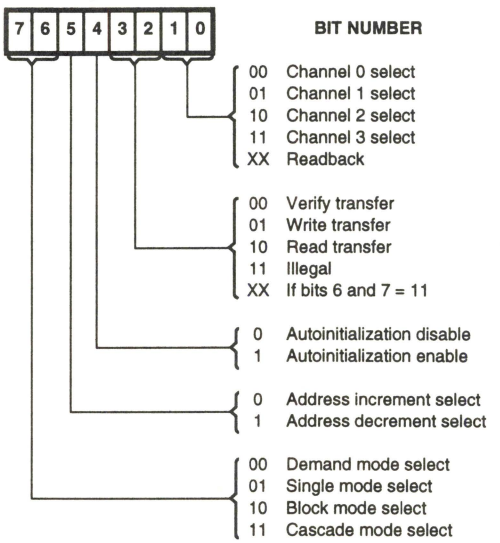
Command Register - This 8-bit register controls the operation of the 82C237. It is programmed by the microprocessor and is cleared by RESET or a Master Clear instruction. The following diagram lists the function of the Command register bits. See Figure 4 for Read and Write addresses.

Command Register



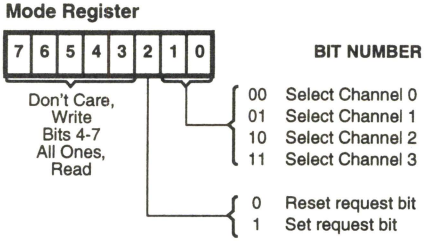
Mode Register - Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program condition, bits 0 and 1 determine which channel Mode register is to be written. When the processor reads a Mode register, bits 0 and 1 will both be ones. See the following diagram and Figure 4 for Mode register functions and addresses.

Mode Register



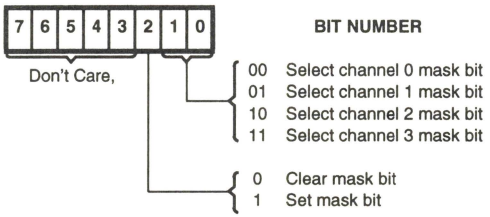
Request Register - The 82C237 can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are non-maskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control. The entire register is cleared by a RESET or Master Clear instruction. To set or reset a bit, the software loads the proper form of the data word. See Figure 4 for register address coding, and the following diagram for Request register format. A software request for DMA operation can be made in block or single modes. For memory-to-memory transfers, the software request for channel 0 should be set. When reading the Request register, bits 4-7 will always read as ones, and bits 0-3 will display the request bits of channels 0-3 respectively.

Mode Register

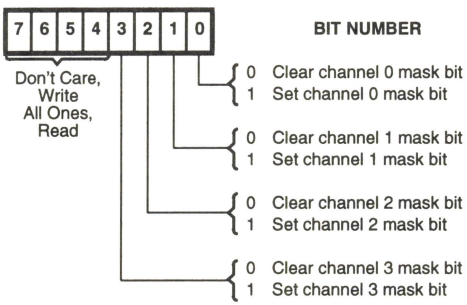


Mask Register - Each channel has associated with it a mask bit which can be set to disable an incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed to Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately or simultaneously under software control. The entire register is also set by a RESET or Master clear. This disables all hardware DMA requests until a Clear Mask Register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. Refer to the following diagram and Figure 4 for details. When reading the Mask register, bits 4-7 will always read as logical ones, and bits 0-3 will display the mask bits of channels 0-3, respectively. The 4-bits of the mask register may be cleared simultaneously by using the Clear Mask Register command (see software commands section).

Mask Register

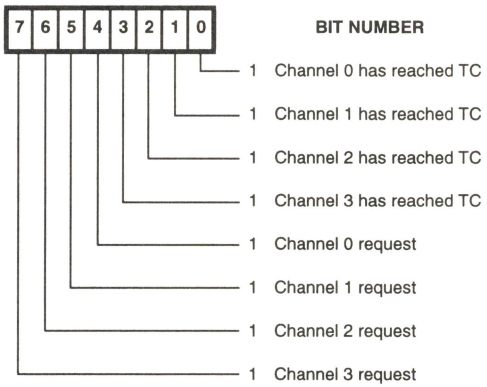


All four bits of the Mask register may also be written with a single command.



Status Register - The Status register is available to be read out of the 82C237 by the microprocessor. It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. These bits are cleared upon RESET, Master Clear, and on each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service, regardless of the mask bit state. If the mask bits are set, software can poll the Status register to determine which channels have DREQs, and selectively clear a mask bit, thus allowing user defined service priority. Status bits 4-7 are updated while the clock is high, and latched on the falling edge. Status Bits 4-7 are cleared upon RESET or Master Clear.

Status Register



Temporary Register - The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last byte moved can be read by the microprocessor. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a RESET or Master Clear.

OPERATION	A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$
Read Status Register	1	0	0	0	0	1
Write Command Register	1	0	0	0	1	0
Read Request Register	1	0	0	1	0	1
Write Request Register	1	0	0	1	1	0
Read Command Register	1	0	1	0	0	1
Write Single Mask Bit	1	0	1	0	1	0
Read Mode Register	1	0	1	1	0	1
Write Mode Register	1	0	1	1	1	0
Set First/Last F/F	1	1	0	0	0	1
Clear First/Last F/F	1	1	0	0	1	0
Read Temporary Register	1	1	0	1	0	1
Master Clear	1	1	0	1	1	0
Clear Mode Reg. Counter	1	1	1	0	0	1
Clear Mask Register	1	1	1	0	1	0
Read All Mask Bits	1	1	1	1	0	1
Write All Mask Bits	1	1	1	1	1	0

FIGURE 4. SOFTWARE COMMAND CODES AND REGISTER CODES

Software Commands

There are special software commands which can be executed by reading or writing to the 82C237. These commands do not depend on the specific data pattern on the data bus, but are activated by the I/O operation itself. On read type commands, the data value is not guaranteed. These commands are:

Clear First/Last Flip-Flop - This command is executed prior to writing or reading new address or word count information to the 82C237. This command initializes the flip-flop to a known state (low byte first) so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

Set First/Last Flip-Flop - This command will set the flip-flop to select the high byte first on read and write operations to address and word count registers.

Master Clear - This software instruction has the same effect as the hardware RESET. The Command, Status, Request, and Temporary registers, and Internal First/Last Flip-Flop and mode register counter are cleared and the Mask register is set. The 82C237 will enter the idle cycle.

Clear Mask Register - This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Clear Mode Register Counter - Since only one address location is available for reading the Mode registers, an internal two-bit counter has been included to select Mode registers during read operation. To read the Mode registers, first execute the Clear Mode Register Counter command, then do consecutive reads until the desired channel is read. Read order is channel 0 first, channel 3 last. The lower two bits on all Mode registers will read as ones.

External $\overline{EOP}$ Operation

The $\overline{EOP}$ pin is a bidirectional, open drain pin which may be driven by external signals to terminate DMA operation. Because $\overline{EOP}$ is an open drain pin an external pull-up resistor to V_{CC} is required. The value of the external pull-up resistor used should guarantee a rise time of less than 125ns. It is important to note that the 82C237 will not accept external $\overline{EOP}$ signals when it is in an SI (Idle) state. The controller must be active to latch EXT $\overline{EOP}$. Once latched, the EXT $\overline{EOP}$ will be acted upon during the next S2 state, unless the 82C237 enters an idle state first. In the latter case, the latched $\overline{EOP}$ is cleared. External $\overline{EOP}$ pulses occurring between active DMA transfers in demand mode will not be recognized, since the 82C237 is in an SI state.

16-Bit Transfer Mode

The 82C237 is fully software and pin for pin compatible with the 82C37A. Therefore, the 82C237 may be used as a faster 82C37A without modifications to software or hardware. The 82C237 may be used as an 82C37A, however, the 82C237 has an additional feature in that it may be programmed to perform 16-bit DMA transfers, thus doubling data transfer rate. In 16-bit transfer mode the device operates the same as in normal (8-bit) transfer mode with exceptions noted in this section.

16-Bit Transfer Mode Initialization - To initialize the 82C237 to 16-bit Transfer Mode, a specific sequence of software commands must be written to the device immediately after a hardware RESET or a Master Clear instruction. The sequence to initialize 16-bit Transfer Mode is as follows:

1) Hardware RESET or Master Clear
2) Set First/Last Flip-Flop
3) Clear First/Last Flip-Flop

These software commands must occur sequentially with no communication to or from the 82C237 between commands. Once in 16-bit mode, the device will remain in this mode until a hardware RESET or Master Clear sets it back to normal (8-bit) transfer mode. If this initialization sequence is not followed exactly, the 82C237 will operate exactly like the 82C37A or the 82C237 in normal 8-bit mode.

16-Bit DMA Transfers - In 16-bit transfer mode, each DMA channel may be programmed to perform 8-bit or 16-bit transfers. Channels which are programmed to perform 8-bit transfers will operate like a normal 82C37A transfer. On channels programmed to perform 16-bit transfers, the Current Address register, which is normally incremented or decremented by one after each transfer, is incremented or decremented by two after each transfer. Also, the Current Word Count register, which is normally decremented by one after each transfer, is decremented by two after each transfer.

16-Bit Memory-to-Memory Transfers - 16-bit memory-to-memory transfers require an external latch to temporarily store the 8 most significant bits of data. When 16-bit transfer mode is enabled, Pin 5 (DWLE) becomes an active output which may be used to enable the external data latch during memory-to-memory operations. See Figure 9 for a 16-bit DMA application. Channels 0 and 1 operate as memory-to-memory transfer channels. IF either channel 0 or channel 1 is programmed to perform 16-bit transfers when a memory-to-memory transfer is initiated, the transfer will be a 16-bit transfer. If 8-bit memory-to-memory transfers are desired while the 82C237 is in 16-bit transfer mode, channels 0 and 1 must both be programmed for 8-bit transfers.

Pin 5 DWLE Output - When the 82C237 is initialized to 16-bit transfer mode, pin 5 is always high impedance three-stated. This insures compatibility with the 82C37A pin 5 description. In 16-bit transfer mode, this output becomes active and serves a dual purpose.

During the S1 cycle of a transfer, the DWLE output indicates the data width (0 = 16-bit, 1 = 8-bit) of the active channel. This signal may be used with the A0 output to generate a High Byte Enable signal for use in chip select decode logic. Since DWLE is a multiplexed pin, Data Width information needs to be captured in an external latch on the falling edge of ADSTB. See Figure 9 for a 16-bit DMA application.

During memory-to-memory transfer, the DWLE output is used to enable an external latch which temporarily stores the 8 most significant bits of data during the read-from-memory half of the transfer. DWLE enables this byte of data onto the data bus during the write-to-memory half of the transfer. See Figure 9 for a 16-bit DMA application.

If an active channel is cascaded, as defined by its mode register, DWLE will be driven low at the start of the transfer, and will remain low for the entire transfer. This allows the DWLE signal from the slave 82C237 to control the system. To form the system DWLE signal for cascaded 82C237s, simply "OR" the individual DWLE outputs of the Master and Slaves.

Registers Affected by 16-Bit Transfer Mode

Current Address Register - Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. On channels programmed to perform 8-bit DMA transfers, the address is automatically incremented or decremented by one after each transfer. On channels programmed for 16-bit DMA transfers, the address is automatically incremented or decremented by two after each transfer.

During all 16-bit transfers, the A0 output will remain low for the entire transfer, even if an odd address is programmed into the channel's Current Address register (i.e. only even word addresses will be generated).

The Current Address register is written or read by the microprocessor in successive 8-bit bytes. See Figure 6 for programming information. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an $\overline{EOP}$. In memory-to-memory mode, the channel 0 Current Address register can be prevented from incrementing or decrementing by setting the address hold bit in the Command register.

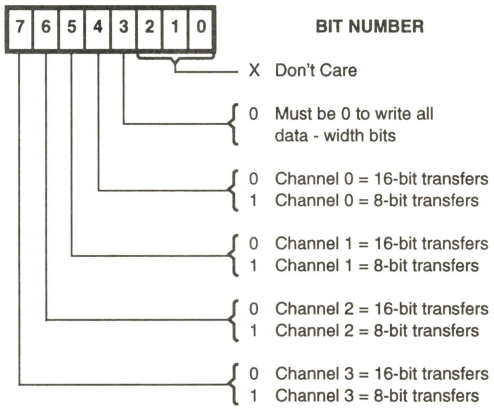
Current Word Count Register - Each channel has a 16-bit Current Word Count register. This register determines the number of transfers to be performed. On channels programmed for 8-bit transfers, the actual number of transfers will be one more than the number programmed in the Current Word Count register (i.e. programming a count of 100 will result in 101 transfers). The word count is decremented by one after each transfer on 8-bit transfer channels.

On channels programmed for 16-bit transfers, the word count is decremented by two after each transfer. This means that for even values in the Current Word Count register, the actual number of transfers will be n/2 + 1, where n is the value in the Current Word Count register. For odd values in this register, the actual number of transfers will be (n+1)/2. When the value in the Current Word Count register decrements past zero (i.e. 0 to FFFEH or 1 to FFFFH), a TC will be generated.

This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. See Figure 6 for programming information. Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialization can occur only when an $\overline{EOP}$ occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC on 8-bit transfers, or FFFEH after TC on 16-bit transfers.

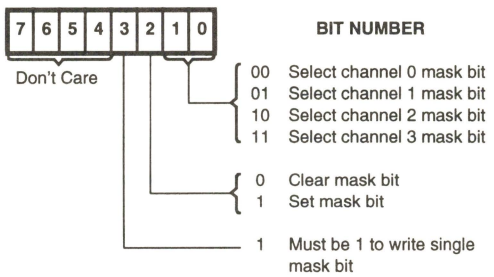
Data-Width Register - When 16-bit transfer mode is enabled, the Data-Width register becomes accessible and is used to program each DMA channel to perform either 8-bit transfers or 16-bit transfers. Data bits 4-7 represent DREQ channels 0-3 respectively and determine the data width (8-bit or 16-bit) of each channel during DMA transfers. When programming this register, bit 3 of the data must be set to "0". Since the address of the Data-Width register is the same as the Mask register, bit 3 selects which register is actually written.

Data-Width Register - 16-bit transfer mode enabled



Mask Register - In 16-bit transfer mode this register operates the same as the previous Mask register description with the exception of bit 3 when writing the instruction to separately set or clear a mask bit. Bit 3 of the data must be "1" when writing a single mask bit. Bits 4-7 are ignored when this instruction is written. Refer to the following diagram for writing single mask bits.

Mask Register - 16-bit transfer mode enabled



The software command to write all four bits of the Mask register has no effect on the state of the Data-Width bits.

When reading the Mask/Data-Width register (they share the same address), bits 0-3 will always display the mask bits of channels 0-3, respectively. With 16-bit transfer mode not enabled, bits 4-7 will always read as logical ones. With 16-bit transfer mode enabled, bits 4-7 will display the data-width bits for channels 0-3 respectively.

The Mask and Data-Width registers are set by RESET or Master Clear. This disables all hardware DMA requests until a clear mask bit instruction allows them to be recognized. RESET or Master Clear forces the Mask and Data-Width

registers to operate as in normal mode (Data-Width register not accessible) until 16-bit transfer mode is again entered. The four mask bits may also be cleared simultaneously by using the Clear Mask Register command (see software commands section). This command has no effect on the data-width bits.

Temporary Register - The internal Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last byte moved can be read by the microprocessor. In the case of 16-bit transfers, only the least significant 8-bits of the last word transferred are stored in this register. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a RESET or Master Clear.

Software Commands Affected by 16-Bit Mode

Master Clear - This software instruction has the same effect as the hardware RESET. The Command, Status, Request, and Temporary registers, and Internal First/Last Flip-Flop and mode register counter are cleared and the Mask register is set. When the Master Clear instruction occurs while in 16-bit transfer mode, the 82C237 enters normal (8-bit) transfer mode in the Idle cycle.

Clear Mask Register - This command clears the mask bits of all four channels, enabling them to accept DMA requests. This command has no effect on data-width bits in 16-bit transfer mode.

OPERATION	A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$
Read Status Register	1	0	0	0	0	1
Write Command Register	1	0	0	0	1	0
Read Request Register	1	0	0	1	0	1
Write Request Register	1	0	0	1	1	0
Read Command Register	1	0	1	0	0	1
Write Single Mask Bit (Note 1)	1	0	1	0	1	0
Write All Data-Width Bits (Notes 1, 2)	1	0	1	0	1	0
Read Mode Register	1	0	1	1	0	1
Write Mode Register	1	0	1	1	1	0
Set First/Last F/F	1	1	0	0	0	1
Clear First/Last F/F	1	1	0	0	1	0
Read Temporary Register	1	1	0	1	0	1
Master Clear	1	1	0	1	1	0
Clear Mode Reg. Counter	1	1	1	0	0	1
Clear Mask Register	1	1	1	0	1	0
Read All Mask/Data-Width Bits (Note 2)	1	1	1	1	0	1
Write All Mask Bits	1	1	1	1	1	0

NOTES:

1. The register to be written is determined by data bit 3.
2. Data-Width bits exist in 82C237, 16-bit mode only.

FIGURE 5. 16-BIT MODE SOFTWARE COMMAND CODES AND REGISTER CODES

CHANNEL	REGISTER	OPERATION	SIGNALS							FIRST/LAST FLIP-FLOP STATE	DATA BUS DB0-DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15

FIGURE 6. WORD COUNT AND ADDRESS REGISTER COMMAND CODES

Application Information

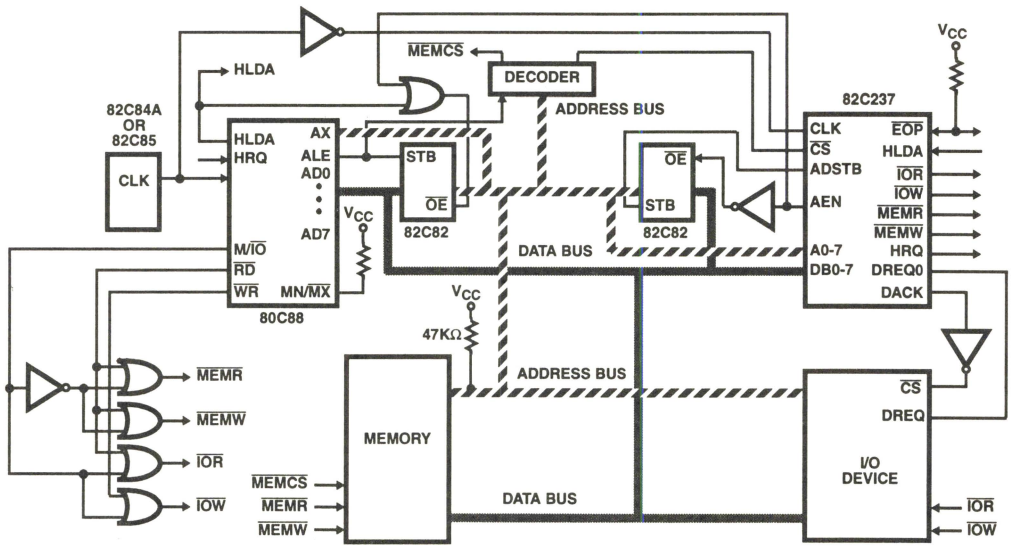
Figure 7 shows an application for a DMA system utilizing the 82C237 DMA controller and the 80C88 Microprocessor. In this application, the 82C237 DMA controller is used to improve system performance by allowing an I/O device to transfer data directly to or from system memory.

Components

The system clock is generated by the 82C84A clock driver and is inverted to meet the clock high and low times required by the 82C237 DMA controller. The four OR gates are used to support the 80C88 Microprocessor in minimum mode by producing the control signals used by the processor to access memory or I/O. A decoder is used to generate chip select for the DMA controller and memory. The most significant bits of the address are output on the address/data bus. Therefore, the 82C82 octal latch is used to demultiplex the address. Hold Acknowledge (HLDA) and Address Enable (AEN) are "ORed" together to insure that the DMA controller does not have bus contention with the microprocessor.

Operation

A DMA request (DREQ) is generated by the I/O device. After receiving the DMA request, the DMA controller will issue a Hold request (HRQ) to the processor. The system busses are not released to the DMA controller until a Hold Acknowledge signal is returned to the DMA controller from the 80C88 processor. After the Hold Acknowledge has been received, addresses and control signals are generated by the DMA controller to accomplish the DMA transfers. Data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active. Note that data is not read into or driven out of the DMA controller in I/O-to-memory or memory-to-I/O data transfers.



NOTE: The address lines need pull-up resistors.

FIGURE 7. APPLICATION FOR DMA SYSTEM

Figure 8 shows an application for a DMA system using the 82C237 DMA controller and the 80C286 Microprocessor.

In this application, the system clock comes from the 82C284 clock generator PCLK signal which is inverted to provide proper READY setup and hold times to the DMA controller in an 80C286 system. The Read and Write signals from the DMA controller may be wired directly to the Read/Write control signals from the 82C288 Bus Controller. The octal latch for A8-A15 from the DMA controller's data bus is on the local 80C286 address bus so that memory chip selects may still be generated during DMA transfers. The transceiver on A0-A7 is controlled by AEN and is not necessary, but may be used to drive a heavily loaded system address bus during transfers. The data bus transceivers simply isolate the DMA controller from the local microprocessor bus and allow programming on the upper or lower half of the data bus.

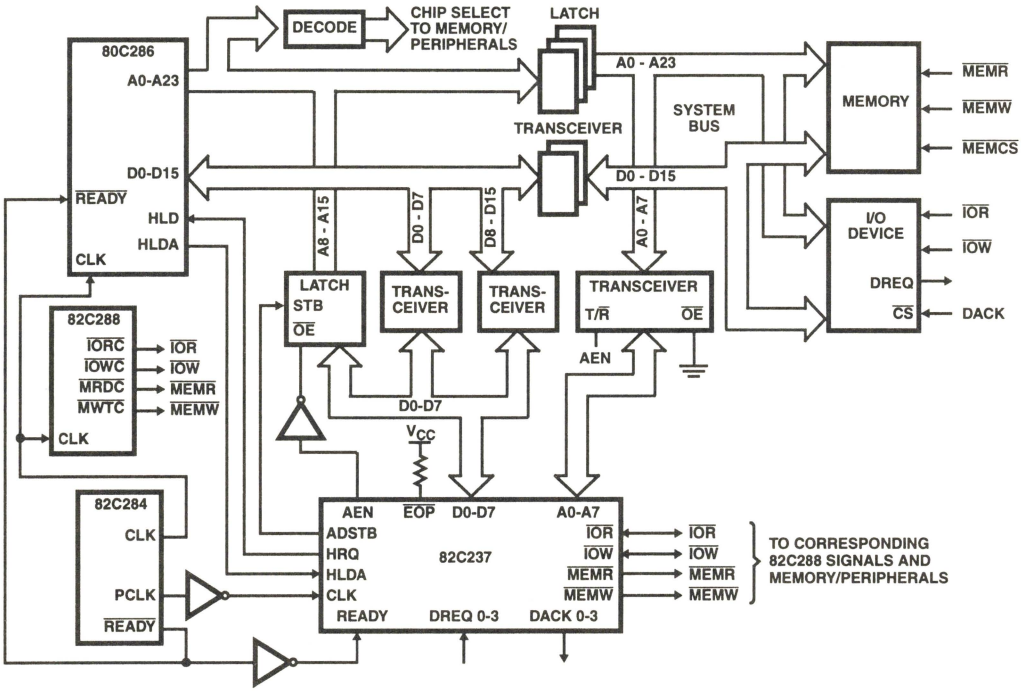
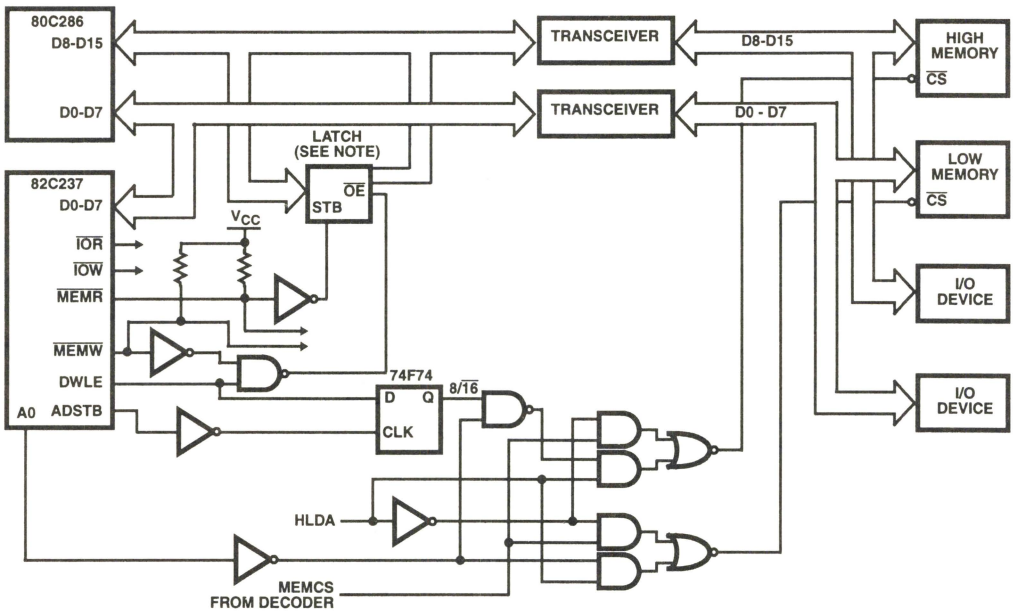


FIGURE 8. 80C286 DMA APPLICATION

Figure 9 shows the data bus for a 16-bit DMA application with the 82C237. High memory and low memory are selected accordingly with A0 and the 8/16 signal during DMA transfers. The 8/16 signal is formed from DWLE with a D flip-flop and ADSTB. ADSTB must be inverted to the D flip-flop since DWLE is set up to the falling edge of ADSTB and the 74F74 latches data on the rising edge of CLK.

The ADSTB inverted could be eliminated by using a 74F75 falling edge D latch. The latch on D8-D15 is needed for 16-bit memory-to-memory transfers. The upper eight bits of data are latched by $\overline{MEMR}$ during the read half of the transfer. The data is then enabled onto the data bus during the write half of the transfer.



NOTE: Only needed for memory-to-memory transfers.

FIGURE 9. DATA BUS FOR 16-BIT DMA APPLICATION

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C237 . . . . . 0°C to +70°C
I82C237 . . . . . -40°C to +85°C
M82C237 . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	50	10
CLCC Package	65	14
PDIP Package	55	N/A
PLCC Package	50	N/A

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature Ceramic Package . . . . . +175°C
Maximum Junction Temperature Plastic Package . . . . . +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
Ceramic Package
Maximum Lead Temperature (Soldering 10s) . . . . . +260°C
Plastic Package

Die Characteristics

Gate Count . . . . . 2325 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = +5.0 ±10%, T_A = 0°C to +70°C (C82C237)
T_A = -40°C to +85°C (I82C237)
T_A = -55°C to +125°C (M82C237)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2	-	V	C82C237, I82C237
		2.2	-	V	M82C237
VIL	Logical Zero Input Voltage	-	0.8	V	
VIHC	CLK Input Logical One Voltage	V_{CC} -0.8	-	V	
VILC	CLK Input Logical Zero Voltage	-	0.8	V	
VOH	Output HIGH Voltage	3.0	-	V	IOH = -2.5mA
		V_{CC} -0.4	-	V	IOH = -100µA
VOL	Output LOW Voltage	-	0.4	V	IOL = +2.5mA all output except $\overline{EOP}$, IOL = +3.2mA for $\overline{EOP}$ pin 36 only.
II	Input Leakage Current	-1	+1	µA	VIN = GND or V_{CC}, Pins 6, 7, 11-13, 16-19
IO	Output Leakage Current	-10	+10	µA	VOUT = GND or V_{CC}, Pins 1-5, 21-23, 26-30, 32-40
ICCSB	Standby Power Supply Current	-	10	µA	V_{CC} = 5.5V, VIN = V_{CC} or GND, Outputs Open
ICCOP	Operating Power Supply Current	-	2	mA/MHz	V_{CC} = 5.5V, CLK FREQ = Maximum, VIN = V_{CC} or GND, Outputs Open

Capacitance

T_A = +25°C

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
CIN	Input Capacitance	25	pF	FREQ = 1MHz, All measurements are referenced to device GND
COUT	Output Capacitance	40	pF	
CI/O	I/O Capacitance	25	pF	

AC Electrical Specifications

V_{CC} = +5.0V ±10%, GND = 0V, T_A = 0°C to +70°C (C82C237),
T_A = -40°C to +85°C (I82C237),
T_A = -55°C to +125°C (M82C237)

SYMBOL	PARAMETER	82C237		82C237-12		UNITS
		MIN	MAX	MIN	MAX	
DMA (MASTER) MODE						
(1)TAEL	AEN HIGH from CLK LOW (S1) Delay Time	-	105	-	50	ns
(2)TAET	AEN LOW from CLK HIGH (SI) Delay Time	-	80	-	50	ns
(3)TAFAB	ADR Active to Float Delay from CLK HIGH	-	55	-	55	ns
(4)TAFC	$\overline{READ}$ or $\overline{WRITE}$ Float Delay from CLK HIGH	-	75	-	50	ns
(5)TAFDB	DB Active to Float Delay from CLK HIGH	-	135	-	90	ns
(6)TAHR	ADR from $\overline{READ}$ HIGH Hold Time	TCY-75	-	TCY-65	-	ns
(7)TAHS	DB from ADSTB LOW Hold Time	TCL-18	-	TCL-18	-	ns
(8)TAHW	ADR from $\overline{WRITE}$ HIGH Hold Time	TCY-65	-	TCY-50	-	ns
(9)TAK	DACK Valid from CLK LOW Delay Time	-	105	-	69	ns
	$\overline{EOP}$ HIGH from CLK HIGH Delay Time	-	105	-	90	ns
	$\overline{EOP}$ LOW from CLK HIGH Delay Time	-	60	-	35	ns
(10)TASM	ADR Stable from CLK HIGH	-	60	-	50	ns
(11)TASS	DB to ADSTB LOW Setup Time	TCH-20	-	TCH-20	-	ns
(12)TCH	CLK HIGH Time (Transitions 10ns)	55	-	30	-	ns
(13)TCL	CLK LOW Time (Transitions 10ns)	43	-	30	-	ns
(14)TCY	CLK Cycle Time	125	-	80	-	ns
(15)TDCL	CLK HIGH to $\overline{READ}$ or $\overline{WRITE}$ LOW Delay	-	130	-	120	ns
(16)TDCTR	$\overline{READ}$ HIGH from CLK HIGH (S4) Delay Time	-	115	-	80	ns
(17)TDCTW	$\overline{WRITE}$ HIGH from CLK HIGH (S4) Delay Time	-	80	-	70	ns
(18)TDQ	HRQ Valid from CLK HIGH Delay Time	-	75	-	30	ns
(19)TEPH	$\overline{EOP}$ Hold Time from CLK LOW (S2)	90	-	50	-	ns
(20)TEPS	$\overline{EOP}$ LOW to CLK LOW Setup Time	25	-	0	-	ns
(21)TEPW	$\overline{EOP}$ Pulse Width	135	-	50	-	ns
(22)TFAAB	ADR Valid Delay from CLK HIGH	-	60	-	50	ns
(23)TFAC	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK HIGH	-	90	-	50	ns
(24)TFADB	DB Valid Delay from CLK HIGH	-	60	-	45	ns
(25)THS	HLDA Valid to CLK HIGH Setup Time	45	-	10	-	ns
(26)TIDH	Input Data from $\overline{MEMR}$ HIGH Hold Time	0	-	0	-	ns
(27)TIDS	Input Data to $\overline{MEMR}$ HIGH Setup Time	90	-	45	-	ns
(28)TODH	Output Data from $\overline{MEMW}$ HIGH Hold Time	15	-	TCY-50	-	ns
(29)TODV	Output Data Valid to $\overline{MEMW}$ HIGH	TCY-35	-	TCY-10	-	ns
(30)TQS	DREQ to CLK LOW (SI, S4) Setup Time	0	-	0	-	ns
(31)TRH	CLK to READY LOW Hold Time	20	-	10	-	ns
(32)TRS	READY to CLK LOW Setup Time	35	-	15	-	ns
(33)TCLSH	ADSTB HIGH from CLK LOW Delay Time	-	70	-	70	ns
(34)TCLSL	ADSTB LOW from CLK LOW Delay Time	-	120	-	60	ns

AC Electrical Specifications V_{CC} = +5.0V ±10%, GND = 0V, T_A = 0°C to +70°C (C82C237), T_A = -40°C to +85°C (I82C237), T_A = -55°C to +125°C (M82C237) **(Continued)**

SYMBOL	PARAMETER	82C237		82C237-12		UNITS
		MIN	MAX	MIN	MAX	
(35)TWRRD	$\overline{READ}$ HIGH Delay from $\overline{WRITE}$ HIGH	0	-	5	-	ns
(36)TRLRH	$\overline{READ}$ Pulse Width, Normal Timing	2TCY-60	-	2TCY-55	-	ns
(37)TSHSL	ADSTB Pulse Width	TCY-50	-	TCY-35	-	ns
(38)TWLWHA	Extended $\overline{WRITE}$ Pulse Width	2TCY-85	-	2TCY-80	-	ns
(39)TWLWH	$\overline{WRITE}$ Pulse Width	TCY-85	-	TCY-80	-	ns
(40)TRLRHC	$\overline{READ}$ Pulse Width, Compressed	TCY-60	-	TCY-55	-	ns
(56)TAVRL	ADR Valid to $\overline{READ}$ LOW	17	-	17	-	ns
(57)TAVWL	ADR Valid to $\overline{WRITE}$ LOW	7	-	7	-	ns
(58)TRHAL	$\overline{READ}$ HIGH to AEN LOW	15	-	15	-	ns
(59)TRHSH	$\overline{READ}$ HIGH to ADSTB HIGH	13	-	13	-	ns
(60)TWHSH	$\overline{WRITE}$ HIGH to ADSTB HIGH	15	-	15	-	ns
(61)TDVRL	DACK Valid to $\overline{READ}$ LOW	25	-	25	-	ns
(62)TDVWL	DACK Valid to $\overline{WRITE}$ LOW	25	-	25	-	ns
(63)TRHDI	$\overline{READ}$ HIGH to DACK Inactive	12	-	12	-	ns
(64)TAZRL	ADR Float to $\overline{READ}$ LOW	-2.5	-	-2.5	-	ns
(65)TOEV	Output Enable Valid Before $\overline{WRITE}$ HIGH	TCY+20	-	TCY+20	-	ns
(66)TOEH	Output Enable Hold Time from $\overline{WRITE}$ HIGH	TCY-50	-	TCY-50	-	ns
PERIPHERAL (SLAVE) MODE						
(41)TAR	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	10	-	0	-	ns
(42)TAWL	ADR Valid to $\overline{WRITE}$ LOW Setup Time	0	-	0	-	ns
(43)TCWL	$\overline{CS}$ LOW to $\overline{WRITE}$ LOW Setup Time	0	-	0	-	ns
(44)TDW	Data Valid to $\overline{WRITE}$ HIGH Setup Time	100	-	60	-	ns
(45)TRA	ADR or $\overline{CS}$ Hold from $\overline{READ}$ HIGH	0	-	0	-	ns
(46)TRDE	Data Access from $\overline{READ}$	-	120	-	80	ns
(47)TRDF	DB Float Delay from $\overline{READ}$ HIGH	5	85	5	55	ns
(48)TRSTD	Power Supply HIGH to RESET LOW Setup Time	500	-	500	-	ns
(49)TRSTS	RESET to First $\overline{IOR}$ or $\overline{IOW}$	2TCY	-	2TCY	-	ns
(50)TRSTW	RESET Pulse Width	300	-	300	-	ns
(51)TRW	$\overline{READ}$ Pulse Width	155	-	85	-	ns
(52)TWA	ADR from $\overline{WRITE}$ HIGH Hold Time	0	-	0	-	ns
(53)TWC	$\overline{CS}$ HIGH from $\overline{WRITE}$ HIGH Hold Time	0	-	0	-	ns
(54)TWD	Data from $\overline{WRITE}$ HIGH Hold Time	10	-	10	-	ns
(55)TWWS	$\overline{WRITE}$ Pulse Width	100	-	45	-	ns

Timing Waveforms

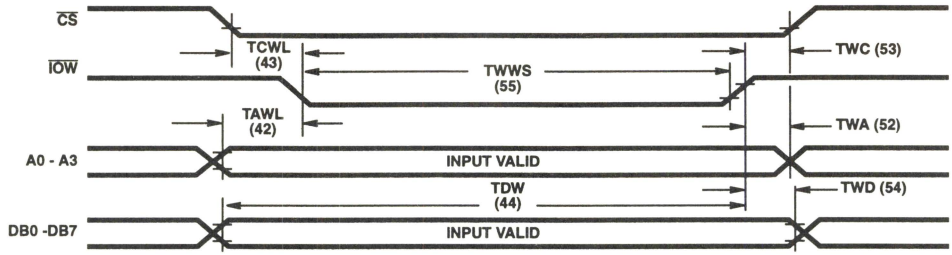


FIGURE 10. SLAVE MODE WRITE

NOTE: Successive WRITE accesses to the 82C237 must allow at least TCY as recovery time between accesses. A TCY recovery time must be allowed before executing a WRITE access after a READ access.

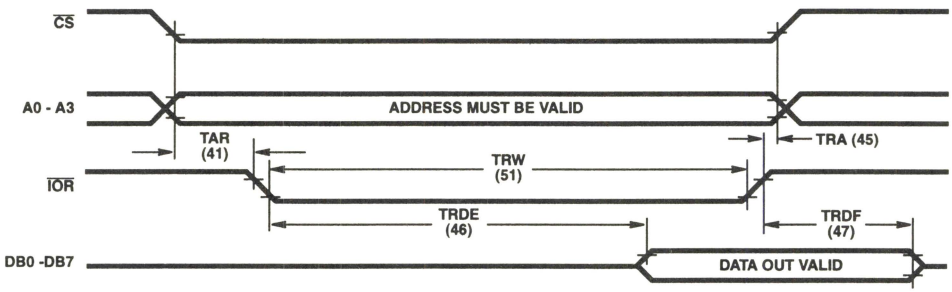


FIGURE 11. SLAVE MODE READ

NOTE: Successive READ accesses to the 82C237 must allow at least TCY as recovery time between accesses. A TCY recovery time must be allowed before executing a READ access after a WRITE access.

Timing Waveforms (Continued)

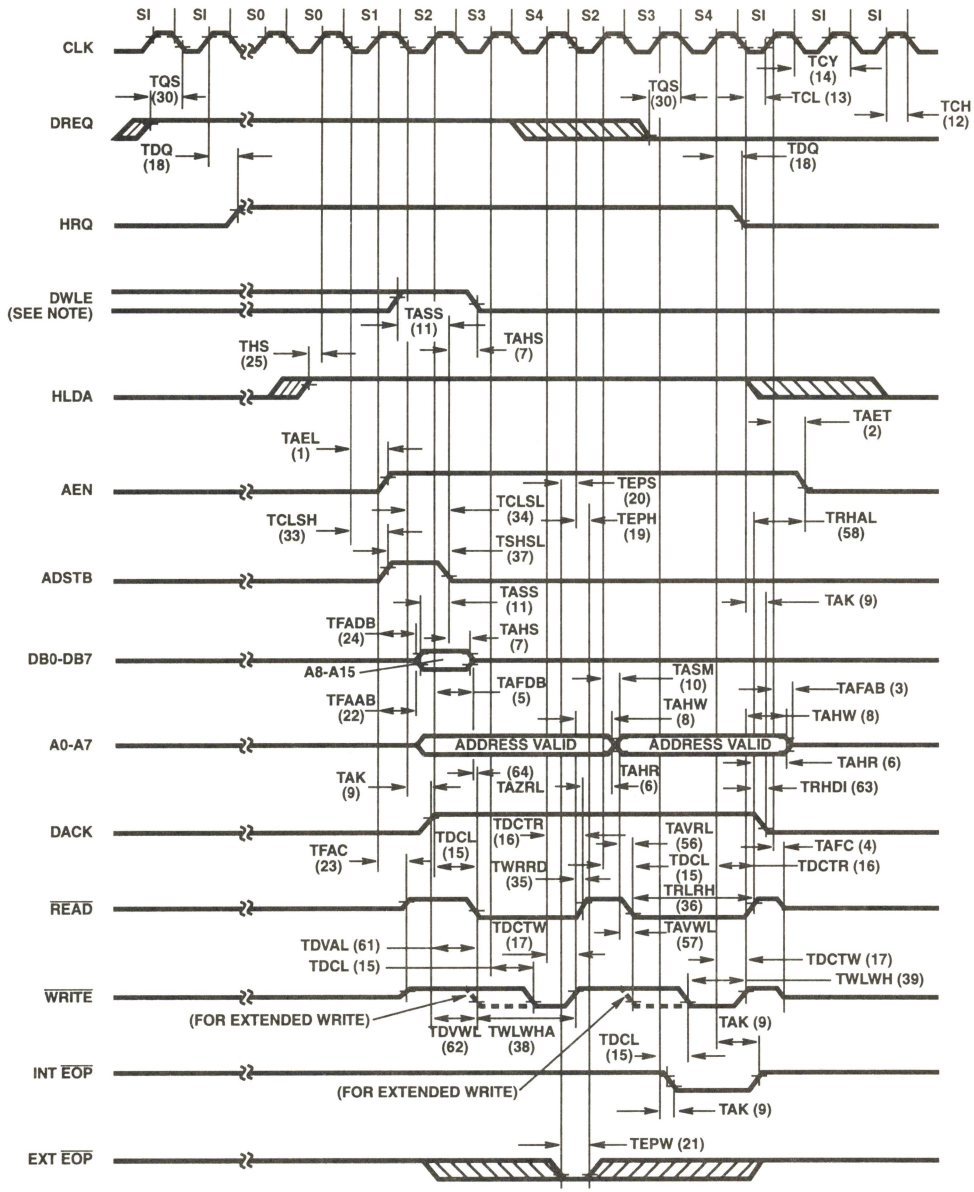


FIGURE 12. DMA TRANSFER

NOTE: For 16-bit mode, 82C237 only. In 8-bit mode this signal is always high impedance three-stated. Waveform shown is for an 8-bit transfer with the 82C237 programmed in 16-bit mode. For a 16-bit transfer, DWLE will go low at least TASS before the falling edge of ADSTB in S2, and remain low for the entire transfer.

Timing Waveforms (Continued)

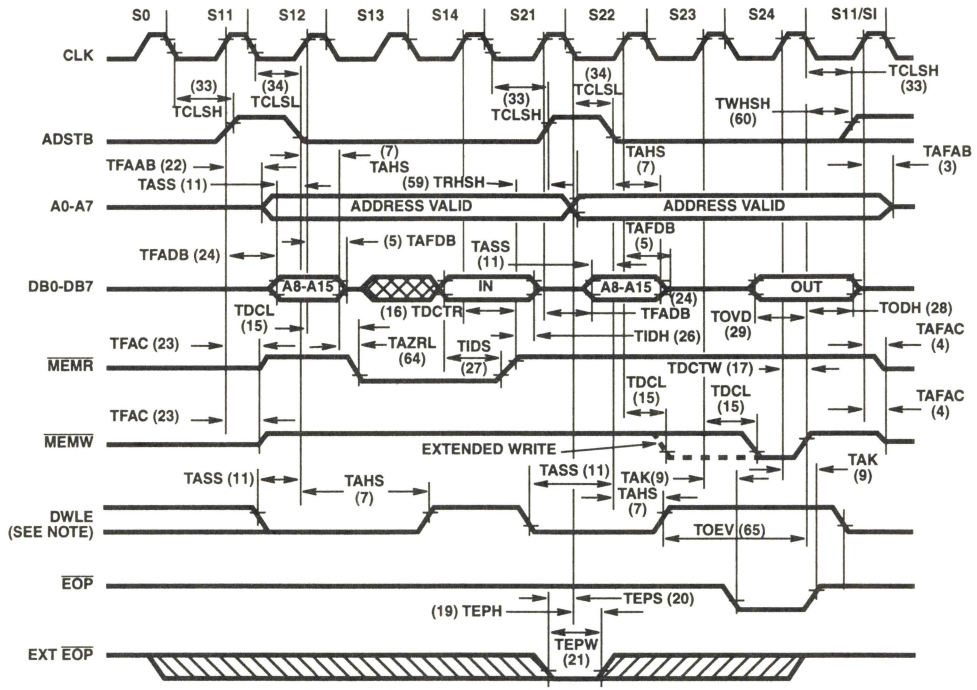


FIGURE 13. MEMORY-TO-MEMORY TRANSFER

NOTE: For 16-bit mode, 82C237 only. In 8-bit mode this signal is always high impedance three-stated. Waveform shown is for a 16-bit memory-to-memory transfer. For an 8-bit transfer in 16-bit mode, DWLE will go high at least TASS before the falling edge of ADSTB in S2, then low TAHS after the falling edge of ADSTB, and will remain low until the next ADSTB where the cycle is repeated.

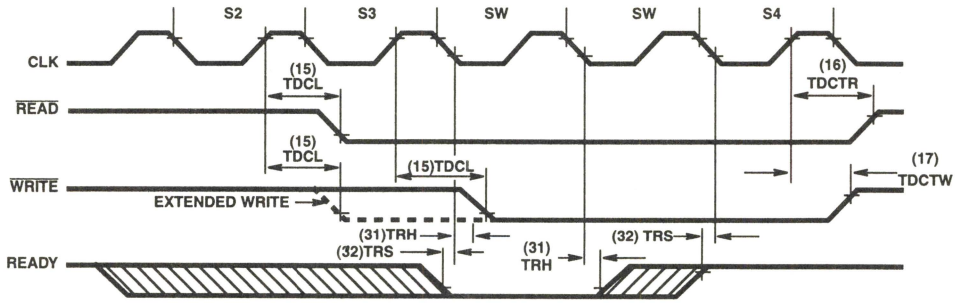


FIGURE 14. READY

NOTE: READY must not transition during the specified setup and hold times.

Timing Waveforms (Continued)

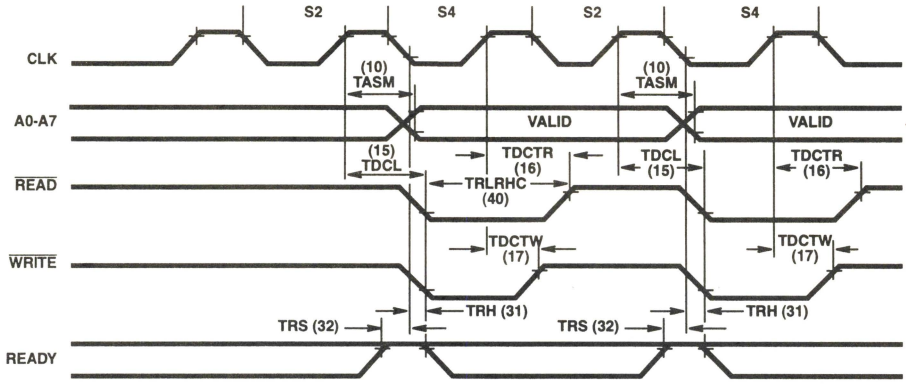


FIGURE 15. COMPRESSED TRANSFER

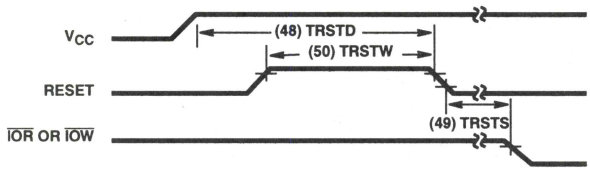
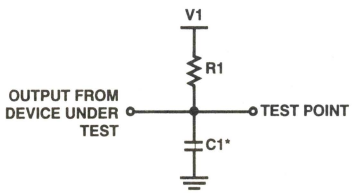


FIGURE 16. RESET

AC Test Circuits

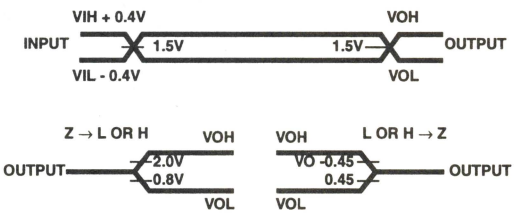


* Includes STRAY and FIXTURE Capacitance

TEST CONDITION DEFINITION TABLE

PINS	V1	R1	C1
All Outputs Except $\overline{EOP}$	1.7V	520Ω	100pF
$\overline{EOP}$	V_{CC}	1.6KΩ	50pF

AC Testing Input, Output Waveforms



NOTE: AC Testing: All AC Parameters tested as per test circuits. Input RISE and FALL times are driven at Ins/V. CLK input must switch between VIHC +0.4V and VILC -0.4V

Die Characteristics

DIE DIMENSIONS:
148 x 159 x 19 ±1mils

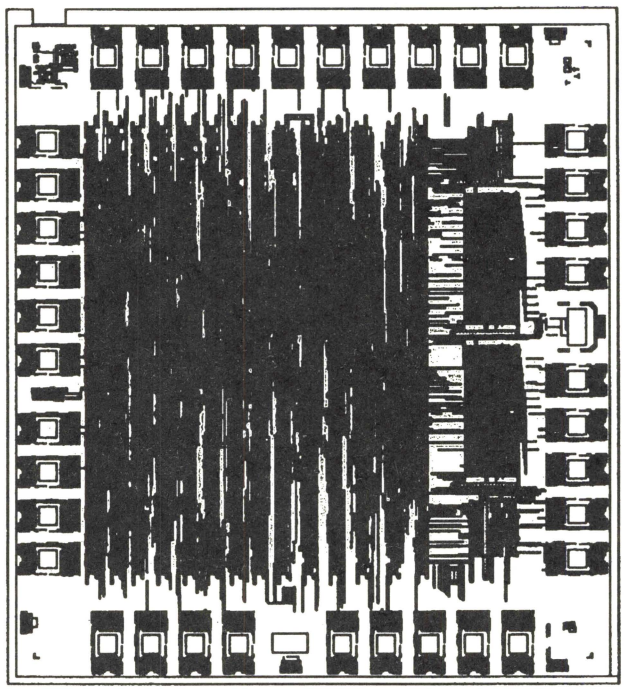
METALLIZATION:
Type: 51Al
Thickness: 8kÅ ± 0.75kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ ± 3kÅ

WORST CASE CURRENT DENSITY:
0.6×10^5 A/cm^2

Metallization Mask Layout

82C237



82C284

Clock Generator and Ready Interface for 80C286 Processors

March 1997

Features

- Generates System Clock for 80C286 Processors
- Generates System Reset Output from Schmitt Trigger Input
  - Improved Hysteresis
- Uses Crystal or External Signal for Frequency Source
- Dynamically Switchable between Two Input Frequencies
- Provides Local $\overline{\text{READY}}$ and MULTIBUS® $\overline{\text{READY}}$ Synchronization
- Static CMOS Technology
- Single +5V Power Supply
- Available in 18 Lead CerDIP Package

Description

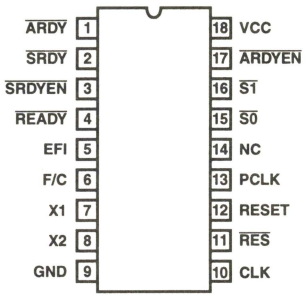
The Harris 82C284 is a clock generator/driver which provides clock signals for 80C286 processors and support components. It also contains logic to supply $\overline{\text{READY}}$ to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis.

Ordering Information

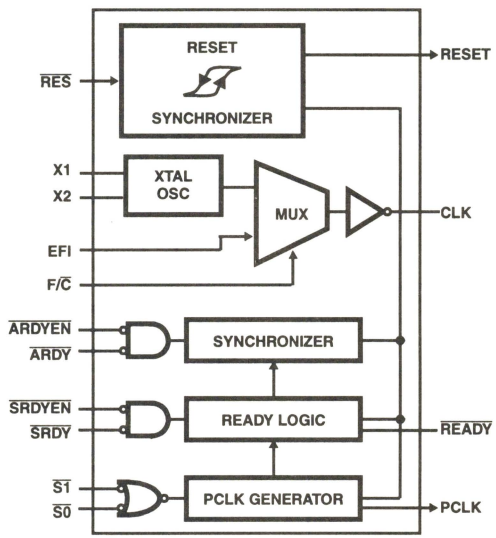
PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
CD82C284-12	0°C to +70°C	18 Ld CERDIP	F18.3
ID82C284-10	-40°C to +85°C	18 Ld CERDIP	F18.3
ID82C284-12	-40°C to +85°C	18 Ld CERDIP	F18.3

Pinout

82C284 (CERDIP)
TOP VIEW



Functional Diagram



4 CMOS PERIPHERALS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Copyright © Harris Corporation 1997

MULTIBUS® is a patented Intel bus.

File Number **2966.1**

Pin Description The following pin function descriptions are for the 82C284 clock generator.

PIN SYMBOL	NUMBER	TYPE	DESCRIPTION
CLK	10	O	SYSTEM CLOCK: the signal used by the processor and support devices which must be synchronous with the processor. The frequency of the CLK output has twice the desired internal processor clock frequency. CLK can drive both TTL and CMOS level inputs.
F/$\overline{C}$	6	I	FREQUENCY/CRYSTAL SELECT: this pin selects the source for the CLK output. When there is a LOW level on this input, the internal crystal oscillator drives CLK. When there is a HIGH level on F/$\overline{C}$, the EFI input drives the CLK input. This pin can be dynamically switched, which allows changing the processor CLK frequency while running for low-power operation, etc.
X1, X2	7, 8	I	CRYSTAL IN: the pin stop which parallel resonant, fundamental mode crystal is attached for the internal oscillator. When F/$\overline{C}$ is LOW, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the desired internal processor clock frequency.
EFI	5	I	EXTERNAL FREQUENCY IN: drives CLK when the F/$\overline{C}$ input is HIGH. The EFI input frequency must be twice the desired internal processor clock frequency.
PCLK	13	O	PERIPHERAL CLOCK: the output which provides a 50% duty cycle clock with one-half the frequency of CLK. PCLK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.
$\overline{\text{ARDYEN}}$	17	I	ASYNCHRONOUS READY ENABLE: an active LOW input which qualifies the $\overline{\text{ARDY}}$ input. $\overline{\text{ARDYEN}}$ selects $\overline{\text{ARDY}}$ as the source of $\overline{\text{READY}}$ for the current bus cycle. Inputs to $\overline{\text{ARDYEN}}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous outputs.
$\overline{\text{ARDY}}$	1	I	ASYNCHRONOUS READY: an active LOW input used to terminate the current bus cycle. The $\overline{\text{ARDY}}$ input is qualified by $\overline{\text{ARDYEN}}$. Inputs to $\overline{\text{ARDY}}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous outputs.
$\overline{\text{SRDYEN}}$	3	I	SYNCHRONOUS READY ENABLE: an active LOW input which qualifies $\overline{\text{SRDY}}$. $\overline{\text{SRDYEN}}$ selects $\overline{\text{SRDY}}$ as the source for $\overline{\text{READY}}$ to the CPU for the current bus cycle. Setup and hold time must be satisfied for proper operation.
$\overline{\text{SRDY}}$	2	I	SYNCHRONOUS READY: an active LOW input used to terminate the current bus cycle. The $\overline{\text{SRDY}}$ input is qualified by the $\overline{\text{SRDYEN}}$ input. Setup and hold time must be satisfied for proper operation.
$\overline{\text{READY}}$	4	O	READY: an active LOW output which signals to the processor that the current bus cycle is to be completed. The $\overline{\text{SRDY}}$ $\overline{\text{SRDYEN}}$, $\overline{\text{ARDY}}$, $\overline{\text{ARDYEN}}$, $\overline{\text{S1}}$, $\overline{\text{S0}}$, and $\overline{\text{RES}}$ inputs control $\overline{\text{READY}}$ as explained later in the $\overline{\text{READY}}$ generator section. $\overline{\text{READY}}$ is an open drain output requiring an external pull-up resistor.
$\overline{\text{S0}}$, $\overline{\text{S1}}$	15,16	I	STATUS: these inputs prepare the 82C284 for a subsequent bus cycle. $\overline{\text{S0}}$ and $\overline{\text{S1}}$ synchronize PCLK to the internal processor clock and control READY. Setup and hold times must be satisfied for proper operation
RESET	12	O	RESET: an active HIGH output which is derived from the $\overline{\text{RES}}$ input RESET is used to force the system into an initial state. When RESET is active, $\overline{\text{READY}}$ will be active (LOW).
$\overline{\text{RES}}$	11	I	RESET IN: an active LOW input which generates the system reset signal (RESET). Signals to $\overline{\text{RES}}$ may be applied asynchronously to CLK. A Schmitt trigger input is provided on $\overline{\text{RES}}$, so that an RC circuit can be used to provide a time delay. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
V_{CC}	18		SYSTEM POWER: The +5V Power Supply Pin. A 0.1μF capacitor between V_{CC} and GND is recommended for decoupling.
GND	9		SYSTEM GROUND: 0V

Functional Description

Introduction

The 82C284 generates the clock, ready, and reset signals required for 80C286 processors and support components. The 82C284 is packaged in an 18-pin DIP and contains a crystal controlled oscillator, clock generator, peripheral clock generator, MULTIBUS® ready synchronization logic, and system reset generation logic.

Clock Generator

The CLK output provides the basic timing control for an 80C286 system. CLK has output characteristics sufficient to drive CMOS devices. CLK is generated by either an internal crystal oscillator, or an external source as selected by the F/$\overline{C}$ input pin. When F/$\overline{C}$ is LOW, the crystal oscillator drives the CLK output. When F/$\overline{C}$ is HIGH, the EFI input drives the CLK output.

The F/$\overline{C}$ pin on the Harris 82C284 is dynamically switchable. This allows the CLK frequency to the processor to be changed from one frequency to another in a running system. With this feature, a system can be designed which operates at maximum speed when needed, and then dynamically switched to a lower frequency to implement a low-power mode. The lower frequency can be anything down to, but excluding, DC. The following 3 conditions apply when dynamically switching the F/$\overline{C}$ pin (see Figure 1):

1) The CLK is stretched in the low portion of the ϕ2 phase of its cycle during transition from one CLK frequency to the other (see Waveforms).
2) When switching CLK frequency sources, there is a maximum transition latency of 2.5 clock cycles of the frequency being switched to, from the time CLK freezes low, until CLK restarts at the new frequency (see Waveforms).
3) The maximum latency from the time F/C is dynamically switched, to the time CLK freezes low, is 4 CLK cycles (see Waveforms).

The following steps describe the sequence of events that transpire when F/C is dynamically switched:

A) F/$\overline{C}$ switched from high (using EFI input) to low (using the crystal input X1 - see Figure 1A).
   1) The state of F/$\overline{C}$ is sampled when both CLK and PCLK are high until a change is detected.
   2) On the second following falling edge of PCLK, CLK is frozen low.
   3) CLK restarts at the crystal frequency on the rising edge of Xl, after the second falling edge of X1.

B) F/$\overline{C}$ switched from low (using the crystal input Xl) to high (using the EFI input - see Figure 1B).
   1) The state of F/C is sampled when both CLK and PCLK are high until a change is detected.
   2) On the second following falling edge of PCLK, CLK is frozen low.
   3) CLK restarts at the EFI input frequency on the falling edge of EFI after the second rising edge of EFI.

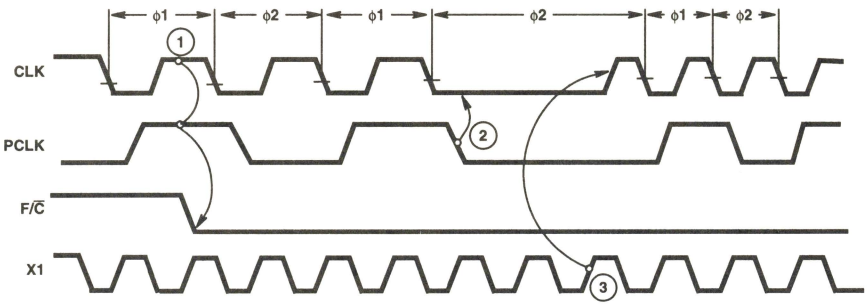


FIGURE 1A. F/$\overline{C}$ SWITCHED FROM HIGH (USING EFI INPUT) TO LOW (USING THE CRYSTAL INPUT X1)

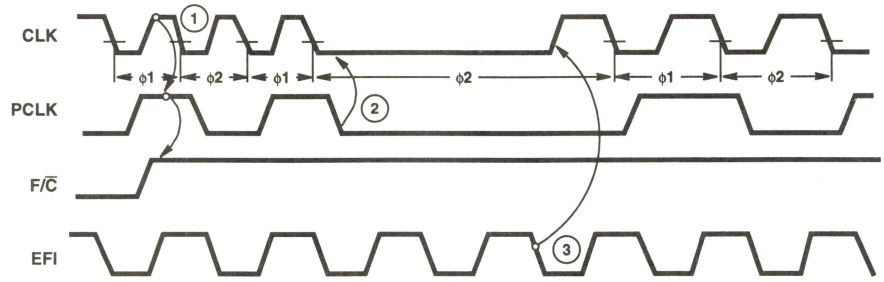


FIGURE 1B. F/C SWITCHED FROM LOW (USING THE CRYSTAL INPUT X1) TO HIGH (USING THE EFI INPUT)
FIGURE 1. DYNAMICALLY SWITCHING THE F/$\overline{C}$ PIN

The 82C284 provides a second clock output, PCLK, for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and CMOS output drive characteristics. PCLK is normally synchronized to the internal processor clock.

After reset, the PCLK signal may be out of phase with the internal processor clock. The $\overline{S1}$ and $\overline{S0}$ signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its HIGH time beyond one system clock (see waveforms). PCLK is forced HIGH whenever either $\overline{S0}$ or $\overline{S1}$ were active (LOW) for the two previous CLK cycles. PCLK continues to oscillate when both $\overline{S0}$ and $\overline{S1}$ are HIGH.

Since the phase of the internal processor clock will not change except during reset, the phase of PCLK will not change except during the first bus cycle after reset.

Oscillator

The oscillator circuit of the 82C284 is a linear Pierce oscillator which requires an external parallel resonant, fundamental mode, crystal. The output of the oscillator is internally buffered. The crystal frequency chosen should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32pF.

X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in Table 1. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10pF between the X1 and X2 pins. Decouple V_{CC} and GND as close to the 82C284 as possible with a 0.1μF polycarbonate capacitor.

TABLE 1. 82C284 CRYSTAL LOADING CAPACITANCE VALUES

CRYSTAL FREQUENCY	CI CAPACITANCE (PIN 7)	C2 CAPACITANCE (PIN 8)
1MHz to 8MHz	60pF	40pF
8MHz to 20MHz	25pF	15pF
20MHz to 25MHz	15pF	15pF

CLK Termination

Due to the CLK output having a very fast rise and fall time, it is recommended to properly terminate the CLK line at frequencies above 10MHz to avoid signal reflections and ringing. Termination is accomplished by inserting a small resistor (typically 10-74Ω) in series with the output, as shown in Figure 2. This is known as series termination. The resistor value plus the circuit output impedance (approximately 25Ω) should be made equal to the impedance of the transmission line.

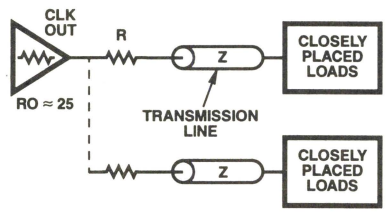


FIGURE 2. SERIES TERMINATION

Reset Operation

The reset logic provides the RESET output to force the system into a known, initial state. When the $\overline{RES}$ input is active (LOW), the RESET output becomes active (HIGH), $\overline{RES}$ is synchronized internally at the falling edge of CLK before generating the RESET output (see waveforms). Synchronization of the $\overline{RES}$ input introduces a one or two CLK delay before affecting the RESET Output.

At power up, a system does not have a stable V_{CC} and CLK. To prevent spurious activity, $\overline{RES}$ should be asserted until V_{CC} and CLK stabilize at their operating values. 80C286 processors and support components also require their RESET inputs be HIGH a minimum of 16 CLK cycles. An RC network, as shown in Figure 3, will keep $\overline{RES}$ LOW long enough to satisfy both needs.

A Schmitt trigger input with hysteresis on $\overline{RES}$ assures a single transition of RESET with an RC circuit on $\overline{RES}$. The hysteresis separates the input voltage level at which the circuit output switches from HIGH to LOW from the input voltage level at which the circuit output switches from LOW to HIGH. The $\overline{RES}$ HIGH to LOW input transition voltage is lower than the $\overline{RES}$

LOW to HIGH input transition voltage. As long as the slope of the $\overline{RES}$ input voltage remains in the same direction (increasing or decreasing) around the $\overline{RES}$ input transition voltage, the RESET output will make a single transition.

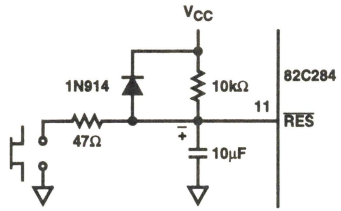


FIGURE 3. TYPICAL RC $\overline{RES}$ TIMING CIRCUIT

Ready Operation

The 82C284 accepts two ready sources for the system ready signal which terminates the current bus cycle. Either a synchronous ($\overline{SRDY}$) or asynchronous ready ($\overline{ARDY}$) source may be used. Each ready input has an enable ($\overline{SRDYEN}$ and $\overline{ARDYEN}$) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

$\overline{READY}$ is enabled (LOW), if either $\overline{SRDY}$ + $\overline{SRDYEN}$ = 0 or $\overline{ARDY}$ + $\overline{ARDYEN}$ = 0 when sampled by the 82C284 $\overline{READY}$ generation logic. $\overline{READY}$ will remain active for at least two CLK cycles.

The $\overline{READY}$ output has an open-drain driver allowing other ready circuits to be wired with it, as shown in Figure 4. The $\overline{READY}$ signal of an 80C286 system requires an external pull-up resistor. To force the $\overline{READY}$ signal inactive (HIGH) at the start of a bus cycle, the $\overline{READY}$ output floats when either $\overline{S1}$ or $\overline{S0}$ are sampled LOW at the falling edge of CLK. Two system clock periods are allowed for the pull-up resistor to pull the $\overline{READY}$ signal to V_{IH}. When RESET is active, $\overline{READY}$ is forced active one CLK later (see Waveforms).

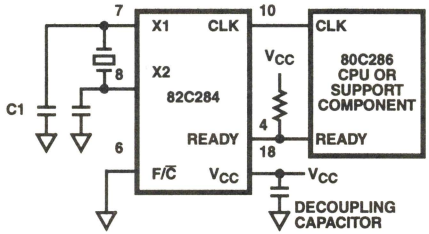


FIGURE 4. RECOMMENDED CRYSTAL AND $\overline{READY}$ CONDITIONS

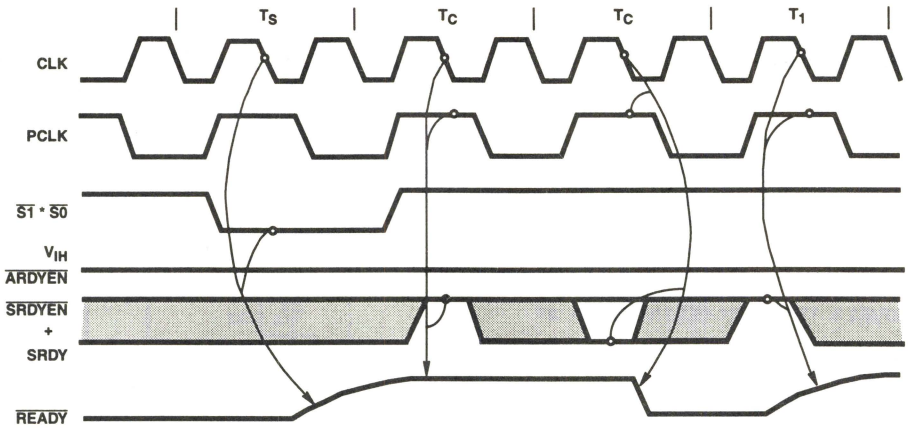


FIGURE 5. SYNCHRONOUS READY OPERATION

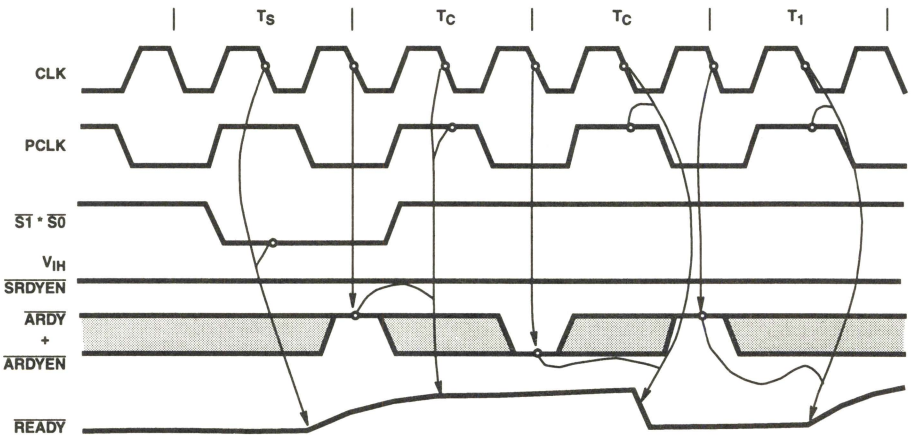


FIGURE 6. ASYNCHRONOUS READY OPERATION

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage Applied. . . . . GND -0.5V to V_{CC} +0.5V
Storage Temperature Range . . . . . -65°C to +150°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	80	20

Gate Count . . . . . 200 Gates
Junction Temperature . . . . . +175°C
Lead Temperature (Soldering, 10s) . . . . . +300°C
ESD Classification . . . . . Class 2

Operating Conditions

Operating Temperature Range
C82C284 . . . . . 0°C to +70°C
I82C284 . . . . . -40°C to +85°C

Operating Supply Voltage . . . . . +4.5V to +5.5V
EFI Rise Time (from 0.8V to 3.2V) . . . . . 8ns (Max)
EFI Fall Time (from 3.2 to 0.8V) . . . . . 8ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

T_A = 0°C to +70°C (CD82C284); V_{CC} = 5V ± 10%
T_A = -40°C to +85°C (ID82C284)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input LOW Voltage	-	0.8	V	V_{CC} = 4.5V
V_{IH}	Input HIGH Voltage	2.2	-	V	V_{CC} = 5.5V
V_{IHC}	EFI, F/$\overline{C}$ Input HIGH Voltage	3.2	-	V	V_{CC} = 5.5V
V_{IHR}	$\overline{RES}$ HIGH Voltage	V_{CC}-0.8	-	V	V_{CC} = 5.5V
V_{HYS}	$\overline{RES}$ Input Hysteresis	0.5	-	V	V_{CC} = 5.5V
V_{OL}	RESET, PCLK Output LOW Voltage	-	0.4	V	I_{OL} = 5mA, V_{CC} = 4.5V, Note 2
V_{OH}	RESET, PCLK Output HIGH Voltage	V_{CC}-0.4	-	V	I_{OH} = -1mA, V_{CC} = 4.5V, Note 2
V_{OLR}	$\overline{READY}$ Output LOW Voltage	-	0.4	V	I_{OL} = 10mA, V_{CC} = 4.5V, Note 2
V_{OLC}	CLK Output LOW Voltage	-	0.4	V	I_{OL} = 5mA, V_{CC} = 4.5V, Note 2
V_{OHC}	CLK Output HIGH Voltage	V_{CC}-0.4	-	V	I_{OH} = -5mA, V_{CC} = 4.5V, Note 2
I_{IL}	Input Leakage Current	-10	10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V
I_{CCOP}	Active Power Supply Current	-	60	mA	82C284-12 (Note 1)
		-	48	mA	82C284-10 (Note 1)

NOTES:

1. I_{CCOP} measured at 10MHz for 82C284-10 and at 12.5MHz for the 82C284-12. V_{IN} = GND or V_{CC}, V_{CC} = 5.5V outputs unloaded.
2. Interchanging of force and sense conditions is permitted.

AC Electrical Specifications

T_A = 0°C to +70°C (CD82C284); V_{CC} = 5V ±10%
T_A = -40°C to +85°C (ID82C284)
AC Timings are Referenced to 0.8V and 2.0V Points of the Signals as Illustrated in Waveforms, Unless Otherwise Noted.

SYMBOL	PARAMETER	10MHz		12.5MHz		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
t1	EFI LOW Time	20	-	16	-	ns	At V_{CC}/2 (Note 8)
t2	EFI HIGH Time	20	-	20	-	ns	At V_{CC}/2 (Note 8)
5A	Status Setup Time for Status Going Active	20	-	18	-	ns	
5B	Status Setup Time for Status Going Inactive	20	-	16	-	ns	

AC Electrical Specifications

$T_A = 0^oC$ to $+70^oC$ (CD82C284); $V_{CC} = 5V \pm 10\%$ **(Continued)**
$T_A = -40^oC$ to $+85^oC$ (ID82C284)
AC Timings are Referenced to 0.8V and 2.0V Points of the Signals as Illustrated in Waveforms, Unless Otherwise Noted.

SYMBOL	PARAMETER	10MHz		12.5MHz		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
t6	Status Hold Time	1	-	1	-	ns	
t7	F/$\overline{C}$ Setup Time	15	-	15	-		
t8	F/$\overline{C}$ Hold Time	15	-	15	-		
t9	$\overline{SRDY}$ or $\overline{SRDYEN}$ Setup Time	15	-	15	-	ns	
t10	$\overline{SRDY}$ or $\overline{SRDYEN}$ Hold Time	2	-	2	-	ns	
t11	$\overline{ARDY}$ or $\overline{ARDYEN}$ Setup Time	5	-	5	-	ns	(Note 3)
t12	$\overline{ARDY}$ or $\overline{ARDYEN}$ Hold Time	30	-	25	-	ns	(Note 3)
t13	$\overline{RES}$ Setup Time	20	-	18	-	ns	(Notes 3, 7)
t14	RES Hold Time	10	-	8	-	ns	(Notes 3, 7)
t16	CLK Period	50	-	40	-		
t17	CLK LOW Time	12	-	11	-	ns	(Notes 2, 6)
t18	CLK HIGH Time	16	-	13	-	ns	(Notes 2, 6)
t21	$\overline{READY}$ Inactive Delay	5	-	5	-	ns	At 0.8V (Note 4), Test Condition 2
t22	$\overline{READY}$ Active Delay	-	24	-	18	ns	At 0.8V (Note 4)
t23	PCLK Delay	-	20	-	16	ns	C_L = 75pF, Test Condition 1
t24	RESET Delay	-	27	-	26	ns	C_L = 75pF, Test Condition 3
t25	PCLK LOW Time	t16 -10	-	t16 -10	-	na	C_L = 75pF (Note 5)
t26	PCLK HIGH Time	t16 -10	-	t16 -10	-	ns	C_L= 75pF (Note 5)

NOTES:

1. V_{CC} = 4.5V and 5.5V unless otherwise specified. CLK loading: C_L = 100pF.
2. With the internal crystal oscillator using recommended crystal and capacitive loading; or with the EFI input meeting specifications t_1 and t_2. The recommended crystal loading for CLK frequencies of 8MHz to 20MHz are 25pF from pin X1 to ground, and 15pF from pin X2 to ground; for CLK frequencies from 20MHz to 25MHz the recommended loading is 15pF from pin X1 to GND. These recommended values are +5pF and include all stray capacitance. Decouple V_{CC} and GND as close to the 82C284 as possible.
3. This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at a specific CLK edge.
4. The pull-up resistor value for the $\overline{READY}$ pin is 620Ω with the rated 150pF load.
5. t_{16} refers to any allowable CLK period.
6. When using a crystal with the recommended capacitive loading, CLK output HIGH and LOW times are guaranteed to meet 80C286 requirements.
7. Measured from 1.0V on the CLK to 0.8V on the $\overline{RES}$ waveform for $\overline{RES}$ waveform for $\overline{RES}$ active and to 4.2V on the $\overline{RES}$ waveform for $\overline{RES}$ inactive.
8. Input test waveform characteristics: V_{IL} = 0V, V_{IH} = 4.5V.

UNTESTED SPECIFICATIONS

SYMBOL	PARAMETER	10MHz		12.5MHz		UNITS	CONDITIONS (NOTE 1)
		MIN	MAX	MIN	MAX		
C_{IN}	Input Capacitance	-	10	-	10	pF	FREQ = 1MHz, All measurements are referenced to device GND, $T_A = +25^oC$
t15A	EFI HIGH to CLK LOW Delay	-	30	-	25	ns	(Note 2)
t15B	EFI LOW to CLK HIGH Delay	-	35	-	30	ns	(Note 3)

UNTESTED SPECIFICATIONS (Continued)

SYMBOL	PARAMETER	10MHz		12.5MHz		UNITS	CONDITIONS (NOTE 1)
		MIN	MAX	MIN	MAX		
t19	CLK Rise Time	-	8	-	8	ns	1.0V to 3.6V, C_L = 100pF
t20	CLK Fall Time	-	8	-	8	ns	3.6V to 1.0V, C_L = 100pF
t27	X1 HIGH to CLK	-	35	-	30	ns	(Note 4)

NOTES:

1. The parameters listed in this table are controlled via design or, process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Measured from 3.2V on the EFI waveform to 1.0V on the CLK.
3. Measured from 0.8V on the EFI waveform to 3.6V on the CLK.
4. Measured from 3.6V on the X1 input to 3.6V on the CLK.

AC Specifications

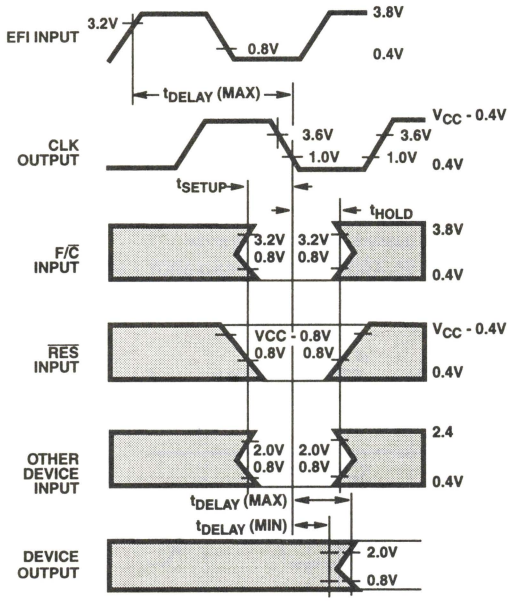


FIGURE 7. A.C. DRIVE, SETUP, HOLD AND DELAY TIME MEASUREMENT POINTS

AC Test Condition

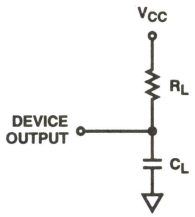
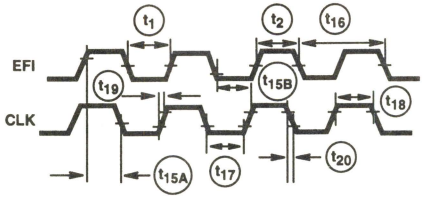


FIGURE 8.

TEST CONDITION	R_L	C_L
1	750Ω	75pF
2	620Ω	150pF
3	∞	75pF

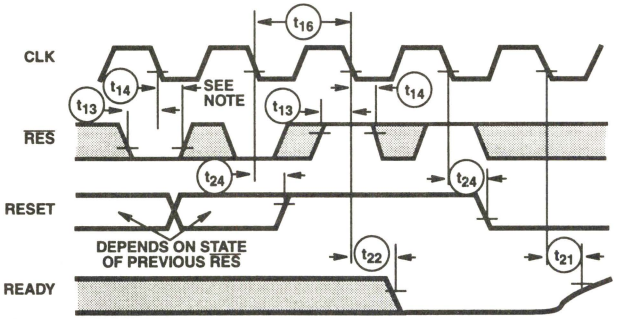
Waveforms



NOTE:

1. The EFI input LOW and HIGH times as shown are required to guarantee the CLK LOW and HIGH times shown.

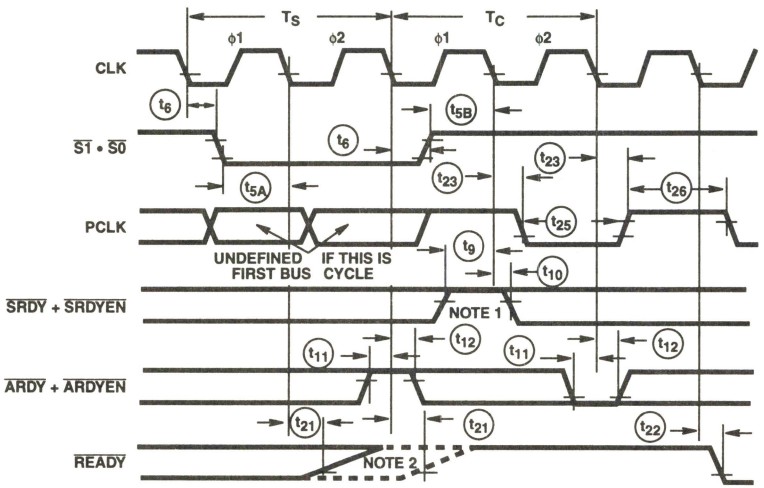
FIGURE 9. CLK AS A FUNCTION OF EFI



NOTE:

1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

FIGURE 10. RESET AND $\overline{\text{READY}}$ TIMING AS A FUNCTION OF RES WITH $\overline{\text{S1}}$, $\overline{\text{S0}}$, $\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$, AND $\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ HIGH

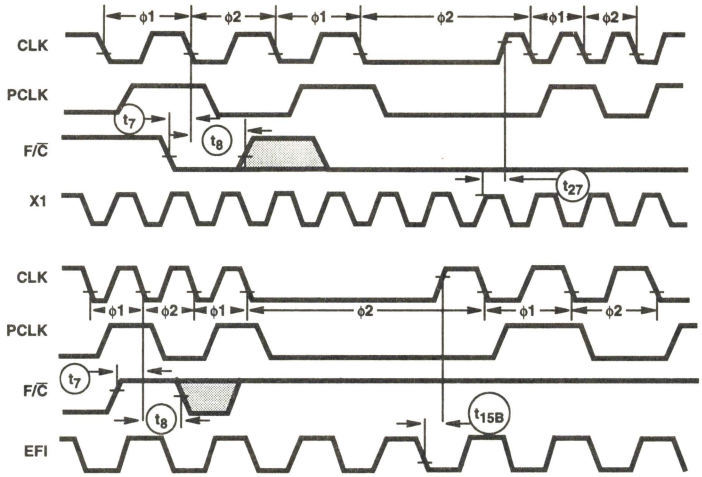


NOTES:

1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
2. If $\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ or $\overline{\text{ARDYEN}}$ are active before and/or during the first bus cycle after RESET, $\overline{\text{READY}}$ may not be deasserted until the falling edge of φ2 of T_S.

FIGURE 11. $\overline{\text{READY}}$ AND PCLK TIMING WITH $\overline{\text{RES}}$ HIGH

Waveforms (Continued)



NOTE:

1. This is an asynchronous input. The setup and hold times are required to guarantee the response shown.

FIGURE 12. CLK AS A FUNCTION OF F/C, PCLK, X1, AND EFI DURING DYNAMIC FREQUENCY SWITCHING

HARRIS SEMICONDUCTOR

82C284/883

Clock Generator and Ready Interface for 80C286 Processors

March 1997

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Generates System Clock for 80C286 Processors**
- **Generates System Reset Output from Schmitt Trigger Input**
  - **Improved Hysteresis**
- **Uses Crystal or External Signal for Frequency Source**
  - **Dynamically Switchable Between Two Input Frequencies**
- **Provides Local $\overline{\text{READY}}$ and MULTIBUS® $\overline{\text{READY}}$ Synchronization**
- **Static CMOS Technology**
- **Single +5V Power Supply**
- **Available in 18 Lead CERDIP Package**

Description

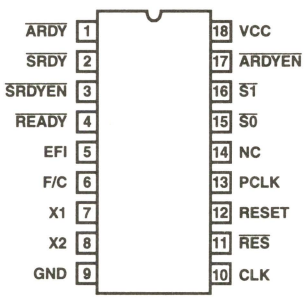
The Harris 82C284/883 is a clock generator/driver which provides clock signals for 80C286 processors and support components. It also contains logic to supply $\overline{\text{READY}}$ to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis.

Ordering Information

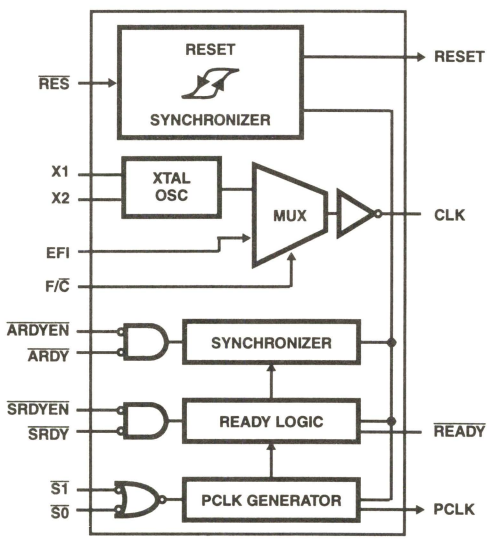
PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
MD82C284-12/883	-55°C to +125°C	CERDIP	F18.3

Pinout

82C284/883
(CERDIP)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Copyright © Harris Corporation 1997

MULTIBUS® is a patented Intel bus.

File Number **2968.1**

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage Applied. . . . . GND -0.1V to VCC +1.0V
ESD Classification . . . . . Class 2

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	80	20

Gate Count . . . . . 200 Gates
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Temperature (Soldering 10s) . . . . . +300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage . . . . . +4.5V to +5.5V
EFI Rise Time (From 0.8V to 3.2V) . . . . . 8ns (Max)
EFI Fall Time (From 3.2V to 0.8V) . . . . . 8ns (Max)

TABLE 1. 82C284/883 D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	MIN	MAX	UNITS
Input LOW Voltage	VIL	VCC = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
Input HIGH Voltage	VIH	VCC = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.2	-	V
EFI, F/$\overline{C}$ Input High Voltage	VIHC	VCC = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	3.2	-	V
$\overline{RES}$ HIGH Voltage	VIHR	VCC = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	VCC -0.8	-	V
$\overline{RES}$ Input Hysteresis	VHYS	VCC = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	0.5	-	V
RESET, PCLK Output LOW Voltage	VOL	IOL = 5mA, VCC = 4.5V, Note 2	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
RESET, PCLK Output Voltage	VOH	IOH = -1mA, VCC = 4.5V, Note 2	1, 2, 3	-55°C ≤ T_A ≤ +125°C	VCC -0.4	-	V
$\overline{READY}$ Output LOW Voltage	VOLR	IOH = 10mA, VCC = 4.55V, Note 2	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
CLK Output LOW Voltage	VOLC	IOL = 5mA, VCC = 4.5V, Note 2	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
CLK Output HIGH Voltage	VOHC	IOH = -5mA, VCC = 4.5V, Note 2	1, 2, 3	-55°C ≤ T_A ≤ +125°C	VCC -0.4	-	V
Input Leakage Current	II	VIN = GND or VCC, VCC = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	10	µA
Active Power Supply Current	ICCOP	82C284-10/883, Note 1	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	48	mA
		82C284-12/883, Note 1	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	60	mA

NOTES:

1. ICCOP measured at 10MHz for the 82C284-10/883 and at 12.5MHz for the 82C284-12/883. VIN = GND or VCC, VCC = 5.5V, outputs unloaded.
2. Interchanging of force and sense conditions is permitted.

TABLE 2. 82C284/883 A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested. A.C. timings are referenced to 0.8V and 2.0V points of the signals as illustrated in datasheet waveforms, unless otherwise specified.

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	10MHz		12MHz		UNITS
					MIN	MAX	MIN	MAX	
EFI LOW Time	t1	At VCC/2, Note 8	9, 10, 11	-55°C ≤ T_A ≤ +125°C	20	-	16	-	ns
EFI HIGH Time	t2	At VCC/2, Note 8	9, 10, 11	-55°C ≤ T_A ≤ +125°C	20	-	20	-	ns

TABLE 2. 82C284/883 A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested. A.C. timings are referenced to 0.8V and 2.0V points of the signals as illustrated in datasheet waveforms, unless otherwise specified. **(Continued)**

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	10MHz		12MHz		UNITS
					MIN	MAX	MIN	MAX	
Status Setup Time for Status Going Active	t5A		9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	18	-	ns
Status Setup Time for Going Inactive	t5B		9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	16	-	ns
Status Hold Time	t6		9, 10, 11	$-55^oC \le T_A \le +125^oC$	1	-	1	-	ns
F/$\overline{C}$ Setup Time	t7		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	15	-	ns
F/$\overline{C}$ Hold Time	t8		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	15	-	ns
$\overline{SRDY}$ or $\overline{SRDYEN}$ Setup Time	t9		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	15	-	ns
$\overline{SRDY}$ or $\overline{SRDYEN}$ Hold Time	t10		9, 10, 11	$-55^oC \le T_A \le +125^oC$	2	-	2	-	ns
$\overline{ARDY}$ or $\overline{ARDYEN}$ Setup Time	t11	Note 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	5	-	5	-	ns
$\overline{ARDY}$ or $\overline{ARDYEN}$ Hold Time	t12	Note 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	30	-	25	-	ns
$\overline{RES}$ Setup Time	t13	Notes 3, 7	9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	18	-	ns
$\overline{RES}$ Hold Time	t14	Notes 3, 7	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	8	-	ns
CLK Period	t16		9, 10, 11	$-55^oC \le T_A \le +125^oC$	50	-	40	-	ns
CLK LOW Period	t17	Notes 2, 6	9, 10, 11	$-55^oC \le T_A \le +125^oC$	12	-	11	-	ns
CLK HIGH Time	t18	Notes 2, 6	9, 10, 11	$-55^oC \le T_A \le +125^oC$	16	-	13	-	ns
$\overline{READY}$ Inactive Delay	t21	At 0.8V, Note 4, Test Condition 2	9, 10, 11	$-55^oC \le T_A \le +125^oC$	5	-	5	-	ns
$\overline{READY}$ Active Delay	t22	At 0.8V, Note 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	24	-	18	ns
PCLK Delay	t23	CL = 75pF, Test Condition 1	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	20	-	16	ns
RESET Delay	t24	CL = 75pF, Test Condition 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	27	-	26	ns
PCLK LOW Time	t25	CL = 75pF, Note 5	9, 10, 11	$-55^oC \le T_A \le +125^oC$	t16-10	-	t16-10	-	ns
PCLK HIGH Time	t26	CL = 75pF, Note 5	9, 10, 11	$-55^oC \le T_A \le +125^oC$	t16-10	-	t16-10	-	ns

NOTES:

1. VCC = 4.5V and 5.5V unless otherwise specified. CLK loading: CL = 100pF.
2. With the internal crystal oscillator using recommended crystal and capacitive loading; or with the EFI input meeting specifications t1 and t2. The recommended crystal loading for CLK frequencies of 8MHz to 20MHz are 25pF from pin X1 to GND, and 15pF from pin X2 to GND; for CLK frequencies from 20MHz to 25MHz the recommended loading is 15pF from pin X1 to GND, and 15pF from X2 to GND. These recommended values are ±5pF and include all stray capacitance. Decouple VCC and GND as close to the 80C284/883 as possible.
3. This is an asychronous input. This specification is given for testing purposes only, to assure recognition at a specific CLK edge.
4. The pull-up resistor value for the $\overline{READY}$ pin is 620Ω with the rated 150pF load.
5. t16 refers to any allowable CLK period.
6. When using a crystal with the recommended capacitive loading, CLK output HIGH and LOW times are guaranteed to meet 80C286 requirements.
7. Measured from 1.0V on the CLK to 0.8V on the $\overline{RES}$ waveform for $\overline{RES}$ active, and to 4.2V on the $\overline{RES}$ waveform for $\overline{RES}$ inactive.
8. Input test waveform characteristics: VIL= 0.0V, VIH = 4.5V.

TABLE 3. 82C284/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	10MHz		12MHz		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	CIN	FREQ = 1MHz, All measurements are referenced to device GND	1	T_A = +25°C	-	10	-	10	pF
EFI HIGH to CLK LOW Delay	t15A		1, 2	-55°C ≤ T_A ≤ +125°C	-	30	-	25	ns
EFI LOW to CLK HIGH Delay	t15B		1, 3	-55°C ≤ T_A ≤ +125°C	-	35	-	30	ns
CLK Rise Time	t19	1.0V to 3.6V, CL = 100pF	1	-55°C ≤ T_A ≤ +125°C	-	8	-	8	ns
CLK Fall Time	t20	3.6V to 1.0V, CL = 100pF	1	-55°C ≤ T_A ≤ +125°C	-	8	-	8	ns
X1 HIGH to CLK	t27		1, 4	-55°C ≤ T_A ≤ +125°C	-	35	-	30	ns

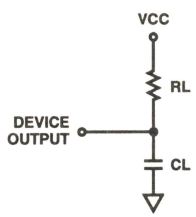
NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Measured from 3.2V on the EFI waveform to 1.0V on the CLK.
3. Measured from 0.8V on the EFI waveform to 3.6V on the CLK.
4. Measured from 3.6V on the X1 input to 3.6V on the CLK.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

A.C. Test Conditions



TEST CONDITION	RL	CL
1	750Ω	75pF
2	620Ω	150pF
3	∞	75pF

A.C. Specifications

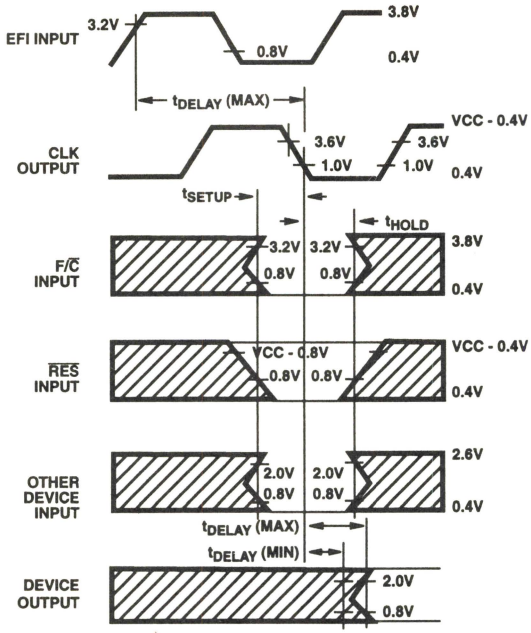


FIGURE 1. A.C. DRIVE, SETUP, HOLD AND DELAY TIME MEASUREMENT POINTS

Timing Waveforms

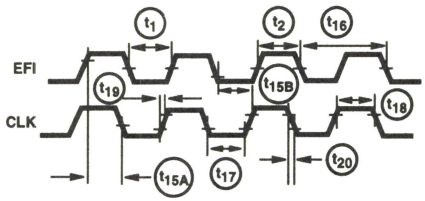
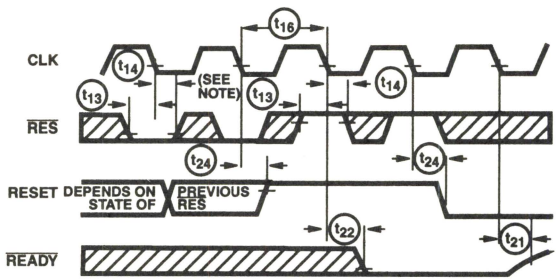


FIGURE 2. CLK AS A FUNCTION OF EFI

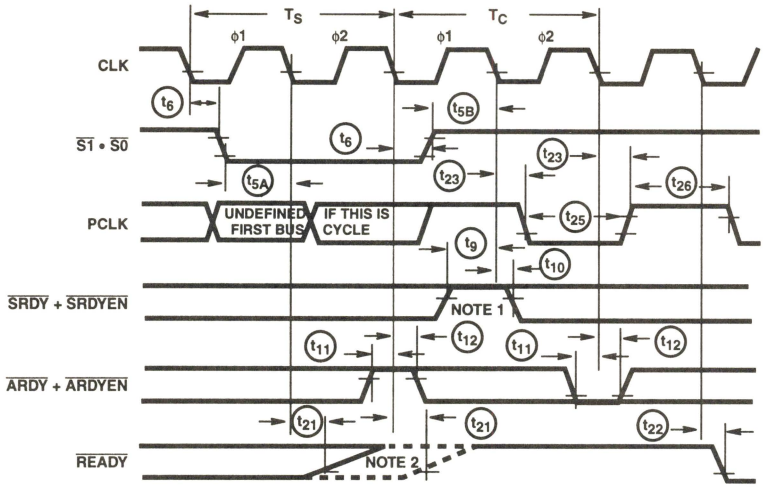
NOTE: The EFI input LOW and HIGH times as shown are required to guarantee the CLK LOW and HIGH times shown.



NOTE: This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

FIGURE 3. RESET AND $\overline{\text{READY}}$ TIMING AS A FUNCTION OF $\overline{\text{RES}}$ WITH $\overline{\text{S1}}$, $\overline{\text{S0}}$, ARDY + $\overline{\text{ARDYEN}}$ AND $\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ HIGH

Timing Waveforms (Continued)



NOTES:

1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
2. If $\overline{SRDY} + \overline{SRDYEN}$ or $\overline{ARDY} + \overline{ARDYEN}$ are active before and/or during the first bus cycle after RESET, $\overline{READY}$ may not be deasserted until the falling edge of φ2 of T_S.

FIGURE 4. $\overline{READY}$ AND PCLK TIMING WITH $\overline{RES}$ HIGH

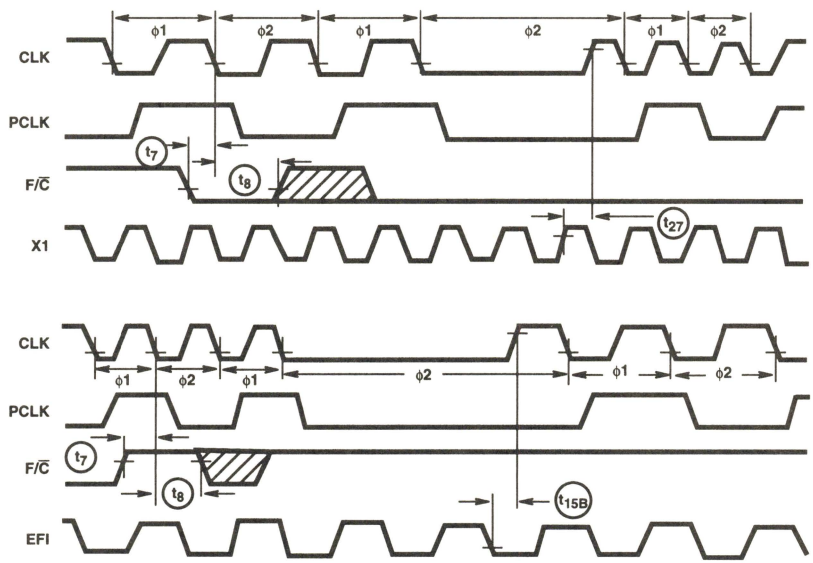
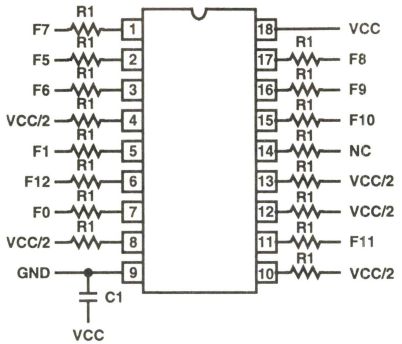


FIGURE 5. CLK AS A FUNCTION OF F/$\overline{C}$, PCLK, X1, AND EFI DURING DYNAMIC FREQUENCY SWITCHING

NOTE: This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

Burn-In Circuit

18 LEAD CERDIP



NOTES:

1. Supply Voltage: VCC = 5.5V, ±0.5V, GND = 0V. Driver Voltage: VIH = 4.5V ± 10%, VIL = 0V
2. Input Voltage Limits: VIL (Max) = 0.4V, VIH (Min) = 2.6V
3. Component Values: R1 = 47kΩ, C1 = 0.1μF (Min)
4. Oven type and frequency requirements microtest, F0 through F12.
5. Approximate current per unit. ICC = 0.3mA.
6. Special requirements:
   (a) Electrostatic Discharge Sensitive. Proper precautions must be used when handling units.
   (b) All power supplies must be at zero volts when the boards are inserted into the ovens. After insertion, apply VCC first, then activate the driver power supplies.
7. Oscilloscope measurements: To be on loaded boards before insertion into the oven.

Die Characteristics

DIE DIMENSIONS:
63 mils x 69 mils x 19 mils ± 1 mil

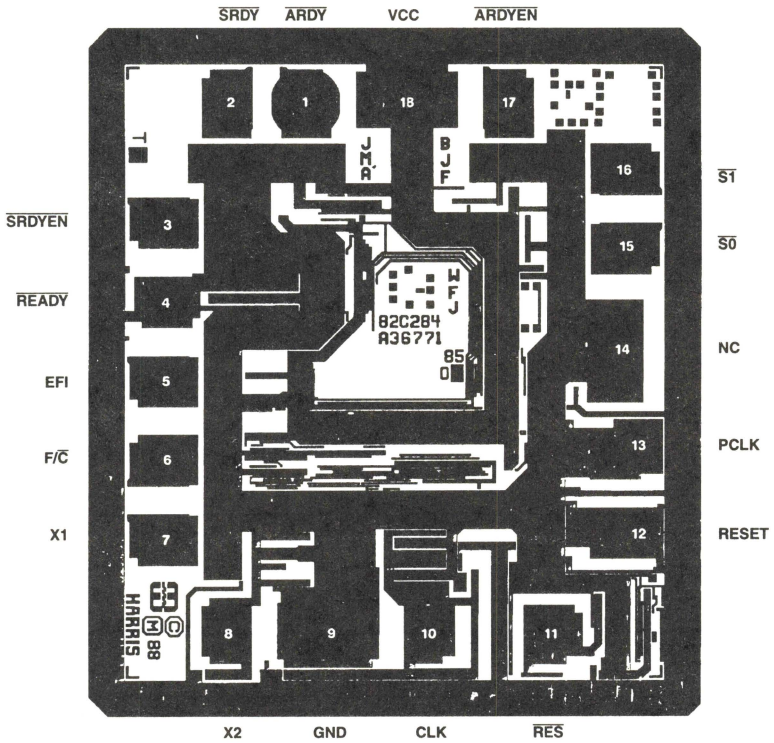
METALLIZATION:
Type: Silicon - Aluminum
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:
2×10^5 A/cm^2

Metallization Mask Layout

82C284/883



HARRIS SEMICONDUCTOR

82C37A

CMOS High Performance Programmable DMA Controller

March 1997

Features

- Compatible with the NMOS 8237A
- Four Independent Maskable Channels with Autoinitialization Capability
- Cascadable to any Number of Channels
- High Speed Data Transfers:
  - Up to 4MBytes/sec with 8MHz Clock
  - Up to 6.25MBytes/sec with 12.5MHz Clock
- Memory-to-Memory Transfers
- Static CMOS Design Permits Low Power Operation
  - ICCSB = 10μA Maximum
  - ICCOP = 2mA/MHz Maximum
- Fully TTL/CMOS Compatible
- Internal Registers may be Read from Software

Description

The 82C37A is an enhanced version of the industry standard 8237A Direct Memory Access (DMA) controller, fabricated using Harris' advanced 2 micron CMOS process. Pin compatible with NMOS designs, the 82C37A offers increased functionality, improved performance, and dramatically reduced power consumption. The fully static design permits gated clock operation for even further reduction of power.

The 82C37A controller can improve system performance by allowing external devices to transfer data directly to or from system memory. Memory-to-memory transfer capability is also provided, along with a memory block initialization feature. DMA requests may be generated by either hardware or software, and each channel is independently programmable with a variety of features for flexible operation.

The 82C37A is designed to be used with an external address latch, such as the 82C82, to demultiplex the most significant 8-bits of address. The 82C37A can be used with industry standard microprocessors such as 80C286, 80286, 80C86, 80C88, 8086, 8088, 8085, Z80, NSC800, 80186 and others. Multimode programmability allows the user to select from three basic types of DMA services, and reconfiguration under program control is possible even with the clock to the controller stopped. Each channel has a full 64K address and word count range, and may be programmed to autoinitialize these registers following DMA termination (end of process).

Ordering Information

PART NUMBER			PACKAGE	TEMPERATURE RANGE	PKG. NO.
5MHz	8MHz	12.5MHz			
CP82C37A-5	CP82C37A	CP82C37A-12	40 Ld PDIP	0°C to +70°C	E40.6
IP82C37A-5	IP82C37A	IP82C37A-12		-40°C to +85°C	E40.6
CS82C37A-5	CS82C37A	CS82C37A-12	44 Ld PLCC	0°C to +70°C	N44.65
IS82C37A-5	IS82C37A	IS82C37A-12		-40°C to +85°C	N44.65
CD82C37A-5	CD82C37A	CD82C37A-12	40 Ld CERDIP	0°C to +70°C	F40.6
ID82C37A-5	ID82C37A	ID82C37A-12		-40°C to +85°C	F40.6
MD82C37A-5/B	MD82C37A/B	MD82C37A-12/B		-55°C to +125°C	F40.6
5962-9054301MQA	5962-9054302MQA	5962-9054303MQA	SMD#		F40.6
MR82C37A-5/B	MR82C37A/B	MR82C37A-12/B	44 Pad CLCC	-55°C to +125°C	J44.A
5962-9054301MXA	5962-9054302MXA	5962-9054303MXA	SMD#		J44.A

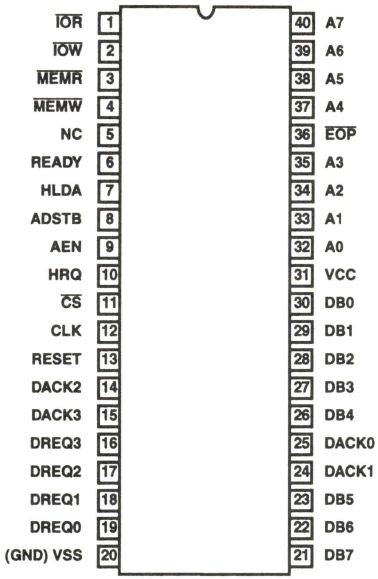
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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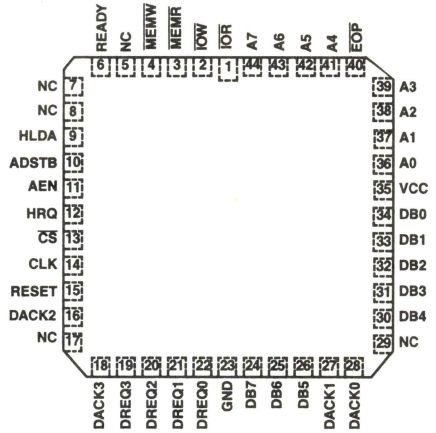
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Pinouts

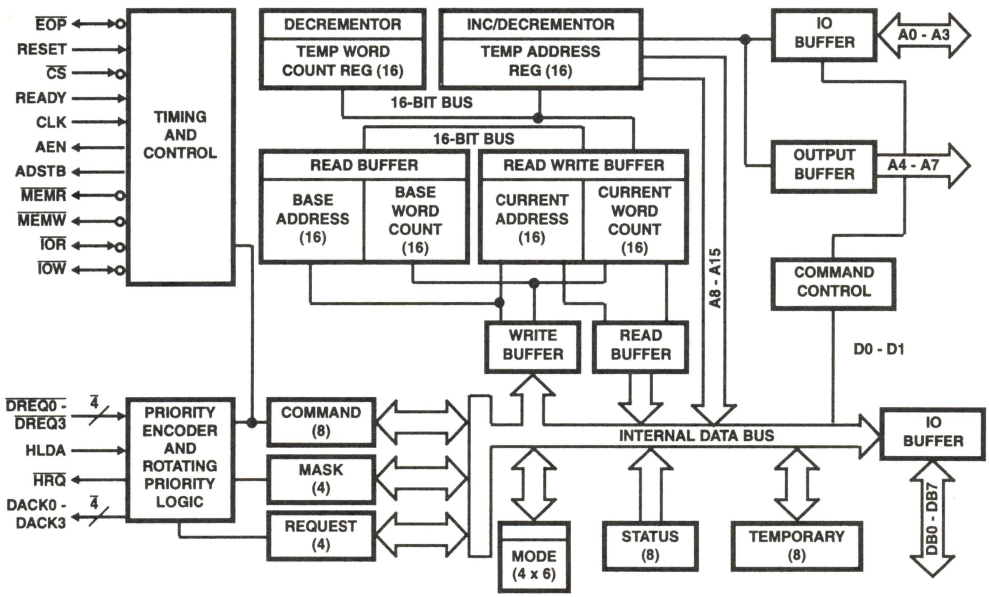
82C37A (PDIP/CERDIP)
TOP VIEW



82C37A (CLCC/PLCC)
TOP VIEW



Block Diagram



Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	31		V_{CC}: is the +5V power supply pin. A 0.1μF capacitor between pins 31 and 20 is recommended for decoupling.
GND	20		Ground
CLK	12	I	CLOCK INPUT: The Clock Input is used to generate the timing signals which control 82C37A operations. This input may be driven from DC to 12.5MHz for the 82C37A-12, from DC to 8MHz for the 82C37A, or from DC to 5MHz for the 82C37A-5. The Clock may be stopped in either state for standby operation.
$\overline{CS}$	11	I	CHIP SELECT: Chip Select is an active low input used to enable the controller onto the data bus for CPU communications.
RESET	13	I	RESET: This is an active high input which clears the Command, Status, Request, and Temporary registers, the First/Last Flip-Flop, and the mode register counter. The Mask register is set to ignore requests. Following a Reset, the controller is in an idle cycle.
READY	6	I	READY: This signal can be used to extend the memory read and write pulses from the 82C37A to accommodate slow memories or I/O devices. READY must not make transitions during its specified set-up and hold times. See Figure 12 for timing. READY is ignored in verify transfer mode.
HLDA	7	I	HOLD ACKNOWLEDGE: The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses. HLDA is a synchronous input and must not transition during its specified set-up time. There is an implied hold time (HLDA inactive) of TCH from the rising edge of CLK, during which time HLDA must not transition.
DREQ0-DREQ3	16-19	I	DMA REQUEST: The DMA Request (DREQ) lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In Fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of a DREQ signal. Polarity of DREQ is programmable. RESET initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active. DREQ will not be recognized while the clock is stopped. Unused DREQ inputs should be pulled High or Low (inactive) and the corresponding mask bit set.
DB0-DB7	21-23 26-30	I/O	DATA BUS: The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of a register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the 82C37A control registers. During DMA cycles, the most significant 8-bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory enters the 82C37A on the data bus during the read-from-memory transfer, then during the write-to-memory transfer, the data bus outputs write the data into the new memory location.
$\overline{IOR}$	1	I/O	I/O READ: I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the 82C37A to access data from the peripheral during a DMA Write transfer.
$\overline{IOW}$	2	I/O	I/O WRITE: I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the 82C37A. In the Active cycle, it is an output control signal used by the 82C37A to load data to the peripheral during a DMA Read transfer.

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{EOP}$	36	I/O	END OF PROCESS: End of Process ($\overline{EOP}$) is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional $\overline{EOP}$ pin. The 82C37A allows an external signal to terminate an active DMA service by pulling the $\overline{EOP}$ pin low. A pulse is generated by the 82C37A when terminal count (TC) for any channel is reached, except for channel 0 in memory-to-memory mode. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. The $\overline{EOP}$ pin is driven by an open drain transistor on-chip, and requires an external pull-up resistor to V_{CC}. When an $\overline{EOP}$ pulse occurs, whether internally or externally generated, the 82C37A will terminate the service, and if autoinitialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for autoinitialize. In that case, the mask bit remains clear.
A0-A3	32-35	I/O	ADDRESS: The four least significant address lines are bidirectional three-state signals. In the Idle cycle, they are inputs and are used by the 82C37A to address the control register to be loaded or read. In the Active cycle, they are outputs and provide the lower 4-bits of the output address.
A4-A7	37-40	O	ADDRESS: The four most significant address lines are three-state outputs and provide 4-bits of address. These lines are enabled only during the DMA service.
HRQ	10	O	HOLD REQUEST: The Hold Request (HRQ) output is used to request control of the system bus. When a DREQ occurs and the corresponding mask bit is clear, or a software DMA request is made, the 82C37A issues HRQ. The HLDA signal then informs the controller when access to the system busses is permitted. For stand-alone operation where the 82C37A always controls the busses, HRQ may be tied to HLDA. This will result in one S0 state before the transfer.
DACK0- DACK3	14, 15 24, 25	O	DMA ACKNOWLEDGE: DMA acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. RESET initializes them to active low.
AEN	9	O	ADDRESS ENABLE: Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active high.
ADSTB	8	O	ADDRESS STROBE: This is an active high signal used to control latching of the upper address byte. It will drive directly the strobe input of external transparent octal latches, such as the 82C82. During block operations, ADSTB will only be issued when the upper address byte must be updated, thus speeding operation through elimination of S1 states. ADSTB timing is referenced to the falling edge of the 82C37A clock.
$\overline{MEMR}$	3	O	MEMORY READ: The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer.
$\overline{MEMW}$	4	O	MEMORY WRITE: The Memory Write signal is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.
NC	5		NO CONNECT: Pin 5 is open and should not be tested for continuity.

Functional Description

The 82C37A direct memory access controller is designed to improve the data transfer rate in systems which must transfer data from an I/O device to memory, or move a block of memory to an I/O device. It will also perform memory-to-memory block moves, or fill a block of memory with data from a single location. Operating modes are provided to handle single byte transfers as well as discontinuous data streams, which allows the 82C37A to control data movement with software transparency.

The DMA controller is a state-driven address and control signal generator, which permits data to be transferred directly from an I/O device to memory or vice versa without ever being stored in a temporary register. This can greatly increase the data transfer rate for sequential operations, compared with processor move or repeated string instructions. Memory-to-memory operations require temporary internal storage of the data byte between generation of the source and destination addresses, so memory-to-memory transfers take place at less than half the rate of I/O operations, but still much faster than with central processor techniques. The maximum data transfer rates obtainable with the 82C37A are shown in Figure 1.

The block diagram of the 82C37A is shown on page 2. The timing and control block, priority block, and internal registers are the main components. Figure 2 lists the name and size of the internal registers. The timing and control block derives internal timing from clock input, and generates external control signals. The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously.

82C37A TRANSFER TYPE	5MHz	8MHz	12.5MHz	UNIT
Compressed	2.50	4.00	6.25	MByte/sec
Normal I/O	1.67	2.67	4.17	MByte/sec
Memory-to-Memory	0.63	1.00	1.56	MByte/sec

FIGURE 1. DMA TRANSFER RATES

DMA Operation

In a system, the 82C37A address and control outputs and data bus pins are basically connected in parallel with the system busses. An external latch is required for the upper address byte. While inactive, the controller's outputs are in a high impedance state. When activated by a DMA request and bus control is relinquished by the host, the 82C37A drives the busses and generates the control signals to perform the data transfer. The operation performed by activating one of the four DMA request inputs has previously been programmed into the controller via the Command, Mode, Address, and Word Count registers.

For example, if a block of data is to be transferred from RAM to an I/O device, the starting address of the data is loaded into the 82C37A Current and Base Address registers for a particular channel, and the length of the block is loaded into the channel's Word Count register. The corresponding Mode register is programmed for a memory-to-I/O operation (read transfer), and various options are selected by the Command register and the other Mode register bits. The channel's mask bit is cleared to enable recognition of a DMA request (DREQ). The DREQ can either be a hardware signal or a software command.

Once initiated, the block DMA transfer will proceed as the controller outputs the data address, simultaneous $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$ pulses, and selects an I/O device via the DMA acknowledge (DACK) outputs. The data byte flows directly from the RAM to the I/O device. After each byte is transferred, the address is automatically incremented (or decremented) and the word count is decremented. The operation is then repeated for the next byte. The controller stops transferring data when the Word Count register underflows, or an external $\overline{\text{EOP}}$ is applied.

NAME	SIZE	NUMBER
Base Address Registers	16-Bits	4
Base Word Count Registers	16-Bits	4
Current Address Registers	16-Bits	4
Current Word Count Registers	16-Bits	4
Temporary Address Register	16-Bits	1
Temporary Word Count Register	16-Bits	1
Status Register	8-Bits	1
Command Register	8-Bits	1
Temporary Register	8-Bits	1
Mode Registers	6-Bits	4
Mask Register	4-Bits	1
Request Register	4-Bits	1

FIGURE 2. 82C37A INTERNAL REGISTERS

To further understand 82C37A operation, the states generated by each clock cycle must be considered. The DMA controller operates in two major cycles, active and idle. After being programmed, the controller is normally idle until a DMA request occurs on an unmasked channel, or a software request is given. The 82C37A will then request control of the system busses and enter the active cycle. The active cycle is composed of several internal states, depending on what options have been selected and what type of operation has been requested.

The 82C37A can assume seven separate states, each composed of one full clock period. State I (SI) is the idle state. It is entered when the 82C37A has no valid DMA requests pending, at the end of a transfer sequence, or when a Reset or Master Clear has occurred. While in SI, the DMA controller is inactive but may be in the Program Condition (being programmed by the processor).

State 0 (S0) is the first state of a DMA service. The 82C37A has requested a hold but the processor has not yet returned an acknowledge. The 82C37A may still be programmed until it has received HLDA from the CPU. An acknowledge from the CPU will signal the DMA transfer may begin. S1, S2, S3, and S4 are the working state of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S3 and S4 in normal transfers by the use of the Ready line on the 82C37A. For compressed transfers, wait states can be inserted between S2 and S4. See timing Figures 14 and 15.

Note that the data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active at the same time. The data is not read into or driven out of the 82C37A in I/O-to-memory or memory-to-I/O DMA transfers.

Memory-to-memory transfers require a read-from and a write-to memory to complete each transfer. The states, which resemble the normal working states, use two-digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four state (S21, S22, S23, S24) for the write-to-memory half of the transfer.

Idle Cycle

When no channel is requesting service, the 82C37A will enter the idle cycle and perform "SI" states. In this cycle, the 82C37A will sample the DREQ lines on the falling edge of every clock cycle to determine if any channel is requesting a DMA service.

Note that for standby operation where the clock has been stopped, DMA requests will be ignored. The device will respond to $\overline{CS}$ (chip select), in case of an attempt by the microprocessor to write or read the internal registers of the 82C37A. When $\overline{CS}$ is low and HLDA is low, the 82C37A enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers.

The 82C37A may be programmed with the clock stopped, provided that HLDA is low and at least one rising clock edge has occurred after HLDA was driven low, so the controller is in an SI state. Address lines A0-A3 are inputs to the device and select which registers will be read or written. The IOR and IOW lines are used to select and time the read or write operations. Due to the number and size of the internal registers, an internal flip-flop called the First/Last Flip-Flop is used to generate an additional bit of address. The bit is used to determine the upper or lower byte of the 16-bit Address and Work Count registers. The flip-flop is reset by Master Clear or RESET. Separate software commands can also set or reset this flip-flop.

Special software commands can be executed by the 82C37A in the Program Condition. These commands are decoded as sets of addresses with $\overline{CS}$, $\overline{IOR}$, and $\overline{IOW}$. The commands do not make use of the data bus. Instructions include Set and Clear First/Last Flip-Flop, Master Clear, Clear Mode Register Counter, and Clear Mask Register.

Active Cycle

When the 82C37A is in the Idle cycle, and a software request or an unmasked channel requests a DMA service, the device will issue HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode - In Single Transfer mode, the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero to FFFFH, a terminal count bit in the status register is set, an $\overline{EOP}$ pulse is generated, and the channel will autoinitialize if this option has been selected. If not programmed to autoinitialize, the mask bit will be set, along with the TC bit and $\overline{EOP}$ pulse.

DREQ must be held active until DACK becomes active. If DREQ is held active throughout the single transfer, HRQ will go inactive and release the bus to the system. It will again go active and, upon receipt of a new HLDA, another single transfer will be performed, unless a higher priority channel takes over. In 8080A, 8085A, 80C88, or 80C86 systems, this will ensure one full machine cycle execution between DMA transfers. Details of timing between the 82C37A and other bus control protocols will depend upon the characteristics of the microprocessor involved.

Block Transfer Mode - In Block Transfer mode, the device is activated by DREQ or software request and continues making transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process ($\overline{EOP}$) is encountered. DREQ need only be held active until DACK becomes active. Again, an Autoinitialization will occur at the end of the service if the channel has been programmed for that option.

Demand Transfer Mode - In Demand Transfer mode the device continues making transfers until a TC or external EOP is encountered, or until DREQ goes inactive. Thus, transfer may continue until the I/O device has exhausted its data capacity. After the I/O device has had a chance to catch up, the DMA service is reestablished by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the 82C37A Current Address and Current Word Count registers. Higher priority channels may intervene in the demand process, once DREQ has gone inactive. Only an EOP can cause an Autoinitialization at the end of service. EOP is generated either by TC or by an external signal.

Cascade Mode - This mode is used to cascade more than one 82C37A for simple system expansion. The HRQ and HLDA signals from the additional 82C37A are connected to the DREQ and DACK signals respectively of a channel for

the initial 82C37A.This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial 82C37A is used only for prioritizing the additional device, it does not output an address or control signals of its own. These could conflict with the outputs of the active channel in the added device. The initial 82C37A will respond to DREQ and generate DACK but all other outputs except HRQ will be disabled. An external $\overline{EOP}$ will be ignored by the initial device, but will have the usual effect on the added device.

Figure 3 shows two additional devices cascaded with an initial device using two of the initial device's channels. This forms a two-level DMA system. More 82C37As could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

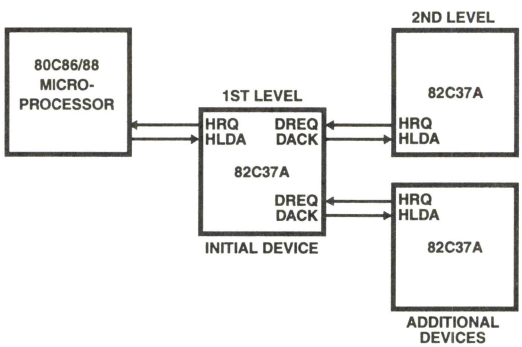


FIGURE 3. CASCADED 82C37As

When programming cascaded controllers, start with the first level device (closest to the microprocessor). After RESET, the DACK outputs are programmed to be active low and are held in the high state. If they are used to drive HLDA directly, the second level device(s) cannot be programmed until DACK polarity is selected as active high on the initial device. Also, the initial device's mask bits function normally on cascaded channels, so they may be used to inhibit second-level services.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating MEMW and IOR. Read transfers move data from memory to an I/O device by activating MEMR and IOW.

Verify transfers are pseudo-transfers. The 82C37A operates as in Read or Write transfers generating addresses and responding to $\overline{EOP}$, etc., however the memory and I/O control lines all remain inactive. Verify mode is not permitted for memory-to-memory operation. READY is ignored during Verify transfers.

Autoinitialize - By setting bit 4 in the Mode register, a channel may be set up as an Autoinitialize channel. During Autoinitialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word Count registers of the channel following $\overline{EOP}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in Autoinitialize mode. Following Autoinitialization, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected, or software request made.

Memory-to-Memory - To perform block moves of data from one memory address space to another with minimum of program effort and time, the 82C37A includes a memory-to-memory transfer feature. Setting bit 0 in the Command register selects channels 0 and 1 to operate as memory-to-memory transfer channels.

The transfer is initiated by setting the software or hardware DREQ for channel 0. The 82C37A requests a DMA service in the normal manner. After HLDA is true, the device, using four-state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the 82C37A internal Temporary register. Another four-state transfer moves the data to memory using the address in channel one's Current Address register and incrementing or decrementing it in the normal manner. The channel 1 Current Word Count is decremented.

When the word count of channel 1 decrements to FFFFH, a TC is generated causing an $\overline{EOP}$ output, terminating the service, and setting the channel 1 TC bit in the Status register. The channel 1 mask bit will also be set, unless the channel 1 mode register is programmed for autoinitialization. Channel 0 word count decrementing to FFFFH will not set the channel 0 TC bit in the status register nor generate an $\overline{EOP}$, nor set the channel 0 mask bit in this mode. It will cause an autoinitialization of channel 0, if that option has been selected.

If full Autoinitialization for a memory-to-memory operation is desired, the channel 0 and channel 1 word counts must be set to equal values before the transfer begins. Otherwise, if channel 0 underflows before channel 1, it will autoinitialize and set the data source address back to the beginning of the block. If the channel 1 word count underflows before channel 0, the memory-to-memory DMA service will terminate, and channel 1 will autoinitialize but channel 0 will not.

In memory-to-memory mode, Channel 0 may be programmed to retain the same address for all transfers. This allows a single byte to be written to a block of memory. This channel 0 address hold feature is selected by setting bit 1 in the Command register.

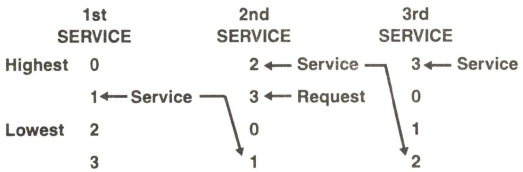
The 82C37A will respond to external $\overline{EOP}$ signals during memory-to-memory transfers, but will only relinquish the system busses after the transfer is complete (i.e. after an

S24 state). It should be noted that an external $\overline{EOP}$ cannot cause the channel 0 Address and Word Count registers to autoinitialize, even if the Mode register is programmed for autoinitialization. An external $\overline{EOP}$ will autoinitialize the channel 1 registers, if so programmed. Data comparators in block search schemes may use the $\overline{EOP}$ input to terminate the service when a match is found. The timing of memory-to-memory transfers is found in Figure 13. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

Priority - The 82C37A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their numbers. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interfering with the service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly. The next lower channel from the channel serviced has highest priority on the following request. Priority rotates every time control of the system busses is returned to the processor.

Rotating Priority



With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.

Regardless of which priority scheme is chosen, priority is evaluated every time a HLDA is returned to the 82C37A.

Compressed Timing - In order to achieve even greater throughput where system characteristics permit, the 82C37A can compress the transfer time to two clock cycles. From Figure 12 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8-A15 need updating (see Address Generation). Timing for compressed transfers is found in Figure 15. $\overline{EOP}$ will output in S2 if compressed timing is selected. Compressed timing is not allowed for memory-to-memory transfers.

Address Generation - In order to reduce pin count, the 82C37A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are output by the 82C37A directly. Lines A0-A7 should be connected to the address bus. Figure 12 shows the time relationships between CLK, AEN, ADSTB, DB0-DB7 and A0-A7.

During Block and Demand Transfer mode service, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the 82C37A executes S1 states only when updating of A8-A15 in the latch is necessary. This means for long services, S1 states and Address Strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

Programming

The 82C37A will accept programming from the host processor anytime that HLDA is inactive, and at least one rising clock edge has occurred after HLDA went low. It is the responsibility of the host to assure that programming and HLDA are mutually exclusive.

Note that a problem can occur if a DMA request occurs on an unmasked channel while the 82C37A is being programmed. For instance, the CPU may be starting to reprogram the two byte Address register of channel 1 when channel 1 receives a DMA request. If the 82C37A is enabled (bit 2 in the Command register is 0), and channel 1 is unmasked, a DMA service will occur after only one byte of the Address register has been reprogrammed. This condition can be avoided by disabling the controller (setting bit 2 in the Command register) or masking the channel before programming any of its registers. Once the programming is complete, the controller can be enabled/unmasked.

After power-up it is suggested that all internal locations be loaded with some known value, even if some channels are unused. This will aid in debugging.

Register Description

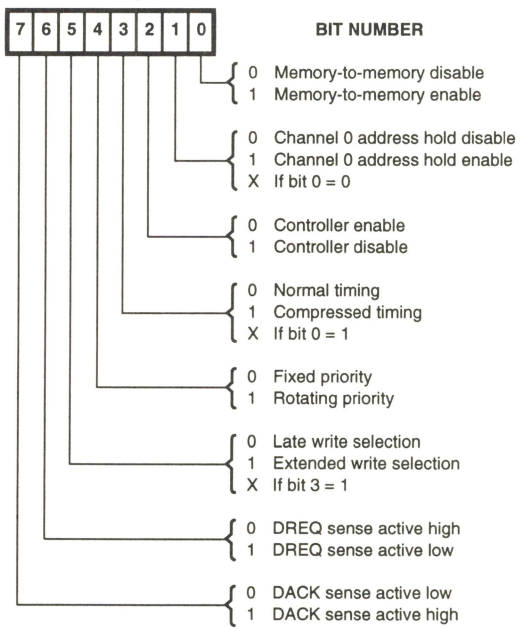
Current Address Register - Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented by one after each transfer and the values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. See Figure 6 for programming information. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an $\overline{EOP}$. In memory-to-memory mode, the channel 0 Current Address register can be prevented from incrementing or decrementing by setting the address hold bit in the Command register.

Current Word Count Register - Each channel has a 16-bit Current Word Count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. See Figure 6 for programming information. Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialization can occur only when an $\overline{EOP}$ occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC.

Base Address and Base Word Count Registers - Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. See Figure 6 for programming information. These registers cannot be read by the microprocessor.

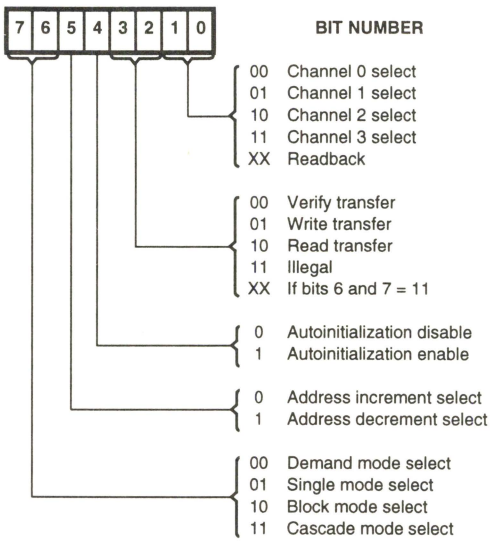
Command Register - This 8-bit register controls the operation of the 82C37A. It is programmed by the microprocessor and is cleared by RESET or a Master Clear instruction. The following diagram lists the function of the Command register bits. See Figure 4 for Read and Write addresses.

Command Register



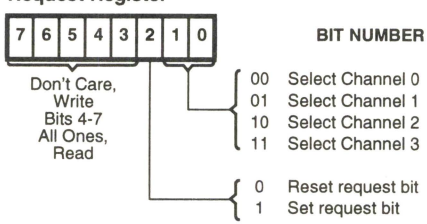
Mode Register - Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program condition, bits 0 and 1 determine which channel Mode register is to be written. When the processor reads a Mode register, bits 0 and 1 will both be ones. See the following diagram and Figure 4 for Mode register functions and addresses.

Mode Register



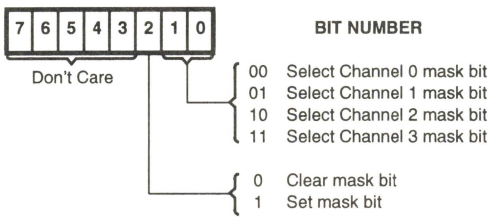
Request Register - The 82C37A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are non-maskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control. The entire register is cleared by a Reset or Master Clear instruction. To set or reset a bit, the software loads the proper form of the data word. See Figure 4 for register address coding, and the following diagram for Request register format. A software request for DMA operation can be made in block or single modes. For memory-to-memory transfers, the software request for channel 0 should be set. When reading the Request register, bits 4-7 will always read as ones, and bits 0-3 will display the request bits of channels 0-3 respectively.

Request Register

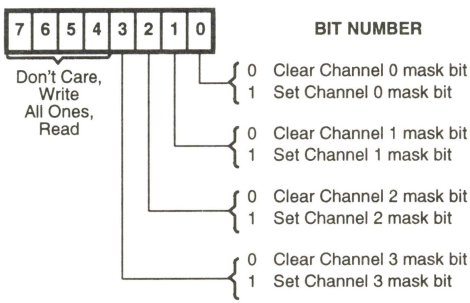


Mask Register - Each channel has associated with it a mask bit which can be set to disable an incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed to Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately or simultaneously under software control. The entire register is also set by a Reset or Master clear. This disables all hardware DMA requests until a Clear Mask Register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. Refer to the following diagram and Figure 4 for details. When reading the Mask register, bits 4-7 will always read as logical ones, and bits 0-3 will display the mask bits of channels 0-3, respectively. The 4 bits of the Mask register may be cleared simultaneously by using the Clear Mask Register command (see software commands section).

Mask Register

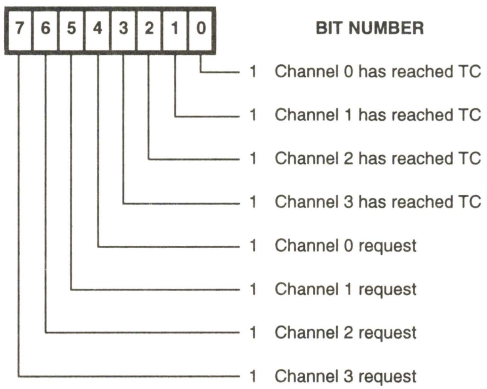


All four bits of the Mask register may also be written with a single command.



Status Register - The Status register is available to be read out of the 82C37A by the microprocessor. It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set every time a TC is reached by that channel or an external EOP is applied. These bits are cleared upon RESET, Master Clear, and on each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service, regardless of the mask bit state. If the mask bits are set, software can poll the Status register to determine which channels have DREQs, and selectively clear a mask bit, thus allowing user defined service priority. Status bits 4-7 are updated while the clock is high, and latched on the falling edge. Status Bits 4-7 are cleared upon RESET or Master Clear.

Status Register



Temporary Register - The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last byte moved can be read by the microprocessor. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset or Master Clear.

OPERATION	A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$
Read Status Register	1	0	0	0	0	1
Write Command Register	1	0	0	0	1	0
Read Request Register	1	0	0	1	0	1
Write Request Register	1	0	0	1	1	0
Read Command Register	1	0	1	0	0	1
Write Single Mask Bit	1	0	1	0	1	0
Read Mode Register	1	0	1	1	0	1
Write Mode Register	1	0	1	1	1	0
Set First/Last F/F	1	1	0	0	0	1
Clear First/Last F/F	1	1	0	0	1	0
Read Temporary Register	1	1	0	1	0	1
Master Clear	1	1	0	1	1	0
Clear Mode Reg. Counter	1	1	1	0	0	1
Clear Mask Register	1	1	1	0	1	0
Read All Mask Bits	1	1	1	1	0	1
Write All Mask Bits	1	1	1	1	1	0

FIGURE 4. SOFTWARE COMMAND CODES AND REGISTER CODES

Software Commands

There are special software commands which can be executed by reading or writing to the 82C37A. These commands do not depend on the specific data pattern on the data bus, but are activated by the I/O operation itself. On read type commands, the data value is not guaranteed. These commands are:

Clear First/Last Flip-Flop - This command is executed prior to writing or reading new address or word count information to the 82C37A. This command initializes the flip-flop to a known state (low byte first) so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

Set First/Last Flip-Flop - This command will set the flip-flop to select the high byte first on read and write operations to address and word count registers.

Master Clear - This software instruction has the same effect as the hardware Reset. The Command, Status, Request, and Temporary registers, and Internal First/Last Flip-Flop and mode register counter are cleared and the Mask register is set. The 82C37A will enter the idle cycle.

Clear Mask Register - This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Clear Mode Register Counter - Since only one address location is available for reading the Mode registers, an internal two-bit counter has been included to select Mode registers during read operation. To read the Mode registers, first execute the Clear Mode Register Counter command, then do consecutive reads until the desired channel is read. Read order is channel 0 first, channel 3 last. The lower two bits on all Mode registers will read as ones.

External $\overline{EOP}$ Operation

The $\overline{EOP}$ pin is a bidirectional, open drain pin which may be driven by external signals to terminate DMA operation. Because $\overline{EOP}$ is an open drain pin an external pull-up resistor to V_{CC} is required. The value of the external pull-up resistor used should guarantee a rise time of less than 125ns. It is important to note that the 82C37A will not accept external $\overline{EOP}$ signals when it is in a SI (Idle) state. The controller must be active to latch EXT $\overline{EOP}$. Once latched, the EXT $\overline{EOP}$ will be acted upon during the next S2 state, unless the 82C37A enters an idle state first. In the latter case, the latched $\overline{EOP}$ is cleared. External $\overline{EOP}$ pulses occurring between active DMA transfers in demand mode will not be recognized, since the 82C37A is in an SI state.

CHANNEL	REGISTER	OPERATION	SIGNALS							FIRST/LAST FLIP-FLOP STATE	DATA BUS DB0-DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15

FIGURE 5. WORD COUNT AND ADDRESS REGISTER COMMAND CODES

Application Information

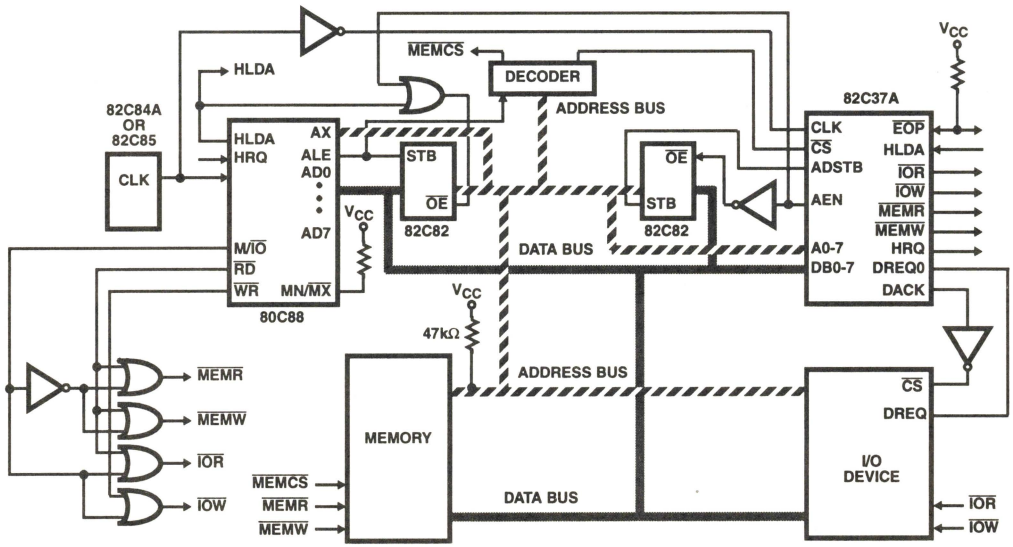
Figure 6 shows an application for a DMA system utilizing the 82C37A DMA controller and the 80C88 Microprocessor. In this application, the 82C37A DMA controller is used to improve system performance by allowing an I/O device to transfer data directly to or from system memory.

Components

The system clock is generated by the 82C84A clock driver and is inverted to meet the clock high and low times required by the 82C37A DMA controller. The four OR gates are used to support the 80C88 Microprocessor in minimum mode by producing the control signals used by the processor to access memory or I/O. A decoder is used to generate chip select for the DMA controller and memory. The most significant bits of the address are output on the address/data bus. Therefore, the 82C82 octal latch is used to demultiplex the address. Hold Acknowledge (HLDA) and Address Enable (AEN) are "ORed" together to insure that the DMA controller does not have bus contention with the microprocessor.

Operation

A DMA request (DREQ) is generated by the I/O device. After receiving the DMA request, the DMA controller will issue a Hold request (HRQ) to the processor. The system busses are not released to the DMA controller until a Hold Acknowledge signal is returned to the DMA controller from the 80C88 processor. After the Hold Acknowledge has been received, addresses and control signals are generated by the DMA controller to accomplish the DMA transfers. Data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active. Note that data is not read into or driven out of the DMA controller in I/O-to-memory or memory-to-I/O data transfers.



NOTE: The address lines need pull-up resistors.

FIGURE 6. APPLICATION FOR DMA SYSTEM

Figure 7 shows an application for a DMA system using the 82C37A DMA controller and the 80C286 Microprocessor.

In this application, the system clock comes from the 82C284 clock generator PCLK signal which is inverted to provide proper READY setup and hold times to the DMA controller in an 80C286 system. The Read and Write signals from the DMA controller may be wired directly to the Read/Write control signals from the 82C288 Bus Controller. The octal latch for A8-A15 from the DMA controller's data bus is on the local 80C286 address bus so that memory chip selects may still be generated during DMA transfers. The transceiver on A0-A7 is controlled by AEN and is not necessary, but may be used to drive a heavily loaded system address bus during transfers. The data bus transceivers simply isolate the DMA controller from the local microprocessor bus and allow programming on the upper or lower half of the data bus.

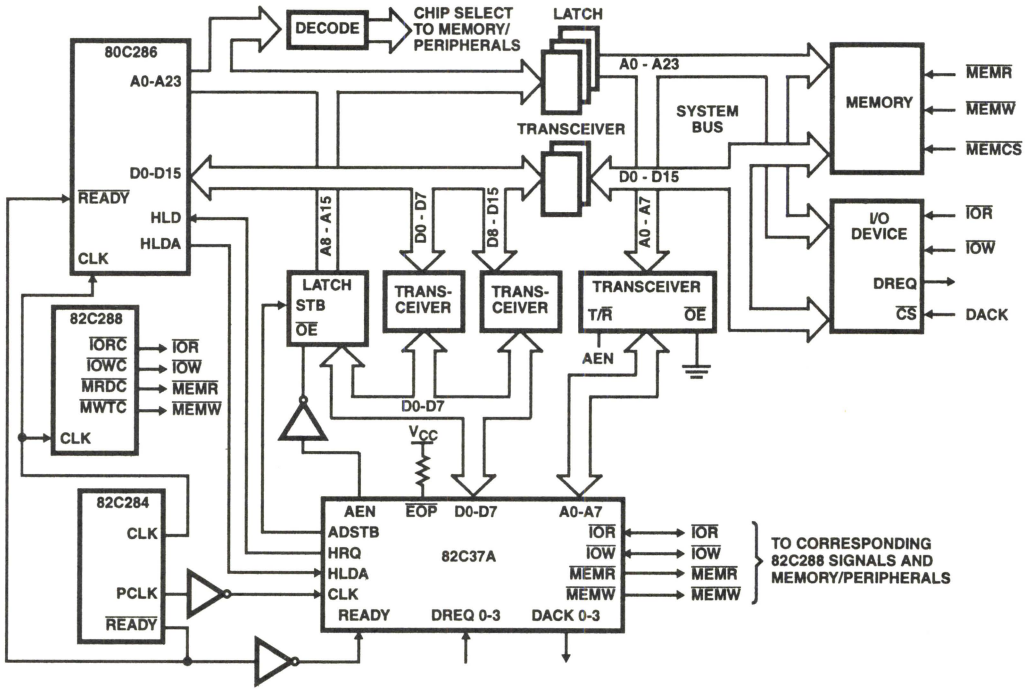


FIGURE 7. 80C286 DMA APPLICATION

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C37A . . . . . 0^oC to $+70^oC$
I82C37A . . . . . -40^oC to $+85^oC$
M82C37A . . . . . -55^oC to $+125^oC$

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	50	10
CLCC Package	65	14
PDIP Package	50	N/A
PLCC Package	46	N/A

Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature Ceramic Package . . . . . $+175^oC$
Maximum Junction Temperature Plastic Package . . . . . $+150^oC$
Maximum Lead Temperature Package
(Soldering 10s) . . . . . $+300^oC$
(PLCC - Lead Tips Only)

Die Characteristics

Gate Count . . . . . 2325 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = +5.0 ±10%, $T_A = 0^oC$ to $+70^oC$ (C82C37A)
$T_A = -40^oC$ to $+85^oC$ (I82C37A)
$T_A = -55^oC$ to $+125^oC$ (M82C37A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2	-	v	C82C37A, I82C37A
		2.2	-	V	M82C37A
VIL	Logical Zero Input Voltage	-	0.8	V	
VIHC	CLK Input Logical One Voltage	V_{CC} -0.8	-	V	
VILC	CLK Input Logical Zero Voltage	-	0.8	V	
VOH	Output HIGH Voltage	3.0	-	V	IOH = -2.5mA
		V_{CC} -0.4	-	V	IOH = -100µA
VOL	Output LOW Voltage	-	0.4	V	IOL = +2.5mA all output except $\overline{EOP}$, IOL = +3.2mA for $\overline{EOP}$ pin 36 only.
II	Input Leakage Current	-1	+1	µA	VIN = GND or V_{CC}, Pins 6, 7, 11-13, 16-19
IO	Output Leakage Current	-10	+10	µA	VOUT = GND or V_{CC}, Pins 1-4, 21-23, 26-30, 32-40
ICCSB	Standby Power Supply Current	-	10	µA	V_{CC} = 5.5V, VIN = V_{CC} or GND, Outputs Open
ICCOP	Operating Power Supply Current	-	2	mA/MHz	V_{CC} = 5.5V, CLK FREQ = Maximum, VIN = V_{CC} or GND, Outputs Open

Capacitance

$T_A = +25^oC$

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
CIN	Input Capacitance	25	pF	FREQ = 1MHz, All measurements are referenced to device GND
COUT	Output Capacitance	40	pF	
CI/O	I/O Capacitance	25	pF	

AC Electrical Specifications

V_{CC} = +5.0V ±10%, GND = 0V, T_A = 0°C to +70°C (C82C37A),
T_A = -40°C to +85°C (I82C37A),
T_A = -55°C to +125°C (M82C37A)

SYMBOL	PARAMETER	82C37A-5		82C37A		82C37A-12		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
DMA (MASTER) MODE								
(1)TAEL	AEN HIGH from CLK LOW (S1) Delay Time	-	175	-	105	-	50	ns
(2)TAET	AEN LOW from CLK HIGH (SI) Delay Time	-	130	-	80	-	50	ns
(3)TAFAB	ADR Active to Float Delay from CLK HIGH	-	90	-	55	-	55	ns
(4)TAFC	$\overline{READ}$ or $\overline{WRITE}$ Float Delay from CLK HIGH	-	120	-	75	-	50	ns
(5)TAFDB	DB Active to Float Delay from CLK HIGH	-	170	-	135	-	90	ns
(6)TAHR	ADR from $\overline{READ}$ HIGH Hold Time	TCY-100	-	TCY-75	-	TCY-65	-	ns
(7)TAHS	DB from ADSTB LOW Hold Time	TCL-18	-	TCL-18	-	TCL-18	-	ns
(8)TAHW	ADR from $\overline{WRITE}$ HIGH Hold Time	TCY-65	-	TCY-65	-	TCY-50	-	ns
(9)TAK	DACK Valid from CLK LOW Delay Time	-	170	-	105	-	69	ns
	$\overline{EOP}$ HIGH from CLK HIGH Delay Time	-	170	-	105	-	90	ns
	$\overline{EOP}$ LOW from CLK HIGH Delay Time	-	100	-	60	-	35	ns
(10)TASM	ADR Stable from CLK HIGH	-	110	-	60	-	50	ns
(11)TASS	DB to ADSTB LOW Setup Time	TCH-20	-	TCH-20	-	TCH-20	-	ns
(12)TCH	CLK HIGH Time (Transitions 10ns)	70	-	55	-	30	-	ns
(13)TCL	CLK LOW Time (Transitions 10ns)	50	-	43	-	30	-	ns
(14)TCY	CLK Cycle Time	200	-	125	-	80	-	ns
(15)TDCL	CLK HIGH to $\overline{READ}$ or $\overline{WRITE}$ LOW Delay	-	190	-	130	-	120	ns
(16)TDCTR	$\overline{READ}$ HIGH from CLK HIGH (S4) Delay Time	-	190	-	115	-	80	ns
(17)TDCTW	$\overline{WRITE}$ HIGH from CLK HIGH (S4) Delay Time	-	130	-	80	-	70	ns
(18)TDQ	HRQ Valid from CLK HIGH Delay Time	-	120	-	75	-	30	ns
(19)TEPH	$\overline{EOP}$ Hold Time from CLK LOW (S2)	90	-	90	-	50	-	ns
(20)TEPS	$\overline{EOP}$ LOW to CLK LOW Setup Time	40	-	25	-	0	-	ns

AC Electrical Specifications V_{CC} = +5.0V ±10%, GND = 0V, T_A = 0°C to +70°C (C82C37A), T_A = -40°C to +85°C (I82C37A), T_A = -55°C to +125°C (M82C37A) **(Continued)**

SYMBOL	PARAMETER	82C37A-5		82C37A		82C37A-12		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
(21)TEPW	$\overline{EOP}$ Pulse Width	220	-	135	-	50	-	ns
(22)TFAAB	ADR Valid Delay from CLK HIGH	-	110	-	60	-	50	ns
(23)TFAC	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK HIGH	-	150	-	90	-	50	ns
(24)TFADB	DB Valid Delay from CLK HIGH	-	110	-	60	-	45	ns
(25)THS	HLDA Valid to CLK HIGH Setup Time	75	-	45	-	10	-	ns
(26)TIDH	Input Data from $\overline{MEMR}$ HIGH Hold Time	0	-	0	-	0	-	ns
(27)TIDS	Input Data to $\overline{MEMR}$ HIGH Setup Time	155	-	90	-	45	-	ns
(28)TODH	Output Data from $\overline{MEMW}$ HIGH Hold Time	15	-	15	-	TCY-50	-	ns
(29)TODV	Output Data Valid to $\overline{MEMW}$ HIGH	TCY-35	-	TCY-35	-	TCY-10	-	ns
(30)TQS	DREQ to CLK LOW (SI, S4) Setup Time	0	-	0	-	0	-	ns
(31)TRH	CLK to READY LOW Hold Time	20	-	20	-	10	-	ns
(32)TRS	READY to CLK LOW Setup Time	60	-	35	-	15	-	ns
(33)TCLSH	ADSTB HIGH from CLK LOW Delay Time	-	80	-	70	-	70	ns
(34)TCLSL	ADSTB LOW from CLK LOW Delay Time	-	120	-	120	-	60	ns
(35)TWRRD	$\overline{READ}$ HIGH Delay from $\overline{WRITE}$ HIGH	0	-	0	-	5	-	ns
(36)TRLRH	$\overline{READ}$ Pulse Width, Normal Timing	2TCY-60	-	2TCY-60	-	2TCY-55	-	ns
(37)TSHSL	ADSTB Pulse Width	TCY-80	-	TCY-50	-	TCY-35	-	ns
(38)TWLWHA	Extended $\overline{WRITE}$ Pulse Width	2TCY-100	-	2TCY-85	-	2TCY-80	-	ns
(39)TWLWH	$\overline{WRITE}$ Pulse Width	TCY-100	-	TCY-85	-	TCY-80	-	ns
(40)TRLRHC	$\overline{READ}$ Pulse Width, Compressed	TCY-60	-	TCY-60	-	TCY-55	-	ns
(56)TAVRL	ADR Valid to $\overline{READ}$ LOW	17	-	17	-	17	-	ns
(57)TAVWL	ADR Valid to $\overline{WRITE}$ LOW	7	-	7	-	7	-	ns
(58)TRHAL	$\overline{READ}$ HIGH to AEN LOW	15	-	15	-	15	-	ns
(59)TRHSH	$\overline{READ}$ HIGH to ADSTB HIGH	13	-	13	-	13	-	ns
(60)TWHSH	$\overline{WRITE}$ HIGH to ADSTB HIGH	15	-	15	-	15	-	ns
(61)TDVRL	DACK Valid to $\overline{READ}$ LOW	25	-	25	-	25	-	ns

AC Electrical Specifications V_{CC} = +5.0V ±10%, GND = 0V, T_A = 0°C to +70°C (C82C37A), T_A = -40°C to +85°C (I82C37A), T_A = -55°C to +125°C (M82C37A) **(Continued)**

SYMBOL	PARAMETER	82C37A-5		82C37A		82C37A-12		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
(62)TDVWL	DACK Valid to $\overline{\text{WRITE}}$ LOW	25	-	25	-	25	-	ns
(63)TRHDI	$\overline{\text{READ}}$ HIGH to DACK Inactive	12	-	12	-	12	-	ns
(64)TAZRL	ADR Float to $\overline{\text{READ}}$ LOW	-2.5	-	-2.5	-	-2.5	-	ns
PERIPHERAL (SLAVE) MODE								
(41)TAR	ADR Valid or $\overline{\text{CS}}$ LOW to $\overline{\text{READ}}$ LOW	10	-	10	-	0	-	ns
(42)TAWL	ADR Valid to $\overline{\text{WRITE}}$ LOW Setup Time	0	-	0	-	0	-	ns
(43)TCWL	$\overline{\text{CS}}$ LOW to $\overline{\text{WRITE}}$ LOW Setup Time	0	-	0	-	0	-	ns
(44)TDW	Data Valid to $\overline{\text{WRITE}}$ HIGH Setup Time	150	-	100	-	60	-	ns
(45)TRA	ADR or $\overline{\text{CS}}$ Hold from $\overline{\text{READ}}$ HIGH	0	-	0	-	0	-	ns
(46)TRDE	Data Access from $\overline{\text{READ}}$	-	140	-	120	-	80	ns
(47)TRDF	DB Float Delay from $\overline{\text{READ}}$ HIGH	5	85	5	85	5	55	ns
(48)TRSTD	Power Supply HIGH to RESET LOW Setup Time	500	-	500	-	500	-	ns
(49)TRSTS	RESET to First $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$	2TCY	-	2TCY	-	2TCY	-	ns
(50)TRSTW	RESET Pulse Width	300	-	300	-	300	-	ns
(51)TRW	$\overline{\text{READ}}$ Pulse Width	200	-	155	-	85	-	ns
(52)TWA	ADR from $\overline{\text{WRITE}}$ HIGH Hold Time	0	-	0	-	0	-	ns
(53)TWC	$\overline{\text{CS}}$ HIGH from $\overline{\text{WRITE}}$ HIGH Hold Time	0	-	0	-	0	-	ns
(54)TWD	Data from $\overline{\text{WRITE}}$ HIGH Hold Time	10	-	10	-	10	-	ns
(55)TWWS	$\overline{\text{WRITE}}$ Pulse Width	150	-	100	-	45	-	ns

Timing Waveforms

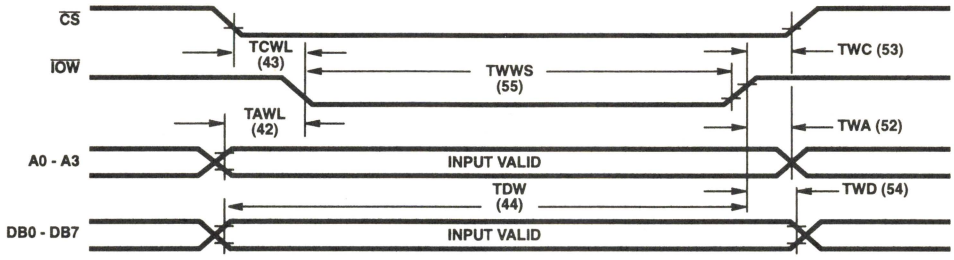


FIGURE 8. SLAVE MODE WRITE

NOTE: Successive WRITE accesses to the 82C37A must allow at least TCY as recovery time between accesses. A TCY recovery time must be allowed before executing a WRITE access after a READ access.

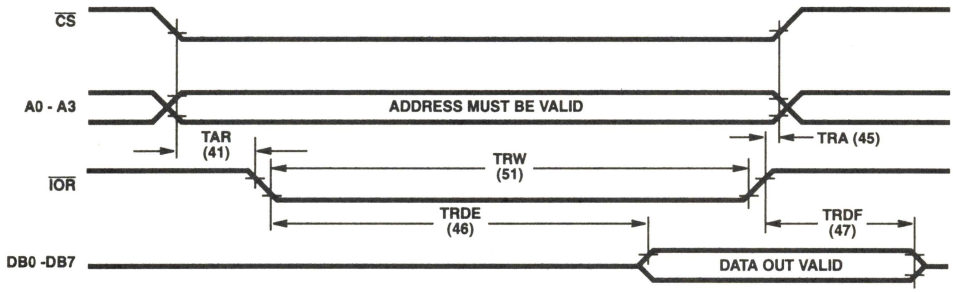


FIGURE 9. SLAVE MODE READ

NOTE: Successive READ accesses to the 82C37A must allow at least TCY as recovery time between accesses. A TCY recovery time must be allowed before executing a READ access after a WRITE access.

Timing Waveforms (Continued)

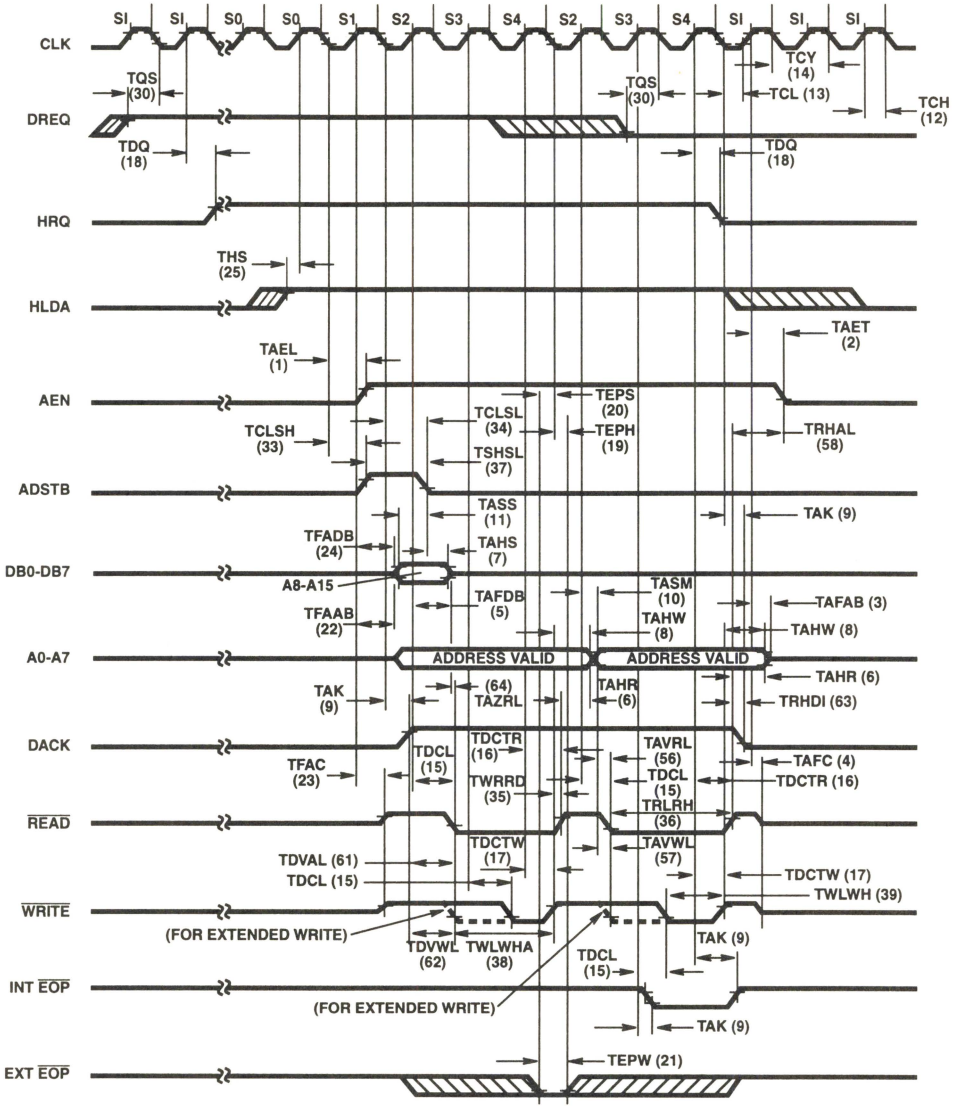


FIGURE 10. DMA TRANSFER

Timing Waveforms (Continued)

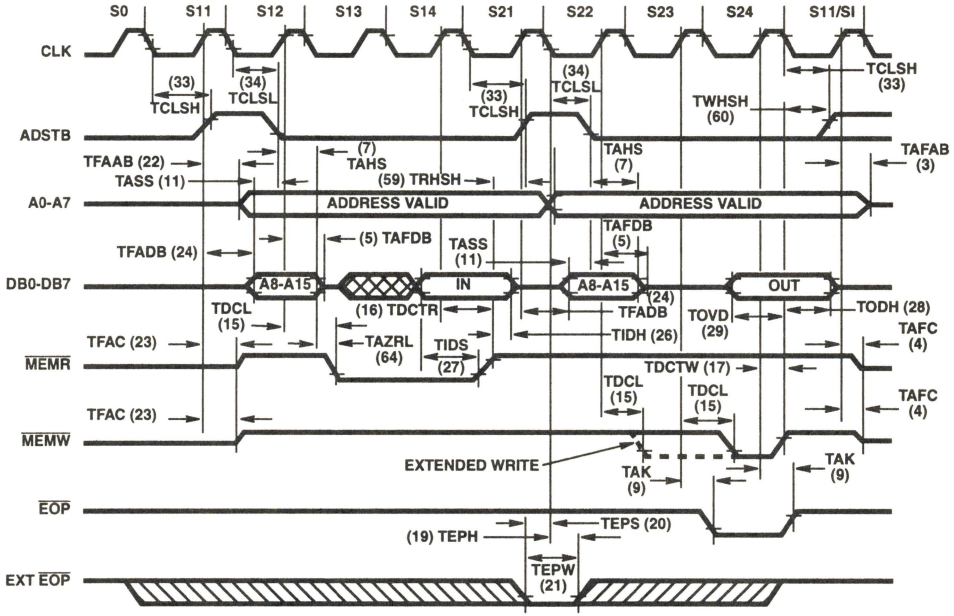


FIGURE 11. MEMORY-TO-MEMORY TRANSFER

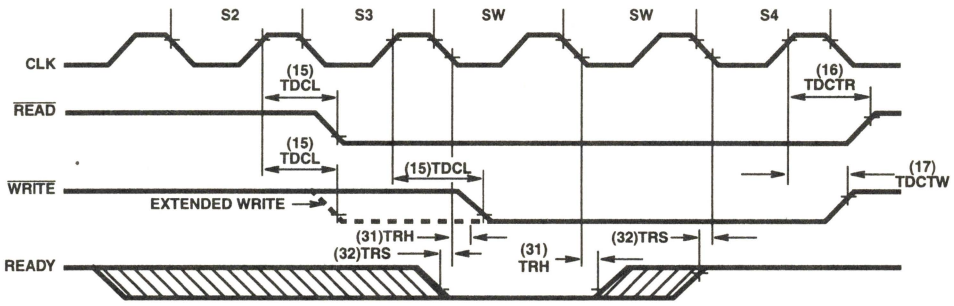


FIGURE 12. READY

NOTE: READY must not transition during the specified setup and hold times.

Timing Waveforms (Continued)

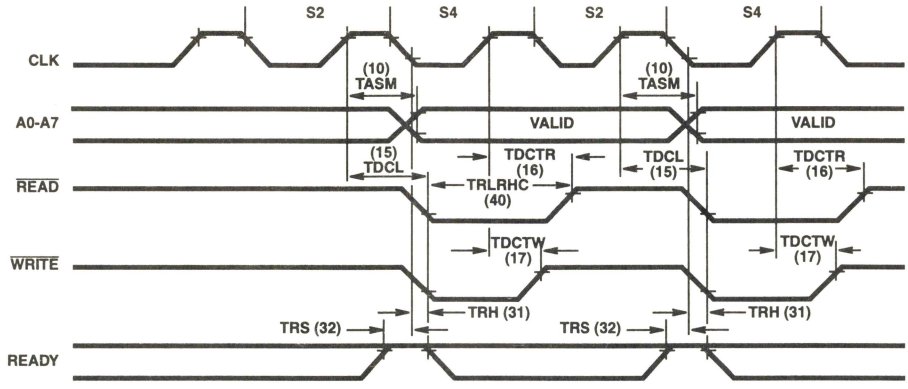


FIGURE 13. COMPRESSED TRANSFER

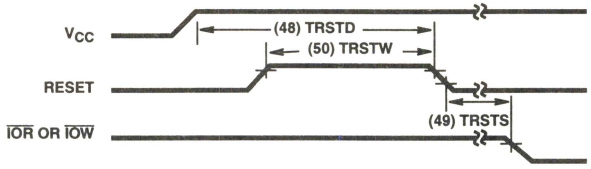
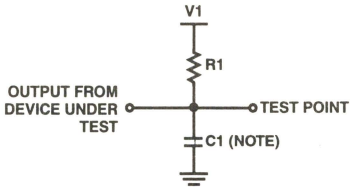


FIGURE 14. RESET

AC Test Circuits

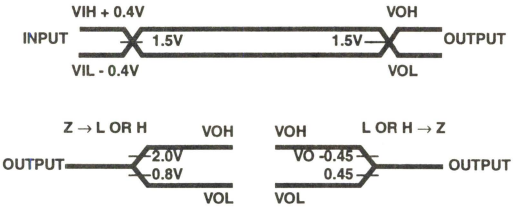


NOTE: Includes STRAY and FIXTURE Capacitance

TEST CONDITION DEFINITION TABLE

PINS	V1	R1	C1
All Outputs Except $\overline{EOP}$	1.7V	520Ω	100pF
$\overline{EOP}$	V_{CC}	1.6kΩ	50pF

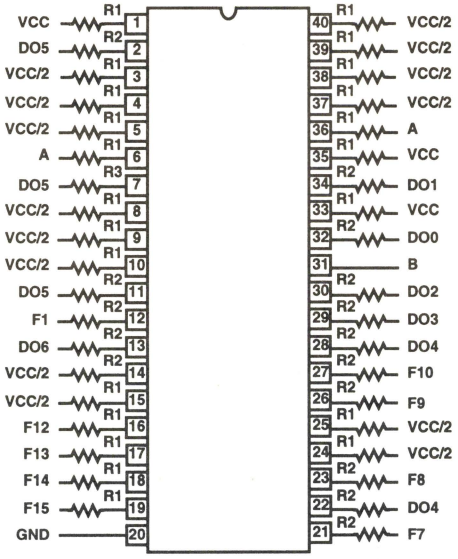
AC Testing Input, Output Waveforms



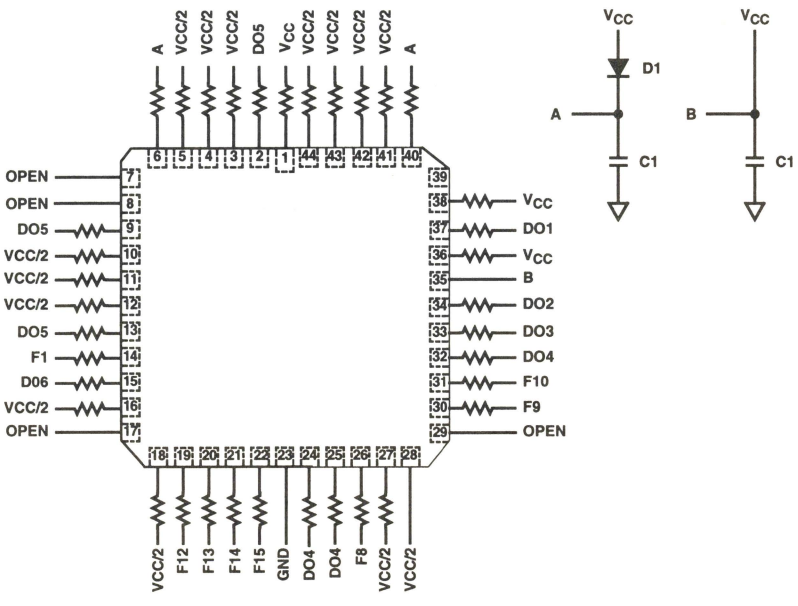
NOTE: AC Testing: All AC Parameters tested as per test circuits. Input RISE and FALL times are driven at Ins/V. CLK input must switch between VIHC +0.4V and VILC -0.4V

Burn-In Circuits

MD82C37A CERDIP



MR82C37A CLCC



NOTES:

1. V_{CC} = 5.5V ± 0.5V
2. VIH = 4.5V ± 10%
3. VIL = -0.2V to 0.4V
4. GND = 0V
5. R1 = 1.2kΩ ±5%
6. R2 = 47kΩ ±5%
7. C1 = 0.01µF minimum
8. C2 = 0.1µF minimum
9. D1 = 1N4002
10. F0 = 100kHz ±10%
11. F1 = F0/2, F2 = F1/2,..., F15 = F14/2
12. DO0 - DO6 are outputs from the 82C82 Octal Latching Bus Driver

Die Characteristics

DIE DIMENSIONS:

148 x 159 x 19 ±1mils
(3760- x 4040 x 525µm)

METALLIZATION:

Type: SiAlCu
Thickness: Metal 1: 8kÅ ± 0.75kÅ
Thickness: Metal 2: 12kÅ ± 1.0kÅ

GLASSIVATION:

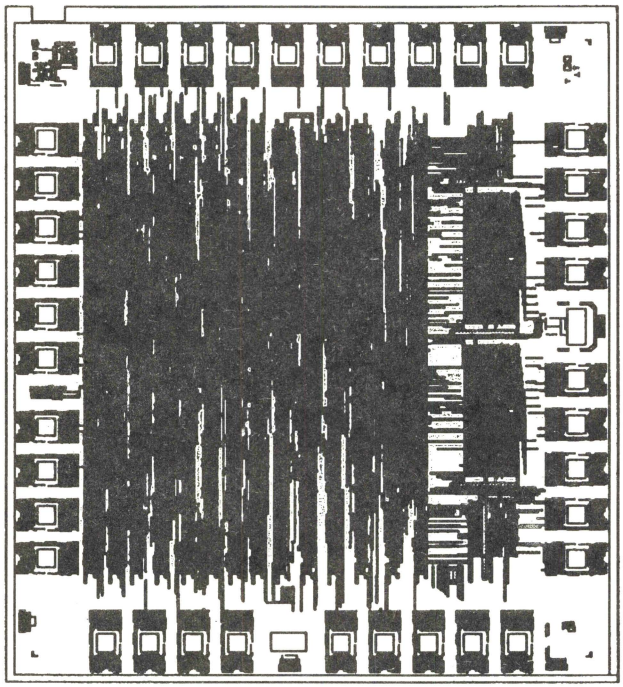
Type: Nitrox
Thickness: 10kÅ ± 3kÅ

WORST CASE CURRENT DENSITY:

0.6×10^5 A/cm^2

Metallization Mask Layout

82C37A



March 1997

CMOS Programmable Interval Timer

Features

- 8MHz to 12MHz Clock Input Frequency
- Compatible with NMOS 8254
  - Enhanced Version of NMOS 8253
- Three Independent 16-Bit Counters
- Six Programmable Counter Modes
- Status Read Back Command
- Binary or BCD Counting
- Fully TTL Compatible
- Single 5V Power Supply
- Low Power
  - ICCSB 10μA
  - ICCOP ..... 10mA at 8MHz
- Operating Temperature Ranges
  - C82C54 ..... 0°C to +70°C
  - I82C54 ..... -40°C to +85°C
  - M82C54 ..... -55°C to +125°C

Description

The Harris 82C54 is a high performance CMOS Programmable Interval Timer manufactured using an advanced 2 micron CMOS process.

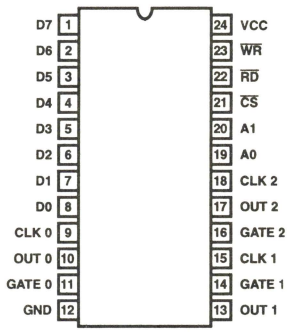
The 82C54 has three independently programmable and functional 16-bit counters, each capable of handling clock input frequencies of up to 8MHz (82C54) or 10MHz (82C54-10) or 12MHz (82C54-12).

The high speed and industry standard configuration of the 82C54 make it compatible with the Harris 80C86, 80C88, and 80C286 CMOS microprocessors along with many other industry standard processors. Six programmable timer modes allow the 82C54 to be used as an event counter, elapsed time indicator, programmable one-shot, and many other applications. Static CMOS circuit design insures low power operation.

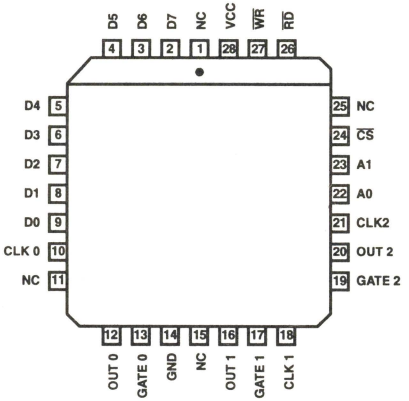
The Harris advanced CMOS process results in a significant reduction in power with performance equal to or greater than existing equivalent products.

Pinouts

82C54 (PDIP, CERDIP, SOIC)
TOP VIEW



82C54 (PLCC/CLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

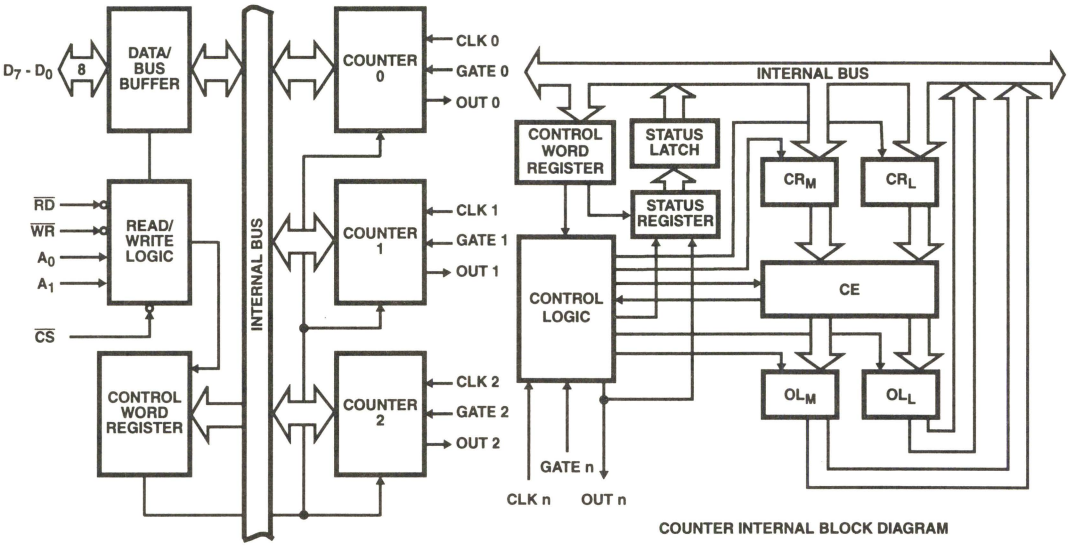
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File Number **2970.1**

Ordering Information

PART NUMBERS			TEMPERATURE RANGE	PACKAGE	PKG. NO.
8MHz	10MHz	12MHz			
CP82C54	CP82C54-10	CP82C54-12	0°C to +70°C	24 Lead PDIP	E24.6
IP82C54	IP82C54-10	IP82C54-12	-40°C to +85°C	24 Lead PDIP	E24.6
CS82C54	CS82C54-10	CS82C54-12	0°C to +70°C	28 Lead PLCC	N28.45
IS82C54	IS82C54-10	IS82C54-12	-40°C to +85°C	28 Lead PLCC	N28.45
CD82C54	CD82C54-10	CD82C54-12	0°C to +70°C	24 Lead CERDIP	F24.6
ID82C54	ID82C54-10	ID82C54-12	-40°C to +85°C	24 Lead CERDIP	F24.6
MD82C54/B	MD82C54-10/B	MD82C54-12/B	-55°C to +125°C	24 Lead CERDIP	F24.6
MR82C54/B	MR82C54-10/B	MR82C54-12/B	-55°C to +125°C	28 Lead CLCC	J28.A
SMD # 8406501JA	-	8406502JA	-55°C to +125°C	24 Lead CERDIP	F24.6
SMD# 84065013A	-	84065023A	-55°C to +125°C	28 Lead CLCC	J28.A
CM82C54	CM82C54-10	CM82C54-12	0°C to +70°C	24 Lead SOIC	M24.3

Functional Diagram



COUNTER INTERNAL BLOCK DIAGRAM

Pin Description

SYMBOL	DIP PIN NUMBER	TYPE	DEFINITION
D7 - D0	1 - 8	I/O	DATA: Bi-directional three-state data bus lines, connected to system data bus.
CLK 0	9	I	CLOCK 0: Clock input of Counter 0.
OUT 0	10	O	OUT 0: Output of Counter 0.
GATE 0	11	I	GATE 0: Gate input of Counter 0.
GND	12		GROUND: Power supply connection.
OUT 1	13	O	OUT 1: Output of Counter 1.
GATE 1	14	I	GATE 1: Gate input of Counter 1.
CLK 1	15	I	CLOCK 1: Clock input of Counter 1.
GATE 2	16	I	GATE 2: Gate input of Counter 2.
OUT 2	17	O	OUT 2: Output of Counter 2.

Pin Description (Continued)

SYMBOL	DIP PIN NUMBER	TYPE	DEFINITION
CLK 2	18	I	CLOCK 2: Clock input of Counter 2.
A0, A1	19 - 20	I	ADDRESS: Select inputs for one of the three counters or Control Word Register for read/write operations. Normally connected to the system address bus.

A1	A0	SELECTS
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

$\overline{CS}$	21	I	CHIP SELECT: A low on this input enables the 82C54 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
$\overline{RD}$	22	I	READ: This input is low during CPU read operations.
$\overline{WR}$	23	I	WRITE: This input is low during CPU write operations.
V_{CC}	24		V_{CC}: The +5V power supply pin. A 0.1μF capacitor between pins VCC and GND is recommended for decoupling.

Functional Description

General

The 82C54 is a programmable interval timer/counter designed for use with microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 82C54 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 82C54 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 82C54 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other computer/timer functions common to microcomputers which can be implemented with the 82C54 are:

- Real time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Data Bus Buffer

This three-state, bi-directional, 8-bit buffer is used to interface the 82C54 to the system bus (see Figure 1).

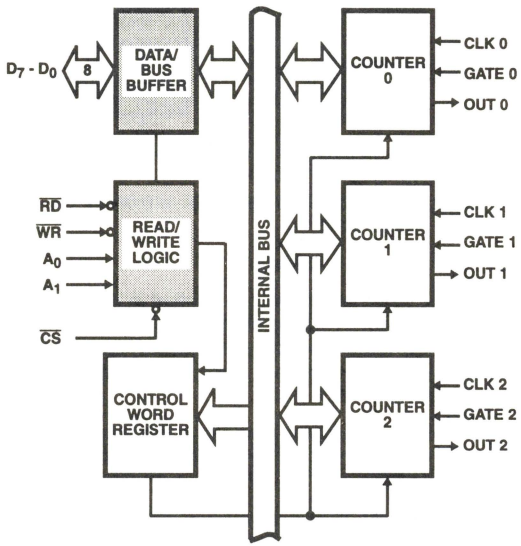


FIGURE 1. DATA BUS BUFFER AND READ/WRITE LOGIC FUNCTIONS

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 82C54. A1 and A0 select one of the three counters or the Control Word Register to be read from/written into. A "low" on the $\overline{RD}$ input tells the 82C54 that the CPU is reading one of the counters. A "low" on the $\overline{WR}$ input tells the 82C54 that the CPU is writing either a Control Word or an initial count. Both $\overline{RD}$ and $\overline{WR}$ are qualified by $\overline{CS}$; $\overline{RD}$ and $\overline{WR}$ are ignored unless the 82C54 has been selected by holding $\overline{CS}$ low.

Control Word Register

The Control Word Register (Figure 2) is selected by the Read/Write Logic when A1, A0 = 11. If the CPU then does a write operation to the 82C54, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the Counter operation.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

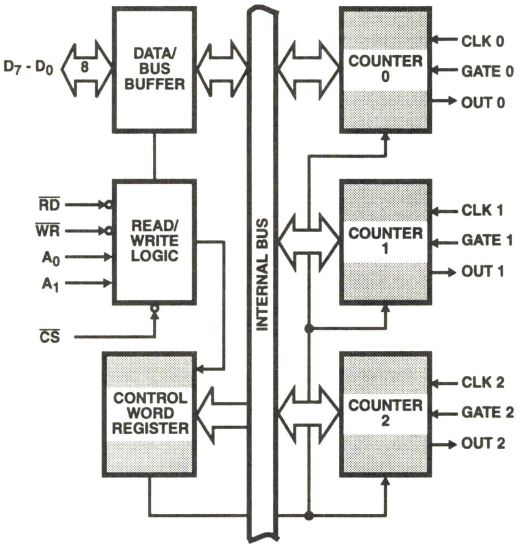


FIGURE 2. CONTROL WORD REGISTER AND COUNTER FUNCTIONS

Counter 0, Counter 1, Counter 2

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a signal counter is shown in Figure 3. The counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

The status register, shown in the figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

The actual counter is labeled CE (for Counting Element). It is a 16-bit presettable synchronous down counter.

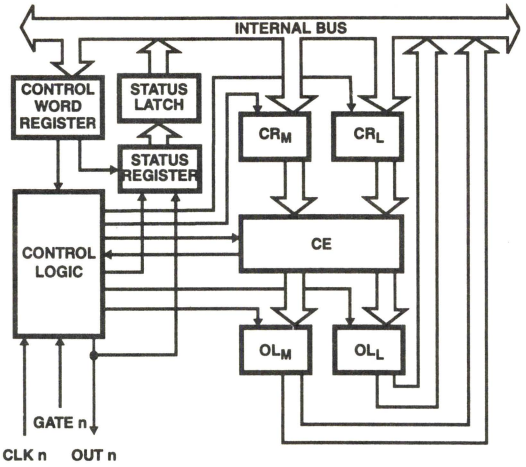


FIGURE 3. COUNTER INTERNAL BLOCK DIAGRAM

OLM and OLL are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L for "Most significant byte" and "Least significant byte", respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the 82C54, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CRM and CRL (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CRM and CRL are cleared when the Counter is programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.

82C54 System Interface

The 82C54 is treated by the system software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method or it can be connected to the output of a decoder.

Operational Description

General

After power-up, the state of the 82C54 is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the 82C54

Counters are programmed by writing a Control Word and then an initial count.

All Control Words are written into the Control Word Register, which is selected when A1, A0 = 11. The Control Word specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A1, A0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

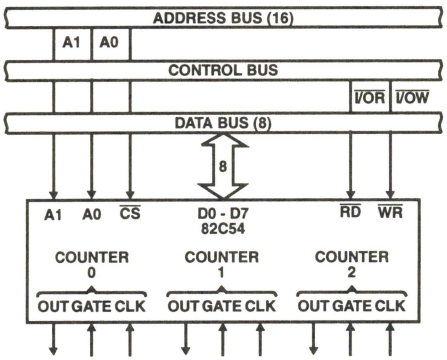


FIGURE 4. 82C54 SYSTEM INTERFACE

Write Operations

The programming procedure for the 82C54 is very flexible. Only two conventions need to be remembered:

1. For Each Counter, the Control Word must be written before the initial count is written.
2. The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A1, A0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

Control Word Format

A1, A0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC - Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW - Read/Write

RW1	RW0	
0	0	Counter Latch Command (See Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

M - Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD - Binary Coded Decimal

0	Binary Counter 16-bit
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

Possible Programming Sequence

	A1	A0
Control Word - Counter 0	1	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 0	0	0
Control Word - Counter 1	1	1
LSB of Count - Counter 1	0	1
MSB of Count - Counter 1	0	1
Control Word - Counter 2	1	1
LSB of Count - Counter 2	1	0
MSB of Count - Counter 2	1	0

Possible Programming Sequence

	A1	A0
Control Word - Counter 0	1	1
Control Word - Counter 1	1	1
Control Word - Counter 2	1	1
LSB of Count - Counter 2	1	0

Possible Programming Sequence (Continued)

	A1	A0
LSB of Count - Counter 1	0	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 0	0	0
MSB of Count - Counter 1	0	1
MSB of Count - Counter 2	1	0

Possible Programming Sequence

	A1	A0
Control Word - Counter 2	1	1
Control Word - Counter 1	1	1
Control Word - Counter 0	1	1
LSB of Count - Counter 2	1	0
MSB of Count - Counter 2	1	0
LSB of Count - Counter 1	0	1
MSB of Count - Counter 1	0	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 0	0	0

Possible Programming Sequence

	A1	A0
Control Word - Counter 1	1	1
Control Word - Counter 0	1	1
LSB of Count - Counter 1	0	1
Control Word - Counter 2	1	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 1	0	1
LSB of Count - Counter 2	1	0
MSB of Count - Counter 0	0	0
MSB of Count - Counter 2	1	0

NOTE: In all four examples, all counters are programmed to Read/Write two-byte counts. These are only four of many programming sequences.

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies. A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 82C54.

There are three possible methods for reading the Counters. The first is through the Read-Back command, which is explained later. The second is a simple read operation of the Counter, which is selected with the A1, A0 inputs. The only requirement is that the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in process of changing when it is read, giving an undefined result.

Counter Latch Command

The other method for reading the Counters involves a special software command called the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when A1, A0 = 11. Also, like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.

A1, A0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 - specify counter to be latched

SC1	SC0	COUNTER
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5, D4 - 00 designates Counter Latch Command, X - Don't Care.
NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

The selected Counter's output latch (OL) latches the count when the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the 82C54 is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a counter is programmed to read or write two-byte counts, the following precaution applies: A program MUST NOT transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

Read-Back Command

The read-back command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Figure 5. The command applies to the counters selected by setting their corresponding bits D3, D2, D1 = 1.

A0, A1 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT 2	CNT 1	CNT 0	0

D5: 0 = Latch count of selected Counter (s)
D4: 0 = Latch status of selected Counter(s)
D3: 1 = Select Counter 2
D2: 1 = Select Counter 1
D1: 1 = Select Counter 0
D0: Reserved for future expansion; Must be 0

FIGURE 5. READ-BACK COMMAND FORMAT

The read-back command may be used to latch multiple counter output latches (OL) by setting the COUNT bit D5 = 0 and selecting the desired counter(s). This signal command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the count, all but the first are ignored; i.e., the count which will be read is the count at the time the first read-back command was issued.

The read-back command may also be used to latch status information of selected counter(s) by setting STATUS bit D4 = 0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in Figure 6. Bits D5 through D0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

D7	D6	D5	D4	D3	D2	D1	D0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D7: 1 = Out pin is 1
0 = Out pin is 0
D6: 1 = Null count
0 = Count available for reading
D5 - D0 = Counter programmed mode (See Control Word Formats)

FIGURE 6. STATUS BYTE

NULL COUNT bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the counter is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown below.

THIS ACTION: **CAUSES:**

A. Write to the control word register:(1) . . . . . Null Count = 1
B. Write to the count register (CR):(2) . . . . . Null Count = 1
C. New count is loaded into CE (CR - CE) . . . . . Null Count = 0

(1) Only the counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected.

(2) If the counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to 1 when the second byte is written.

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

COMMANDS								DESCRIPTION	RESULT
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	0	0	1	0	Read-Back Count and Status of Counter 0	Count and Status Latched for Counter 0
1	1	1	0	0	1	0	0	Read-Back Status of Counter 1	Status Latched for Counter 1
1	1	1	0	1	1	0	0	Read-Back Status of Counters 2, 1	Status Latched for Counter 2, But Not Counter 1
1	1	0	1	1	0	0	0	Read-Back Count of Counter 2	Count Latched for Counter 2
1	1	0	0	0	1	0	0	Read-Back Count and Status of Counter 1	Count Latched for Counter 1, But Not Status
1	1	1	0	0	0	1	0	Read-Back Status of Counter 1	Command Ignored, Status Already Latched for Counter 1

FIGURE 7. READ-BACK COMMAND EXAMPLE

Both count and status of the selected counter(s) may be latched simultaneously by setting both COUNT and STATUS bits D5, D4 = 0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 7.

If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (Three-State)
1	X	X	X	X	No-Operation (Three-State)
0	1	1	X	X	No-Operation (Three-State)

FIGURE 8. READ/WRITE OPERATIONS SUMMARY

Mode Definitions

The following are defined for use in describing the operation of the 82C54.

CLK PULSE:

A rising edge, then a falling edge, in that order, of a Counter's CLK input.

TRIGGER:

A rising edge of a Counter's Gate input.

COUNTER LOADING:

The transfer of a count from the CR to the CE (See "Functional Description")

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written to the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

(1) Writing the first byte disables counting. Out is set low immediately (no clock pulse required).

(2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the counter as this has already been done.

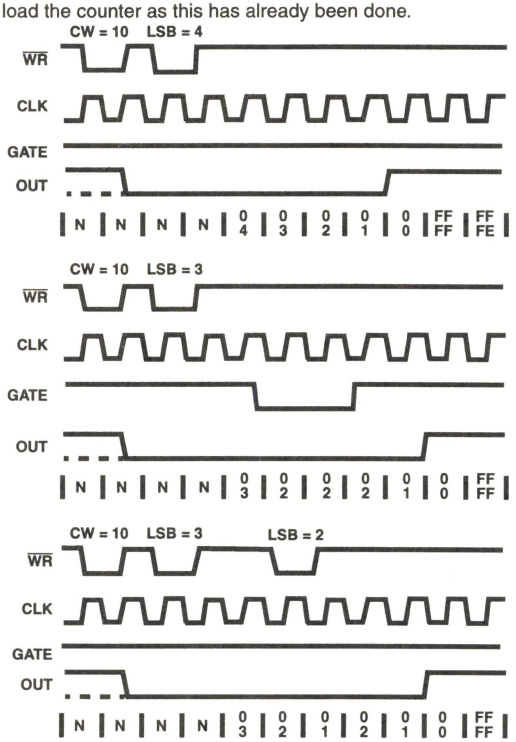


FIGURE 9. MODE 0

NOTES: The following conventions apply to all mode timing diagrams.

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a control word of 10, Hex is written to the counter.
4. LSB stands for Least significant "byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

Mode 1: Hardware Retriggerable One-Shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggerable. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

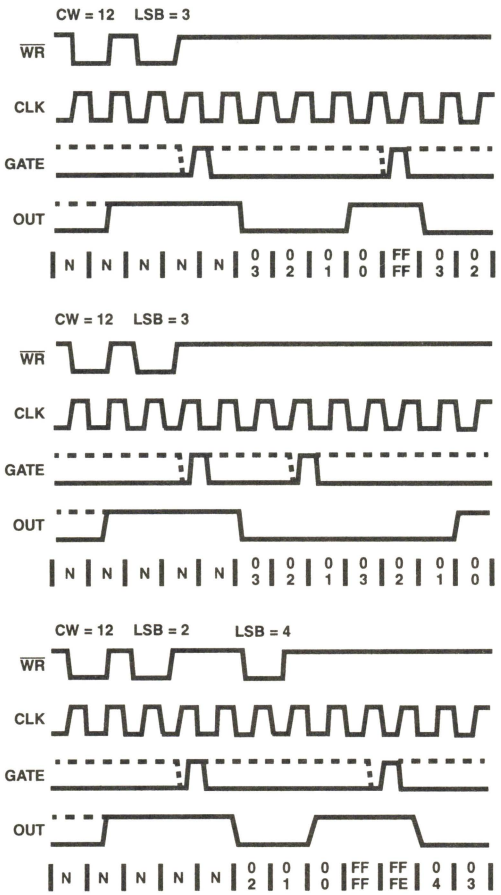


FIGURE 10. MODE 1

Mode 2: Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock Interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the end of the current counting cycle.

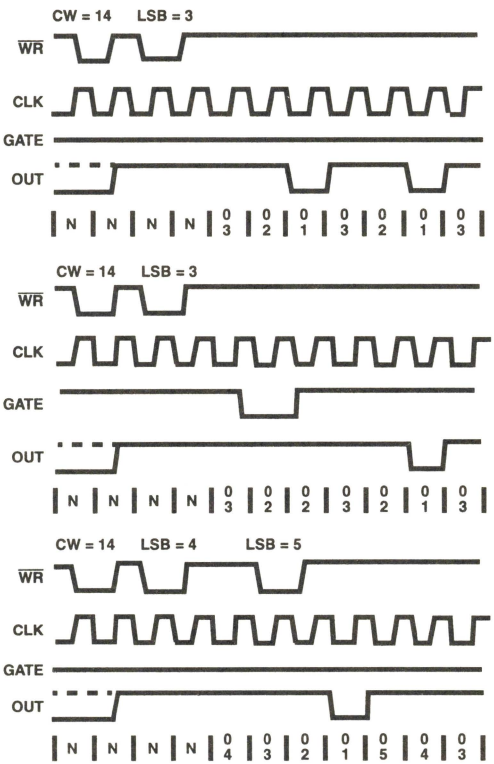


FIGURE 11. MODE 2

Mode 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

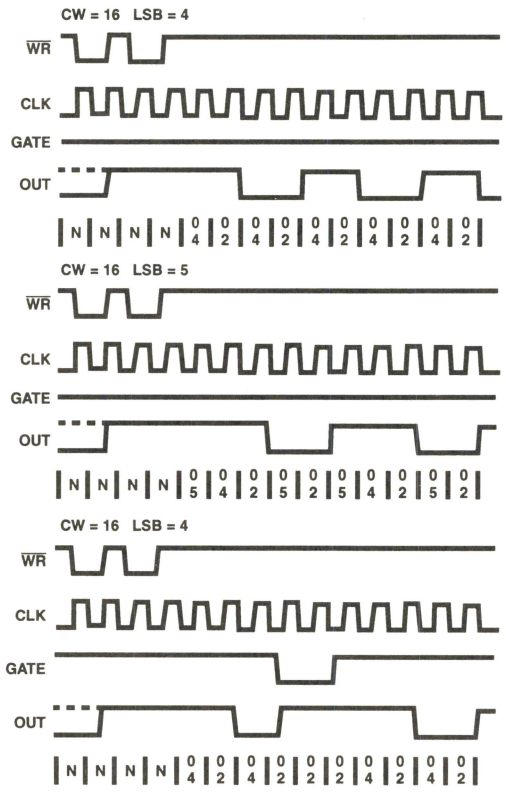


FIGURE 12. MODE 3

Mode 3 is Implemented as Follows:

EVEN COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires, OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

ODD COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse, decremented by one on the next CLK pulse, and then decremented by two on succeeding CLK pulses. When the count expires, OUT goes low and the Counter is reloaded with the initial count. The count is decremented by three on the next CLK pulse, and then by two on succeeding CLK pulses. When the count expires, OUT goes high again and the Counter is reloaded with the initial count. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N + 1)/2 counts and low for (N - 1)/2 counts.

Mode 4: Software Triggered Mode

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse then go high again. The counting sequence is "Triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

(1) Writing the first byte has no effect on counting.

(2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

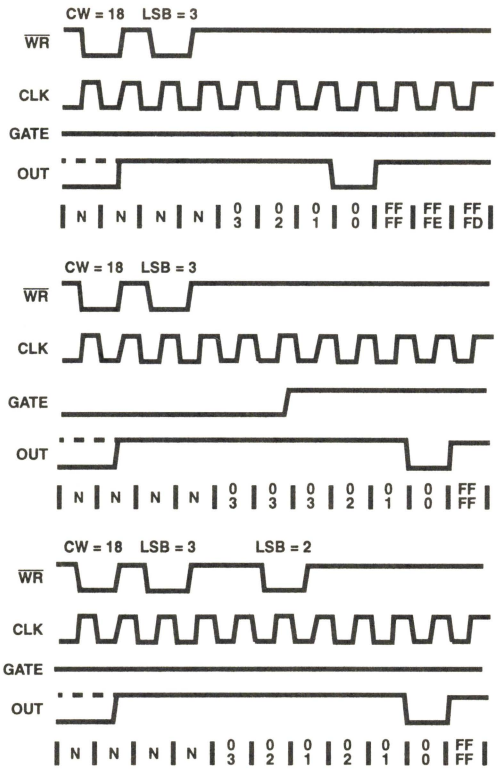


FIGURE 13. MODE 4

Mode 5: Hardware Triggered Strobe (Retriggerable)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is triggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with new count on the next CLK pulse and counting will continue from there.

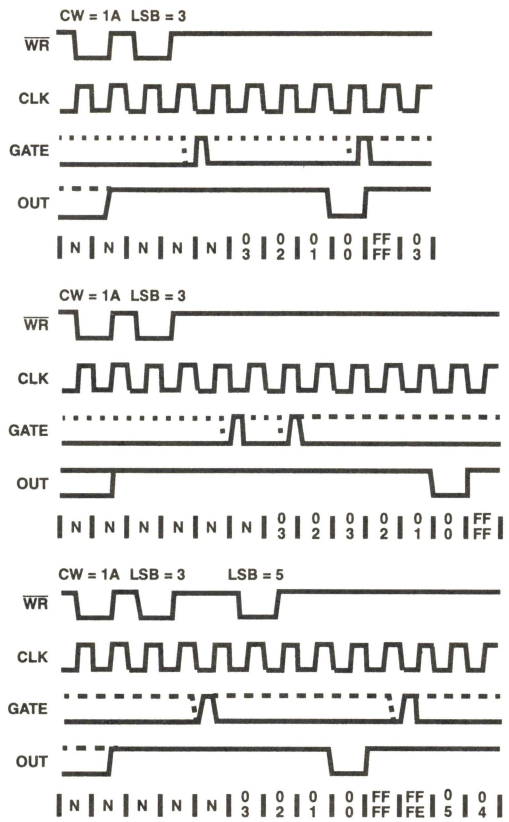


FIGURE 14. MODE 5

Operation Common to All Modes

Programming

When a Control Word is written to a Counter, all Control Logic, is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

Gate

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3 and 4 the GATE input is level sensitive, and logic level is sampled on the rising edge of CLK. In modes 1, 2, 3 and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of Gate (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK. The flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs - a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge- and level-sensitive.

Counter

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The counter does not stop when it reaches zero. In Modes 0, 1, 4, and 5 the Counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

SIGNAL STATUS MODES	LOW OR GOING LOW	RISING	HIGH
0	Disables Counting	-	Enables Counting
1	-	1) Initiates Counting 2) Resets output after next clock	-
2	1) Disables counting 2) Sets output immediately high	Initiates Counting	Enables Counting
3	1) Disables counting 2) Sets output immediately high	Initiates Counting	Enables Counting
4	1) Disables Counting	-	Enables Counting
5	-	Initiates Counting	-

FIGURE 15. GATE PIN OPERATIONS SUMMARY

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

NOTE: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

FIGURE 16. MINIMUM AND MAXIMUM INITIAL COUNTS

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND-0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C54, C82C54-10, -12 . . . . . 0°C to +70°C
I82C54, I82C54-10, -12 . . . . . -40°C to +85°C
M82C54, M82C54-10, -12 . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	55	12
CLCC Package	65	14
PDIP Package	60	N/A
PLCC Package	65	N/A
SOIC Package	75	N/A

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature Ceramic Package . . . . . +175°C
Maximum Junction Temperature Plastic Package . . . . . +150°C
Maximum Lead Temperature Package (Soldering 10s) . . . . +300°C
(PLCC and SOIC - Lean Tips Only)

Die Characteristics

Gate Count . . . . . 2250 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = +5.0V ± 10%, T_A = 0°C to +70°C (C82C54, C82C54-10, C82C54-12)
T_A = -40°C to +85°C (I82C54, I82C54-10, I82C54-12)
T_A = -55°C to +125°C (M82C54, M82C54-10, M82C54-12

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0	-	V	C82C54, I82C54
		2.2	-	V	M82C54
VIL	Logical Zero Input Voltage	-	0.8	V	
VOH	Output HIGH Voltage	3.0	-	V	IOH = -2.5mA
		V_{CC} -0.4	-	V	IOH = -100µA
VOL	Output LOW Voltage	-	0.4	V	IOL = +2.5mA
II	Input Leakage Current	-1	+1	µA	VIN = GND or V_{CC} DIP Pins 9,11,14-16,18-23
IO	Output Leakage Current	-10	+10	µA	VOUT = GND or V_{CC} DIP Pins 1-8
ICCSB	Standby Power Supply Current	-	10	µA	V_{CC} = 5.5V, VIN = GND or V_{CC}, Outputs Open, Counters Programmed
ICCOP	Operating Power Supply Current	-	10	mA	V_{CC} = 5.5V, CLK0 = CLK1 = CLK2 = 8MHz, VIN = GND or V_{CC}, Outputs Open

Capacitance

T_A = +25°C; All Measurements Referenced to Device GND, Note 1

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
CIN	Input Capacitance	20	pF	FREQ = 1MHz
COUT	Output Capacitance	20	pF	FREQ = 1MHz
CI/O	I/O Capacitance	20	pF	FREQ = 1MHz

NOTE:

1. Not tested, but characterized at initial design and at major process/design changes.

AC Electrical Specifications

V_{CC} = +5.0V ± 10%, T_A = 0°C to +70°C (C82C54, C82C54-10, C82C54-12)
T_A = -40°C to +85°C (I82C54, I82C54-10, I82C54-12)
T_A = -55°C to +125°C (M82C54, M82C54-10, M82C54-12)

SYMBOL		PARAMETER	82C54		82C54-10		82C54-12		UNITS	TEST CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE										
(1)	TAR	Address Stable Before $\overline{RD}$	30	-	25	-	25	-	ns	1
(2)	TSR	$\overline{CS}$ Stable Before $\overline{RD}$	0	-	0	-	0	-	ns	1
(3)	TRA	Address Hold Time After $\overline{RD}$	0	-	0	-	0	-	ns	1
(4)	TRR	$\overline{RD}$ Pulse Width	150	-	95	-	95	-	ns	1
(5)	TRD	Data Delay from $\overline{RD}$	-	120	-	85	-	85	ns	1
(6)	TAD	Data Delay from Address	-	210	-	185	-	185	ns	1
(7)	TDF	$\overline{RD}$ to Data Floating	5	85	5	65	5	65	ns	2, Note 1
(8)	TRV	Command Recovery Time	200	-	165	-	165	-	ns	
WRITE CYCLE										
(9)	TAW	Address Stable Before $\overline{WR}$	0	-	0	-	0	-	ns	
(10)	TSW	$\overline{CS}$ Stable Before $\overline{WR}$	0	-	0	-	0	-	ns	
(11)	TWA	Address Hold Time After $\overline{WR}$	0	-	0	-	0	-	ns	
(12)	TWW	$\overline{WR}$ Pulse Width	95	-	95	-	95	-	ns	
(13)	TDW	Data Setup Time Before $\overline{WR}$	140	-	95	-	95	-	ns	
(14)	TWD	Data Hold Time After $\overline{WR}$	25	-	0	-	0	-	ns	
(15)	TRV	Command Recovery Time	200	-	165	-	165	-	ns	
CLOCK AND GATE										
(16)	TCLK	Clock Period	125	DC	100	DC	80	DC	ns	1
(17)	TPWH	High Pulse Width	60	-	30	-	30	-	ns	1
(18)	TPWL	Low Pulse Width	60	-	40	-	30	-	ns	1
(19)	TR	Clock Rise Time	-	25	-	25	-	25	ns	
(20)	TF	Clock Fall Time	-	25	-	25	-	25	ns	
(21)	TGW	Gate Width High	50	-	50	-	50	-	ns	1
(22)	TGL	Gate Width Low	50	-	50	-	50	-	ns	1
(23)	TGS	Gate Setup Time to CLK	50	-	40	-	40	-	ns	1
(24)	TGH	Gate Hold Time After CLK	50	-	50	-	50	-	ns	1
(25)	TOD	Output Delay from CLK	-	150	-	100	-	100	ns	1
(26)	TODG	Output Delay from Gate	-	120	-	100	-	100	ns	1
(27)	TWO	OUT Delay from Mode Write	-	260	-	240	-	240	ns	1
(28)	TWC	CLK Delay for Loading	0	55	0	55	0	55	ns	1
(29)	TWG	Gate Delay for Sampling	-5	40	-5	40	-5	40	ns	1
(30)	TCL	CLK Setup for Count Latch	-40	40	-40	40	-40	40	ns	1

NOTE:

1. Not tested, but characterized at initial design and at major process/design changes.

Timing Waveforms

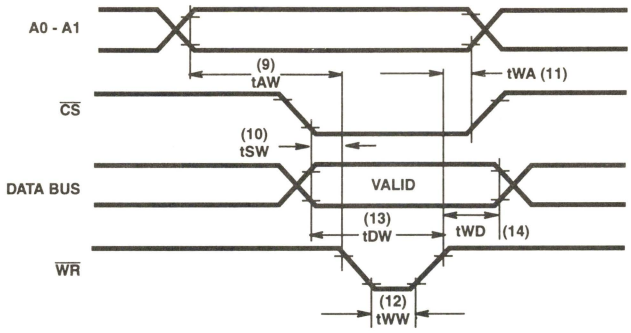


FIGURE 17. WRITE

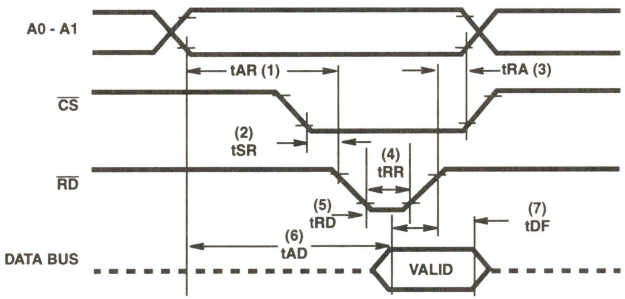


FIGURE 18. READ

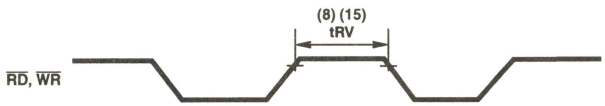


FIGURE 19. RECOVERY

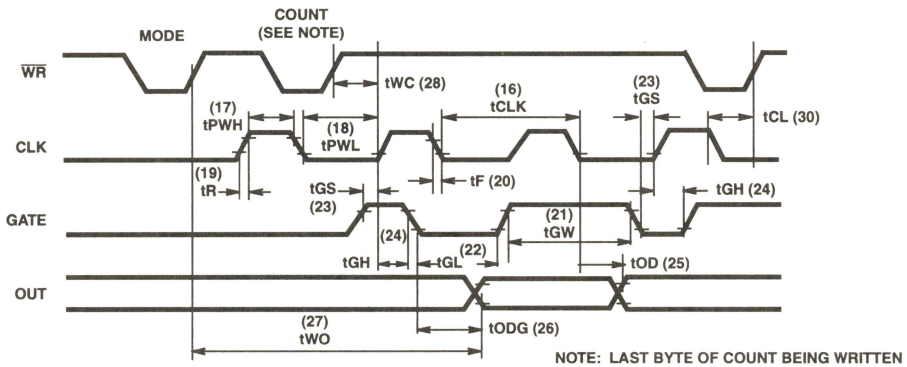
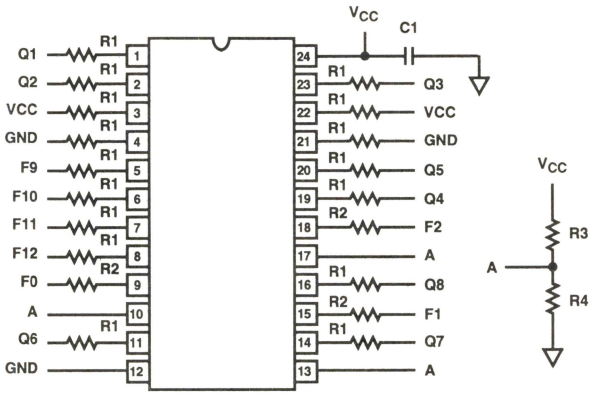


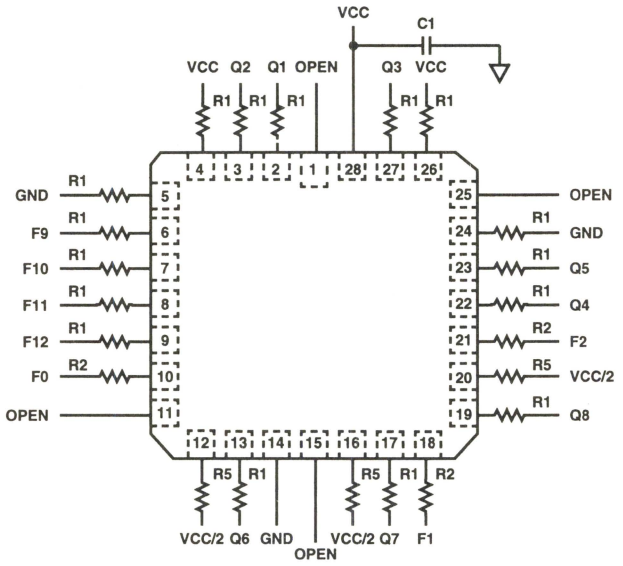
FIGURE 20. CLOCK AND GATE

Burn-In Circuits

MD 82C54 CERDIP



MR 82C54 CLCC



NOTES:

1. V_{CC} = 5.5V ± 0.5V
2. GND = 0V
3. VIH = 4.5V ±10%
4. VIL = -0.2V to 0.4V
5. R1 = 47kΩ ±5%
6. R2 = 1.0kΩ ±5%
7. R3 = 2.7kΩ ±5%
8. R4 = 1.8kΩ ±5%
9. R5 = 1.2kΩ ±5%
10. C1 = 0.01µF Min
11. F0 = 100kHz ±10%
12. F1 = F0/2, F2 = F1/2, ...F12 = F11/2

Die Characteristics

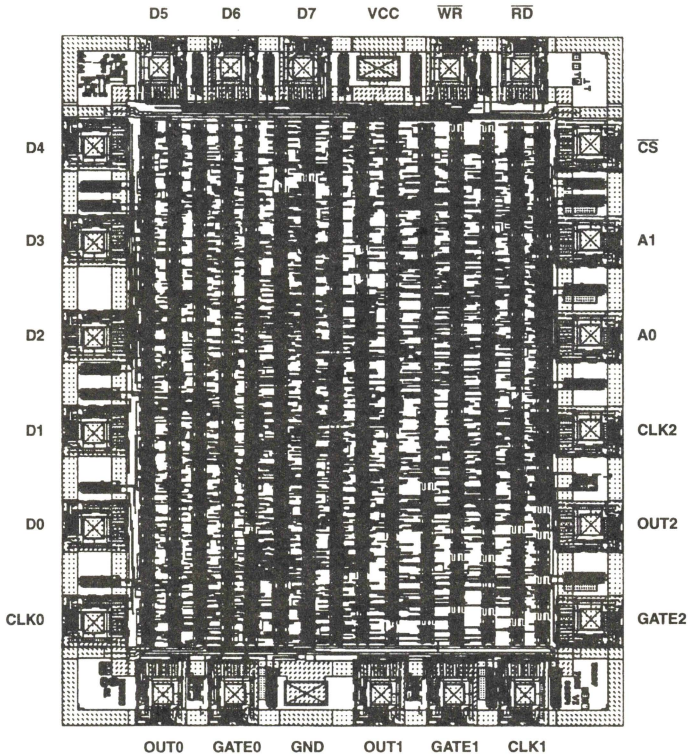
DIE DIMENSIONS:
129mils x 155mils x 19mils
(3270µm x 3940µm x 483µm)

METALLIZATION:
Type: Si-Al-Cu
Thickness: Metal 1: 8kÅ ± 0.75kÅ
Metal 2: 12kÅ ± 1.0kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ ± 3.0kÅ

Metallization Mask Layout

82C54



HARRIS SEMICONDUCTOR

82C55A

CMOS Programmable Peripheral Interface

March 1997

Features

- Pin Compatible with NMOS 8255A
- 24 Programmable I/O Pins
- Fully TTL Compatible
- High Speed, No "Wait State" Operation with 5MHz and 8MHz 80C86 and 80C88
- Direct Bit Set/Reset Capability
- Enhanced Control Word Read Capability
- L7 Process
- 2.5mA Drive Capability on All I/O Ports
- Low Standby Power (ICCSB) 10μA

Ordering Information

PART NUMBERS		PACKAGE	TEMPERATURE RANGE	PKG. NO.
5MHz	8MHz			
CP82C55A-5	CP82C55A	40 Ld PDIP	0°C to +70°C	E40.6
IP82C55A-5	IP82C55A		-40°C to +85°C	E40.6
CS82C55A-5	CS82C55A	44 Ld PLCC	0°C to +70°C	N44.65
IS82C55A-5	IS82C55A		-40°C to +85°C	N44.65
CD82C55A-5	CD82C55A	40 Ld CERDIP	0°C to +70°C	F40.6
ID82C55A-5	ID82C55A		-40°C to +85°C	F40.6
MD82C55A-5/B	MD82C55A/B		-55°C to +125°C	F40.6
8406601QA	8406602QA	SMD#		F40.6
MR82C55A-5/B	MR82C55A/B	44 Pad CLCC	-55°C to +125°C	J44.A
8406601XA	8406602XA	SMD#		J44.A

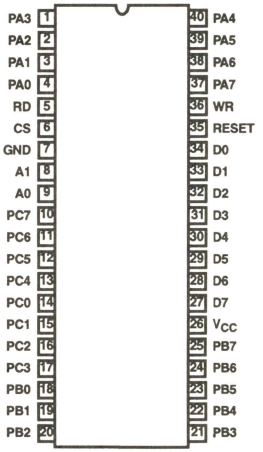
Description

The Harris 82C55A is a high performance CMOS version of the industry standard 8255A and is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance and industry standard configuration of the 82C55A make it compatible with the 80C86, 80C88 and other microprocessors.

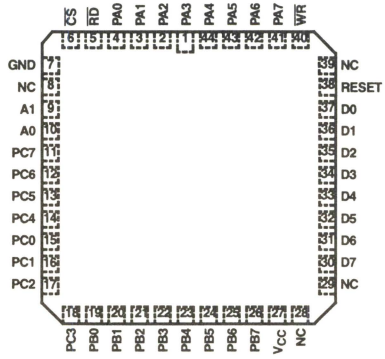
Static CMOS circuit design insures low operating power. TTL compatibility over the full military temperature range and bus hold circuitry eliminate the need for pull-up resistors. The Harris advanced SAJI process results in performance equal to or greater than existing functionally equivalent products at a fraction of the power

Pinouts

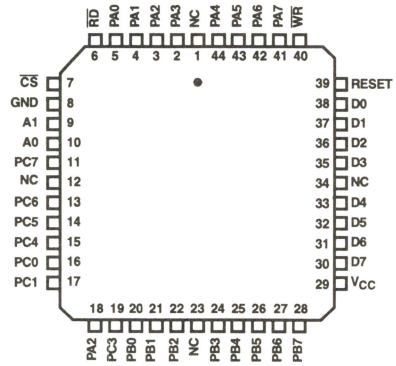
82C55A (DIP)
TOP VIEW



82C55A (CLCC)
TOP VIEW



82C55A (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

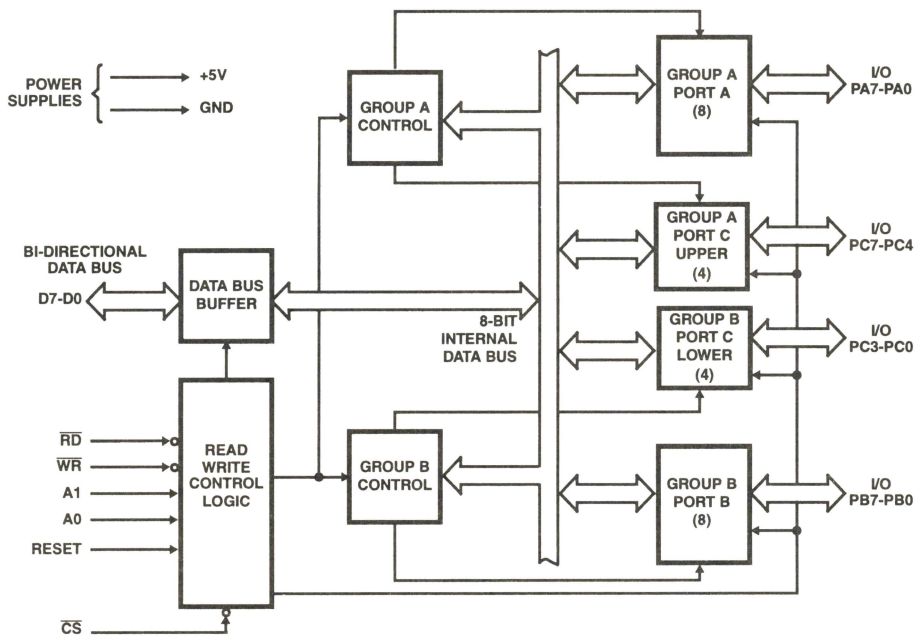
Copyright © Harris Corporation 1997

File Number **2969.1**

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	26		V_{CC}: The +5V power supply pin. A 0.1μF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7		GROUND
D0-D7	27-34	I/O	DATA BUS: The Data Bus lines are bidirectional three-state pins connected to the system data bus.
RESET	35	I	RESET: A high on this input clears the control register and all ports (A, B, C) are set to the input mode with the "Bus Hold" circuitry turned on.
$\overline{CS}$	6	I	CHIP SELECT: Chip select is an active low input used to enable the 82C55A onto the Data Bus for CPU communications.
$\overline{RD}$	5	I	READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus.
$\overline{WR}$	36	I	WRITE: Write is an active low input control signal used by the CPU to load control words and data into the 82C55A.
A0-A1	8, 9	I	ADDRESS: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word register. A0 and A1 are normally connected to the least significant bits of the Address Bus A0, A1.
PA0-PA7	1-4, 37-40	I/O	PORT A: 8-bit input and output port. Both bus hold high and bus hold low circuitry are present on this port.
PB0-PB7	18-25	I/O	PORT B: 8-bit input and output port. Bus hold high circuitry is present on this port.
PC0-PC7	10-17	I/O	PORT C: 8-bit input and output port. Bus hold circuitry is present on this port.

Functional Description



Functional Description

Data Bus Buffer

This three-state bi-directional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

(CS) Chip Select. A "low" on this input pin enables the communcation between the 82C55A and the CPU.

(RD) Read. A "low" on this input pin enables 82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 82C55A.

(WR) Write. A "low" on this input pin enables the CPU to write data or control words into the 82C55A.

(A0 and A1) Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).

82C55A BASIC OPERATION

A1	A0	RD	WR	CS	INPUT OPERATION (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
1	1	0	1	0	Control Word → Data Bus
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					DISABLE FUNCTION
X	X	X	X	1	Data Bus → Three-State
X	X	1	1	0	Data Bus → Three-State

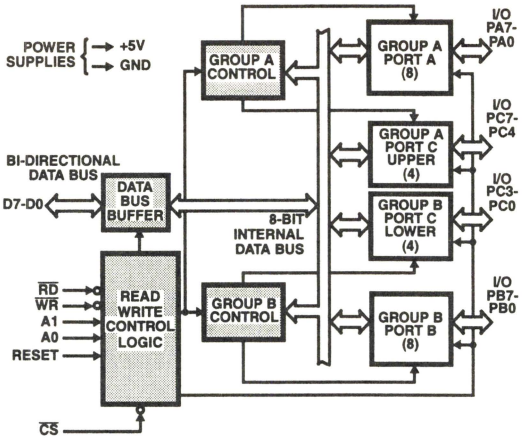


FIGURE 1. 82C55A BLOCK DIAGRAM. DATA BUS BUFFER, READ/WRITE, GROUP A & B CONTROL LOGIC FUNCTIONS

(RESET) Reset. A "high" on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode. "Bus hold" devices internal to the 82C55A will hold the I/O port inputs to a logic "1" state with a maximum hold current of 400µA.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7 - C4)

Control Group B - Port B and Port C lower (C3 - C0)

The control word register can be both written and read as shown in the "Basic Operation" table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A. See Figure 2A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer. See Figure 2B.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal output and status signal inputs in conjunction with ports A and B. See Figure 2B.

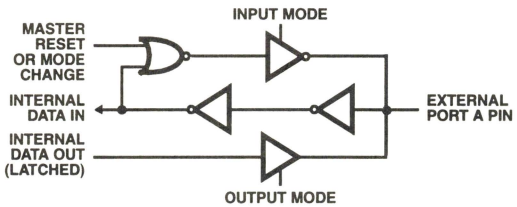


FIGURE 2A. PORT A BUS-HOLD CONFIGURATION

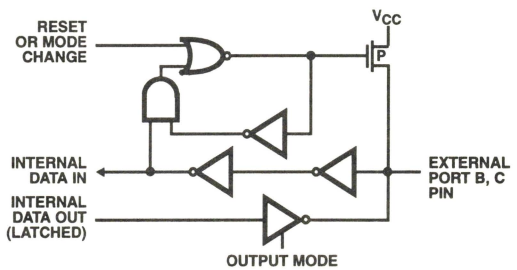


FIGURE 2B. PORT B AND C BUS-HOLD CONFIGURATION

FIGURE 2. BUS-HOLD CONFIGURATION

Operational Description

Mode Selection

There are three basic modes of operation than can be selected by the system software:

Mode 0 - Basic Input/Output
Mode 1 - Strobed Input/Output
Mode 2 - Bi-directional Bus

When the reset input goes "high", all ports will be set to the input mode with all 24 port lines held at a logic "one" level by internal bus hold devices. After the reset is removed, the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need to pullup or pulldown resistors in all-CMOS designs. The control word register will contain 9Bh. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine. Any port programmed as an output port is initialized to all zeros when the control word is written.

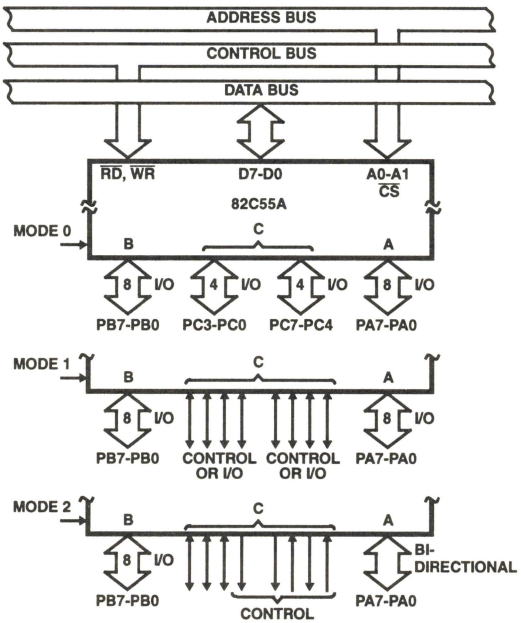


FIGURE 3. BASIC MODE DEFINITIONS AND BUS INTERFACE

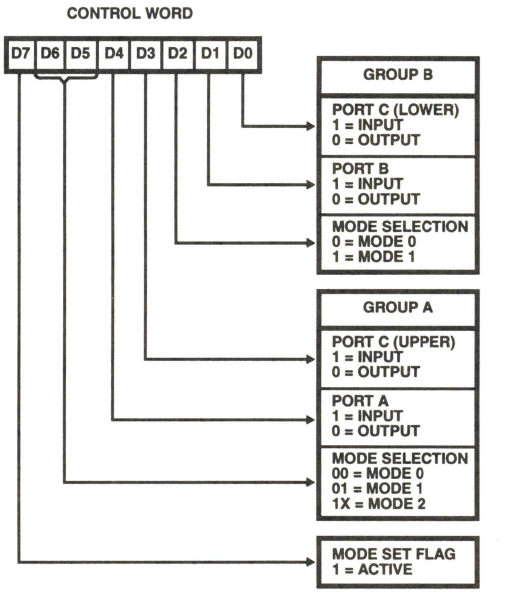


FIGURE 4. MODE DEFINITION FORMAT

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

The mode definitions and possible mode combinations may seem confusing at first, but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs. PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature (Figure 5)

Any of the eight bits of Port C can be Set or Reset using a single Output instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were output ports.

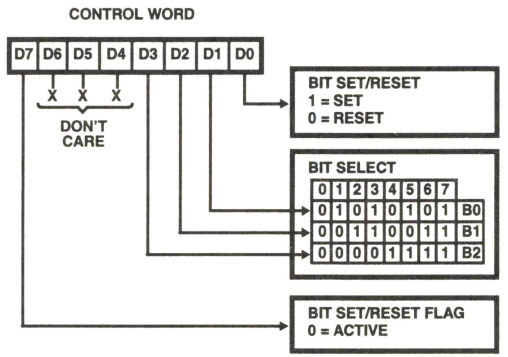


FIGURE 5. BIT SET/RESET FORMAT

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-Flop Definition

(BIT-SET)-INTE is SET - Interrupt Enable

(BIT-RESET)-INTE is Reset - Interrupt Disable

NOTE: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

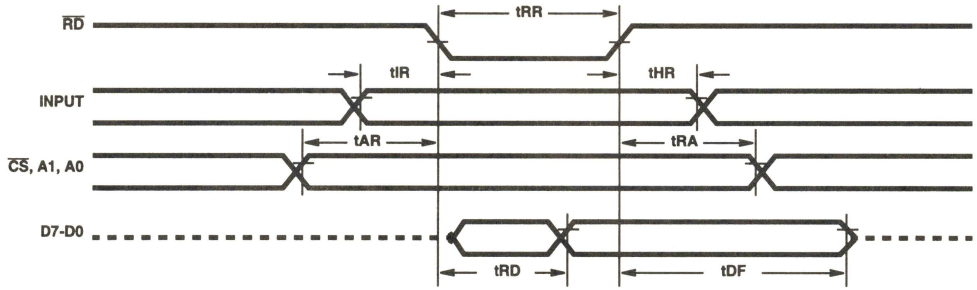
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any Port can be input or output
- Outputs are latched
- Input are not latched
- 16 different Input/Output configurations possible

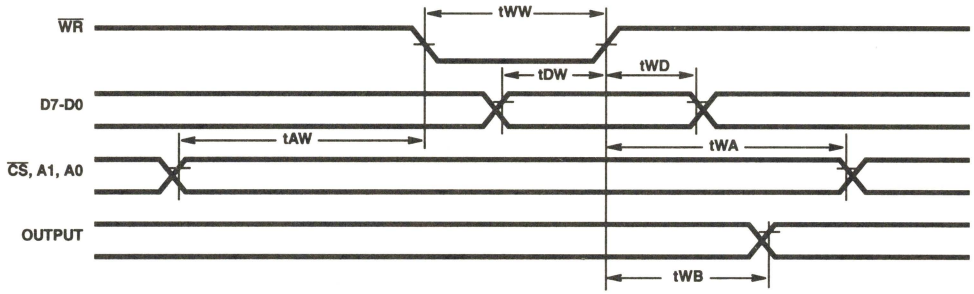
MODE 0 PORT DEFINITION

A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (Upper)	#	PORT B	PORT C (Lower)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

Mode 0 (Basic Input)

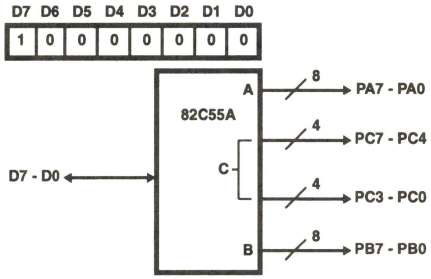


Mode 0 (Basic Output)

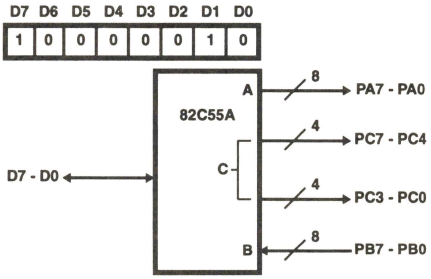


Mode 0 Configurations

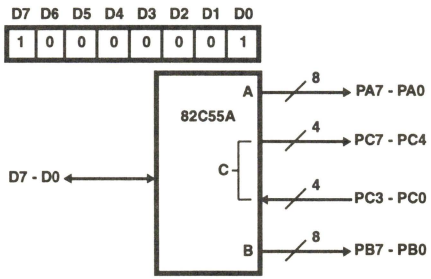
CONTROL WORD #0



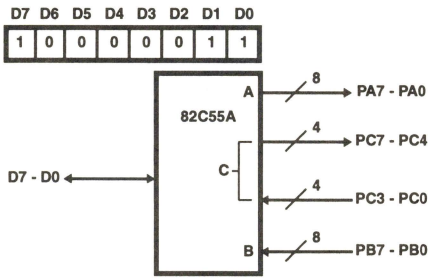
CONTROL WORD #2



CONTROL WORD #1



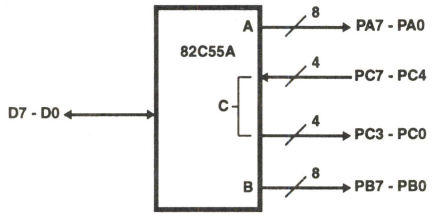
CONTROL WORD #3



Mode 0 Configurations (Continued)

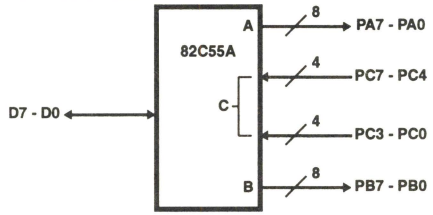
CONTROL WORD #4

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0



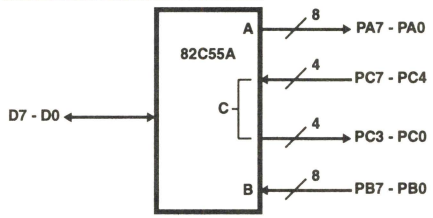
CONTROL WORD #5

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	1



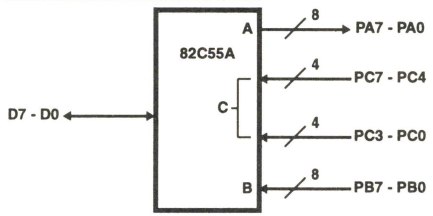
CONTROL WORD #6

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	0



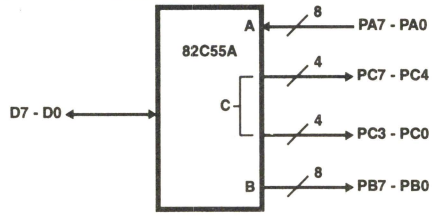
CONTROL WORD #7

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	1



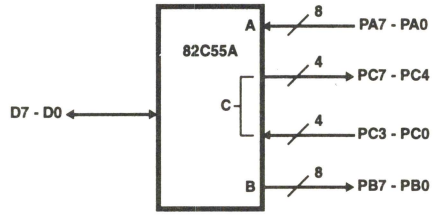
CONTROL WORD #8

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0



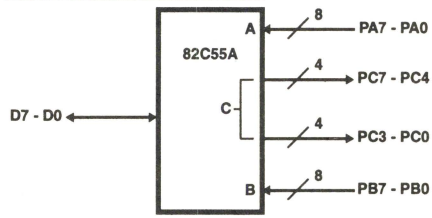
CONTROL WORD #9

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	1



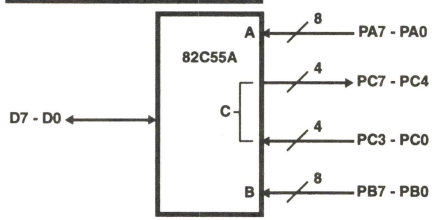
CONTROL WORD #10

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	0



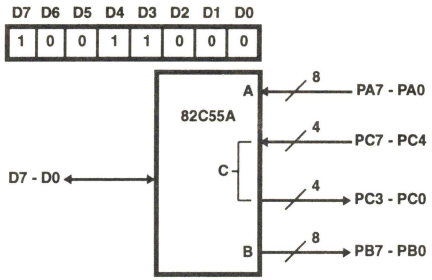
CONTROL WORD #11

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	1

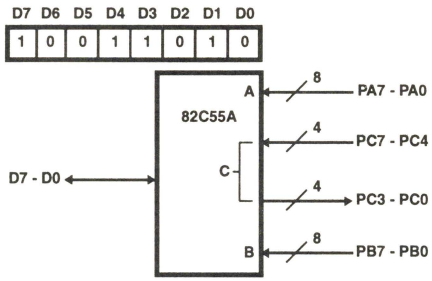


Mode 0 Configurations (Continued)

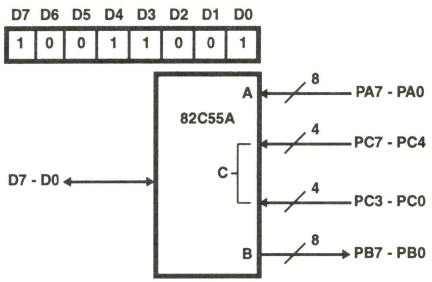
CONTROL WORD #12



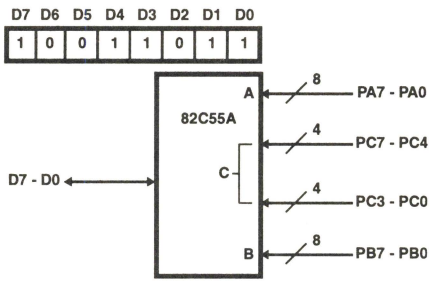
CONTROL WORD #14



CONTROL WORD #13



CONTROL WORD #15



Operating Modes

Mode 1 - (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "hand shaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "hand shaking" signals.

Mode 1 Basic Function Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

(Figures 6 and 7)

STB (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch: in essence, and acknowledgment. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

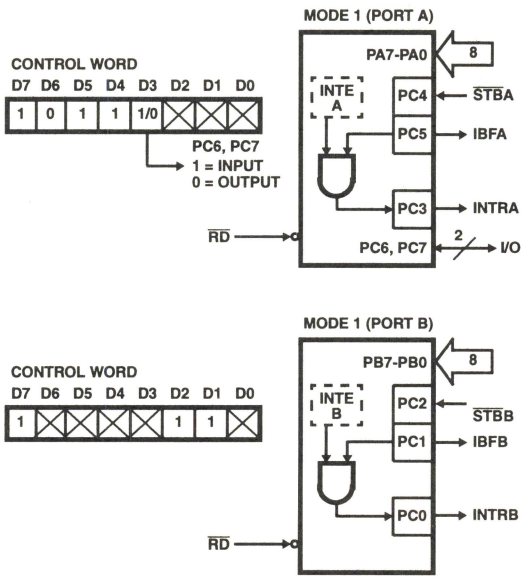


FIGURE 6. MODE 1 INPUT

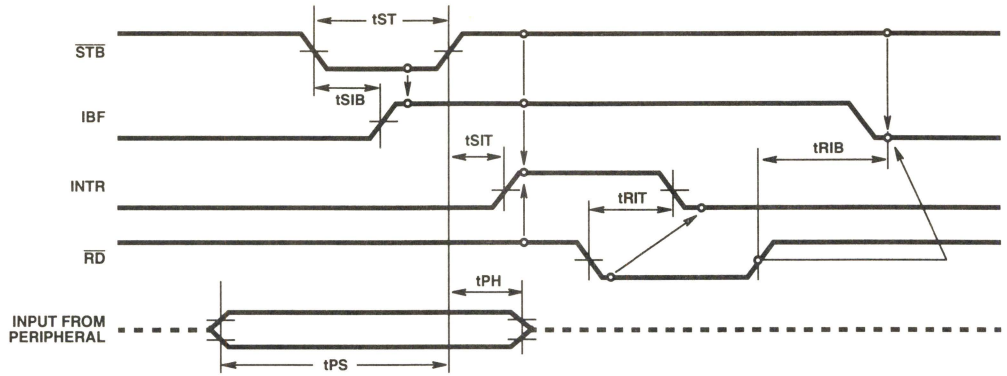


FIGURE 7. MODE 1 (STROBED INPUT)

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when and input device is requesting service. INTR is set by the condition: $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC4.

INTE B

Controlled by bit set/reset of PC2.

Output Control Signal Definition

(Figure 8 and 9)

$\overline{OBF}$ - Output Buffer Full F/F). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to be specified port. This does not mean valid data is sent out of the part at this time since $\overline{OBF}$ can go true before data is available. Data is guaranteed valid at the rising edge of $\overline{OBF}$, (See Note 1). The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ - Acknowledge Input). A "low" on this input informs the 82C55A that the data from Port A or Port B is ready to be accepted. In essence, a response from the peripheral device indicating that it is ready to accept data, (See Note 1).

INTR - (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by Bit Set/Reset of PC6.

INTE B

Controlled by Bit Set/Reset of PC2.

NOTE: To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The user needs to send $\overline{OBF}$ to the peripheral device, generates an $\overline{ACK}$ from the peripheral device and then latch data into the peripheral device on the rising edge of $\overline{OBF}$.

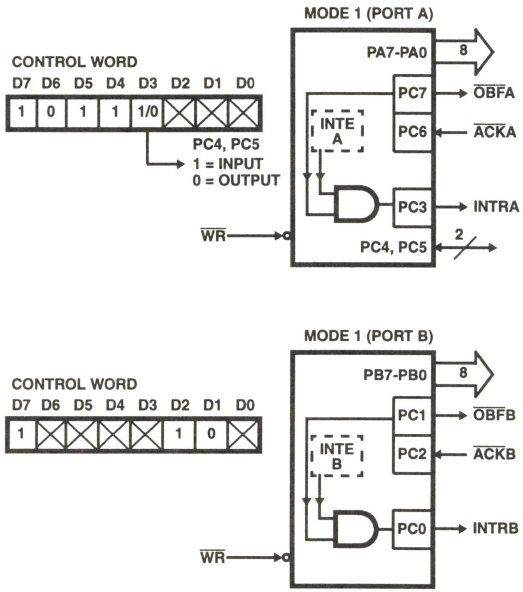


FIGURE 8. MODE 1 OUTPUT

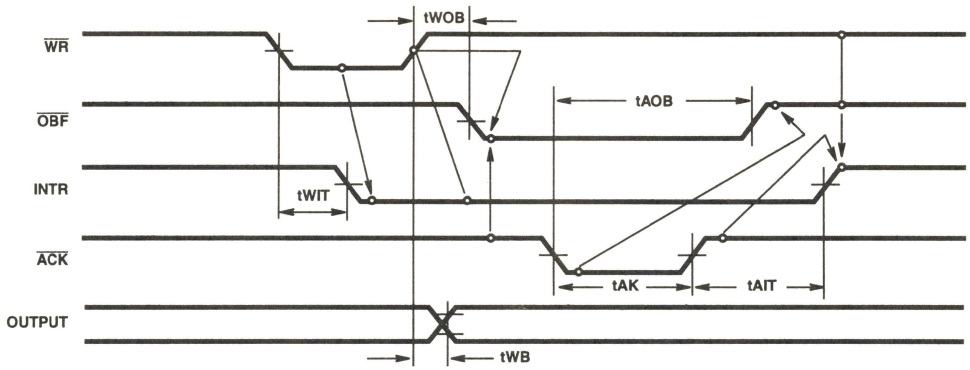
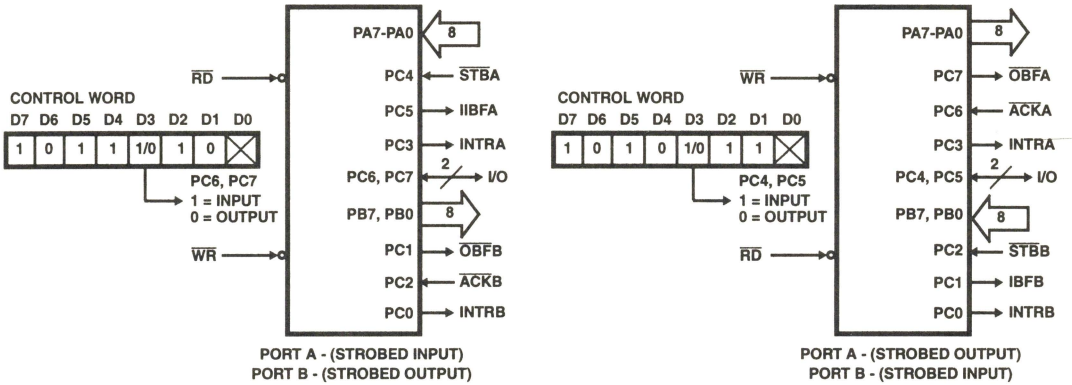


FIGURE 9. MODE 1 (STROBED OUTPUT)



Combinations of Mode 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

FIGURE 10. COMBINATIONS OF MODE 1

Operating Modes

Mode 2 (Strobed Bi-Directional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). "Hand shaking" signals are provided to maintain proper bus flow discipline similar to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C)
- Both inputs and outputs are latched
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A)

Bi-Directional Bus I/O Control Signal Definition

(Figures 11, 12, 13, 14)

INTR - (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ - (Output Buffer Full). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ - (Acknowledge). A "low" on this input enables the three-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 - (The INTE flip-flop associated with $\overline{OBF}$). Controlled by bit set/reset of PC4.

Input Operations

$\overline{STB}$ - (Strobe Input). A "low" on this input loads data into the input latch.

IBF - (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 - (The INTE flip-flop associated with IBF). Controlled by bit set/reset of PC4.

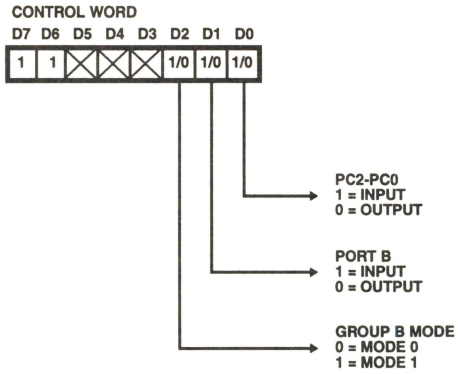


FIGURE 11. MODE CONTROL WORD

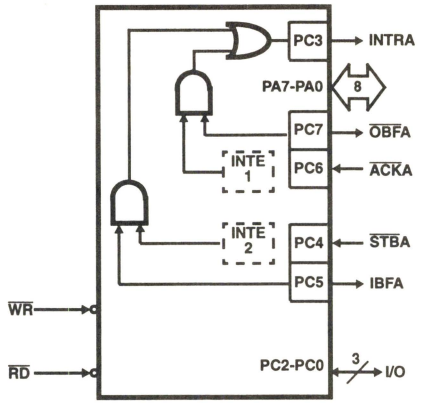
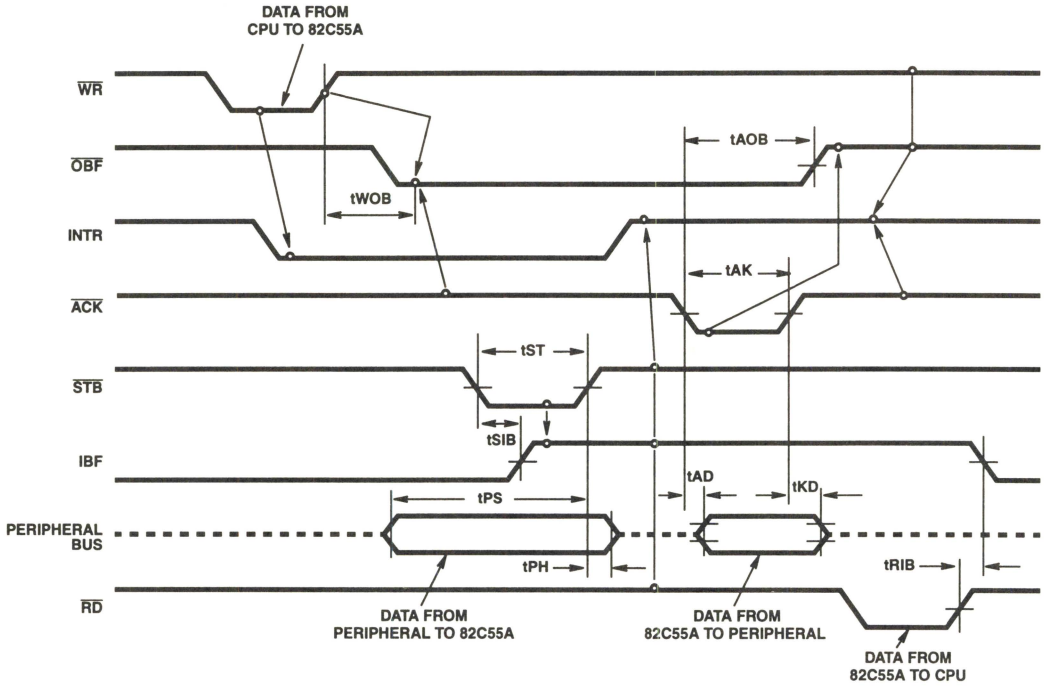


FIGURE 12. MODE 2



NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before RD is permissible. (INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • MASK • $\overline{ACK}$ • $\overline{WR}$)

FIGURE 13. MODE 2 (BI-DIRECTIONAL)

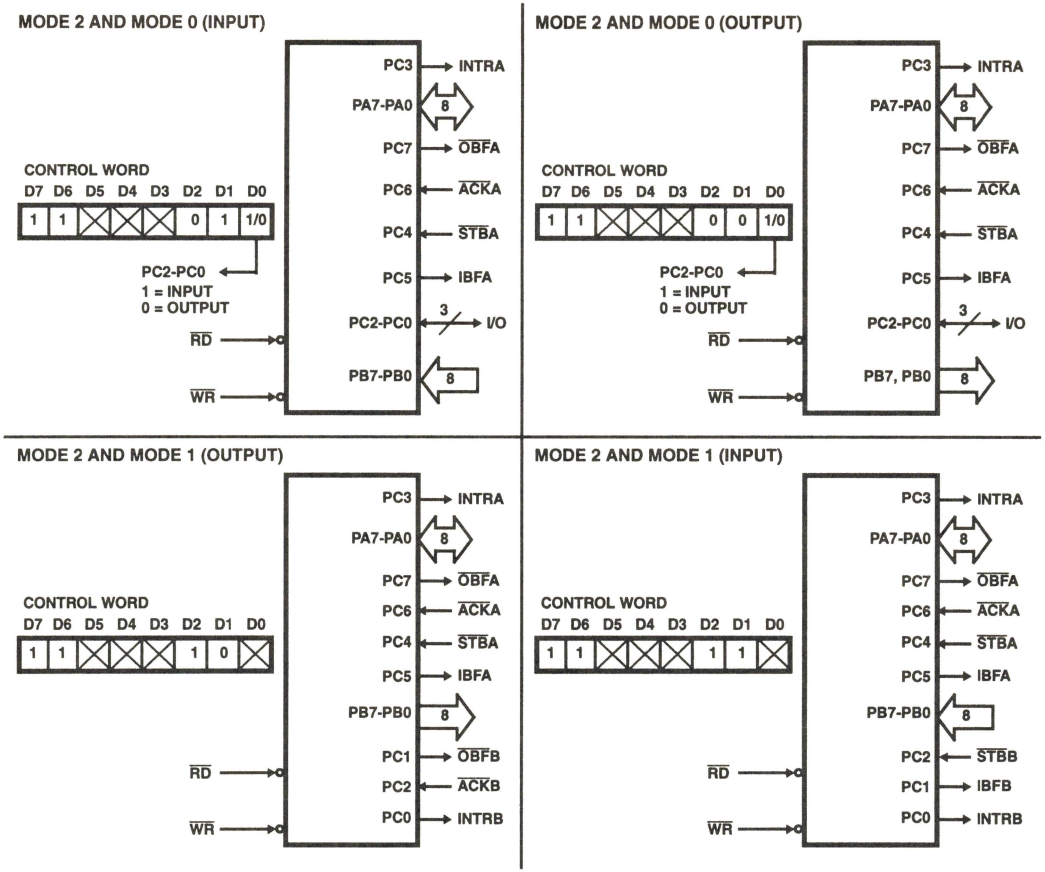


FIGURE 14. MODE 2 COMBINATIONS

MODE DEFINITION SUMMARY

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA0	In	Out	In	Out	←	
PA1	In	Out	In	Out	←	
PA2	In	Out	In	Out	←	
PA3	In	Out	In	Out	←	
PA4	In	Out	In	Out	←	
PA5	In	Out	In	Out	←	
PA6	In	Out	In	Out	←	
PA7	In	Out	In	Out	←	
PB0	In	Out	In	Out		Mode 0 or Mode 1 Only
PB1	In	Out	In	Out		
PB2	In	Out	In	Out		
PB3	In	Out	In	Out		
PB4	In	Out	In	Out		
PB5	In	Out	In	Out		
PB6	In	Out	In	Out		
PB7	In	Out	In	Out		
PC0	In	Out	INTRB	INTRB	I/O	
PC1	In	Out	IBFB	$\overline{OBF}$B	I/O	
PC2	In	Out	$\overline{STB}$B	$\overline{ACK}$B	I/O	
PC3	In	Out	INTRA	INTRA	INTRA	
PC4	In	Out	$\overline{STB}$A	I/O	$\overline{STB}$A	
PC5	In	Out	IBFA	I/O	IBFA	
PC6	In	Out	I/O	$\overline{ACK}$A	$\overline{ACK}$A	
PC7	In	Out	I/O	$\overline{OBF}$A	$\overline{OBF}$A	

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C fare not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

INPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB
GROUP A					GROUP B		

OUTPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
OBFA	INTEA	I/O	I/O	INTRA	INTEB	OBFB	INTRB
GROUP A					GROUP B		

FIGURE 15. MODE 1 STATUS WORD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
OBFA	INTE1	IBFA	INTE2	INTRA	X	X	X
GROUP A					GROUP B		

(Defined by Mode 0 or Mode 1 Selection)

FIGURE 16. MODE 2 STATUS WORD FORMAT

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status (Figures 15 and 16)

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is not special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

INTERRUPT ENABLE FLAG	POSITION	ALTERNATE PORT C PIN SIGNAL (MODE)
INTE B	PC2	$\overline{ACK}$B (Output Mode 1) or $\overline{STB}$B (Input Mode 1)
INTE A2	PC4	$\overline{STB}$A (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}$A (Output Mode 1 or Mode 2)

FIGURE 17. INTERRUPT ENABLE FLAGS IN MODES 1 AND 2

Applications of the 82C55A

The 82C55A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 82C55A to exactly "fit" the application. Figures 18 through 24 present a few examples of typical applications of the 82C55A.

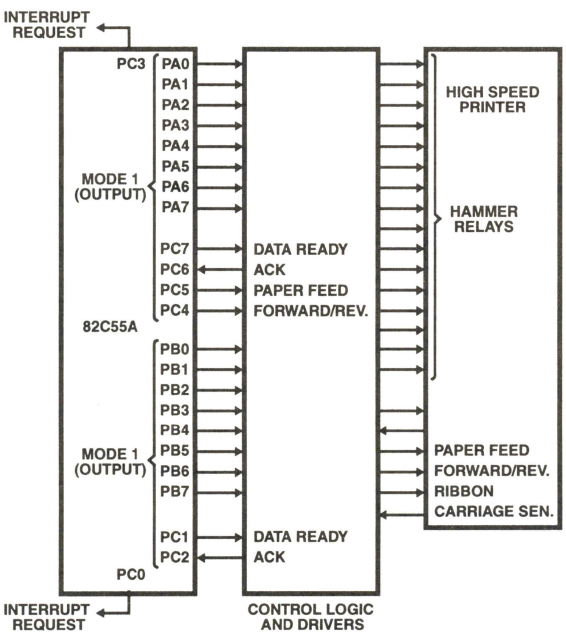


FIGURE 18. PRINTER INTERFACE

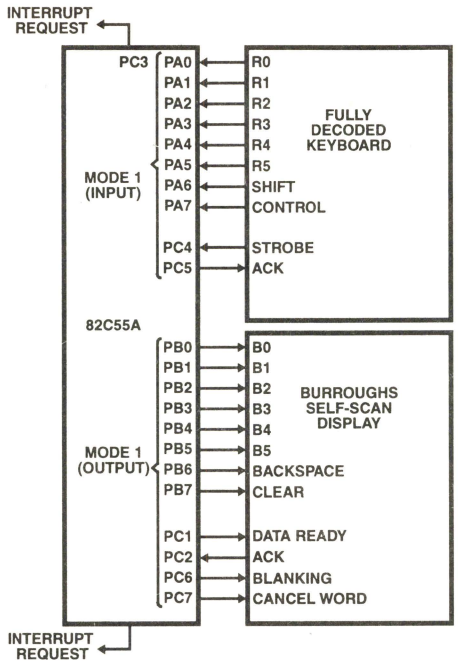


FIGURE 19. KEYBOARD AND DISPLAY INTERFACE

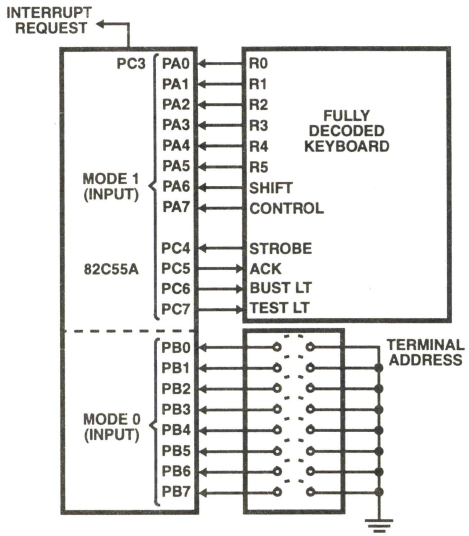


FIGURE 20. KEYBOARD AND TERMINAL ADDRESS INTERFACE

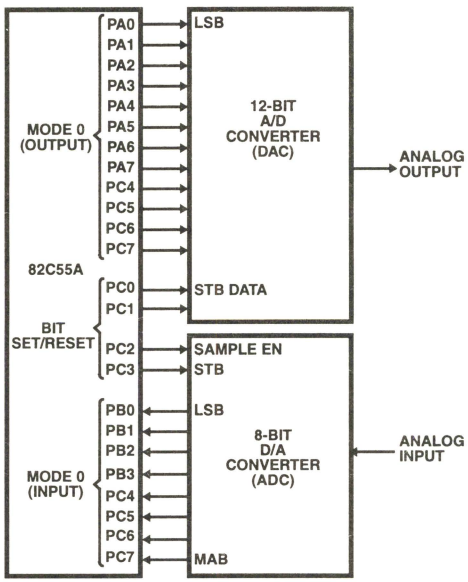


FIGURE 21. DIGITAL TO ANALOG, ANALOG TO DIGITAL

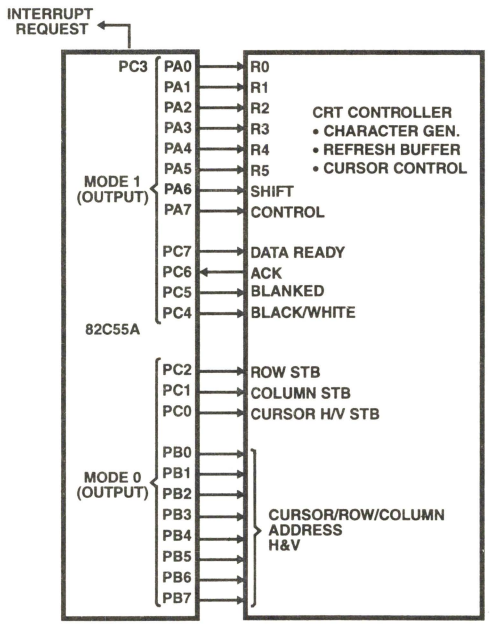


FIGURE 22. BASIC CRT CONTROLLER INTERFACE

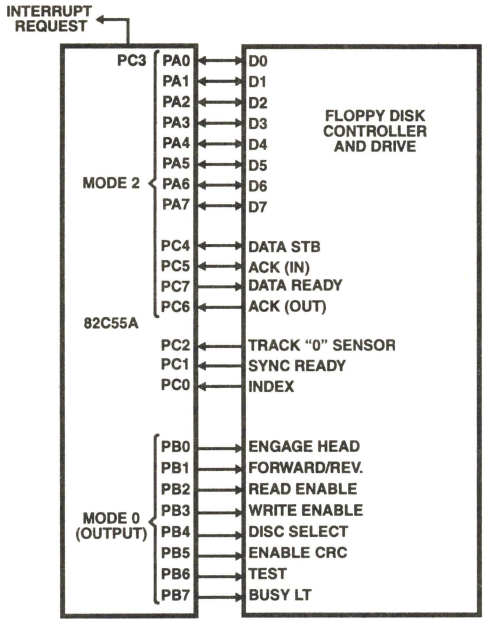


FIGURE 23. BASIC FLOPPY DISC INTERFACE

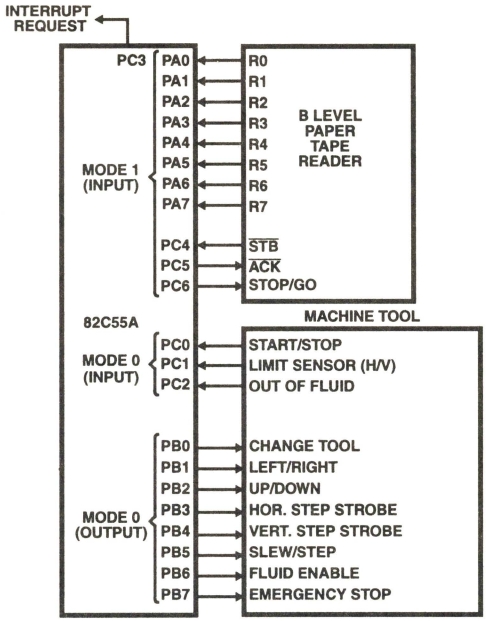


FIGURE 24. MACHINE TOOL CONTROLLER INTERFACE

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND-0.5V to V_{CC}+0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C55A . . . . . 0°C to +70°C
I82C55A . . . . . -40°C to +85°C
M82C55A . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package	50°C/W	10°C/W
CLCC Package	65°C/W	14°C/W
PDIP Package	50°C/W	N/A
PLCC Package	46°C/W	N/A

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package . . . . . +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(PLCC - Lead Tips Only)

Die Characteristics

Gate Count . . . . . 1000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C (C82C55A);
T_A = -40°C to +85°C (I82C55A);
T_A = -55°C to +125°C (M82C55A)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0 2.2	-	V	I82C55A, C82C55A, M82C55A
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
V_{OH}	Logical One Output Voltage	3.0 V_{CC} -0.4	-	V	I_{OH} = -2.5mA, I_{OH} = -100µA
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} +2.5mA
I_I	Input Leakage Current	-1.0	+1.0	µA	V_{IN} = V_{CC} or GND, DIP Pins: 5, 6, 8, 9, 35, 36
IO	I/O Pin Leakage Current	-10	+10	µA	VO = V_{CC} or GND DIP Pins: 27 - 34
IBHH	Bus Hold High Current	-50	-400	µA	VO = 3.0V. Ports A, B, C
IBHL	Bus Hold Low Current	50	400	µA	VO = 1.0V. Port A ONLY
IDAR	Darlington Drive Current	-2.5	Note 1, 3	mA	Ports A, B, C. Test Condition 3
ICCSB	Standby Power Supply Current	-	10	µA	V_{CC} = 5.5V, V_{IN} = V_{CC} or GND. Output Open
ICCOP	Operating Power Supply Current	-	1	mA/MHz	T_A = +25°C, V_{CC} = 5.0V, Typical (See Note2)

NOTES:

1. No internal current limiting exists on Port Outputs. A resistor must be added externally to limit the current.
2. ICCOP = 1mA/MHz of Peripheral Read/Write cycle time. (Example: 1.0µs I/O Read/Write cycle time = 1mA).
3. Tested as V_{OH} at -2.5mA.

Capacitance

T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	10	pF	FREQ = 1MHz, All Measurements are referenced to device GND
CI/O	I/O Capacitance	20	pF	

AC Electrical Specifications

V_{CC} = +5V± 10%, GND = 0V; T_A = -55°C to +125°C (M82C55A) (M82C55A-5);
T_A = -40°C to +85°C (I82C55A) (I82C55A-5);
T_A = 0°C to +70°C (C82C55A) (C82C55A-5)

SYMBOL	PARAMETER	82C55A-5		82C55A		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
READ TIMING							
(1) tAR	Address Stable Before $\overline{RD}$	0	-	0	-	ns	
(2) tRA	Address Stable After $\overline{RD}$	0	-	0	-	ns	
(3) tRR	$\overline{RD}$ Pulse Width	250	-	150	-	ns	
(4) tRD	Data Valid From $\overline{RD}$	-	200	-	120	ns	1
(5) tDF	Data Float After $\overline{RD}$	10	75	10	75	ns	2
(6) tRV	Time Between $\overline{RD}$s and/or $\overline{WR}$s	300	-	300	-	ns	
WRITE TIMING							
(7) tAW	Address Stable Before $\overline{WR}$	0	-	0	-	ns	
(8) tWA	Address Stable After $\overline{WR}$	20	-	20	-	ns	
(9) tWW	$\overline{WR}$ Pulse Width	100	-	100	-	ns	
(10) tDW	Data Valid to $\overline{WR}$ High	100	-	100	-	ns	
(11) tWD	Data Valid After $\overline{WR}$ High	30	-	30	-	ns	
OTHER TIMING							
(12) tWB	$\overline{WR}$ = 1 to Output	-	350	-	350	ns	1
(13) tIR	Peripheral Data Before $\overline{RD}$	0	-	0	-	ns	
(14) tHR	Peripheral Data After $\overline{RD}$	0	-	0	-	ns	
(15) tAK	ACK Pulse Width	200	-	200	-	ns	
(16) tST	STB Pulse Width	100	-	100	-	ns	
(17) tPS	Peripheral Data Before STB High	20	-	20	-	ns	
(18) tPH	Peripheral Data After STB High	50	-	50	-	ns	
(19) tAD	ACK = 0 to Output	-	175	-	175	ns	1
(20) tKD	ACK = 1 to Output Float	20	250	20	250	ns	2
(21) tWOB	$\overline{WR}$ = 1 to OBF = 0	-	150	-	150	ns	1
(22) tAOB	ACK = 0 to OBF = 1	-	150	-	150	ns	1
(23) tSIB	STB = 0 to IBF = 1	-	150	-	150	ns	1
(24) tRIB	$\overline{RD}$ = 1 to IBF = 0	-	150	-	150	ns	1
(25) tRIT	$\overline{RD}$ = 0 to INTR = 0	-	200	-	200	ns	1
(26) tSIT	STB = 1 to INTR = 1	-	150	-	150	ns	1
(27) tAIT	ACK = 1 to INTR = 1	-	150	-	150	ns	1
(28) tWIT	$\overline{WR}$ = 0 to INTR = 0	-	200	-	200	ns	1
(29) tRES	Reset Pulse Width	500	-	500	-	ns	1, (Note 1)

NOTE:

1. Period of initial Reset pulse after power-on must be at least 50µsec. Subsequent Reset pulses may be 500ns minimum.

Timing Waveforms

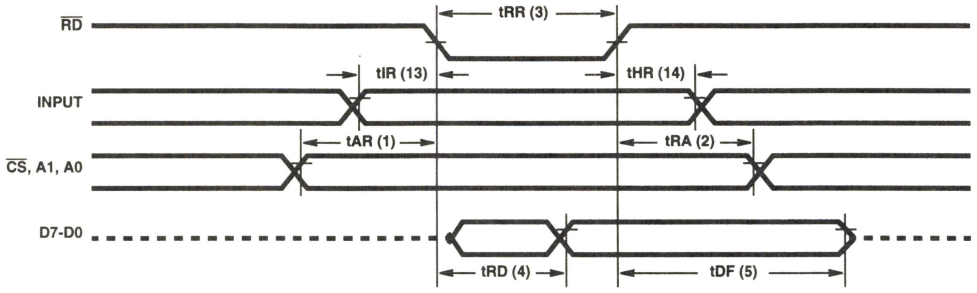


FIGURE 25. MODE 0 (BASIC INPUT)

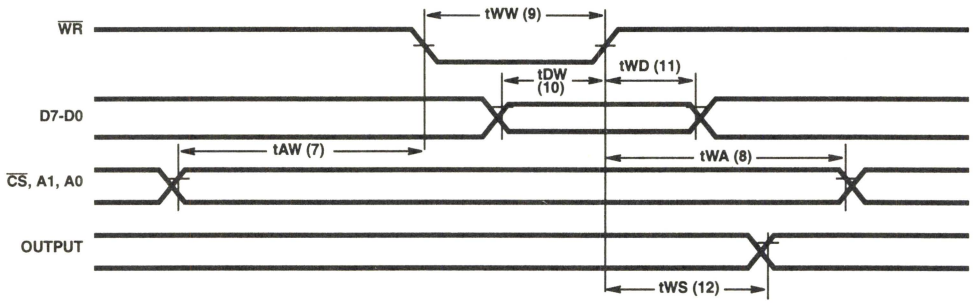


FIGURE 26. MODE 0 (BASIC OUTPUT)

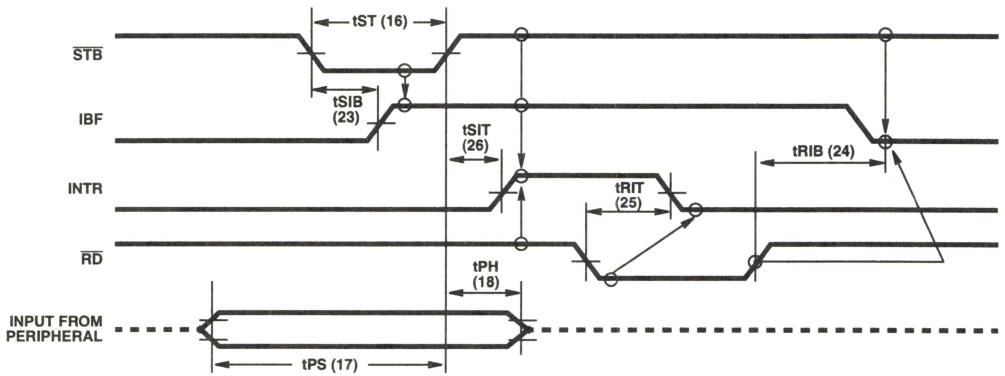


FIGURE 27. MODE 1 (STROBED INPUT)

Timing Waveforms (Continued)

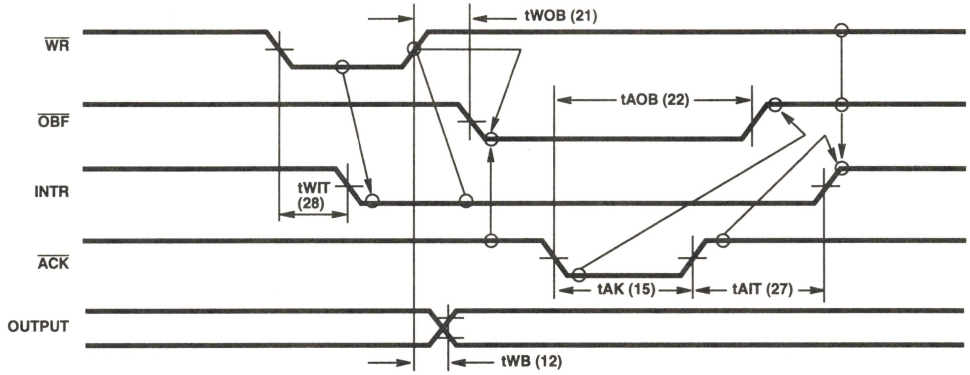


FIGURE 28. MODE 1 (STROBED OUTPUT)

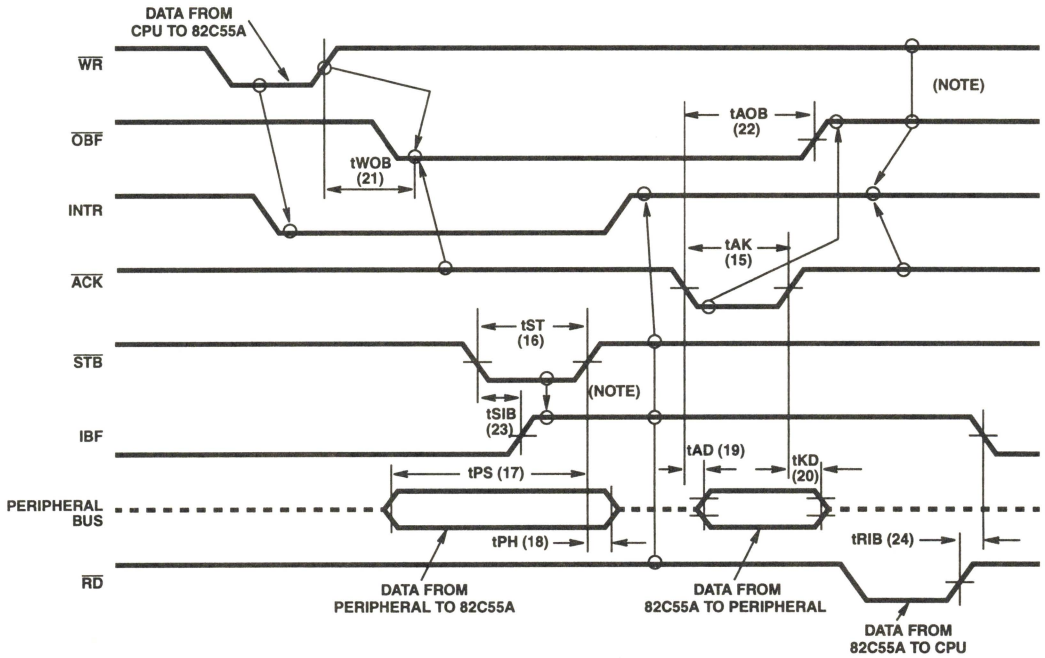


FIGURE 29. MODE 2 (BI-DIRECTIONAL)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible. (INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ • $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

Timing Waveforms (Continued)

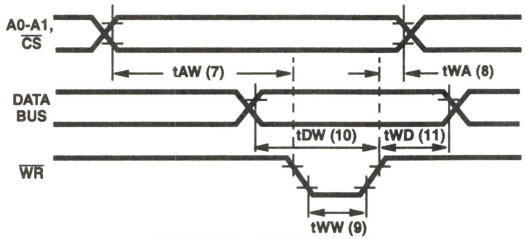


FIGURE 30. WRITE TIMING

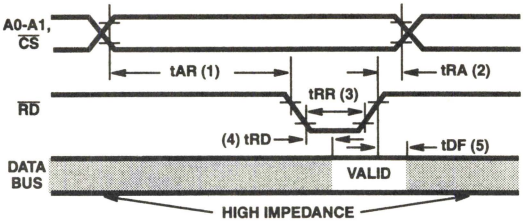
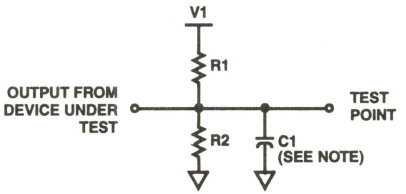


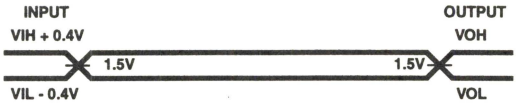
FIGURE 31. READ TIMING

AC Test Circuit



NOTE: Includes STRAY and JIG Capacitance

AC Testing Input, Output Waveforms



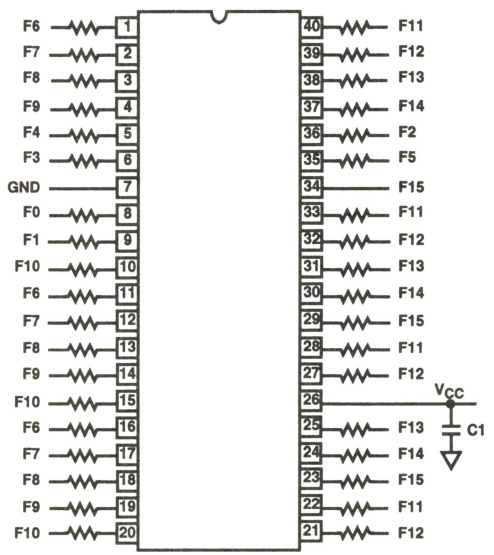
AC Testing: All AC Parameters tested as per test circuits. Input RISE and FALL times are driven at 1ns/V.

TEST CONDITION DEFINITION TABLE

TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	Open	150pF
2	V_{CC}	2kΩ	1.7kΩ	50pF
3	1.5V	750Ω	Open	50pF

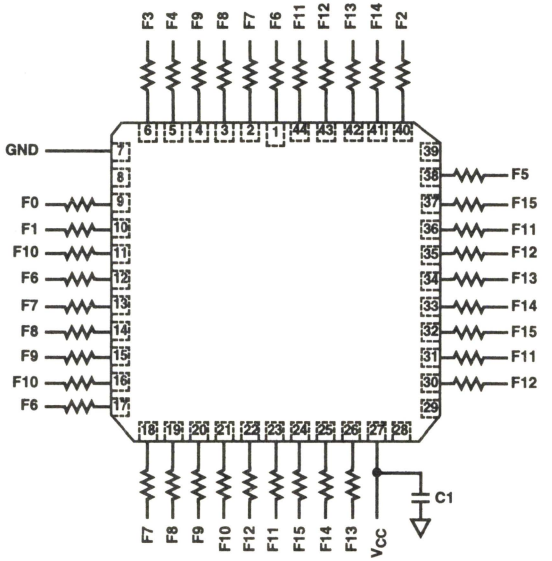
Burn-In Circuits

MD82C55A CERDIP



NOTES:
1. V_{CC} = 5.5V ± 0.5V
2. VIH = 4.5V ± 10%
3. VIL = -0.2V to 0.4V
4. GND = 0V

MR82C55A CLCC



NOTES:
1. C1 = 0.01µF minimum
2. All resistors are 47kΩ ± 5%
3. f0 = 100kHz ± 10%
4. f1 = f0 ÷ 2; f2 = f1 ÷ 2; . . . ; f15 = f14 ÷ 2

Die Characteristics

DIE DIMENSIONS:
95 x 100 x 19 ±1mils

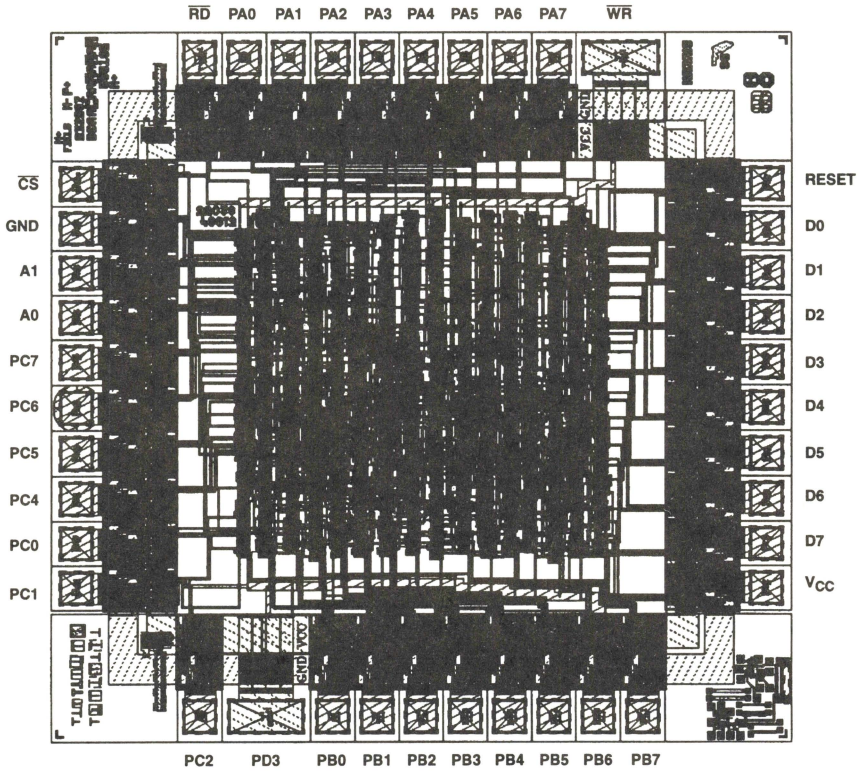
METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ±1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
0.78 x 10^5 A/cm^2

Metallization Mask Layout

82C55A



HARRIS SEMICONDUCTOR

82C59A

March 1997

CMOS Priority Interrupt Controller

Features

- 12.5MHz, 8MHz and 5MHz Versions Available
  - 12.5MHz Operation 82C59A-12
  - 8MHz Operation 82C59A
  - 5MHz Operation 82C59A-5
- High Speed, "No Wait-State" Operation with 12.5MHz 80C286 and 8MHz 80C86/88
- Pin Compatible with NMOS 8259A
- 80C86/88/286 and 8080/85/86/88/286 Compatible
- Eight-Level Priority Controller, Expandable to 64 Levels
- Programmable Interrupt Modes
- Individual Request Mask Capability
- Fully Static Design
- Fully TTL Compatible
- Low Power Operation
  - ICCSB . . . . . 10μA Maximum
  - ICCOP . . . . . 1mA/MHz Maximum
- Single 5V Power Supply
- Operating Temperature Ranges
  - C82C59A . . . . . 0°C to +70°C
  - I82C59A . . . . . -40°C to +85°C
  - M82C59A . . . . . -55°C to +125°C

Description

The Harris 82C59A is a high performance CMOS Priority Interrupt Controller manufactured using an advanced 2μm CMOS process. The 82C59A is designed to relieve the system CPU from the task of polling in a multilevel priority system. The high speed and industry standard configuration of the 82C59A make it compatible with microprocessors such as 80C286, 80286, 80C86/88, 8086/88, 8080/85 and NSC800.

The 82C59A can handle up to eight vectored priority interrupting sources and is cascadable to 64 without additional circuitry. Individual interrupting sources can be masked or prioritized to allow custom system configuration. Two modes of operation make the 82C59A compatible with both 8080/85 and 80C86/88/286 formats.

Static CMOS circuit design ensures low operating power. The Harris advanced CMOS process results in performance equal to or greater than existing equivalent products at a fraction of the power.

Ordering Information

PART NUMBER			PACKAGE	TEMPERATURE RANGE	PKG. NO.
5MHz	8MHz	12.5MHz			
CP82C59A-5	CP82C59A	CP82C59A-12	28 Ld PDIP	0°C to +70°C	E28.6
IP82C59A-5	IP82C59A	IP82C59A-12		-40°C to +85°C	E28.6
CS82C59A-5	CS82C59A	CS82C59A-12	28 Ld PLCC	0°C to +70°C	N28.45
IS82C59A-5	IS82C59A	IS82C59A-12		-40°C to +85°C	N28.45
CD82C59A-5	CD82C59A	CD82C59A-12	CERDIP	0°C to +70°C	F28.6
ID82C59A-5	ID82C59A	ID82C59A-12		-40°C to +85°C	F28.6
MD82C59A-5/B	MD82C59A/B	MD82C59A-12/B		-55°C to +125°C	F28.6
5962-8501601YA	5962-8501602YA	-	SMD#		F28.6
MR82C59A-5/B	MR82C59A/B	MR82C59A-12/B	28 Pad CLCC	-55°C to +125°C	J28.A
5962-85016013A	5962-85016023A	-	SMD#		J28.A
CM82C59A-5	CM82C59A	CM82C59A-12	28 Ld SOIC	0°C to +70°C	M28.3

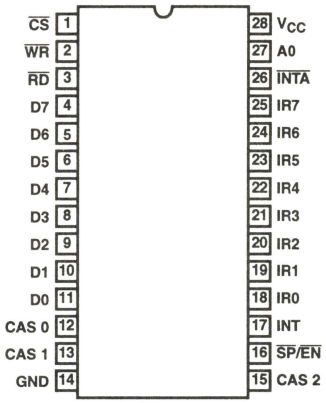
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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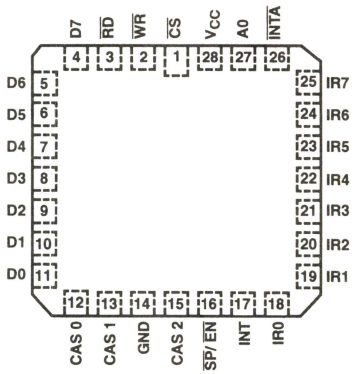
File Number **2784.2**

Pinouts

82C59A (PDIP, CERDIP, SOIC)
TOP VIEW



82C59A (PLCC, CLCC)
TOP VIEW



PIN	DESCRIPTION
D7 - D0	Data Bus (Bidirectional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0	Command Select Address
$\overline{CS}$	Chip Select
CAS 2 - CAS 0	Cascade Lines
$\overline{SP/EN}$	Slave Program Input Enable
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0 - IR7	Interrupt Request Inputs

Functional Diagram

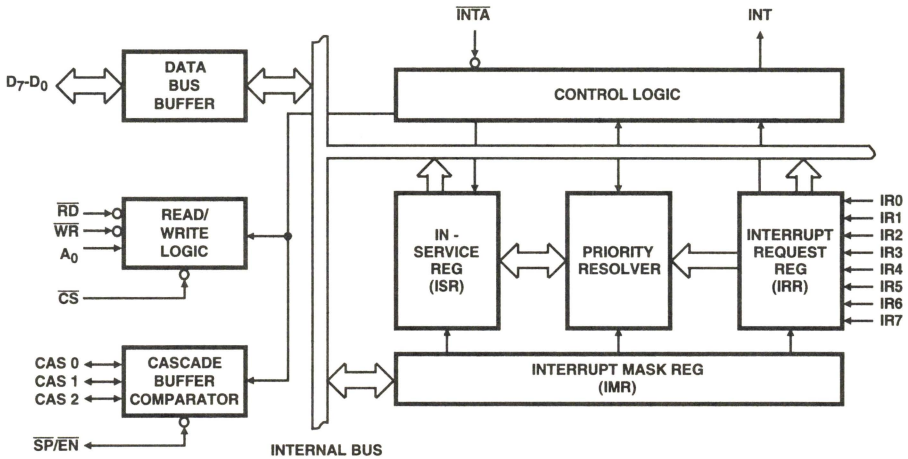


FIGURE 1.

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	28	I	V_{CC}: The +5V power supply pin. A 0.1µF capacitor between pins 28 and 14 is recommended for decoupling.
GND	14	I	GROUND
$\overline{CS}$	1	I	CHIP SELECT: A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communications between the CPU and the 82C59A. $\overline{INTA}$ functions are independent of $\overline{CS}$.
$\overline{WR}$	2	I	WRITE: A low on this pin when $\overline{CS}$ is low enables the 82C59A to accept command words from the CPU.
$\overline{RD}$	3	I	READ: A low on this pin when $\overline{CS}$ is low enables the 82C59A to release status onto the data bus for the CPU.
D7 - D0	4 - 11	I/O	BIDIRECTIONAL DATA BUS: Control, status, and interrupt-vector information is transferred via this bus.
CAS0 - CAS2	12, 13, 15	I/O	CASCADE LINES: The CAS lines form a private 82C59A bus to control a multiple 82C59A structure. These pins are outputs for a master 82C59A and inputs for a slave 82C59A.
$\overline{SP}/\overline{EN}$	16	I/O	SLAVE PROGRAM/ENABLE BUFFER: This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers ($\overline{EN}$). When not in the Buffered Mode it is used as an input to designate a master ($\overline{SP}$ = 1) or slave ($\overline{SP}$ = 0).
INT	17	O	INTERRUPT: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus, it is connected to the CPU's interrupt pin.
IR0 - IR7	18 - 25	I	INTERRUPT REQUESTS: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode). Internal pull-up resistors are implemented on IR0 - 7.
$\overline{INTA}$	26	I	INTERRUPT ACKNOWLEDGE: This pin is used to enable 82C59A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A0	27	I	ADDRESS LINE: This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 82C59A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for 80C86/88/286).

Functional Description

Interrupts in Microcomputer Systems

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the Polled approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system throughput, thus, limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

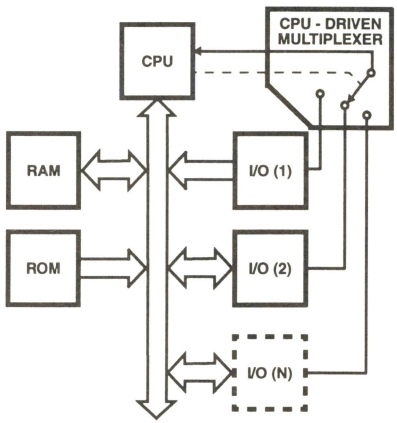


FIGURE 2. POLLED METHOD

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

This is the Interrupt-driven method. It is easy to see that system throughput would drastically increase, and thus, more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

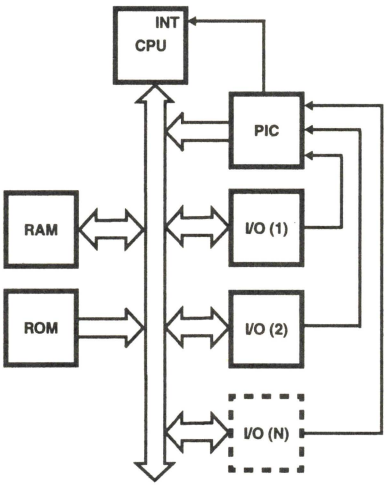


FIGURE 3. INTERRUPT METHOD

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.

82C59A Functional Description

The 82C59A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels of requests and has built-in features for expandability to other 82C59As (up to 64 levels). It is programmed by system software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 82C59A can be configured to match system requirements. The priority modes can be changed or reconfigured dynamically at any time during main program operation. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Interrupt Request Register (IRR) and In-Service Register (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to indicate all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are currently being serviced.

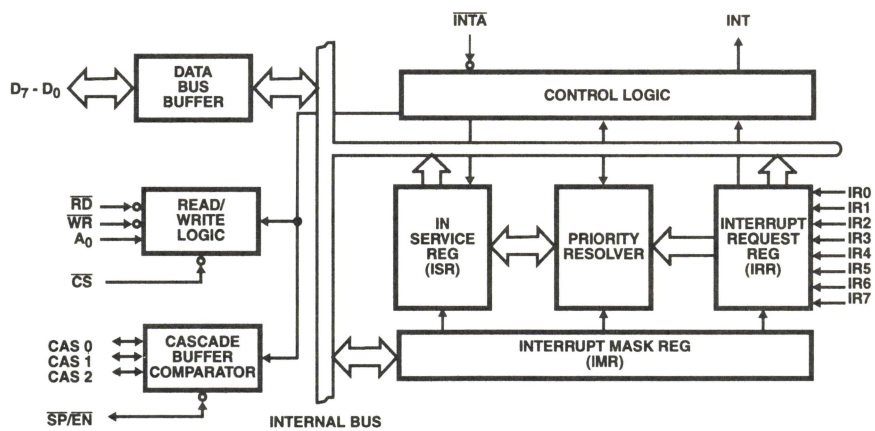


FIGURE 4. 82C59A FUNCTIONAL DIAGRAM

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during the $\overline{INTA}$ sequence.

Interrupt Mask Register (IMR)

The IMR stores the bits which disable the interrupt lines to be masked. The IMR operates on the output of the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

Interrupt (INT)

This output goes directly to the CPU interrupt input. The VOH level on this line is designed to be fully compatible with the 8080, 8085, 8086/88, 80C86/88, 80286, and 80C286 input levels.

Interrupt Acknowledge ($\overline{INTA}$)

$\overline{INTA}$ pulses will cause the 82C59A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the 82C59A.

Data Bus Buffer

This 3-state, bidirectional 8-bit buffer is used to interface the 82C59A to the System Data Bus. Control words and status information are transferred through the Data Bus Buffer.

Read/Write Control Logic

The function of this block is to accept output commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 82C59A to be transferred onto the Data Bus.

Chip Select ($\overline{CS}$)

A LOW on this input enables the 82C59A. No reading or writing of the device will occur unless the device is selected.

Write ($\overline{WR}$)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 82C59A.

Read ($\overline{RD}$)

A LOW on this input enables the 82C59A to send the status of the Interrupt Request Register (IRR), In-Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level (in the poll mode) onto the Data Bus.

A0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as to read the various status registers of the chip. This line can be tied directly to one of the system address lines.

The Cascade Buffer/Comparator

This function block stores and compares the IDs of all 82C59As used in the system. The associated three I/O pins (CAS0 - 2) are outputs when the 82C59A is used as a master and are inputs when the 82C59A is used as a slave. As a master, the 82C59A sends the ID of the interrupting slave device onto the CAS0 - 2 lines. The slave, thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{INTA}$ pulses. (See section "Cascading the 82C59A".)

Interrupt Sequence

The powerful features of the 82C59A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specified interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

These events occur in an 8080/8085 system:

1. One or more of the INTERRUPT REQUEST lines (IR0 - IR7) are raised high, setting the corresponding IRR bit(s).
2. The 82C59A evaluates those requests in the priority resolver and sends an interrupt (INT) to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 82C59A will also release a CALL instruction code (11001101) onto the 8-bit data bus through D0 - D7.
5. This CALL instruction will initiate two additional $\overline{INTA}$ pulses to be sent to 82C59A from the CPU group.
6. These two $\overline{INTA}$ pulses allow the 82C59A to release its preprogrammed subroutine address onto the data bus. The lower 8-bit address is released at the first $\overline{INTA}$ pulse and the higher 8-bit address is released at the second $\overline{INTA}$ pulse.
7. This completes the 3-byte CALL instruction released by the 82C59A. In the AEOI mode, the ISR bit is reset at the end of the third $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an 80C86/88/286 system are the same until step 4.

4. The 82C59A does not drive the data bus during the first $\overline{INTA}$ pulse.
5. The 80C86/88/286 CPU will initiate a second $\overline{INTA}$ pulse. During this $\overline{INTA}$ pulse, the appropriate ISR bit is set and the corresponding bit in the IRR is reset. The 82C59A outputs the 8-bit pointer onto the data bus to be read by the CPU.

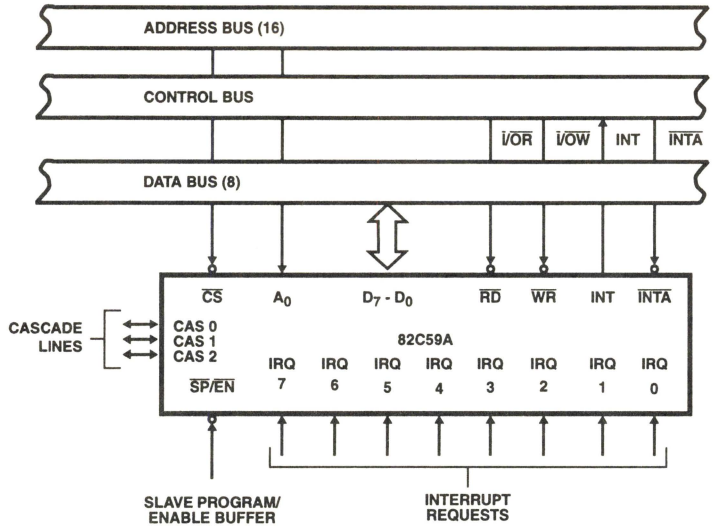


FIGURE 5. 82C59A STANDARD SYSTEM BUS INTERFACE

6. This completes the interrupt cycle. In the AEOI mode, the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e., the request was too short in duration), the 82C59A will issue an interrupt level 7. If a slave is programmed on IR bit 7, the CAS lines remain inactive and vector addresses are output from the master 82C59A.

Interrupt Sequence Outputs

8080, 8085 Interrupt Response Mode

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse, the CALL opcode is enabled onto the data bus.

First Interrupt Vector Byte Data: Hex CD

	D7	D6	D5	D4	D3	D2	D1	D0
Call Code	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse, the lower address of the appropriate service routine is enabled onto the data bus. When interval = 4 bits, A5 - A7 are programmed, while A0 - A4 are automatically inserted by the 82C59A. When interval = 8, only A6 and A7 are programmed, while A0 - A5 are automatically inserted.

CONTENT OF SECOND INTERRUPT VECTOR BYTE

IR	INTERVAL = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	INTERVAL = 8							
	D7	D6	DS	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third $\overline{INTA}$ pulse, the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A8 - A15), is enabled onto the bus.

CONTENT OF THIRD INTERRUPT VECTOR BYTE

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

80C86, 8OC88, 80C286 Interrupt Response Mode

80C86/88/286 mode is similar to 8080/85 mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of 8080/85 systems in that the 82C59A uses it to internally freeze the state of the interrupts for priority resolution and, as a master, it issues the interrupt code on the cascade lines. On this first cycle, it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in the 86/88/286 mode, the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A5 - A11 are unused in the 86/88/286 mode).

CONTENT OF INTERRUPT VECTOR BYTE FOR 80C86/88/286 SYSTEM MODE

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

Programming the 82C59A

The 82C59A accepts two types of command words generated by the CPU:

1. **Initialization Command Words (ICWs):** Before normal operation can begin, each 82C59A in the system must be brought to a starting point - by a sequence of 2 to 4 bytes timed by $\overline{WR}$ pulses.
2. **Operation Command Words (OCWs):** These are the command words which command the 82C59A to operate in various interrupt modes. Among these modes are:
   a. Fully nested mode.
   b. Rotating priority mode.
   c. Special mask mode.
   d. Polled mode.

The OCWs can be written into the 82C59A anytime after initialization.

Initialization Command Words (ICWs)

General

Whenever a command is issued with A0 = 0 and D4 = 1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the following automatically occur:

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.

b. The Interrupt Mask Register is cleared.

c. IR7 input is assigned priority 7.

d. Special Mask Mode is cleared and Status Read is set to IRR.

e. If IC4 = 0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode (see note), no Auto-EOI, 8080/85 system).

NOTE: Master/Slave in ICW4 is only used in the buffered mode.

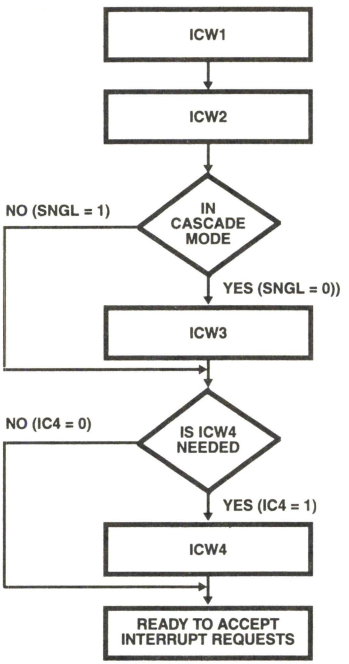
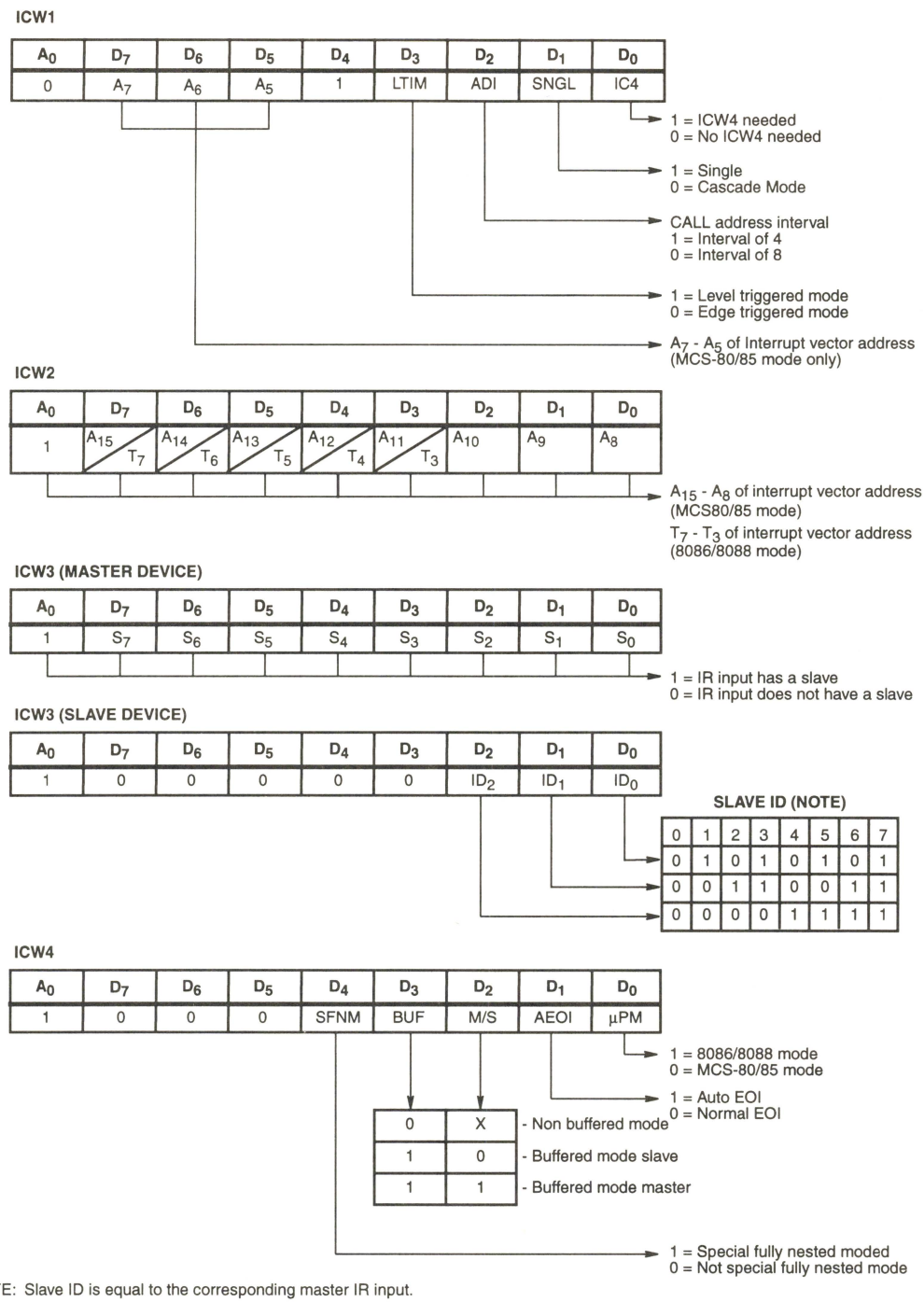


FIGURE 6. 82C59A INITIALIZATION SEQUENCE

Initialization Command Words 1 and 2 (ICW1, ICW2)

A5 - A15: Page starting address of service routines. In an 8080/85 system the 8 request levels will generate CALLS to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus, the 8 routines will occupy a page of 32 or 64 bytes, respectively.



NOTE: Slave ID is equal to the corresponding master IR input.

FIGURE 7. 82C59A INITIALIZATION COMMAND WORD FORMAT

The address format is 2 bytes long (A0 - A15). When the routine interval is 4, A0 - A4 are automatically inserted by the 82C59A, while A5 - A15 are programmed externally. When the routine interval is 8, A0 - A5 are automatically inserted by the 82C59A while A6 - A15 are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an 80C86/88/286 system, A15 - A11 are inserted in the five most significant bits of the vectoring byte and the 82C59A sets the three least significant bits according to the interrupt level. A10 - A5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the 82C59A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: ALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only 82C59A in the system. If SNGL = 1, no ICW3 will be issued.

IC4: If this bit is set - ICW4 has to be issued. If ICW4 is not needed, set IC4 = 0.

Initialization Command Word 3 (ICW3)

This word is read only when there is more than one 82C59A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when $\overline{SP}$ = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the bit corresponding to the appropriate IR line for the slave. The master then will release byte 1 of the call sequence (for 8080/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for 80C86/88/286, only byte 2) through the cascade lines.

b. In the slave mode (either when $\overline{SP}$ = 0, or if BUF = 1 and M/S = 0 in ICW4), bits 2 - 0 identify the slave. The slave compares its cascade input with these bits and if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for 80C86/88/286) are released by it on the Data Bus.

NOTE: (The slave address must correspond to the IR line it is connected to in the master ID).

Initialization Command Word 4 (ICW4)

SFNM: If SFNM = 1, the special fully nested mode is programmed.

BUF: If BUF = 1, the buffered mode is programmed. In buffered mode, $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 82C59A is programmed to be a master, M/S = 0 means the 82C59A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1, the automatic end of interrupt mode is programmed.

µPM: Microprocessor mode: µPM = 0 sets the 82C59A for 8080/85 system operation, µPM = 1 sets the 82C59A for 80C86/88/286 system operation.

Operation Command Words (OCWs)

After the Initialization Command Words (ICWs) are programmed into the 82C59A, the device is ready to accept interrupt requests at its input lines. However, during the 82C59A operation, a selection of algorithms can command the 82C59A to operate in various modes through the Operation Command Words (OCWs).

OPERATION COMMAND WORDS (OCWs)

A0	D7	D6	D5	D4	D3	D2	D1	D0
OCW1								
1	M7	M6	M5	M4	M3	M2	M1	M0
OCW2								
0	R	SL	EOI	0	0	L2	L1	L0
OCW3								
0	0	ESMM	SMM	0	1	P	RR	RIS

Operation Command Word 1 (OCW1)

OCW1 sets and clears the mask bits in the Interrupt Mask Register (IMR) M7 - M0 represent the eight mask bits. M = 1 indicates the channel is masked (inhibited), M = 0 indicates the channel is enabled.

Operation Command Word 2 (OCW2)

R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L2, L1, L0 - These bits determine the interrupt level acted upon when the SL bit is active.

Operation Command Word 3 (OCW3)

ESMM - Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM = 0, the SMM bit becomes a "don't care".

SMM - Special Mask Mode. If ESMM = 1 and SMM = 1, the 82C59A will enter Special Mask Mode. If ESMM = 1 and SMM = 0, the 82C59A will revert to normal mask mode. When ESMM = 0, SMM has no effect.

Fully Nested Mode

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (IS0 - 7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command

immediately before returning from the service routine, or if the AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last $\overline{INTA}$. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained in the rotating priority mode or via the set priority command.

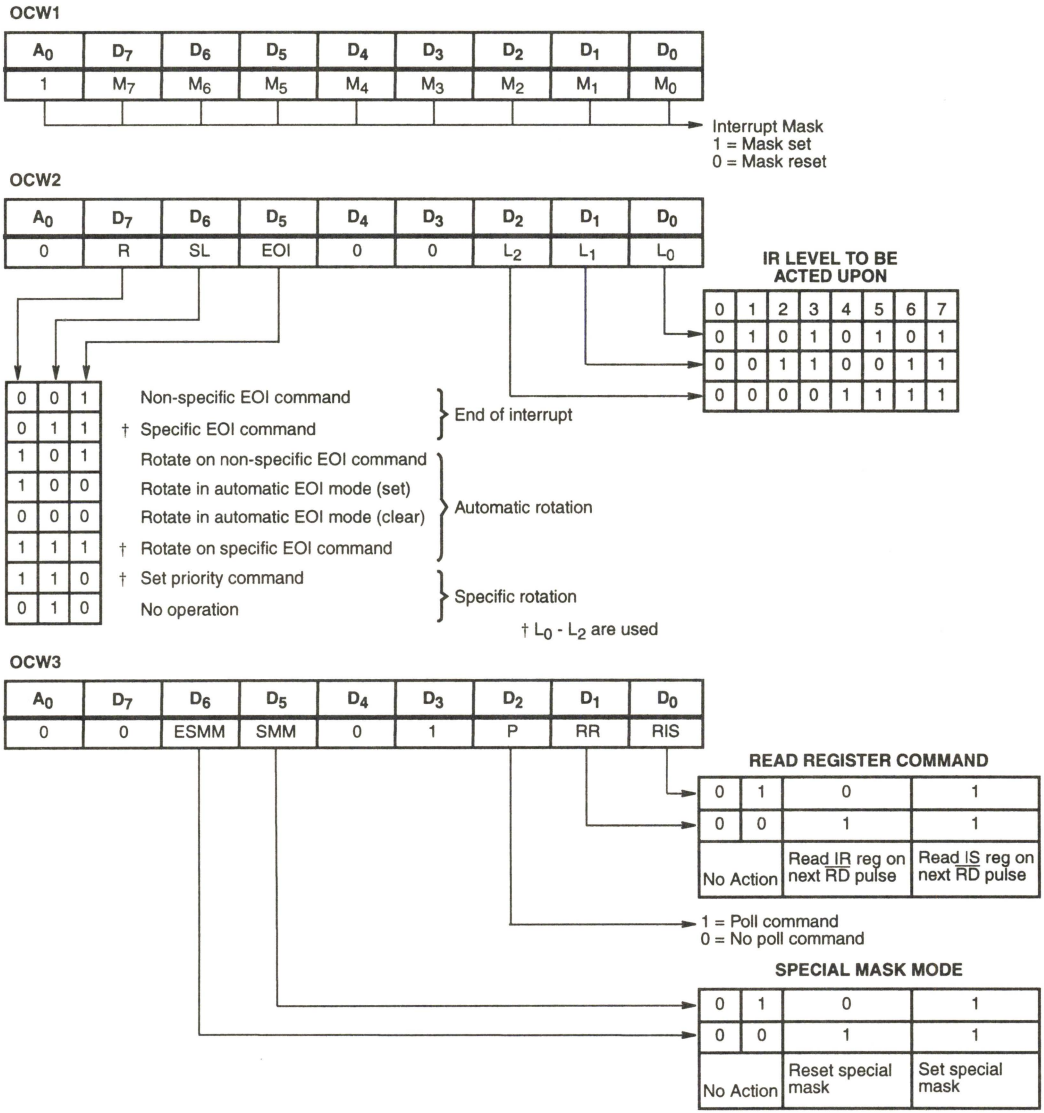


FIGURE 8. 82C59A OPERATION COMMAND WORD FORMAT

End of Interrupt (EOI)

The In-Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence $\overline{INTA}$ pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the 82C59A before returning from a service routine (EOI Command). An EOI command must be issued twice if servicing a slave in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the 82C59A is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific command is issued the 82C59A will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI = 1, SL = 0, R = 0).

When a mode is used which may disturb the fully nested structure, the 82C59A may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI = 1, SL = 1, R = 0, and L0 - L2 is the binary level of the IS bit to be reset).

An IRR bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 82C59A is in the Special Mask Mode.

Automatic End of Interrupt (AEOI) Mode

If AEOI = 1 in ICW4, then the 82C59A will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the 82C59A will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in 8080/85, second in 80C86/88/286). Note that from a system standpoint, this mode should be used only when a nested multilevel interrupt structure is not required within a single 82C59A.

Automatic Rotation (Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most once. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" Status	0	1	0	1	0	0	0	0
Priority Status	7	6	5	4	3	2	1	0
	↑ lowest							↑ highest

After Rotate (IR4 was serviced, all other priorities rotated correspondingly)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" Status	0	1	0	0	0	0	0	0
Priority Status	2	1	0	7	6	5	4	3
	↑ highest							↑ lowest

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R = 1, SL = 0, EOI = 1) and the Rotate in Automatic EOI Mode which is set by (R = 1, SL = 0, EOI = 0) and cleared by (R = 0, SL = 0, EOI = 0).

Specific Rotation (Specific Priority)

The programmer can change priorities by programming the lowest priority and thus, fixing all other priorities; i.e., if IR5 is programmed as the lowest priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R = 1, SL = 1, L0 - L2 is the binary priority level code of the lowest priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R = 1, SL = 1, EOI = 1, and L0 - L2 = IR level to receive lowest priority).

Interrupt Masks

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the operation of other channels.

Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 82C59A would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the Special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level and enables interrupts from all other levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The Special Mask Mode is set by OCW3 where: ESMM = 1, SMM = 1, and cleared where ESMM = 1, SMM = 0.

Poll Command

In this mode, the INT output is not used or the microprocessor internal Interrupt Enable flip flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P = 1 in OCW3. The 82C59A treats the next $\overline{RD}$ pulse to the 82C59A (i.e., $\overline{RD}$ = 0, $\overline{CS}$ = 0) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

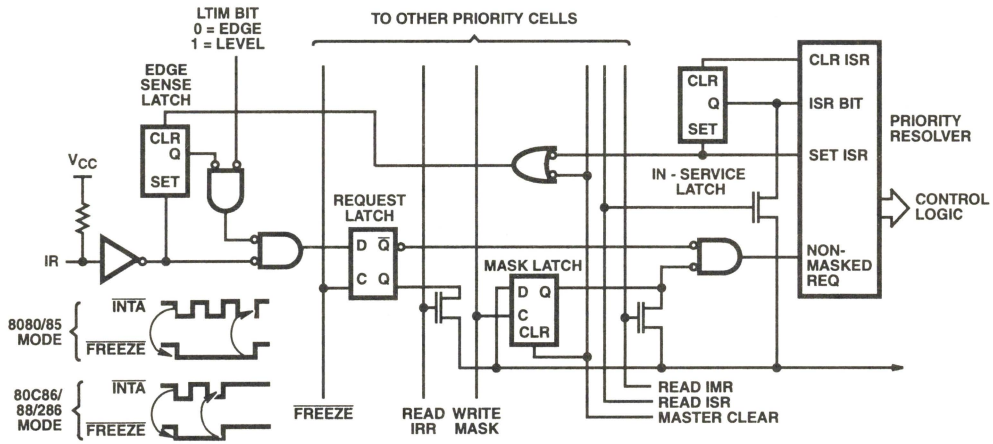
The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
I	-	-	-	-	W2	W1	W0

W0 - W2: Binary code of the highest priority level requesting service.

I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.



NOTES:

1. Master clear active only during ICW1.
2. $\overline{FREEZE}$ is active during $\overline{INTA}$ and poll sequence only.
3. Truth Table for D-latch.

C	D	Q	Operation
1	D1	D1	Follow
0	X	Qn-1	Hold

FIGURE 9. PRIORITY CELL - SIMPLIFIED LOGIC DIAGRAM

Reading the 82C59A Status

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR) or OCW1 (IMR).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. IRR is not affected by IMR.

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the $\overline{RD}$ pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 0).

The ISR can be read when, prior to the $\overline{RD}$ pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 1).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one: i.e., the 82C59A "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used. In the poll mode, the 82C59A

treats the $\overline{RD}$ following a "poll write" operation as an $\overline{INTA}$. After initialization, the 82C59A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{RD}$ is active and A0 = 1 (OCW1). Polling overrides status read when P = 1, RR = 1 in OCW3.

Edge and Level Triggered Modes

This mode is programmed using bit 3 in ICW1.

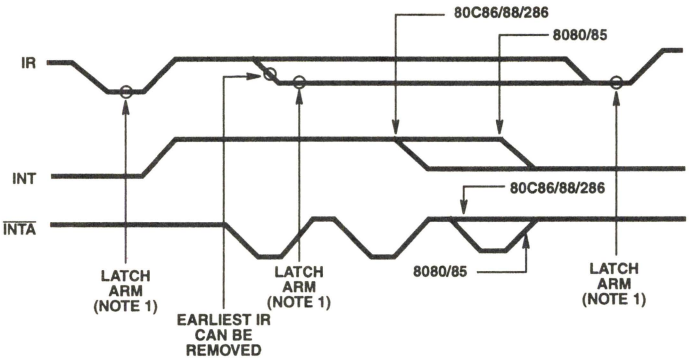
If LTIM = "0", an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

If LTIM = "1", an interrupt request will be recognized by a "high" level on an IR input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occurring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the 82C59A. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first $\overline{INTA}$. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus, ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

In power sensitive applications, it is advisable to place the 82C59A in the edge-triggered mode with the IR lines normally high. This will minimize the current through the internal pull-up resistors on the IR pins.



NOTE:

1. Edge triggered mode only.

FIGURE 10. IR TRIGGERING TIMING REQUIREMENTS

The Special Fully Nested Mode

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the special fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IRs within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specified EOI can be sent to the master, too. If not, no EOI should be sent.

Buffered Mode

When the 82C59A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers

The buffered mode will structure the 82C59A to send an enable signal on $\overline{SP}/\overline{EN}$ to enable the buffers. In this mode, whenever the 82C59A's data bus outputs are enabled, the $\overline{SP}/\overline{EN}$ output becomes active.

This modification forces the use of software programming to determine whether the 82C59A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

Cascade Mode

The 82C59A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

The master controls the slaves through the 3 line cascade bus (CAS2 - 0). The cascade bus acts like chip selects to the slaves during the $\overline{INTA}$ sequence.

In a cascade configuration, the slave interrupt outputs (INT) are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of $\overline{INTA}$. (Byte 2 only for 80C86/88/286).

The cascade bus lines are normally low and will contain the slave address code from the leading edge of the first $\overline{INTA}$ pulse to the trailing edge of the last $\overline{INTA}$ pulse. Each 82C59A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. Chip select decoding is required to activate each 82C59A.

NOTE: Auto EOI is supported in the slave mode for the 82C59A.

The cascade lines of the Master 82C59A are activated only for slave inputs, non-slave inputs leave the cascade line inactive (low). Therefore, it is necessary to use a slave address of 0 (zero) only after all other addresses are used.

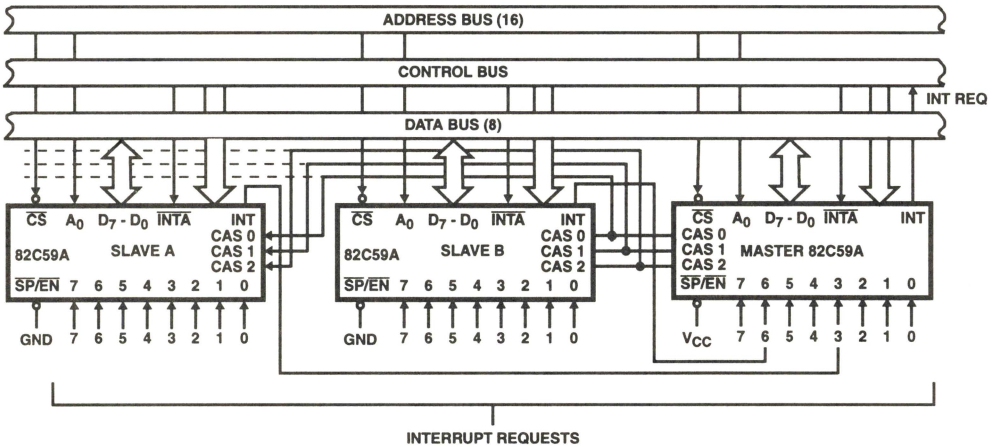


FIGURE 11. CASCADING THE 82C59A

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND-0.5V to V_{CC}+0.5V
ESD Classification . . . . . Class I

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . 0V to +0.8V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	55	12
CLCC Package	65	14
PDIP Package	55	N/A
PLCC Package	65	N/A
SOIC Package	75	N/A

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature Ceramic Package . . . . . +175°C
Maximum Junction Temperature Plastic Package . . . . . +150°C
Maximum Lead Temperature Package (Soldering 10s) . . . . +300°C
(PLCC and SOIC - Lead Tips Only)

Die Characteristics

Gate Count . . . . . 1250 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = +5.0V ±10%, T_A = 0°C to +70°C (C82C59A), T_A = -40°C to +85°C (I82C59A), T_A = -55°C to +125°C (M82C59A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0 2.2	-	V V	C82C59A, I82C59A M82C59A
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
V_{OH}	Output HIGH Voltage	3.0 VCC -0.4	-	V V	I_{OH} = -2.5mA I_{OH} = -100µA
V_{OL}	Output LOW Voltage	-	0.4	V	I_{OL} = +2.5mA
II	Input Leakage Current	-1.0	+1.0	µA	V_{IN} = GND or V_{CC}, Pins 1-3, 26-27
IO	Output Leakage Current	-10.0	+10.0	µA	V_{OUT} = GND or V_{CC}, Pins 4-13, 15-16
ILIR	IR Input Load Current	- -	-200 10	µA µA	V_{IN} = 0V V_{IN} = V_{CC}
ICCSB	Standby Power Supply Current	-	10	µA	V_{CC} = 5.5V, V_{IN} = V_{CC} or GND Outputs Open, (Note 1)
ICCOP	Operating Power Supply Current	-	1	mA/MHz	V_{CC} = 5.0V, V_{IN} = V_{CC} or GND, Outputs Open, T_A = 25°C, (Note 2)

NOTES:

1. Except for IR0 - IR7 where V_{IN} = V_{CC} or open.
2. ICCOP = 1mA/MHz of peripheral read/write cycle time. (ex: 1.0µs I/O read/write cycle time = 1mA).

Capacitance T_A = +25°C

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
CIN	Input Capacitance	15	pF	FREQ = 1MHz, all measurements reference to device GND.
COUT	Output Capacitance	15	pF	
CI/O	I/O Capacitance	15	pF	

AC Electrical Specifications

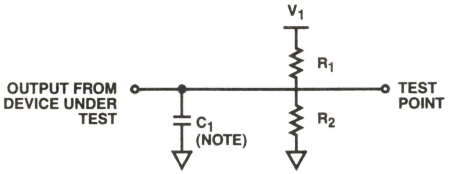
V_{CC} = +5.0V ±10%, GND = 0V, T_A = 0°C to +70°C (C82C59A), T_A -40°C to +85°C (I82C59A), T_A = -55°C to +125°C (M82C59A)

SYMBOL	PARAMETER	82C59A-5		82C59A		82C59A-12		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS									
(1) TAHRL	A0/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$	10	-	10	-	5	-	ns	
(2) TRHAX	A0/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$	5	-	5	-	0	-	ns	
(3) TRLRH	$\overline{RD}$/$\overline{INTA}$ Pulse Width	235	-	160	-	60	-	ns	
(4) TAHWL	A0/$\overline{CS}$ Setup to $\overline{WR}$	0	-	0	-	0	-	ns	
(5) TWHAX	A0/$\overline{CS}$ Hold after $\overline{WR}$	5	-	5	-	0	-	ns	
(6) TWLWH	$\overline{WR}$ Pulse Width	165	-	95	-	60	-	ns	
(7) TDVWH	Data Setup to $\overline{WR}$	240	-	160	-	70	-	ns	
(8) TWHDX	Data Hold after $\overline{WR}$	5	-	5	-	0	-	ns	
(9) TJLJH	Interrupt Request Width Low	100	-	100	-	40	-	ns	
(10) TCVIAL	Cascade Setup to Second or Third $\overline{INTA}$ (Slave Only)	55	-	40	-	30	-	ns	
(11) TRHRL	End of $\overline{RD}$ to next $\overline{RD}$, End of $\overline{INTA}$ (within an $\overline{INTA}$ sequence only)	160	-	160	-	90	-	ns	
(12) TWHWL	End of $\overline{WR}$ to next $\overline{WR}$	190	-	190	-	60	-	ns	
(13) TCHCL (Note 1)	End of Command to next command (not same command type), End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence	500	-	400	-	90	-	ns	
TIMING RESPONSES									
(14) TRLDV	Data Valid from $\overline{RD}$/$\overline{INTA}$	-	160	-	120	-	40	ns	1
(15) TRHDZ	Data Float after $\overline{RD}$/$\overline{INTA}$	5	100	5	85	5	22	ns	2
(16) TJHIH	Interrupt Output Delay	-	350	-	300	-	90	ns	1
(17) TIALCV	Cascade Valid from First $\overline{INTA}$ (Master Only)	-	565	-	360	-	50	ns	1
(18) TRLEL	Enable Active from $\overline{RD}$ or $\overline{INTA}$	-	125	-	100	-	40	ns	1
(19) TRHEH	Enable Inactive from $\overline{RD}$ or $\overline{INTA}$	-	60	-	50	-	22	ns	1
(20) TAHDV	Data Valid from Stable Address	-	210	-	200	-	60	ns	1
(21) TCVDV	Cascade Valid to Valid Data	-	300	-	200	-	70	ns	1

NOTE:

1. Worst case timing for TCHCL in an actual microprocessor system is typically greater than the values specified for the 82C59A, (i.e. 8085A = 1.6µs, 8085A -2 = 1µs, 80C86 = 1µs, 80C286 -10 = 131ns, 80C286 -12 = 98ns).

AC Test Circuit



NOTE: Includes stray and jig capacitance.

TEST CONDITION DEFINITION TABLE

TEST CONDITION	V_1	R_1	R_2	C_1
1	1.7V	523Ω	Open	100pF
2	V_{CC}	1.8kΩ	1.8kΩ	50pF

AC Testing Input, Output Waveform



NOTE: AC Testing: All input signals must switch between V_{IL} - 0.4V and V_{IH} + 0.4V. Input rise and fall times are driven at 1ns/V.

Timing Waveforms

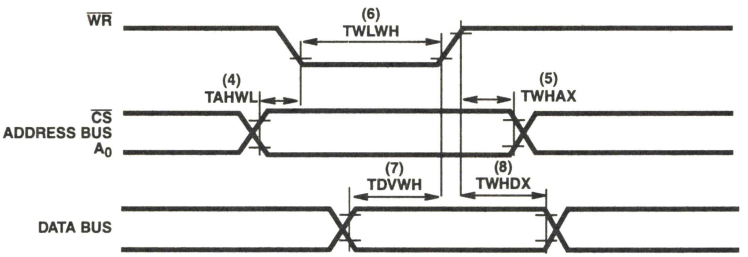


FIGURE 12. WRITE

Timing Waveforms (Continued)

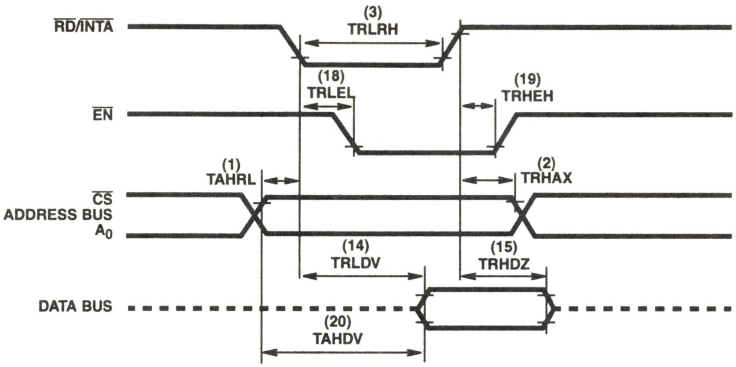


FIGURE 13. $\overline{\text{READ}}/\overline{\text{INTA}}$

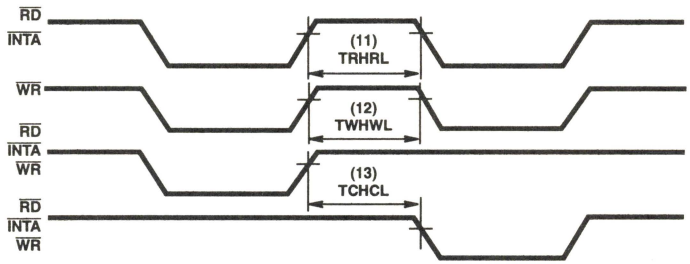
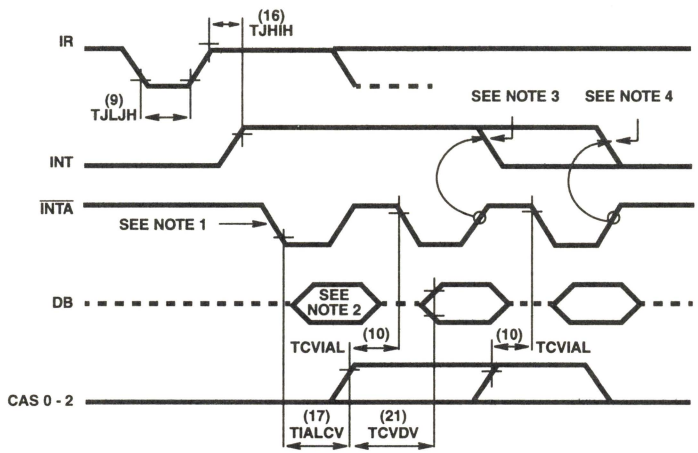


FIGURE 14. OTHER TIMING



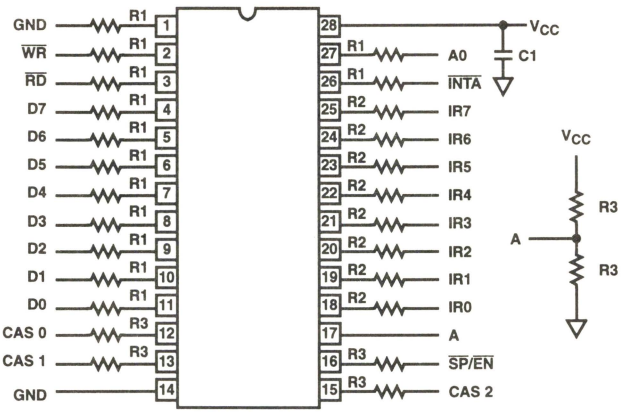
NOTES:

1. Interrupt Request (IR) must remain HIGH until leading edge of first $\overline{\text{INTA}}$.
2. During first $\overline{\text{INTA}}$ the Data Bus is not active in 80C86/88/286 mode.
3. 80C86/88/286 mode.
4. 8080/8085 mode.

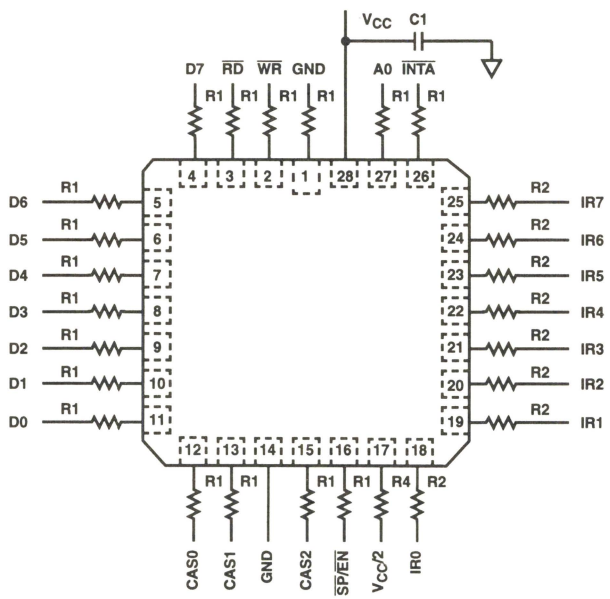
FIGURE 15. $\overline{\text{INTA}}$ SEQUENCE

Burn-In Circuits

MD82C59A CERDIP



MR82C59A CLCC



NOTES:

1. V_{CC} = 5.5V ±0.5V.
2. V_{IH} = 4.5V ±10%.
3. V_{IL} = -0.2V to 0.4V.
4. GND = 0V.
5. R1 = 47kΩ ±5%.
6. R2 = 510Ω ±5%.
7. R3 = 10kΩ ±5%.
8. R4 = 1.2kΩ ±5%.
9. C1 = 0.01µF min.
10. F0 = 100kHz ±10%.
11. F1 = F0/2, F2 = F1/2, ...F8 = F7/2.

Die Characteristics

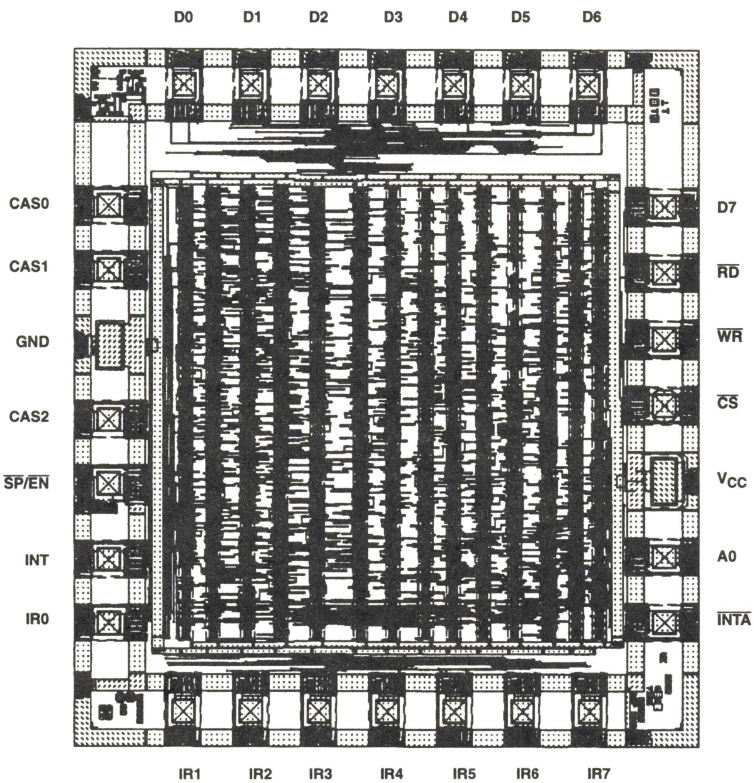
DIE DIMENSIONS:
143 x 130 x 19 ±1mils
(3630 x 3310 x 525µm)

METALLIZATION:
Type: Si-Al-Cu
Thickness: Metal 1: 8kÅ ± 0.75kÅ
Metal 2: 12kÅ ± 1.0kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ ± 3.0kÅ

Metallization Mask Layout

82C59A



HARRIS SEMICONDUCTOR

82C82

March 1997

CMOS Octal Latching Bus Driver

Features

- Full Eight-Bit Parallel Latching Buffer
- Bipolar 8282 Compatible
- Three-State Noninverting Outputs
- Propagation Delay . . . . . 35ns Max.
- Gated Inputs:
  - Reduce Operating Power
  - Eliminate the Need for Pull-Up Resistors
- Single 5V Power Supply
- Low Power Operation . . . . . ICCSB = 10μA
- Operating Temperature Ranges
  - C82C82 . . . . . 0°C to +70°C
  - I82C82 . . . . . -40°C to +85°C
  - M82C82 . . . . . -55°C to +125°C

Description

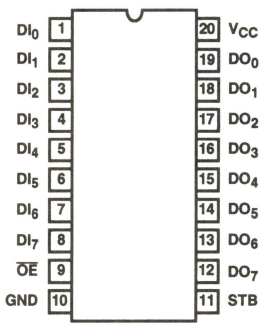
The Harris 82C82 is a high performance CMOS Octal Latching Buffer manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C82 provides an eight-bit parallel latch/buffer in a 20 pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable ($\overline{OE}$) permits simple interface to state-of-the-art microprocessor systems.

Ordering Information

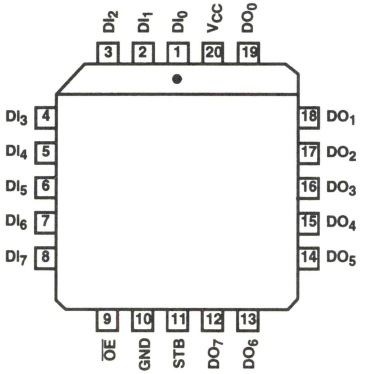
PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
CP82C82	0°C to +70°C	20 Ld PDIP	E20.3
IP82C82	-40°C to +85°C		
CS82C82	0°C to +70°C	20 Ld PLCC	N20.35
IS82C82	-40°C to +85°C		
CD82C82	0°C to +70°C	20 Ld CERDIP	F20.3
ID82C82	-40°C to +85°C		
MD82C82/B	-55°C to +125°C		
8406701RA		SMD #	
MR82C82/B	-55°C to +125°C	20 Pad CLCC	J20.A
84067012A		SMD #	

Pinouts

82C82 (PDIP, CERDIP)
TOP VIEW



82C82 (PLCC, CLCC)
TOP VIEW



TRUTH TABLE

STB	$\overline{OE}$	DI	DO
X	H	X	Hi-Z
H	L	L	L
H	L	H	H
↓	L	X	†

H = Logic One
L = Logic Zero
X = Don't Care
† = Latched to Value of Last Data
Hi-Z = High Impedance
↓ = Neg. Transition

PIN NAMES

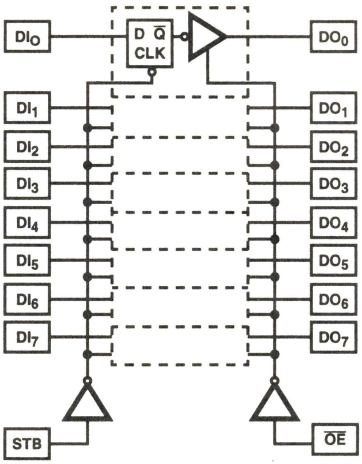
PIN	DESCRIPTION
DI_0-DI_7	Data Input Pins
DO_0-DO_7	Data Output Pins
STB	Active High Strobe
$\overline{OE}$	Active Low Output Enable

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2975.1**

Functional Diagram



Gated Inputs

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between V_{CC} and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance ("float" condition), it could create an indeterminate logic state at the input and cause a disruption in device operation.

The Harris 82C8X Series of bus drivers eliminates these conditions by turning off data inputs when data is latched (STB = logic zero for the 82C82/83H) and when the device is disabled ($\overline{OE}$ = logic one for 82C86H/87H). These gated inputs disconnect the input circuitry from the V_{CC} and ground power supply pins by turning off the upper P-channel and lower N-channel (see Figures 1, 2). No new current flow from V_{CC} to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

DC input voltage levels can also cause an increase in ICC if these input levels approach the minimum V_{IH} or maximum V_{IL} conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the trans parent mode (STB = logic one). ICC remains below the maximum ICC standby specification of l0mA during the time inputs are disabled, thereby, greatly reducing the average power dissipation of the 82C8X series devices

Typical 82C82 System Example

In a typical 80C86/88 system, the 82C82 is used to latch multiplexed addresses and the STB input is driven by ALE (Address Latch Enable) (see Figure 3). The high pulse width of ALE is approximately 100ns with a bus cycle time of 800ns (80C86/88 at 5MHz). The 82C82 inputs are active only 12.5% of the bus cycle time. Average power dissipation related to input transitioning is reduced by this factor also.

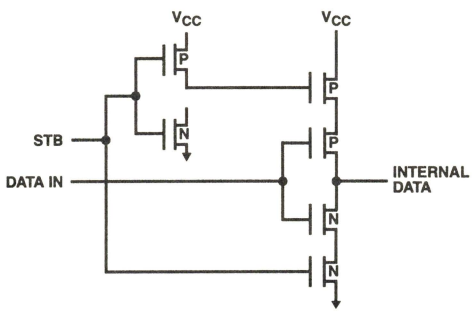


FIGURE 1. 82C82/83H

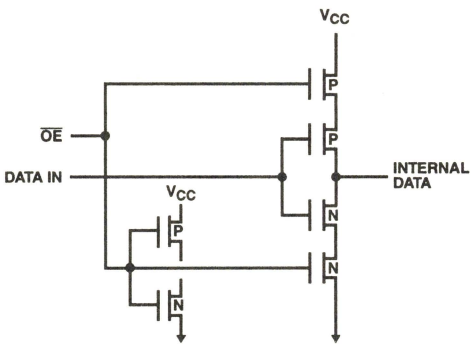


FIGURE 2. 82C86H/87H GATED INPUTS

Application Information

Decoupling Capacitors

The transient current required to charge and discharge the 300pF load capacitance specified in the 82C82 data sheet is determined by:

$$I = C_L(dv/dt) \quad \text{(EQ. 1)}$$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = C_L \quad \text{(EQ. 2)}$$

$$\frac{(V_{CC} \times 80\%)}{tR/tF} \quad \text{(EQ. 3)}$$

where tR = 20ns, V_{CC} = 5.0V, C_L = 300pF on each of eight outputs.

$$I = (8 \times 300 \times 10^{-12}) \times (5.0V \times 0.8)/(20 \times 10^{-9}) = 480mA \quad \text{(EQ. 4)}$$

This current spike may cause a large negative voltage spike on V_{CC}, which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1µF ceramic disc decoupling capacitor be placed between V_{CC} and GND at each device, with placement being as near to the device as possible.

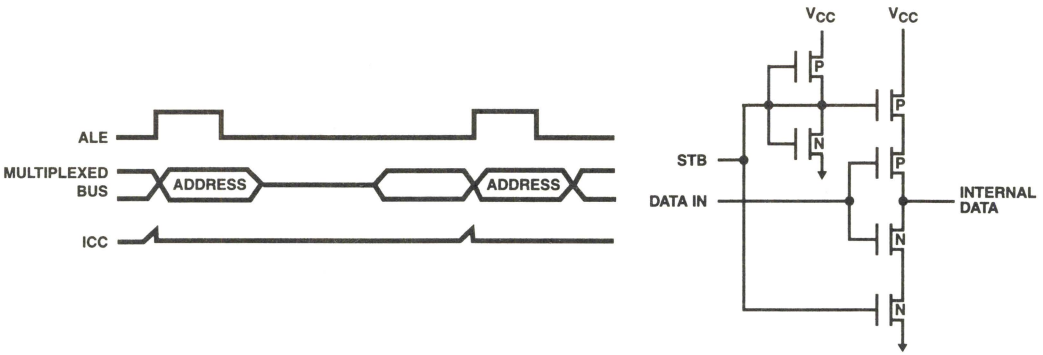


FIGURE 3. SYSTEM EFFECTS OF GATED INPUTS

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND-0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C82 . . . . . 0°C to +70°C
I82C82 . . . . . -40°C to +85°C
M82C82 . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP	75°C/W	18°C/W
CLCC	85°C/W	22°C/W
PDIP	75	N/A
PLCC	75	N/A

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package . . . . . +150°C
Minimum Lead Temperature (Soldering 10s) . . . . . +300°C
(PLCC Lead Tips Only)

Die Characteristics

Gate Count . . . . . 65 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5.0V ±10%; T_A = 0°C to +70°C (C82C82); T_A = -40°C to +85°C (I82C82); T_A = -55°C to +125°C (M82C82)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0	-	V	C82C82, I82C82 (Note 1)
		2.2	-	V	M82C82 (Note 1)
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
V_{OH}	Logical One Output Voltage	2.9	-	V	I_{OH} = -8mA, $\overline{OE}$ = GND
		V_{CC} -0.4V	-	V	I_{OH} = -100µA, $\overline{OE}$ = GND
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} = 8mA, $\overline{OE}$ = GND
II	Input Leakage Current	-1.0	1.0	µA	V_{IN} = GND or V_{CC}, DIP Pins 1-9, 11
IO	Output Leakage Current	-10.0	10.0	µA	V_O = GND or V_{CC}, $\overline{OE} \geq V_{CC}$ -0.5V DIP Pins 12-19
ICCSB	Standby Power Supply Current	-	10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs Open
ICCOP	Operating Power Supply Current	-	1	mA/MHz	T_A = +25°C, V_{CC} = 5V, Typical (See Note 2)

NOTES:

1. V_{IH} is measured by applying a pulse of magnitude = V_{IH} min to one data input at a time and checking the corresponding device output for a valid logical "1" during valid input high time. Control pins (STB, $\overline{OE}$) are tested separately with all device data input pins at V_{CC} -0.4.
2. Typical ICCOP = 1mA/MHz of STB cycle time. (Example: 5MHz µP, ALE = 1.25MHz, ICCOP = 1.25mA).

Capacitance

T_A = +25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	13	pF	Freq = 1MHz, all measurements are referenced to device GND
C_{OUT}	Output Capacitance	20	pF	

AC Electrical Specifications

V_{CC} = 5.0V ±10%; C_L = 300pF (Note 1), Freq = 1MHz

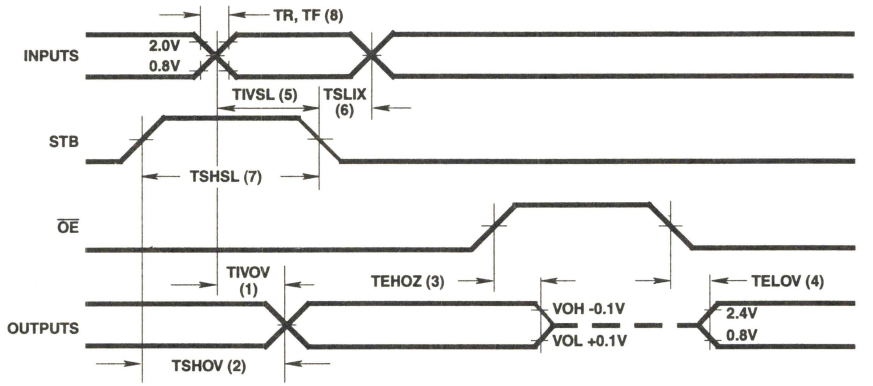
T_A = 0°C to +70°C (C82C82);
T_A = -40°C to +85°C (I82C82);
T_A = -55°C to +125°C (M82C82)

	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1)	TIVOV	Propagation Delay Input to Output	-	35	ns	Notes 2, 3
(2)	TSHOV	Propagation Delay STB to Output	-	55	ns	Notes 2, 3
(3)	TEHOZ	Output Disable Time	-	35	ns	Notes 2, 3
(4)	TELOV	Output Enable Time	-	50	ns	Notes 2, 3
(5)	TIVSL	Input to STB Setup Time	0	-	ns	Notes 2, 3
(6)	TSLIX	Input to STB Hold Time	25	-	ns	Notes 2, 3
(7)	TSHSL	STB High Time	25	-	ns	Notes 2, 3
(8)	TR, TF	Input Rise/Fall Times	-	20	ns	Notes 2, 3

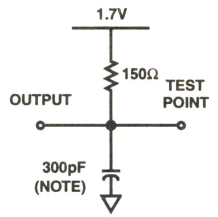
NOTES:

1. Output load capacitance is rated at 300pF for ceramic and plastic packages.
2. All AC parameters tested as per test circuits and definitions below. Input rise and fall times are driven at 1ns/V.
3. Input test signals must switch between V_{IL} - 0.4V and V_{IH} +0.4V.

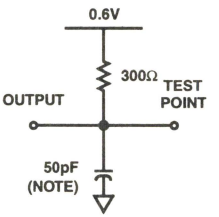
Timing Waveforms



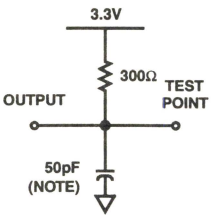
Test Load Circuits



TIVOV, TSHOV, TELOV



TEHOZ OUTPUT HIGH DISABLE

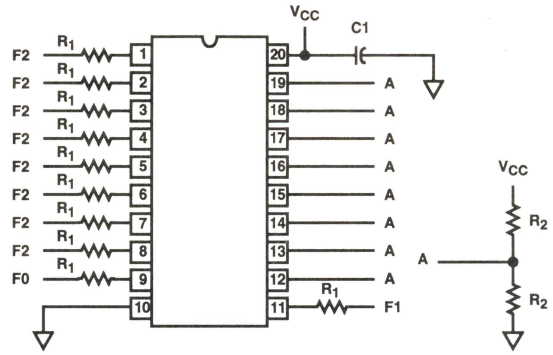


TEHOZ OUTPUT LOW DISABLE

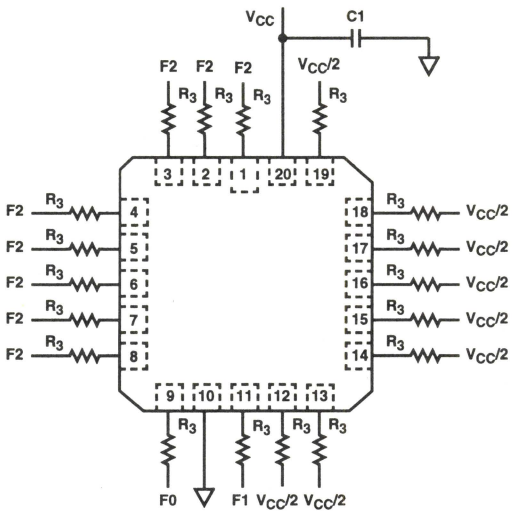
NOTE: Includes stray and jig capacitance.

Burn-In Circuits

MD 82C82 CERDIP



MR 82C82 CLCC



NOTES:

1. V_{CC} = 5.5 ± 0.5V, GND = 0V.
2. V_{IH} = 4.5V ±10%.
3. V_{IL} = -0.2V to 0.4V.
4. R_1 = 47kΩ ±5%.
5. R_2 = 2.0kΩ ±5%.
6. R_3 = 4.2kΩ ±5%.
7. R_4 = 470kΩ ±5%.
8. C_1 = 0.01μF minimum.
9. F_0 = 100kHz ±10%.
10. $F_1 = F_0/2$, $F_2 = F_1/2$.

Die Characteristics

DIE DIMENSIONS:
118.1 x 92.1 x 19 ±1mils

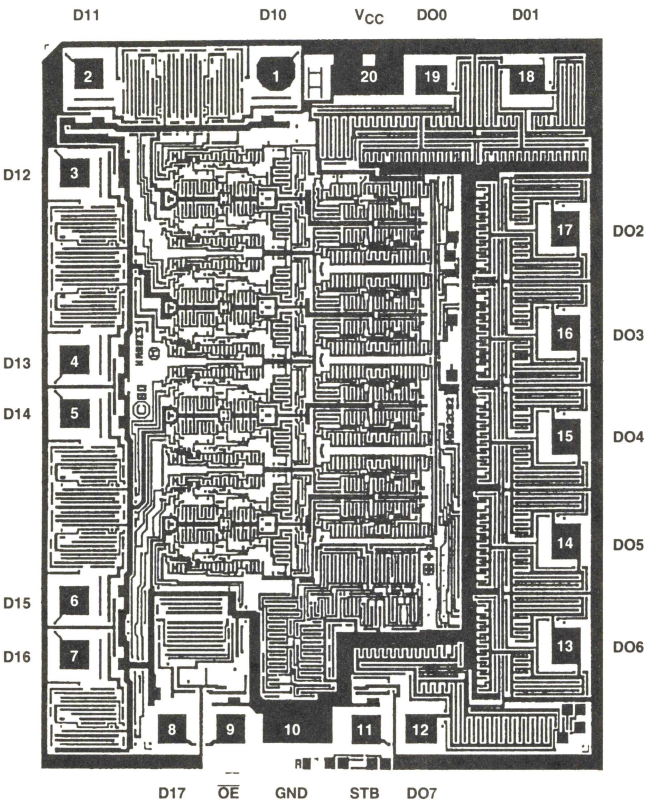
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
2.00 x 10^5 A/cm^2

Metallization Mask Layout

82C82



March 1997

CMOS Octal Latching Inverting Bus Driver

Features

- Full 8-Bit Parallel Latching Buffer
- Bipolar 8283 Compatible
- Three-State Inverting Outputs
- Propagation Delay . . . . . 25ns Max
- Gated Inputs
  - Reduce Operating Power
  - Eliminate the Need for Pull-Up Resistors
- Single 5V Power Supply
- Low Power Operation
  - ICCSB 10mA
- Operating Temperature Ranges
  - C82C83H . . . . . 0°C to +70°C
  - I82C83H . . . . . -40°C to +85°C
  - M82C83H . . . . . -55°C to +125°C

Description

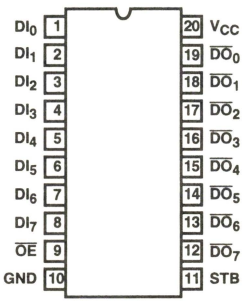
The Harris 82C83H is a high performance CMOS Octal Latching Buffer manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C83H provides an 8-bit parallel latch/buffer in a 20 lead pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable (OE) permits simple interface to microprocessor systems. The 82C83H provides inverted data at the outputs.

Ordering Information

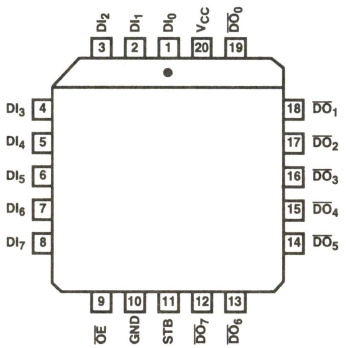
PART NO.	PACKAGE	TEMP RANGE	PKG. NO
CP82C83H	20 Ld PDIP	0°C to +70°C	E20.3
IP82C83H		-40°C to +85°C	E20.3
CS82C83H	20 Ld PLCC	0°C to +70°C	N20.35
IS82C83H		-40°C to +85°C	N20.35
CD82C83H	20 Ld CERDIP	0°C to +70°C	F20.3
ID82C83H		-40°C to +85°C	F20.3
MD82C83H/B		0°C to +70°C	F20.3
8406702RA	SMD#	-55°C to +125°C	F20.3
MR82C83H/B	20 Pad CLCC	-55°C to +125°C	J20.A
84067022A	SMD#	-55°C to +125°C	J20.A

Pinouts

82C83H (PDIP, CERDIP)
TOP VIEW



82C83H (PLCC, CLCC)
TOP VIEW



TRUTH TABLE

STB	OE	DI	DO
X	H	X	HI-Z
H	L	L	H
H	L	H	L
↓	L	X	†

H = Logic One
L = Logic Zero
X = Don't Care

HI-Z = High Impedance
↓ = Negative Transition
† = Latched to Value of Last Data

PIN NAMES

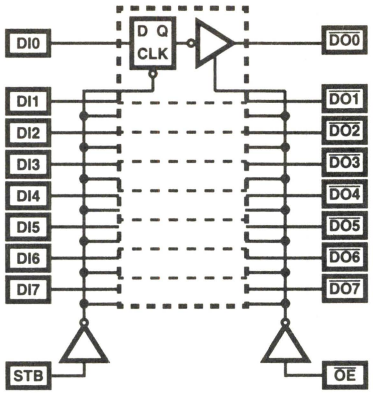
PIN	DESCRIPTION
DI_0 - DI_7	Data Input Pins
DO_0 - DO_7	Data Output Pins
STB	Active High Strobe
OE	Active Low Output Enable

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 2971.1

Functional Diagram



Gated Inputs

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between V_{CC} and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance (``float'' condition), it could create an indeterminate logic state at the inputs and cause a disruption in device operation.

The Harris 82C8X series of bus drivers eliminates these conditions by turning off data inputs when data is latched (STB = logic zero for the 82C82/83H) and when the device is disabled ($\overline{OE}$ = logic one for the 82C86H/87H). These gated inputs disconnect the input circuitry from the V_{CC} and ground power supply pins by turning off the upper P-channel and lower N-channel (See Figures 1 and 2). No current flow from V_{CC} to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

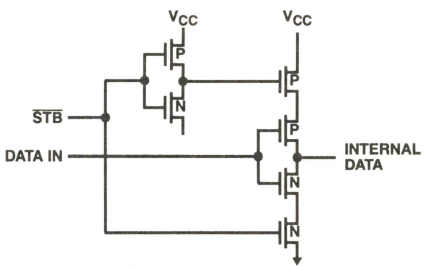


FIGURE 1. 82C82/83H

D.C. input voltage levels can also cause an increase in ICC if these input levels approach the minimum V_{IH} or maximum V_{IL} conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the transparent mode (STB = logic one). ICC remains below the maximum ICC standby specification of 10µA during the time inputs are disabled, thereby greatly reducing the average power dissipation of the 82C8X series devices.

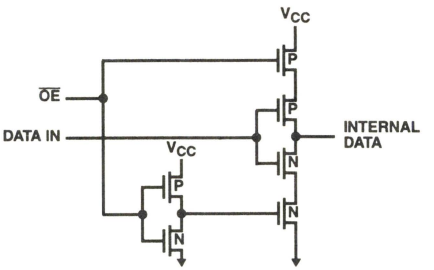


FIGURE 2. 82C86H/87H GATED INPUTS

Decoupling Capacitors

The transient current required to charge and discharge the 300pF load capacitance specified in the 82C83H data sheet is determined by

$I = C_L (dv/dt)$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = C_L \frac{(V_{CC} \times 80 \text{ percent})}{t_R/t_F} \qquad \text{(EQ. 1)}$$

where t_R = 20ns, V_{CC} = 5.0V, C_L = 300pF on each eight outputs.

$I = (8 \times 300 \times 10^{-12}) \times (5.0V \times 0.8)/(20 \times 10^{-9}) = 480mA$

This current spike may cause a large negative voltage spike on V_{CC} which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1µF ceramic disc capacitor be placed between V_{CC} and GND at each device, with placement being as near to the device as possible.

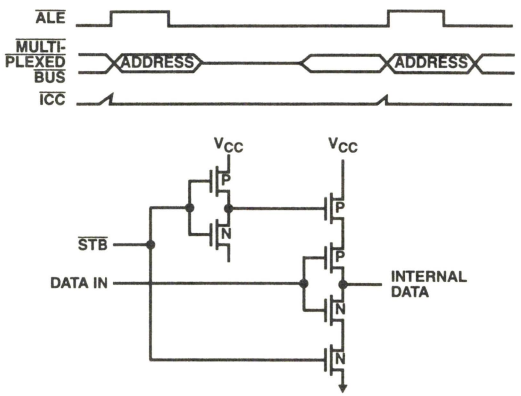


FIGURE 3. SYSTEM EFFECTS OF GATED INPUTS

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND 0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C83H . . . . . 0^oC to $+70^oC$
I82C83H . . . . . -40^oC to $+85^oC$
M82C83H . . . . . -55^oC to $+125^oC$

Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}{}^oC/W$	$\theta_{JC}{}^oC/W$
CERDIP Package	70	16
CLCC Package	80	20
PDIP Package	75	N/A
PLCC Package	75	N/A

Storage Temperature Range . . . . . -65^oC to $+150^oC$
Max Junction Temperature Ceramic Package . . . . . $+175^oC$
Max Junction Temperature Plastic Package . . . . . $+150^oC$
Lead Temperature (Soldering 10s) (PLCC - Lead Tips Only) . . $+300^oC$

Die Characteristics

Gate Count . . . . . 265 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5.0V ± 10%; T_A = 0^oC to $+70^oC$ (C82C83H);
T_A = -40^oC to $+85^oC$ (I82C83H);
T_A = -55^oC to $+125^oC$ (M82C83H)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0 2.2	-	V	C82C83H, I82C83H, M82C83H, (Note 1)
V_{IL}	Logical Zero Input Voltage		0.8	V	
V_{OH}	Logical One Output Voltage	3.0 V_{CC} -0.4V	-	V	I_{OH} = -8mA, I_{OH} = -100mA, $\overline{OE}$ = GND
V_{OL}	Logical Zero Output Voltage		0.45	V	I_{OL} = 20mA, $\overline{OE}$ = GND
I_I	Input Leakage Current	-10	10	µA	V_{IN} = GND or V_{CC}, DIP Pins 1-9,11
I_O	Output Leakage Current	-10	10	µA	V_O = GND or $\overline{OE} \geq V_{CC}$ -0.5V DIP Pins 12-19
ICCSB	Standby Power Supply Current	-	10	µA	V_{IN} = V_{CC} or GND V_{CC} = 5.5V Outputs Open
IC COP	Operating Power Supply Current	-	1	mA/MHz	T_A = $+25^oC$, V_{CC} = 5V, Typical (See Note 2)

NOTES:

1. V_{IH} is measured by applying a pulse of magnitude = V_{IHMIN} to one data Input at a time and checking the corresponding device output for a valid logical 1 - during valid input high time. Control pins (STB, $\overline{CE}$) are tested separately with all device data input pins at V_{CC} -0.4V.
2. Typical ICCOP = 1 mA/MHz of STB cycle time. (Example: 5MHz µP, ALE = 1.25MHz, ICCOP = 1.25mA).

Capacitance

T_A = $+25^oC$

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	13	pF	FREQ = 1MHz, all measurements are referenced to device GND
C_{OUT}	Output Capacitance	20	pF	

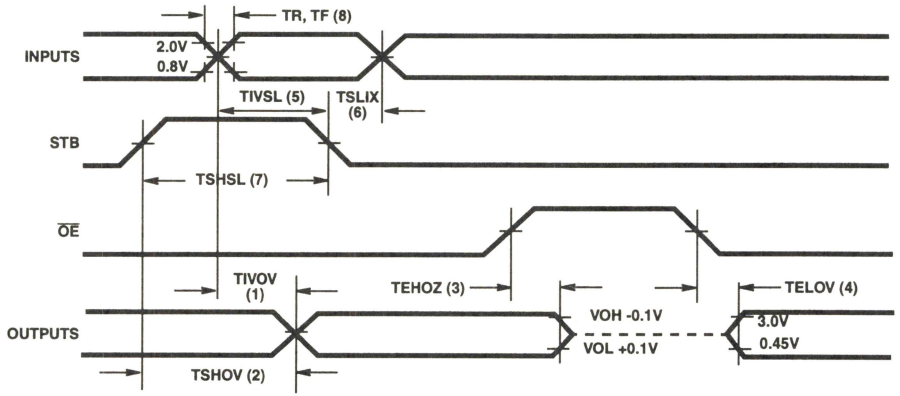
AC Electrical Specifications V_{CC} = 5.0V ±10%; C_L = 300pF (Note 1), FREQ = 1MHz
T_A = 0°C to +70°C (C82C83H);
T_A = -40°C to +85°C (I82C83H);
T_A = -55°C to +125°C (M82C83H)

SYMBOL	PARAMETER	LIMITS		UNITS	TEST CONDITIONS
		MIN	MAX		
(1) TIVOV	Propagation Delay Input to Output	5	25	ns	See Notes 2, 3
(2) TSHOV	Propagation Delay STB to Output	10	50	ns	See Notes 2, 3
(3) TEHOZ	Output Disable Time	5	22	ns	See Notes 2, 3
(4) TELOV	Output Enable Time	10	45	ns	See Notes 2, 3
(5) TIVSL	Input to STB Set Up Time	0	-	ns	See Notes 2, 3
(6) TSLIX	Input to STB Hold Time	30	-	ns	See Notes 2, 3
(7) TSHSL	STB High Time	15	-	ns	See Notes 2, 3
(8) TR, TF	Input Rise/Fall Times	-	20	ns	See Notes 2, 3

NOTES:

1. Output load capacitance is rated 300pF for both ceramic and plastic packages.
2. All AC Parameters tested as per test load circuits. Input rise and tall times are driven at 1ns/V.
3. Input test signals must switch between V_{IL} -0.4V and V_{IH} +0.4V.

Timing Waveforms



All Timing measurements are made at 1.5V unless otherwise noted.

FIGURE 4. TIMING WAVEFORMS

Test Load Circuits

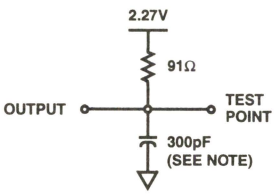


FIGURE 5. TIVOV, TSHOV

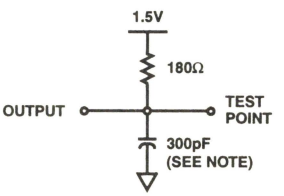
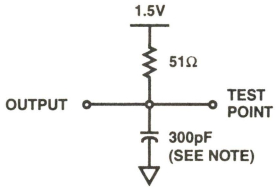


FIGURE 6. TELOV OUTPUT HIGH ENABLE

Test Load Circuits (Continued)



NOTE: Includes jig and stray capacitance.

FIGURE 7. TELOV OUTPUT LOW ENABLE

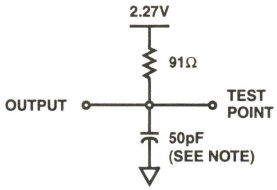


FIGURE 8. TEHOZ OUTPUT LOW/HIGH DISABLE

Burn-In Circuits

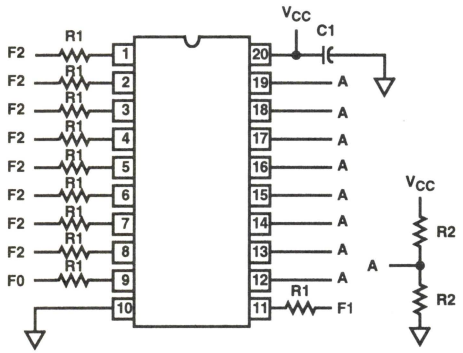


FIGURE 9. MD82C83H CERDIP

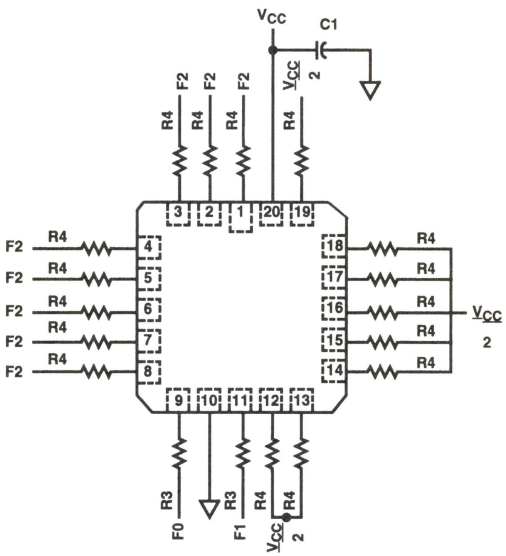


FIGURE 10. MR82C83H CLCC

NOTES:

1. V_{CC} = 5.5V ± 0.5V GND = 0V
2. V_{IH} = 4.5V ± 10%
3. V_{IL} = -0.2 to 0.4V
4. R1 = 47kW ± 5%
5. R2 = 2.0kW ± 5%
6. R3 = 1.0kW ± 5%
7. R4 = 5.0kW ± 5%
8. C1 = 0.01µF Minimum
9. F0 = 100kHz ± 10%
10. F1 = F0/2, F2 = F1/2, F3 = F2/2

Die Characteristics

DIE DIMENSIONS:
138.6 x 155.5 x 19 ± 1 mils

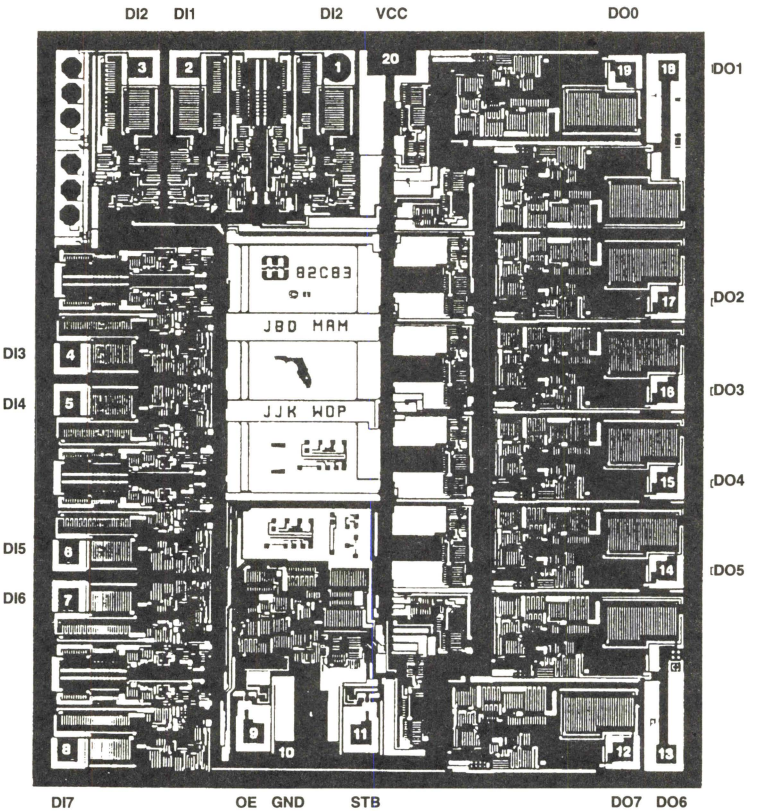
METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
2.0 x 10^5 A/cm^2

Metallization Mask Layout

82C83H



Features

- Generates the System Clock For CMOS or NMOS Microprocessors
- Up to 25MHz Operation
- Uses a Parallel Mode Crystal Circuit or External Frequency Source
- Provides Ready Synchronization
- Generates System Reset Output From Schmitt Trigger Input
- TTL Compatible Inputs/Outputs
- Very Low Power Consumption
- Single 5V Power Supply
- Operating Temperature Ranges
  - C82C84A . . . . . .0°C to +70°C
  - I82C84A . . . . . -40°C to +85°C
  - M82C84A . . . . . -55°C to +125°C

Description

The Harris 82C84A is a high performance CMOS Clock Generator-driver which is designed to service the requirements of both CMOS and NMOS microprocessors such as the 80C86, 80C88, 8086 and the 8088. The chip contains a crystal controlled oscillator, a divide-by-three counter and complete "Ready" synchronization and reset logic.

Static CMOS circuit design permits operation with an external frequency source from DC to 25MHz. Crystal controlled operation to 25MHz is guaranteed with the use of a parallel, fundamental mode crystal and two small load capacitors.

All inputs (except X1 and $\overline{RES}$) are TTL compatible over temperature and voltage ranges.

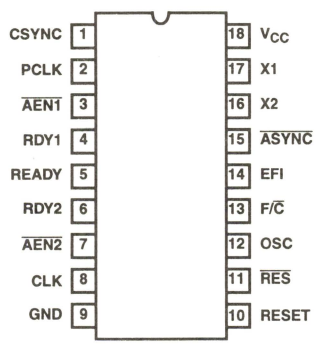
Power consumption is a fraction of that of the equivalent bipolar circuits. This speed-power characteristic of CMOS permits the designer to custom tailor his system design with respect to power and/or speed requirements.

Ordering Information

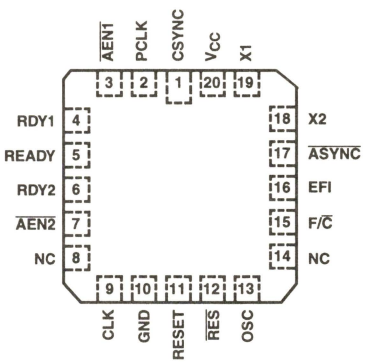
PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
CP82C84A	0°C to +70°C	18 Ld PDIP	E18.3
IP82C84A	-40°C to +85°C		E18.3
CS82C84A	0°C to +70°C	20 Ld PLCC	N20.35
IS82C84A	-40°C to +85°C		N20.35
CD82C84A	0°C to +70°C	18 Ld CERDIP	F18.3
ID82C84A	-40°C to +85°C		F18.3
MD82C84A/B	-55°C to +125°C		F18.3
8406801VA		SMD#	F18.3
MR82C84A/B	-55°C to +125°C	20 Pad CLCC	J20.A
84068012A		SMD#	J20.A

Pinouts

82C84A (PDIP, CERDIP)
TOP VIEW

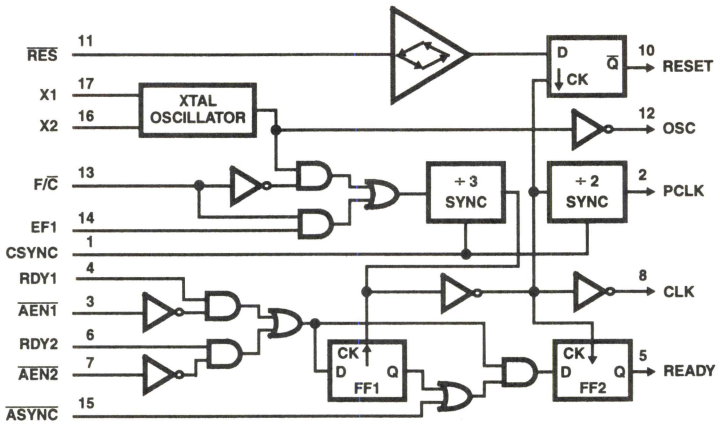


82C84A (PLCC, CLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Functional Diagram



CONTROL PIN	LOGICAL 1	LOGICAL 0
F/$\overline{C}$	External Clock	Crystal Drive
$\overline{RES}$	Normal	Reset
RDY1, RDY2	Bus Ready	Bus Not Ready
$\overline{AEN1}$, $\overline{AEN2}$	Address Disabled	Address Enable
$\overline{ASYNC}$	1 Stage Ready Synchronization	2 Stage Ready Synchronization

Pin Description

SYMBOL	NUMBER	TYPE	DESCRIPTION
$\overline{AEN1}$, $\overline{AEN2}$	3, 7	I	ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN}$1 validates RDY1 while $\overline{AEN2}$ validates RDY2. Two $\overline{AEN}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non-Multi-Master configurations, the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY1, RDY2	4, 6	I	BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{ASYNC}$	15	I	READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH, a single stage of READY synchronization is provided.
READY	5	O	READY: READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	17, 16	I O	CRYSTAL IN: X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency, (Note 1).
F/$\overline{C}$	13	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{C}$ is a strapping option. When strapped LOW. F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated for the EFI input, (Note 1).
EFI	14	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	8	O	PROCESSOR CLOCK: CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus. CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle.
PCLK	2	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
OSC	12	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	11	I	RESET IN: $\overline{RES}$ is an active LOW signal which is used to generate RESET. The 82C84A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	10	O	RESET: RESET is an active HIGH signal which is used to reset the 80C86 family processors. Its timing characteristics are determined by $\overline{RES}$.
CSYNC	1	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple 82C84As to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND	9		Ground
V_{CC}	18		V_{CC}: The +5V power supply pin. A 0.1µF capacitor between V_{CC} and GND is recommended for decoupling.

NOTE:

1. If the crystal inputs are not used X1 must be tied to V_{CC} or GND and X2 should be left open.

Functional Description

Oscillator

The oscillator circuit of the 82C84A is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

TABLE 1. CRYSTAL SPECIFICATIONS

PARAMETER	TYPICAL CRYSTAL SPEC
Frequency	2.4 - 25MHz, Fundamental, "AT" cut
Type of Operation	Parallel
Unwanted Modes	6dB (Minimum)
Load Capacitance	18 - 32pF

Capacitors C1, C2 are chosen such that their combined capacitance

$$CT = \frac{C1 \times C2}{C1 + C2} \text{ (Including stray capacitance)}$$

matches the load capacitance as specified by the crystal manufacturer. This ensures operation within the frequency tolerance specified by the crystal manufacturer.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another 82C84A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 82C84A. This is accomplished with two flip-flops. (See Figure 1). The counter output is a 33% duty cycle clock at one-third the input frequency.

NOTE: The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷ 3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle clock driver designed to drive the 80C86, 80C88 processors directly. PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 82C84A.

READY Synchronization

Two READY input (RDY1, RDY2) are provided to accommodate two system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

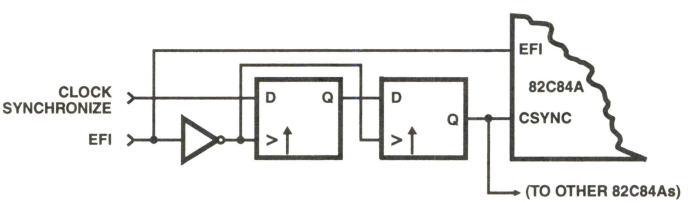
Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation.

When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one of the rising edge of CLK (requiring a setup time tR1VCH) and the synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, TR1VCL, on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.



NOTE: If EFI input is used, then crystal input X1 must be tied to V_{CC} or GND and X2 should be left open. If the crystal inputs are used, then EFI should be tied to V_{CC} or GND.

FIGURE 1. CSYNC SYNCHRONIZATION

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C84A . . . . . 0^oC to $+70^oC$
I82C84A . . . . . -40^oC to $+85^oC$
M82C84A . . . . . -55^oC to $+125^oC$

Thermal Information

Thermal Resistance	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	80	20
CLCC Package	95	28
PDIP Package	85	N/A
PLCC Package	85	N/A

Storage Temperature Range . . . . . -65^oC to $+150^oC$
Max Junction Temperature . . . . . $+175^oC$
Lead Temperature (Soldering 10s) . . . . . $+300^oC$
(PLCC - Lead Tips Only)

Die Characteristics

Gate Count . . . . . 50 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = +5.0V ±10%,
T_A = 0^oC to $+70^oC$ (C82C84A),
T_A = -40^oC to $+85^oC$ (I82C84A),
T_A = -55^oC to $+125^oC$ (M82C84A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0 2.2	-	V V	C82C84A, I82C84 M82C84A, Notes 1, 2
V_{IL}	Logical Zero Input Voltage	-	0.8	V	Notes 1, 2, 3
V_{IHR}	Reset Input High Voltage	V_{CC} -0.8	-	V	
V_{ILR}	Reset Input Low Voltage	-	0.5	V	
VT+ - VT-	Reset Input Hysteresis	0.2 V_{CC}	-	-	
V_{OH}	Logical One Output Current	V_{CC} -0.4	-	V	I_{OH} = -4.0mA for CLK Output I_{OH} = -2.5mA for All Others
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} = +4.0mA for CLK Output I_{OL} = +2.5mA for All Others
II	Input Leakage Current	-1.0	1.0	µA	V_{IN} = V_{CC} or GND except $\overline{ASYNC}$, X1: (Note 4)
I_{CCOP}	Operating Power Supply Current	-	40	mA	Crystal Frequency = 25MHz Outputs Open, Note 5

NOTES:

1. F/$\overline{C}$ is a strap option and should be held either ≤ 0.8V or ≥ 2.2V. Does not apply to X1 or X2 pins.
2. Due to test equipment limitations related to noise, the actual tested value may differ from that specified, but the specified limit is guaranteed.
3. $\overline{CSYNC}$ pin is tested with V_{IL} ≤ 0.8V.
4. $\overline{ASYNC}$ pin includes an internal 17.5kΩ nominal pull-up resistor. For $\overline{ASYNC}$ input at GND, $\overline{ASYNC}$ input leakage current = 300µA nominal, X1 - crystal feedback input.
5. f = 25MHz may be tested using the extrapolated value based on measurements taken at f = 2MHz and f = 10MHz.

Capacitance

T_A = $+25^oC$

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	10	pF	FREQ = 1MHz, all measurements are referenced to device GND
C_{OUT}	Output Capacitance	15	pF	

AC Electrical Specifications

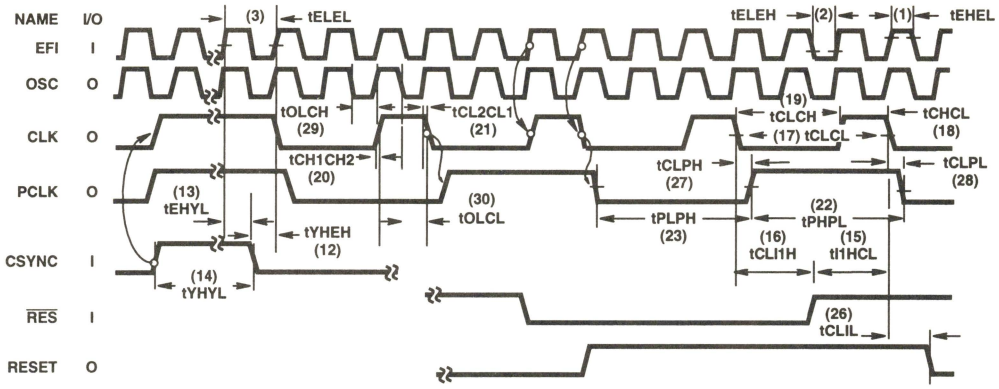
V_{CC} = +5V± 10%,
T_A = 0°C to +70°C (C82C84A),
T_A = -40°C to +85°C (I82C84A),
T_A = -55°C to +125°C (M82C84A)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	(NOTE 1) TEST CONDITIONS
TIMING REQUIREMENTS					
(1) TEHEL	External Frequency HIGH Time	13	-	ns	90%-90% V_{IN}
(2) TELEH	External Frequency LOW Time	13	-	ns	10%-10% V_{IN}
(3) TELEL	EFI Period	36	-	ns	
	XTAL Frequency	2.4	25	MHz	Note 2
(4) TR2VCL	RDY1, RDY2 Active Setup to CLK	35	-	ns	ASYNC = HIGH
(5) TR1VCH	RDY1, RDY2 Active Setup to CLK	35	-	ns	ASYNC = LOW
(6) TR1VCL	RDY1, RDY2 Inactive Setup to CLK	35	-	ns	
(7) TCLR1X	RDY1, RDY2 Hold to CLK	0	-	ns	
(8) TAYVCL	$\overline{\text{ASYNC}}$ Setup to CLK	50	-	ns	
(9) TCLAYX	$\overline{\text{ASYNC}}$ Hold to CLK	0	-	ns	
(10) TA1VR1V	$\overline{\text{AEN1}}$, $\overline{\text{AEN2}}$ Setup to RDY1, RDY2	15	-	ns	
(11) TCLA1X	$\overline{\text{AEN1}}$, $\overline{\text{AEN2}}$ Hold to CLK	0	-	ns	
(12) TYHEH	CSYNC Setup to EFI	20	-	ns	
(13) TEHYL	CSYNC Hold to EFI	20	-	ns	
(14) TYHYL	CSYNC Width	2 TELEL	-	ns	
(15) TI1HCL	$\overline{\text{RES}}$ Setup to CLK	65	-	ns	Note 3
(16) TCLI1H	$\overline{\text{RES}}$ Hold to CLK	20	-	ns	Note 3
TIMING RESPONSES					
(17) TCLCL	CLK Cycle Period	125	-	ns	Note 6
(18) TCHCL	CLK HIGH Time	(1/3 TCLCL) +2.0	-	ns	Note 6
(19) TCLCH	CLK LOW Time	(2/3 TCLCL) -15.0	-	ns	Note 6
(20) TCH1CH2 (21) TCL2CL1	CLK Rise or Fall Time	-	10	ns	1.0V to 3.0V
(22) TPHPL	PCLK HIGH Time	TCLCL-20	-	ns	Note 6
(23) TPLPH	PCLK LOW Time	TCLCL-20	-	ns	Note 6
(24) TRYLCL	Ready Inactive to CLK (See Note 4)	-8	-	ns	Note 4
(25) TRYHCH	Ready Active to CLK (See Note 3)	(2/3 TCLCL) -15.0	-	ns	Note 5
(26) TCLIL	CLK to Reset Delay	-	40	ns	
(27) TCLPH	CLK to PCLK HIGH Delay	-	22	ns	
(28) TCLPL	CLK to PCLK LOW Delay	-	22	ns	
(29) TOLCH	OSC to CLK HIGH Delay	-5	22	ns	
(30) TOLCL	OSC to CLK LOW Delay	2	35	ns	

NOTES:

1. Tested as follows: f = 2.4MHz, V_{IH} = 2.6V, V_{IL} = 0.4V, C_L = 50pF, $V_{OH} \geq$ 1.5V, $V_{OL} \leq$ 1.5V, unless otherwise specified. $\overline{\text{RES}}$ and F/$\overline{\text{C}}$ must switch between 0.4V and V_{CC} -0.4V. Input rise and fall times driven at 1ns/V. $V_{IL} \leq V_{IL}$ (max) - 0.4V for CSYNC pin. V_{CC} = 4.5V and 5.5V.
2. Tested using EFI or X1 input pin.
3. Setup and hold necessary only to guarantee recognition at next clock.
4. Applies only to T2 states.
5. Applies only to T3 TW states.
6. Tested with EFI input frequency = 4.2MHz.

Timing Waveforms



NOTE: All timing measurements are made at 1.5V, unless otherwise noted.

FIGURE 2. WAVEFORMS FOR CLOCKS AND RESETS SIGNALS

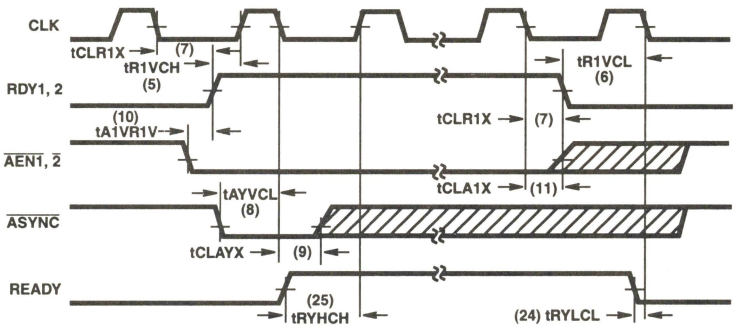


FIGURE 3. WAVEFORMS FOR READY SIGNALS (FOR ASYNCHRONOUS DEVICES)

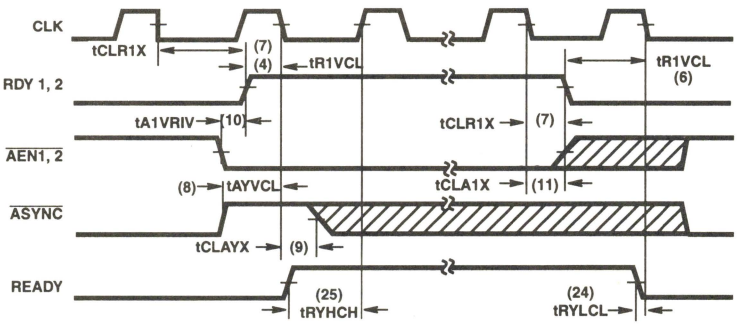
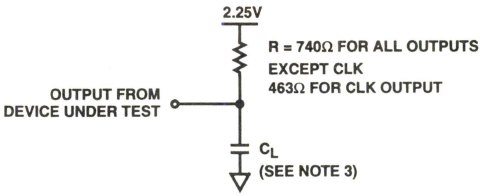


FIGURE 4. WAVEFORMS FOR READY SIGNALS (FOR SYNCHRONOUS DEVICES)

Test Load Circuits



NOTES:

1. C_L =100pF for CLK output.
2. C_L = 50pF for all outputs except CLK.
3. C_L = Includes probe and jig capacitance.

FIGURE 5. TEST LOAD MEASUREMENT CONDITIONS

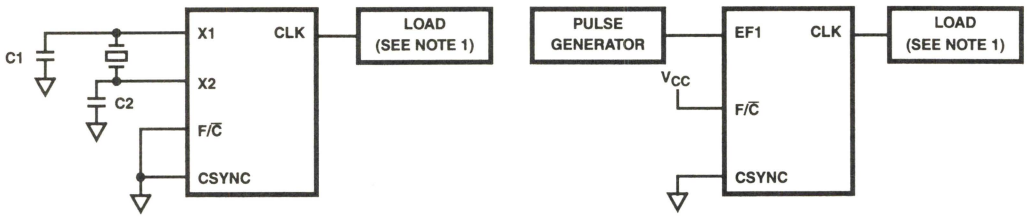


FIGURE 6. TCHCL, TCLCH LOAD CIRCUITS

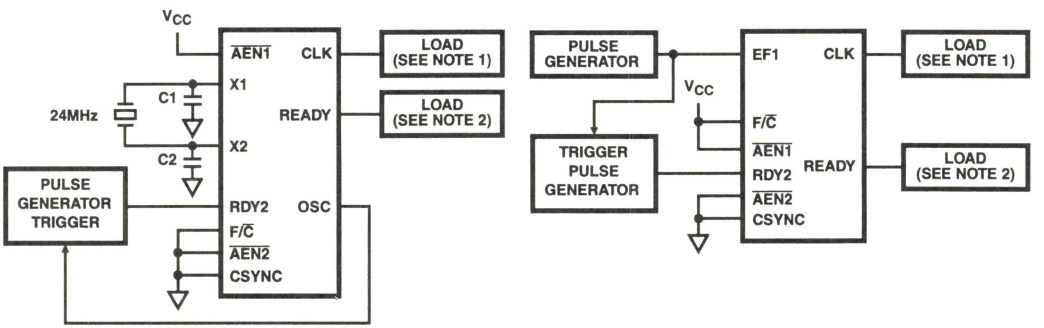
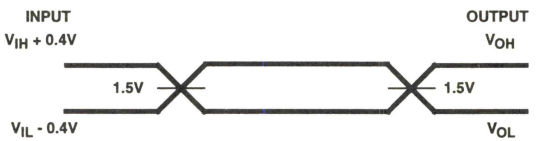


FIGURE 7. TRYLCL, TRYHCH LOAD CIRCUITS

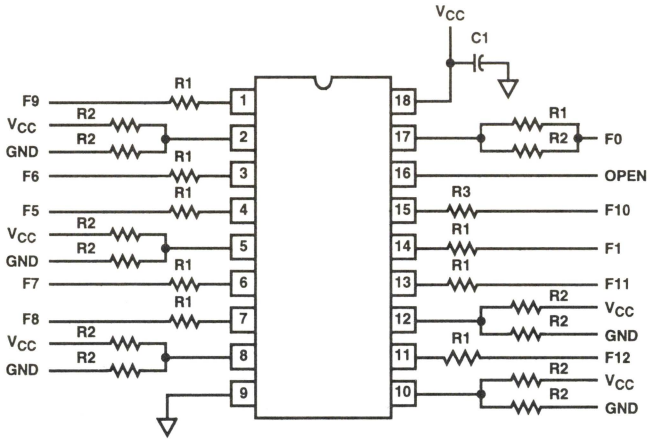
AC Testing Input, Output Waveform



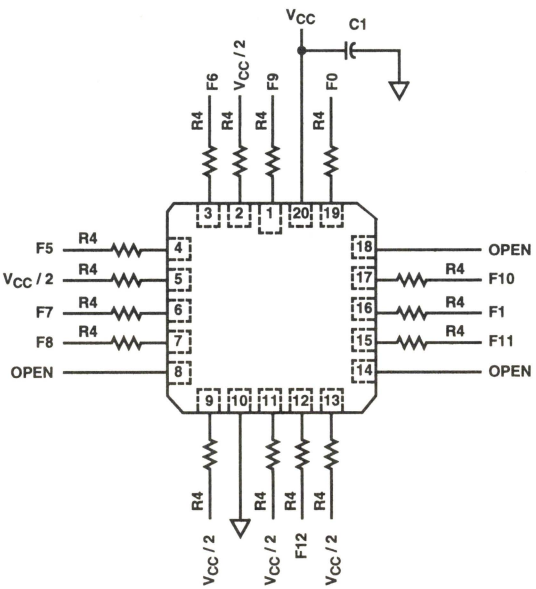
NOTE: Input test signals must switch between V_{IL} (maximum) -0.4V and V_{IH} (minimum) +0.4V. $\overline{RES}$ and F/$\overline{C}$ must switch between 0.4V and V_{CC} -0.4V. Input rise and fall times driven at 1ns/V. $V_{IL} \leq V_{IL}$ (max) -0.4V for CSYNC pin. V_{CC} -4.5V and 5.5V.

Burn-In Circuits

MD82C84A CERDIP



MR82C84A CLCC



NOTES:

V_{CC} = 5.5V ±0.5V, GND = 0V.
V_{IH} = 4.5V ±10%.
V_{IL} = -0.2 to 0.4V.
R1 = 47kΩ, ±5%.
R2 = 10kΩ, ±5%.
R3 = 2.2kΩ, ±5%.
R4 = 1.2kΩ, ±5%.
C1 = 0.01µF (minimum).
F0 = 100kHz ±10%.
F1 = F0/2, F2 = F1/2, . . . F12 = F11/2.

Die Characteristics

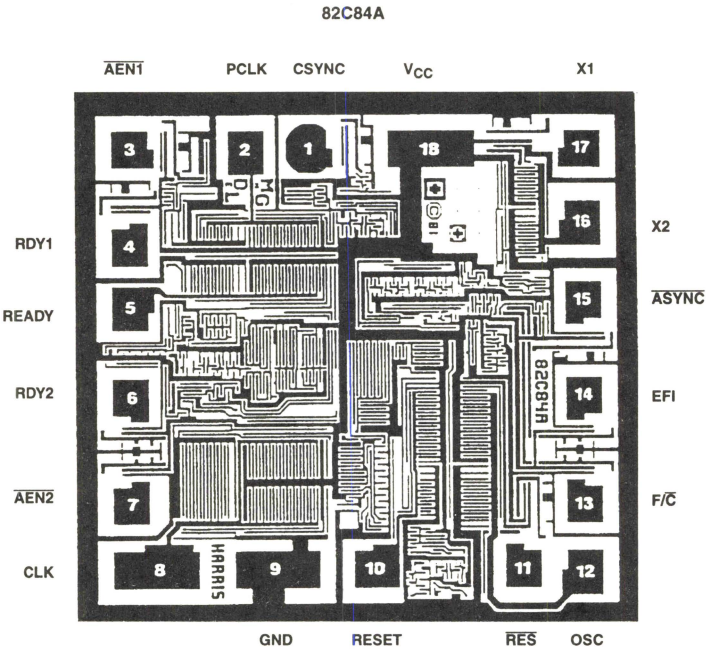
DIE DIMENSIONS:
66.1 x 70.5 x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
1.42×10^5 A/cm^2

Metallization Mask Layout



March 1997

CMOS Static Clock Controller/Generator

Features

- **Generates the System Clock For CMOS or NMOS Microprocessors and Peripherals**
- **Complete Control Over System Operation for Very Low System Power**
  - **Stop-Oscillator**
  - **Low Frequency**
  - **Stop-Clock**
  - **Full Speed Operation**
- **DC to 25MHz Operation (DC to 8MHz System Clock)**
- **Generates 50% and 33% Duty Cycle Clocks (Synchronized)**
- **Uses a Parallel Mode Crystal Circuit or External Frequency Source**
- **TTL Compatible Inputs/Outputs**
- **24 Lead Slimline Dual-In-Line or 28 Pad Square LCC Package Options**
- **Single 5V Power Supply**
- **Operating Temperature Range**
  - **C82C85 . . . . . .0°C to +70°C**
  - **I82C85 . . . . . -40°C to +85°C**
  - **M82C85 . . . . . -55°C to +125°C**

Ordering Information

PART NUMBER	PACKAGE	TEMP. RANGE	PKG. NO.
CS82C85	28 Ld PLCC	0°C to +70°C	N28.45
IS82C85		-40°C to +85°C	N28.45
CD82C85	24 Ld CERDIP	0°C to +70°C	F24.3
ID82C85		-40°C to +85°C	F24.3
MD82C85/B		-55°C to +125°C	F24.3
MR82C85/B	28 Pad CLCC	-55°C to +125°C	J28.A

Description

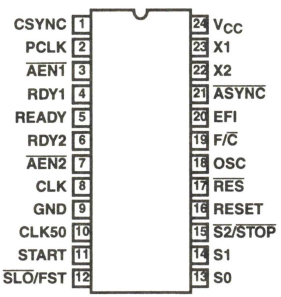
The Harris 82C85 Static CMOS Clock Controller/Generator provides complete control of static CMOS system operating modes and supports full speed, slow, stop-clock and stop-oscillator operation. While directly compatible with the Harris 80C86 and 80C88 16-bit Static CMOS Microprocessor Family, the 82C85 can also be used for general system clock control.

For static system designs, separate signals are provided on the 82C85 for stop (S0, S1, $\overline{S2}$/STOP) and start (START) control of the crystal oscillator and system clocks. A single control line ($\overline{SLO}$/FST) determines 82C85 fast (crystal/EFI frequency divided by 3) or slow (crystal/EFI frequency divided by 768) mode operation. Automatic maximum mode 80C86 and 80C88 software HALT instruction decode logic in the 82C85 enables software-based clock control. Restart logic insures valid clock start-up and complete synchronization of system clocks.

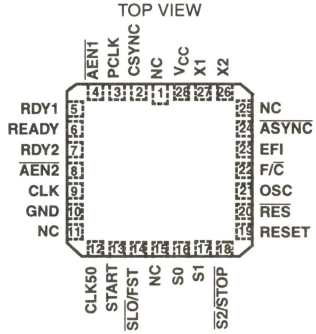
The 82C85 is manufactured using the Harris advanced Scaled SAJI IV CMOS process. In addition to clock control circuitry, the 82C85 also contains a crystal controlled oscillator (up to 25MHz), clock generation logic, complete "Ready" synchronization and reset logic. This permits the designer to tailor the system power-performance product to provide optimum performance at low power levels.

Pinouts

24 LEAD CERDIP
TOP VIEW



28 LEAD PLCC, CLCC
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

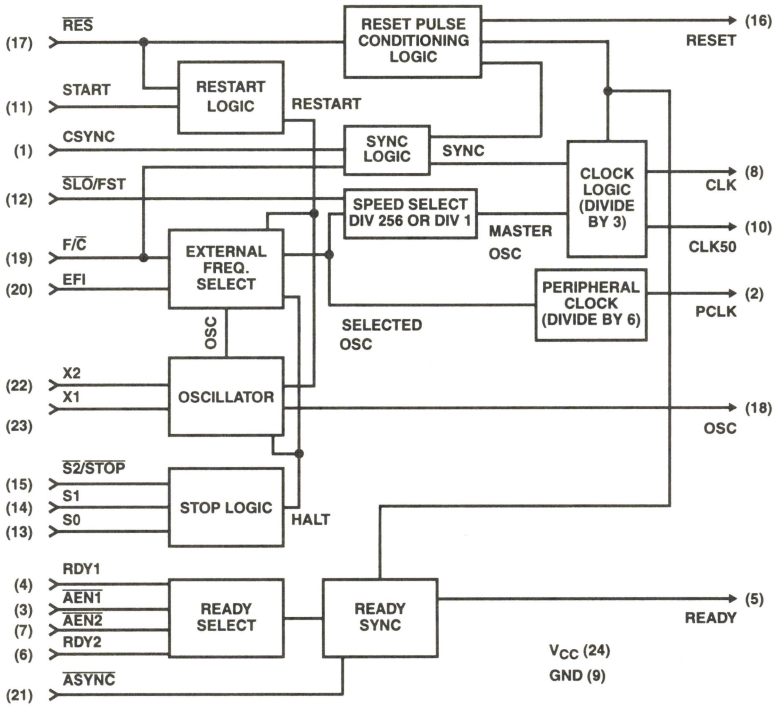
Pin Descriptions

SYMBOL	DIP PIN NUMBER	TYPE	DESCRIPTION
X1 X2	23 22	I O	CRYSTAL CONNECTIONS: X1 and X2 are the crystal oscillator connections. The crystal frequency must be 3 times the maximum desired processor clock frequency. X1 is the oscillator circuit input and X2 is the output of the oscillator circuit. If the crystal inputs are not used, X1 must be tied to V_{CC} or GND, and X2 should be left open.
EFI	20	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is HIGH, CLK is generated from the EFI input signal. This input signal should be a square wave with a frequency of three times the maximum desired CLK output frequency. If the crystal inputs are not used. XI must be tied to V_{CC} or GND, and X2 should be left open.
F/$\overline{C}$	19	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{C}$ selects either the crystal oscillator or the EFI input as the main frequency source. When F/$\overline{C}$ is LOW, the 82C85 clocks are derived from the crystal oscillator circuit. When F/$\overline{C}$ is HIGH, CLK is generated from the EFI input. F/$\overline{C}$ cannot be dynamically switched during normal operation.
START	11	I	A low-to-high transition on START will restart the CLK, CLK50 and PCLK outputs after the appropriate restart sequence is completed. When in the crystal mode (F/$\overline{C}$ LOW) with the oscillator stopped. The oscillator will be restarted when a Start command is received. The CLK, CLK50 and PCLK outputs will start after the oscillator input signal (X1) reaches the Schmitt trigger input threshold and 8K internal counter reaches terminal count. If F/$\overline{C}$ is HIGH (EFI mode), CLK, CLK50 and PCLK will restart within 3 EFI cycles after START is recognized. The 82C85 will restart in the same mode ($\overline{SLO}$/FST) in which it stopped. A high level on START disables the STOP mode.
SO S1 $\overline{S2}$/$\overline{STOP}$	13 14 15	I I I	$\overline{S2}$/$\overline{STOP}$, S1, SO are used to stop the 82C85 clock outputs (CLK, CLK50, PCLK) and are sampled by the rising edge of CLK, CLK50 and PCLK are stopped by $\overline{S2}$/$\overline{STOP}$, S1, SO being in the LHH state on the low-to-high transition of CLK. This LHH state must follow a passive HHH state occurring on the previous low-to-high CLK transition. CLK and CLK50 stop in the high state when F/$\overline{C}$ is low and may stop in either the high or low state when F/$\overline{C}$ is high. PCLK stops in its current state (high or low). When in the crystal mode (F/$\overline{C}$) low and a STOP command is issued, the 82C85 oscillator will stop along with the CLK, CLK50 and PCLK outputs. When in the EFI mode, only the CLK, CLK50 and PCLK outputs will be halted. The oscillator circuit if operational, will continue to run. The oscillator and/or clock is restarted by the START input signal going true (HIGH) or the reset input ($\overline{RES}$) going low.
$\overline{SLO}$/FST	12	I	$\overline{SLO}$/FST is a level-triggered input. When HIGH, the CLK and CLK50 outputs run at the maximum frequency (crystal or EFI frequency divided by 3). When LOW, CLK and CLK50 frequencies are equal to the crystal or EFI frequency divided by 768. $\overline{SLO}$/FST changes are internally synchronized so proper CLK and CLK50 phase relationships are maintained and minimum pulse width specifications are met. START and STOP control of the oscillator or EFI is available in either the SLOW or FAST frequency modes. The $\overline{SLO}$/FST input must be held LOW for at least 195 OSC/EFI clock cycles before it will be recognized. This eliminates unwanted frequency changes which could be caused by glitches or noise transients. The $\overline{SLO}$/FST input must be held HIGH for at least 6 OSC/EFI clock pulses to guarantee a transition to FAST mode operation.
CLK	8	O	PROCESSOR CLOCK: CLK is the clock output used by the 80C86 or 80C88 processor and other peripheral devices. When $\overline{SLO}$/FST is high, CLK has an output frequency which is equal to the crystal or EFI input frequency divided by three. When $\overline{SLO}$/FST is low, CLK has an output frequency which is equal to the crystal or EFI input frequency divided by 768. CLK has a 33% duty cycle.
CLK50	10	O	50% DUTY CYCLE CLOCK: CLK50 is an auxiliary clock with a 50% duty cycle and is synchronized to the falling edge of CLK. When $\overline{SLO}$/FST is high, CLK50 has an output frequency which is equal to the crystal or EFI input frequency divided by 3. When $\overline{SLO}$/FST is low, CLK50 has an output frequency equal to the crystal or EFI input frequency divided by 768.
PCLK	2	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is equal to the crystal or EFI input frequency divided by 6 and has a 50% duty cycle. PCLK frequency is unaffected by the state of the $\overline{SLO}$/FST input.
OSC	18	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal oscillator circuit. OSC is unaffected by the state of the $\overline{SLO}$/FST input. When the 82C85 is in the crystal mode (F/$\overline{C}$ low) and a STOP command is issued, the OSC output will stop in the HIGH state. When the 82C85 is in the EFI mode (F/$\overline{C}$ HIGH, the oscillator (if operational) will continue to run when a STOP command is issued and OSC remains active.

Pin Descriptions (Continued)

SYMBOL	DIP PIN NUMBER	TYPE	DESCRIPTION
$\overline{RES}$	17	I	RESET IN: $\overline{RES}$ is an active LOW signal which is used to generate RESET. The 82C85 provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration. $\overline{RES}$ starts crystal oscillator operation.
RESET	16	O	RESET: RESET is an active HIGH signal which is used to reset the 80C86 family processors. Its timing characteristics are determined by $\overline{RES}$. RESET is guaranteed to be HIGH for a minimum of 16 CLK pulses after the rising edge of $\overline{RES}$.
CSYNC	1	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple 82C85 and 82C84A to be synchronized to provide multiple in-phase clock signals When CSYNC is HIGH, the internal counters are reset and force CLK, CLK50 and PCLK into a HIGH state. When CSYNC is LOW, the internal counters are allowed to count and the CLK, CLK50 and PCLK outputs are active. CSYNC must be externally synchronized to EFI.
$\overline{AEN1}$ $\overline{AEN2}$	3 7	I I	ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two $\overline{AEN}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Buses.
RDY1 RDY2	4 6	I I	BUS READY: (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{ASYNC}$	21	I	READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is LOW, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH a single stage of READY synchronization is provided.
READY	5	O	READY: READY is an active HIGH signal which is the synchronized RDY signal input.
GND	9	I	Ground
V_{CC}	24	I	V_{CC}: is the +5V power supply pin. A 0.1mF capacitor between V_{CC} and GND is recommended.

Functional Block Diagram



Functional Description

The 82C85 Static Clock Controller/Generator provides simple and complete control static CMOS system operating modes. The 82C85 supports full speed, slow, stop-clock and stop-oscillator operation. While it is directly compatible with the Harris 80C86 and 80C88 CMOS 16-bit static microprocessors, the 82C85 can also be used for general purpose system clock control.

The 82C85 pinout is a superset of the 82C84A Clock Generator/Driver. 82C85 pins 1-9, 16-24 are compatible with 82C84A pins 1-9, 10-18 respectively. An 82C84A can be placed in the upper 18 pins of an 82C85 socket and it will operate correctly (without the ability to control the clock and oscillator operation.) This allows dual design for simple system upgrades. The 82C85 will also emulate an 82C84A when pins 11-15 on the 82C85 are tied to V_{CC}.

For static systems designs, separate signals are provided on the 82C85 for stop and start control of the crystal oscillator and clock outputs. A single control line determines 82C85 fast (crystal/EFI frequency divided by 3) or slow (crystal/EFI frequency divided by 768) mode operation. The 82C85 also contains a crystal controlled oscillator, clock generation logic, complete "Ready" synchronization and reset logic.

Automatic 80C86/88 software HALT instruction decode logic is present to ease the design of software-based clock control systems and provide complete software control of STOP mode operation. Restart logic insures valid clock start-up and complete synchronization of CLK, CLK50 and PCLK.

Static Operating Modes

In static CMOS system design, there are four basic operating modes. The 82C85 Static Clock Controller supports each of them. These modes are: FAST, SLOW, STOP-CLOCK and STOP-OSCILLATOR. Each has distinct power and performance characteristics which can be matched to the needs of a particular system at a specific time (See Table 1).

Keep in mind that a single system may require all of these operating modes at one time or another during normal operation. A design need not be limited to a single operating mode or a specific combination of modes. The appropriate operating mode can be matched to the power-performance level needed at a specific time or in a particular circumstance.

Reset Logic

The 82C85 reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 82C85.

When in the crystal oscillator (F/$\overline{C}$ = LOW) or the EFI (F/$\overline{C}$ = HIGH) mode, a LOW state on the RES input will set the RESET output to the HIGH state. It will also restart the oscillator circuit if it is in the idle state. The RESET output is guaranteed to stay in the HIGH state for a minimum of 16 CLK cycles after a low-to-high transition of the $\overline{RES}$ input.

An oscillator restart count sequence will not be disturbed by RESET if this count is already in progress. After the restart counter expires, the RESET output will stay HIGH at least for 16 periods of CLK before going LOW. RESET can be kept high beyond this time by a continuing low input on the $\overline{RES}$ input.

If F/$\overline{C}$ is low (crystal oscillator mode), a low state on $\overline{RES}$ starts the crystal oscillator circuit. The stopped outputs remain inactive, until the oscillator signal amplitude reaches the X1 Schmitt trigger input threshold voltage and 8192 cycles of the crystal oscillator output are counted by an internal counter. After this count is complete, the stopped outputs (CLK, CLK50, PCLK, and OSC) start cleanly with the proper phase relationships.

This 8192 count requirement insures that the CLK, CLK50 and PCLK outputs will meet minimum clock requirements and will not be affected by unstable oscillator characteristics which may exist during the oscillator start-up sequence. This sequence is also followed when a START command is issued while the 82C85 oscillator is stopped.

Oscillator/Clock Start Control

Once the oscillator is stopped (or committed to stop) or at power-on, the restart sequence is initiated by a HIGH state on START or LOW state on $\overline{RES}$. If F/$\overline{C}$ is HIGH, then restart occurs immediately after the START or RES input is synchronized internally. This insures that stopped outputs (CLK, PCLK, OSC and CLK50) start cleanly with the proper phase relationship.

If F/$\overline{C}$ is low (crystal oscillator mode), a HIGH state on the START input or a low state on $\overline{RES}$ causes the crystal oscillator to be restarted. The stopped outputs remain stopped,

TABLE 1. STATIC SYSTEM OPERATING MODE CHARACTERISTICS

OPERATING MODE	DESCRIPTION	POWER LEVEL	PERFORMANCE
Stop-Oscillator	All system clocks and main clock oscillator are stopped	Maximum Savings	Slowest response due to oscillator restart time
Stop-Clock	System CPU and peripherals clocks stop but main clock oscillator continues to run at rated frequency	Reduced System Power	Fast restart-no oscillator restart time
Slow	System CPU clocks are slowed while peripheral clock and main clock oscillator run at rated frequency	Power Dissipation Slightly Higher Than Stop-Clock	Continuous operation at low frequency
Fast	All clocks and oscillators run at rated frequency	Highest Power	Fastest response

until the oscillator signal amplitude reaches the X1 Schmitt trigger input threshold voltage and 8192 cycles of the crystal oscillator output are counted by an internal counter. After this count is complete, the stopped outputs (CLK, CLK50, PCLK, and OSC) start cleanly with the proper phase relationships.

Typically, any input signal which meets the START input timing requirements can be used to start the 82C85. In many cases, this would be the INT output from an 82C59A CMOS Priority Interrupt Controller (See Figure 1). This output, which is active high, can be connected to both the 82C85 START pin and to the appropriate interrupt request input on the microprocessor.

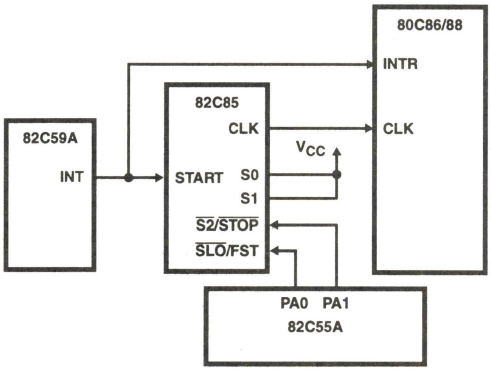


FIGURE 1. CMOS PERIPHERAL CONTROL OF 82C85 STOP, START AND SLOW/FAST OPERATIONS

When the INT output becomes active, the oscillator/clock circuit on the 82C85 will restart. Upon completion of the appropriate restart sequence, the CLK signal to the CPU will become active. The CPU can then respond to the still pending interrupt request.

If the 82C59A/82C85 restart combination is used in conjunction with an 82C55A $\overline{\text{STOP}}$ control, the 82C55A must be initialized prior to the 82C59A after reset. The 82C59A interrupt output is driven high at reset, causing the 82C85 to remain in the START mode regardless of the state of the $\overline{\text{S2}}/\overline{\text{STOP}}$ input. This will avoid stopping the 82C85 due to negative transitions on the $\overline{\text{S2}}/\overline{\text{STOP}}$ input which may occur during a mode change on the 82C55A or during the operation of any peripheral I/O device prior to initialization.

Another method of insuring proper operation of the START function upon reset or system initialization is to bias the $\overline{\text{S2}}/\overline{\text{STOP}}$ input low with an external pull-down resistor. The $\overline{\text{S2}}/\overline{\text{STOP}}$ input will remain low until driven high by the 82C55A port pin or by external logic. This insures that the 82C85 STOP command (HHH prior to LHH requirement on the status inputs) will not be satisfied. To minimize power dissipation in this case (using a pulldown resistor), the $\overline{\text{S2}}/\overline{\text{STOP}}$ input should be normally LOW and pulsed HIGH to develop the necessary HHH-to-LHH $\overline{\text{STOP}}$ sequence. In this manner, the output driving the $\overline{\text{S2}}/\overline{\text{STOP}}$ input will be normally LOW and will not be driving to the opposite state of the pull-down resistor.

Fast Mode

The most common operating mode for a system is the FAST mode. In this mode, the 82C85 operates at the maximum frequency determined by the main oscillator or EFI frequency.

TABLE 2. TYPICAL SYSTEM POWER SUPPLY CURRENT FOR STATIC CMOS OPERATING MODES

	FAST	SLOW	STOP-CLOCK	STOP-OSC
CPU Frequency	5MHz	20 KHz	DC	DC
XTAL Frequency	15MHz	15MHz	15MHz	DC
ICC				
82C85	24.7mA	16.9mA	14.1mA	24.4mA
80C88	23.8mA	173.0mA	106.6mA	106.6mA
82C82	1.7mA	6.5mA	1.0mA	1.0mA
82C86	1.4mA	14.0mA	1.0mA	1.0mA
82C88	3.5mA	14.3mA	3.8mA	3.8mA
82C52	151.2mA	72.0mA	1.0mA	1.0mA
82C54	943.0mA	915.0mA	3.5mA	1.0mA
82C55A	3.2mA	1.2mA	1.0mA	1.0mA
82C59A	580.0mA	520.0mA	1.0mA	1.0mA
74HCXX + other	2.9mA	10.0mA	90.0mA	90.0mA
HM-6516	820.0mA	32.0mA	1.9mA	1.9mA
HM-6616	6.3mA	52.5mA	12.0mA	12.0mA
Total	66.8mA	18.9mA	14.3mA	244.7mA

All measurements taken at room temperature, V_{CC} = +5.0V. Power supply current levels will be dependent upon system configuration and frequency of operation.

FAST mode operation is enabled by each of two conditions:

- The $\overline{SLO}$/FST input is HIGH and a START or reset command is issued
- The $\overline{SLO}$/FST input is held HIGH for at least 6 oscillator or EFI cycles.

Alternate Operating Modes

Using alternate modes of operation (slow, stop-clock, stop-oscillator) will reduce the average system operating power dissipation in a static CMOS system (See Table 2). This does not mean that system speed or throughput must be reduced. When used appropriately, the slow, stopclock, stop-oscillator modes can make your design more power efficient while maintaining maximum system performance.

Stop-Oscillator Mode

When the 82C85 is stopped while in the crystal mode (F/$\overline{C}$ LOW), the oscillator, in addition to all system clock signals (CLK, CLK50 and PCLK), are stopped. CLK and CLK50 stop in the high state. PCLK stops in it's current state (high or low).

With the oscillator stopped, 82C85 power drops to it's lowest level. All clocks and oscillators are stopped. All devices in the system which are driven by the 82C85 go into the lowest power standby mode. The 82C85 also goes into standby and requires a power supply current of less than 100μA.

Stop-Clock Mode

When the 82C85 is in the EFI mode (F/$\overline{C}$ HIGH) and a $\overline{STOP}$ command is issued, all system clock signals (CLK, CLK50, and PCLK) are stopped. CLK and CLK50 stop in the high state when F/$\overline{C}$ is low and may stop in either the high or low state when F/$\overline{C}$ is high. PCLK stops in its current state (high or low).

The 82C85 can also provide it's own EFI source simply by connecting the OSC output to the EFI input and pulling the F/C input HIGH. This puts the 82C85 into the External Frequency Mode using it's own oscillator as an external source signal (See Figure 2). In this configuration, when the 82C85 is stopped in the EFI mode, the oscillator continues to run. Only the clocks to the CPU and peripherals (CLK, CLK50 and PCLK) are stopped.

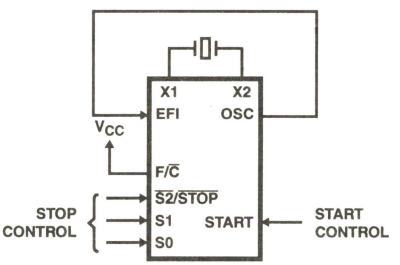


FIGURE 2. STOP-CLOCK MODE USING 82C85 IN EFI MODE WITH OSCILLATOR AS FREQUENCY SOURCE

Oscillator/Clock Stop Operation

Three control lines determine when the 82C85 clock outputs or oscillator will stop. These are S0, S1 and $\overline{S2}$/$\overline{STOP}$. These three lines are designed to connect directly to the MAXimum mode 80C86 and 80C88 status lines or to be driven by external I/O signals (such as an 82C55A output port).

In the MAXimum mode configuration, the 82C85 will automatically recognize a software HALT command from the 80C86 or 80C88 and stop the system clocks or oscillator. This allows complete software control of the $\overline{STOP}$ function.

If the 80C86 or 80C88 is used in the MINimum mode, the 82C85 can be controlled using the $\overline{S2}$/$\overline{STOP}$ input (with S0 and S1 held high). This can be done using an external I/O control line, such as from an 82C55A or by decoding the state of the 80C86 MINimum mode status signals.

82C85 status inputs $\overline{S2}$/$\overline{STOP}$, S1, S0 are sampled on the rising edge of CLK. The oscillator (F/$\overline{C}$ LOW only) and clock outputs are stopped by $\overline{S2}$/$\overline{STOP}$, S1, S0 being in the LHH state on a low-to-high transition of CLK. This LHH state must follow a passive HHH state occurring on the previous low-to-high CLK transition. CLK and CLK50 will stop in the logic HIGH state after two additional complete cycles of CLK. PCLK stops in it's current state (HIGH or LOW). This is true for both SLOW and FAST mode operation.

80C86/88 Maximum Mode Clock Control

The 82C85 $\overline{STOP}$ function has been optimized for 80C86/88 MAXimum mode operation. In this mode, the three 82C85 status inputs ($\overline{S2}$/$\overline{STOP}$, S1, S0) are connected directly to the MAXimum mode status lines (S2, S1, S0) of the Harris 80C86 or 80C88 static CMOS microprocessors (See Figure 3).

When in the MAXimum mode, the 80C86/88 status lines identify which type of bus cycle the CPU is starting to execute. 82C85 $\overline{S2}$/$\overline{STOP}$, S1 and S0 control input logic will recognize a valid MAXimum mode software HALT executed by the 80C86 or 80C88. Once this state has been recognized, the 82C85 stops the clock (F/$\overline{C}$ HIGH) and oscillator (F/$\overline{C}$ LOW) operation.

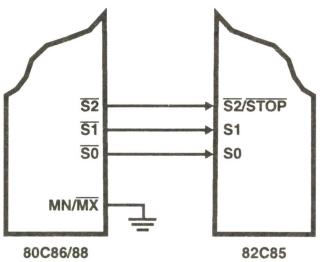


FIGURE 3. 82C85 STOP CONTROL USING 80C86/88 MAXIMUM MODE STATUS LINES

The 82C85 $\overline{S2}/\overline{STOP}$, S1 and S0 control lines were designed to detect a passive 111 state followed by a HALT 011 logic state before recognizing the HALT instruction and stopping the system clocks. In the MAXimum mode, the 80C86/88 status lines go into a passive (no bus cycle) logic 111 state prior to executing a HALT instruction. The qualification of a passive no bus cycle logic 111 state insures that random transitions of the status lines into a logic 011 state will not stop the system clock. This is necessary since the status lines of the 80C86/88 transition through an unknown state during T3 of the bus cycle.

Once the HALT instruction is decoded by the 82C85, either the oscillator is stopped (STOP-OSCILLATOR mode F/$\overline{C}$ tied low) or the external frequency source is gated off internally (STOP-CLOCK mode F/$\overline{C}$ HIGH). When the HALT instruction is decoded with F/$\overline{C}$ low, the CLK and CLK50 will be stopped in a logic high state after 2 additional cycles of the clock. PCLK stops in it's current state (high or low). This is true for both SLOW and FAST mode operation. The HALT instruction is detected in the same manner whether the 82C85 is in the SLOW or FAST mode.

Independent Stop Control for Minimum Mode Operation

When the 80C86 and 80C88 microprocessors are configured in MINimum Mode (MN/$\overline{MX}$ pin tied high), their status lines S0, S1, and S2 assume alternate functions. The logic states and sequences (passive before a HALT) necessary for automatic HALT detect in the 82C85 do not occur as in the MAXimum mode. The 82C85 controller cannot use the microprocessor status lines to detect a software Halt instruction when operating in MINimum mode.

However, the negative edge-activated $\overline{S2}/\overline{STOP}$ pin provides a simple means for clock control in MINimum mode 80C86 and 80C88 systems. $\overline{S2}/\overline{STOP}$ can be used as an independent $\overline{STOP}$ control when S1 and S0 are held in the logical HIGH state. Keeping the S0 and S1 inputs at a logic 1 level and transitioning $\overline{S2}/\overline{STOP}$ from high to low will meet the passive 111 state prior to a 011 state requirement of the 82C85. This feature allows 82C85 operation with the 80C86 and 80C88 in the MINimum mode, provides compatibility with other static CMOS microprocessors and allows maximum flexibility in a system.

With S2/$\overline{STOP}$ being used as a stand-alone STOP command line, system clocks can be controlled via an 82C55A programmable peripheral interface or other similar interface circuits. This is accomplished by driving the $\overline{S2}/\overline{STOP}$ input with a PORT pin on the 82C55A (See Figure 1). The 82C55A port pin should be configured as an output and must present a logic HIGH to the $\overline{S2}/\overline{STOP}$ input for at least one CLK cycle, followed by a LOW state. This will meet the 82C85 status input requirement of 111 followed by a 011.

When a logic 0 is written to a 82C55A port pin, the $\overline{S2}$/ $\overline{STOP}$ pin is pulled low, stopping the system clocks (CLK, CLK50, PCLK). In essence, the 82C85 is software controlled via the 82C55A. As with the $\overline{SLO}$/FST interface, PORT C is a logical choice for this job since the individual bit set and reset commands available for this port make control of the $\overline{S2}/\overline{STOP}$ input simple.

A START command issued to the 82C85 will override a $\overline{STOP}$ command and the 82C85 will begin normal operation. The low state of the negative-edge triggered $\overline{S2}/\overline{STOP}$ input will not prohibit the clocks from restarting. After a START or $\overline{RES}$ command, the 82C85 must see a passive (111) state followed by a HALT (011) state to stop the system clocks. To accomplish this, the 82C55A port output must be brought high and then returned low again for the 82C85 to recognize the next $\overline{STOP}$ command.

External Decode Adds Halt Control

SS0, IO/$\overline{M}$ and DT/$\overline{R}$ can identify a MINimum mode 80C88 HALT execution. During T2 of the system timing (while ALE is high), SS0, IO/$\overline{M}$, and DT/$\overline{R}$ go into a 111 state when the 80C88 is executing a software HALT. These signals cannot be tied directly to the $\overline{S2}/\overline{STOP}$, S1 and S0 inputs since they are not guaranteed to go into a passive state prior to their 111 state. These signals can be decoded during the time ALE is high to indicate a software HALT execution.

Slow Mode

When continuous operation is critical but power consumption remains a concern, the 82C85 SLOW mode operation provides a lower frequency at the CLK and CLK50 outputs (crystal/EFI frequency divided by 768). The frequency of PCLK is unaffected. The SLOW mode allows the CPU and the system to operate at a reduced rate which, in turn, reduces system power.

For example, the operating power for the 80C86 or 80C88 CPU is 10mA/MHz of clock frequency. When the SLOW mode is used in a typical 5MHz system, CLK and CLK50 run at approximately 20kHz. At this reduced frequency, the average operating current of the CPU drops to 200µA. Adding the 80C86/88 500µA standby current brings the total current to 700µA.

While the CPU and peripherals run slower and the 82C85 CLK and CLK50 outputs switch at a reduced frequency, the main 82C85 oscillator is still running at the maximum frequency (determined by the crystal or EFI input frequency.) Since CMOS power is directly related to operating frequency, 82C85 power supply current will typically be reduced by 15-20%.

Clock Slow/Fast Operation

The $\overline{SLO}$/FST input determines whether the CLK and CLK50 outputs run at full speed (crystal or EFI frequency divided by 3) or at slow speed (crystal or EFI frequency divided by 768) (See Figure 4). When in the SLOW mode, 82C85 stop-clock and stop-oscillator functions operate in the same manner as in the FAST mode.

Internal logic requires that the $\overline{SLO}$/FST pin be held low for at least 195 oscillator or EFI clock pulses before the SLOW mode command is recognized. This requirement eliminates unwanted FAST-to-SLOW mode frequency changes which could be caused by glitches or noise spikes.

To guarantee FAST mode recognition, the SLO/FST pin must be held high for at least 6 OSC or EFI pulses. The 82C85 will begin FAST mode operation on the next PCLK

edge after FAST command recognition. Proper CLK and CLK 50 phase relationships are maintained and minimum pulse width specifications are met.

FAST-to-SLOW or SLOW-to-FAST mode changes will occur on the next rising or falling edge of PCLK. It is important to remember that the transition time for operating frequency changes, which are dependent upon PCLK, will vary with the 82C85 oscillator or EFI frequency.

Slow Mode Control

The 82C55A programmable peripheral interface can be used to provide control of the $\overline{SLO}$/FST pin by connecting a port pin of the 82C55A directly to the $\overline{SLO}$/FST pin (See Figure 1). With the port pin configured as an output, software control of the $\overline{SLO}$/FST pin is provided by simply writing a logical one (FAST mode) or logical zero (SLOW Mode) to the corresponding port. PORT C is well-suited for this function due to it's bit set and reset capabilities. Since PCLK continues to run at a frequency equal to the oscillator or EFI frequency divided by 6, it can be used by other devices in the system which need a fixed high frequency clock. For example, PCLK could be used to clock an 82C54 programmable interval timer to produce a real-time clock for the system or as a baud rate generator to maintain serial data communications during SLOW mode operation.

Oscillator

The oscillator circuit of the 82C85 is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived. The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input connections. The output of the oscillator is buffered and available at the OSC output (pin 18) for generation of other system timing signals.

For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) are recommended. Capacitors C1 and C2 are chosen such that their combined capacitance matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

The crystal/capacitor configuration and the formula used to determine the capacitor values are shown in Figure 4. Crystal Specifications are shown in Table 3.

$$CT = \frac{C1 \bullet C2}{C1 + C2} \text{ (Including Stray Capacitance)} \qquad \text{(EQ. 1)}$$

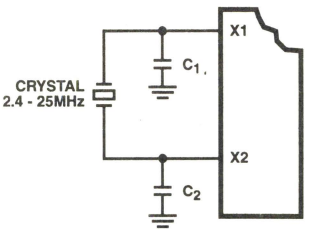


FIGURE 4. 82C85 CRYSTAL CONNECTION

TABLE 3. CRYSTAL SPECIFICATIONS

PARAMETER	TYPICAL CRYSTAL SPECIFICATION
Frequency	2.4 to 25MHz
Type of Operation	Parallel Resonant, Fund. Mode
Load Capacitance	20 or 32pF
RSERIES (Max)	35X (f = 25MHz, C_L = 32pF) 66X (f = 25MHz, C_L = 20pF)

Frequency Source Selection

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the source frequency for clock generation. If the EFI input is selected as the source, the oscillator section (OSC output) can be used independently for another clock source. If a crystal is not used, then crystal input X1 (pin 23) must be tied to V_{CC} or GND and X2 (pin 22) should be left open. If the EFI mode is not used, then EFI (pin 20) should be tied to V_{CC} or GND.

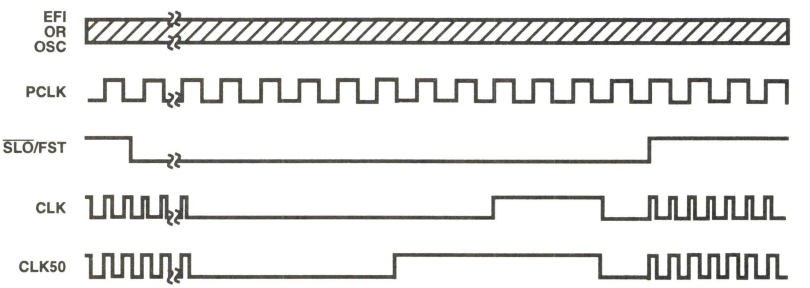


FIGURE 5. $\overline{SLO}$/FST TIMING OVERVIEW

Clock Generator

The clock generator consists of two synchronous divide-by-three counters with special clear inputs that inhibit the counting. One counter generates a 33% duty cycle waveform (CLK) and the other generates a 50% duty cycle waveform (CLK50). These two counters are negative-edge synchronized, with the low-going transitions of both waveforms occurring on the same oscillator transition. The CLK and CLK50 output frequencies are one-third of the base input frequency when $\overline{SLO}$/FST is high and are equal to the base input frequency divided by 768 when $\overline{SLO}$/FST is low.

The CLK output is a 33% duty cycle clock signal designed to drive the 80C86 and 80C88 microprocessors directly. CLK50 has a 50% duty cycle output synchronous with CLK, designed to drive co-processors and peripherals requiring a 50% duty cycle clock. When $\overline{SLO}$/FST is high, CLK and CLK50 have output frequencies which are 1/3 that of EFI/OSC. When $\overline{SLO}$/FST is low, CLK and CLK50 have output frequencies which are OSC (EFI) divided by 768.

PCLK is a peripheral clock signal with an output frequency equal to the oscillator or EFI frequency divided by 6. PCLK has a 50% duty cycle. PCLK is unaffected by $\overline{SLO}$/FST. When the 82C85 is placed in the $\overline{STOP}$ mode, PCLK will remain in it's current state (logic high or logic low) until a RESET or START command restarts the 82C85 clock circuitry. PCLK is negative-edge synchronized with CLK and CLK50.

Clock Synchronization

The clock synchronization (CSYNC) input allows the output clocks to be synchronized with an external event (such as another 82C85 or 82C84A clock signal). CSYNC going active causes all clocks (CLK, CLK50 and PCLK) to stop in the HIGH state.

It is necessary to synchronize the CSYNC input to the EFI clock external to the 82C85. This is accomplished with two flip-flops when synchronizing two 82C85s and with three flip-flops when synchronizing an 82C85 to an 82C84A (See Figure 6). Multiple external flip-flops are necessary to minimize the occurrence of metastable (or indeterminate) states.

Ready Synchronization

Two READY inputs (RDY1, RDY2) are provided to accommodate two system busses. Each READY input is qualified by ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY set up and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation. When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK (requiring a setup time TR1VCH) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go HIGH.

Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing (TR1VCL) on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time. $\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

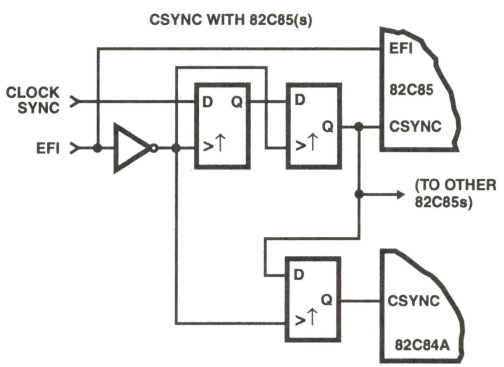


FIGURE 6. 82C85 AND 82C84A CSYNC SYNCHRONIZATION METHODS

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C85 . . . . . 0°C to +70°C
I82C85 . . . . . -40°C to +85°C
M82C85 . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	70	16
CCC Package	75	18
PLCC Package	65	N/A

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature Ceramic Package . . . . . +175°C
Maximum Junction Temperature Plastic Package . . . . . +150°C
(Soldering 10s)
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(PLCC - Lead Tips Only)

Die Characteristics

Gate Count . . . . . 500 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5.0V 10%; T_A = 0°C to +70°C (C82C85);
T_A = -40°C to +85°C (I82C85);
T_A = -55°C to +125°C (M82C85)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0 2.2	-	V V	C82C85, I82C85 M82C85
V_{IHR}	Reset Input High Voltage	2.8	-	V	
V_{IL}	Logical Zero Input Voltage	-	0.8	V	Note 1
$V_{T+} - V_T$	Reset Input Hysteresis	0.25	-	V	
V_{OH}	Logical One Output Voltage	V_{CC}-0.4	-	V	I_{OH} = -5.0 mA (CLK, CLK50) I_{OH} = -1.0mA (X2) I_{OH} = -2.5mA (all other outputs)
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} = +2.5mA (X2) I_{OL} = +5.0mA (all other outputs)
II	Input Leakage Current	-1.0	1.0	µA	V_{IN} = V_{CC} or GND, except DIP Pins 11 - 15, 21, 23
IBHH	Bus-hold High Leakage Current	-10	-200	µA	V_{IN} = 3.0V; Pins 11 - 15, 21
ICCSB	Standby Power Supply Current	-	100	µA	82C85 in HALT state with oscillator stopped
ICCOP	Operating Power Supply Current	-	50	mA	Crystal Frequency = 15MHz, outputs open, inputs = GND or V_{CC}
		-	70	mA	Crystal Frequency = 25MHz, outputs open, inputs = GND or V_{CC}
ICCSLOW	Slow Mode Operating Current	-	40	mA Crystal Freq = 15MHz	Outputs Open; $\overline{SLO}$/FST = GND, START = V_{CC}, Other inputs - V_{IN} = V_{CC} or GND
		-	60	mA Crystal Freq = 25MHz	

NOTE:

1. For CSYNC, V_{IL} = GND

Capacitance

T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	15	pF	FREQ = 1MHz, all measurements are referenced to device GND
C_{OUT}	Output Capacitance	20	pF	

AC Electrical Specifications

V_{CC} = 5V ±10%; T_A = 0°C to +70°C (C82C85);
T_A = -40°C to +85°C (I82C85);
T_A = -55°C to +125°C (M82C85)

SYMBOL	PARAMETER	LIMITS		UNITS	CONDITIONS
		MIN	MAX		
TIMING REQUIREMENTS					
(1) TEHEL	External Frequency HIGH Time	15	-	ns	90%-90% V_{IN}, Note 1, f = 25MHz
(2) TELEH	External Frequency LOW Time	15	-	ns	10%-10% V_{IN}, Note 1, f = 25MHz
(3) TELEL	EFI or Crystal Period	40	-	ns	Note 1
(4) TEFIDC	External Frequency Input Duty Cycle	45	55	%	f = 25MHz, Note 1
(5) Fx	Crystal Frequency	2.4	25	MHz	Note 1
(6) TR1VCL	RDY1, RDY2 Active Setup to CLK	35	-	ns	$\overline{\text{ASYNC}}$ = HIGH
(7) TR1VCH	RDY1, RDY2 Active Setup to CLK	35	-	ns	$\overline{\text{ASYNC}}$ = LOW
(8) TR1VCL	RDY1, RDY2 Inactive Setup to CLK	35	-	ns	
(9) TCLR1X	RDY1, RDY2 Hold to CLK	0	-	ns	
(10) TAYVCL	$\overline{\text{ASYNC}}$ Setup to CLK	50	-	ns	
(11) TCLAYX	$\overline{\text{ASYNC}}$ Hold to CLK	0	-	ns	
(12) TA1VR1V	$\overline{\text{AEN1}}$, $\overline{\text{AEN2}}$ Setup to RDY1, RDY2	15	-	ns	
(13) TCLA1X	$\overline{\text{AEN1}}$, $\overline{\text{AEN2}}$ Hold to CLK	0	-	ns	
(14) TYHEH	CSYNC Setup to EFI	10	-	ns	
(15) TEHYL	CSYNC Hold to EFI	10	-	ns	
(16) TYHYL	CSYNC Pulse Width	2TELEL	-	ns	
(17) TI1HCL	$\overline{\text{RES}}$ Setup to CLK	65	-	ns	Note 2
(18) TSVCH	S0, S1, $\overline{\text{S2}}$/$\overline{\text{STOP}}$ Setup to CLK	35	-	ns	
(19) TCHSV	S0, S1, $\overline{\text{S2}}$/$\overline{\text{STOP}}$ Hold to CLK	35	-	ns	
(20) TRSVCH	$\overline{\text{RES}}$, START Setup to CLK	65	-	ns	Note 2
(21) TSHSL	$\overline{\text{RES}}$ (Low) or START (High) Pulse Width	TCLCLs3	-	ns	
(22) TSFPC	$\overline{\text{SLO}}$/FST Setup to PCLK	TEHEL + 100	-	ns	Note 2
(23) TSTART	$\overline{\text{RES}}$ or START Valid to CLK Low	2TELEL + 2	-	ns	
(24) TSTOP	$\overline{\text{STOP}}$ Command Valid to CLK High	2TCHCH + TRSVCH	3TCHCH + 34	ns	TCHCH = TCLCL
TIMING RESPONSES					
(25) TCLCL	CLK/CLK50 Cycle Period	125	-	ns	Note 1
(26) TCHCL	CLK HIGH Time	(1/3 TCLCL)+2	-	ns	

AC Electrical Specifications

V_{CC} = 5V ±10%; T_A = 0°C to +70°C (C82C85);
T_A = -40°C to +85°C (I82C85);
T_A = -55°C to +125°C (M82C85) **(Continued)**

SYMBOL	PARAMETER	LIMITS		UNITS	CONDITIONS
		MIN	MAX		
(27) TCLCH	CLK LOW Time	(2/3 TCLCL)-15	-	ns	
(28) T5CHCL	CLK50 HIGH Time	(1/2 TCLCL)-7.5	-	ns	
(29) T5CLCH	CLK50 LOW Time	(1/2 TCLCL)-7.5	-	ns	
(30) TCH1CH2	CLK/CLK50 Rise Time	-	8	ns	1.0V to 3.5V
(31) TCL2CL1	CLK/CLK50 Fall Time	-	8	ns	1.0V to 3.5V
(32) TPHPL	PCLK HIGH Time	TCLCL-20	-	ns	
(33) TPLPH	PCLK LOW Time	TCLCL-20	-	ns	
(34) TRYLCL	Ready Inactive to CLK	-8	-	ns	Note 4
(35) TRYHCH	Ready Active to CLK	2/3(TCLCL)-15	-	ns	Note 3
(36) TCLIL	CLK to Reset Delay	-	40	ns	
(37) TCLPH	CLK to PCLK HIGH Delay	-	22	ns	
(38) TCLPL	CLK to PCLK LOW Delay	-	22	ns	
(39) TOST	Start/Reset Valid to Clock LOW	-	2	ms	Typ. - Note 8
(40) TOLOH	Output Rise Time (except CLK)	-	15	ns	From 0.8V to 2.0V
(41) TOHOL	Output Fall Time (except CLK)	-	12	ns	From 2.0V to 0.8V
(42) TRST	RESET output HIGH Time	16 x TCLCL	-	ns	
(43) TCLC50L	CLK LOW to CLK50 LOW Skew	-	5	ns	

NOTES:

1. Slow and Fast Modes.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T3, TW states.
4. Applies only to T2 states.
5. All timing delays are measured at 1.5V unless otherwise noted.
6. Input signals must switch between V_{IL} max - 0.4 and V_{IH} min + 0.4 volts
7. Timing measurements made with EFI duty cycle = 50%.
8. Oscillator start up time depends on several factors including crystal frequency, crystal manufacturer, capacitive load, temperature, power supply voltage, etc. This parameter is given for information only.
9. Output signals switch between V_{OH} and V_{OL} unless otherwise specified.

Timing Waveforms

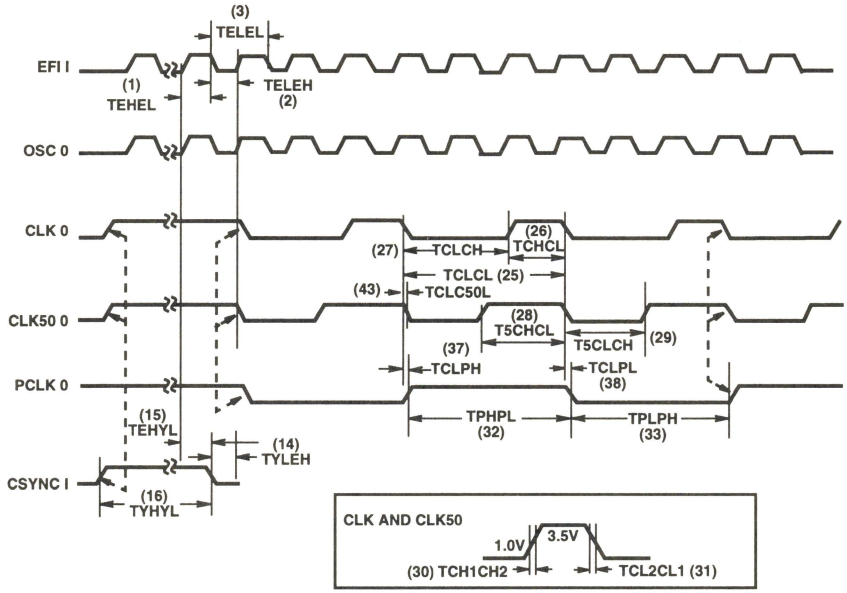


FIGURE 7. WAVEFORMS FOR CLOCKS

NOTE: All Timing Measurements are made at 1.5V, Unless Otherwise Noted.

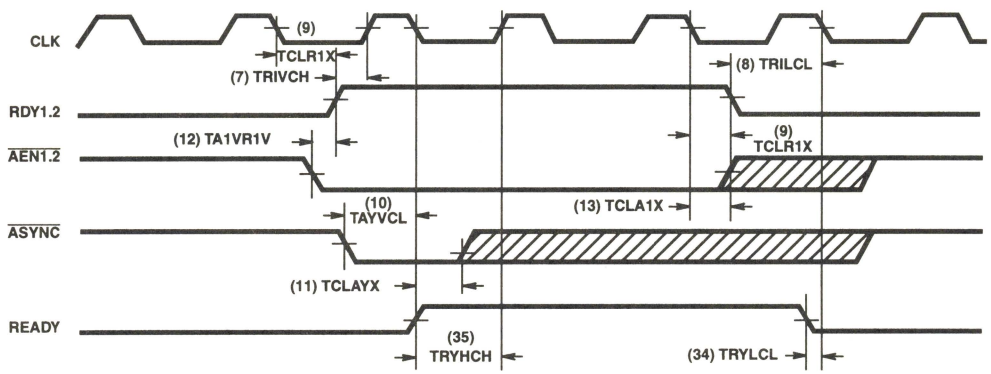


FIGURE 8. WAVEFORMS FOR READY SIGNALS (FOR ASYNCHRONOUS DEVICES)

Timing Waveforms (Continued)

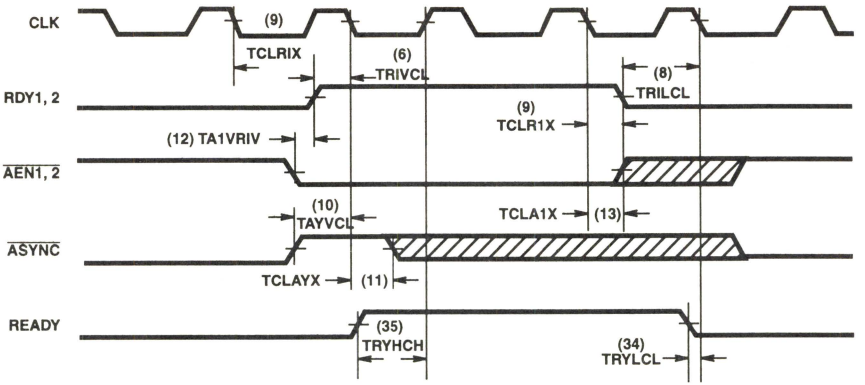


FIGURE 9. WAVEFORMS FOR READY SIGNALS (FOR SYNCHRONOUS DEVICES)

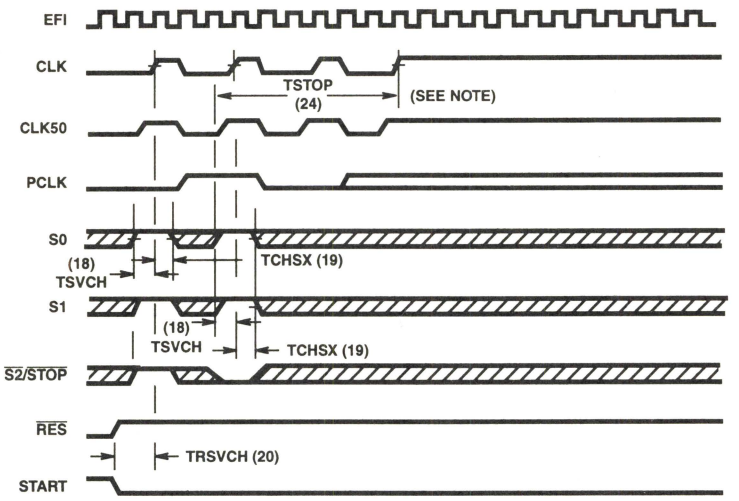


FIGURE 10. CLOCK STOP (F/$\overline{C}$ HIGH OR F/$\overline{C}$ LOW)

NOTE: When F/$\overline{C}$ is low, CLK and CLK50 stop high. When F/$\overline{C}$ is high, CLK and CLK50 may stop either high or low.

Timing Waveforms (Continued)

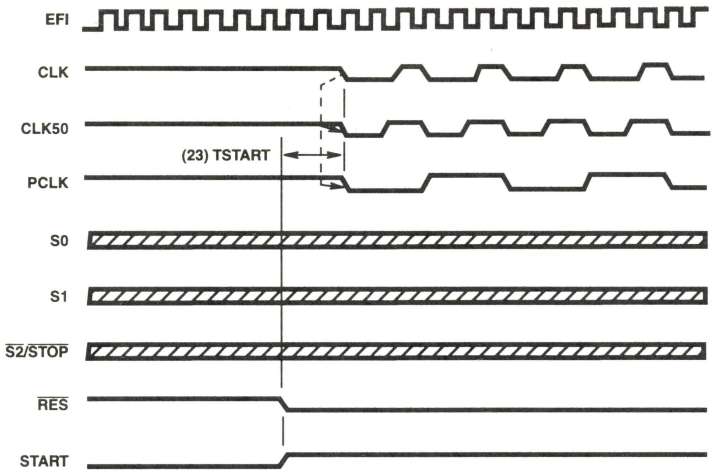


FIGURE 11. CLOCKS START (F/$\overline{C}$ HIGH)

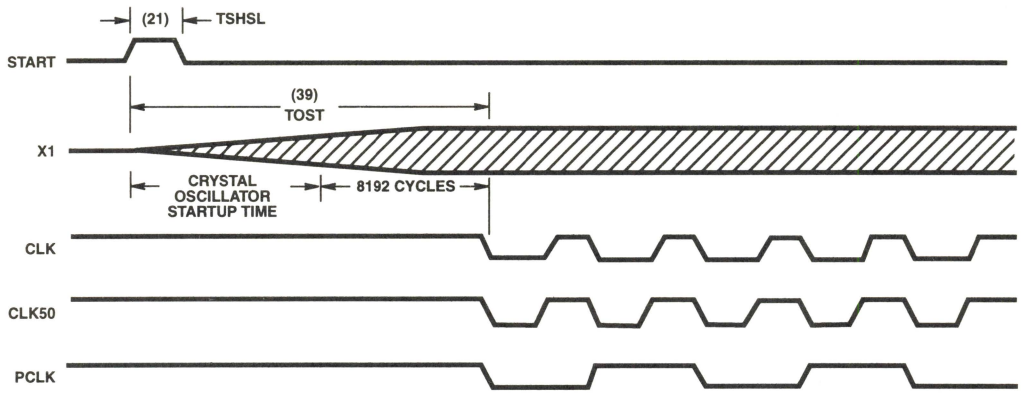


FIGURE 12. CLOCK START (F/$\overline{C}$ LOW)

NOTE: Start up count begins when the crystal oscillator reaches a suitable threshold level.

Timing Waveforms (Continued)

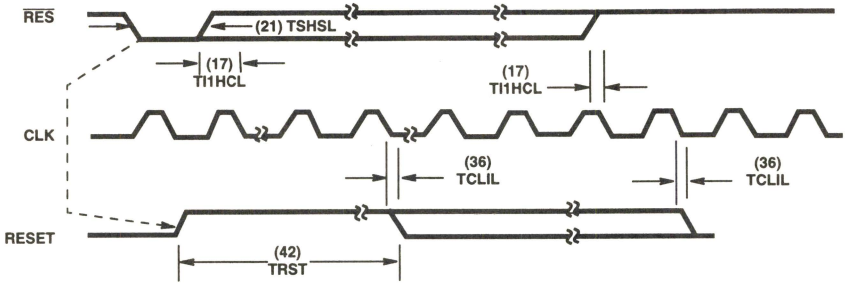


FIGURE 13. RESET TIMING (CLK RUNNING WITH F/$\overline{C}$ LOW-OSC MODE)
(CLK RUNNING-OR STOPPED WITH F/$\overline{C}$ HIGH EFI MODE)

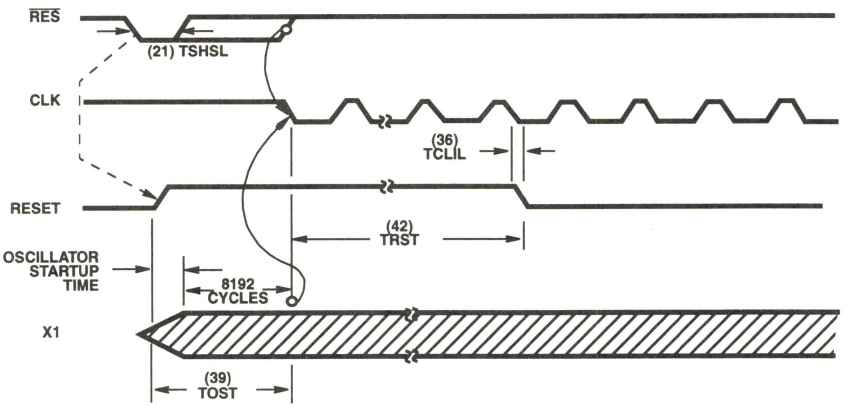


FIGURE 14. RESET TIMING (OSCILLATOR STOPPED, F/$\overline{C}$ LOW)

NOTE: CLK, CLK50, PCLK Remain in the High State until $\overline{RES}$ goes high and 8192 valid oscillator cycles have been registered by the 82C85 internal counter (TOST time period). After $\overline{RES}$ goes high and CLK, CLK50, PCLK become active, the RESET output will remain high for minimum of 16 CLK cycles (TRST).

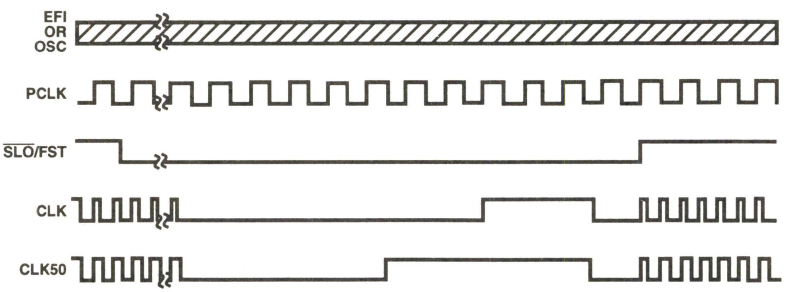


FIGURE 15. SLO/FST TIMING OVERVIEW

NOTE: See Fast to Slow Clock Mode Transition for Detailed Timing; See Slow to Fast Clock Mode Transition for Detailed Timing

Timing Waveforms (Continued)

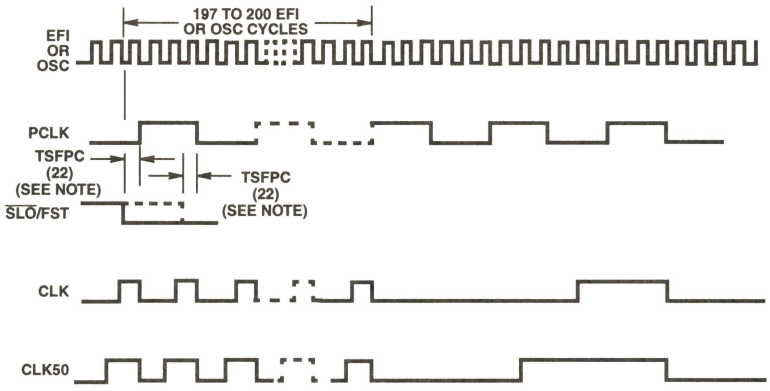


FIGURE 16. FAST TO SLOW CLOCK MODE TRANSITION

NOTE: IF TSFPC is not met on one edge of PLCK. SLO/FST will be recognized on the next edge of PLCK.

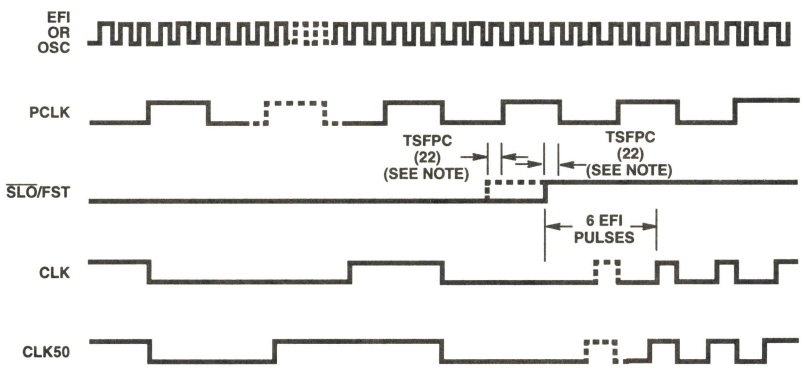
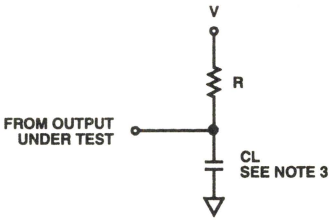


FIGURE 17. SLOW TO FAST CLOCK MODE TRANSITION

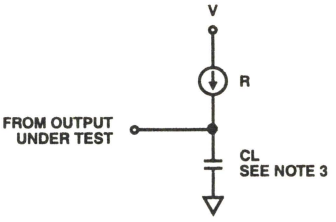
NOTE: IF TSFPC is not met on one edge of PLCK. SLO/FST will be recognized on the next edge of PLCK.

Test Load Circuits

PASSIVE LOAD



DYNAMIC LOAD

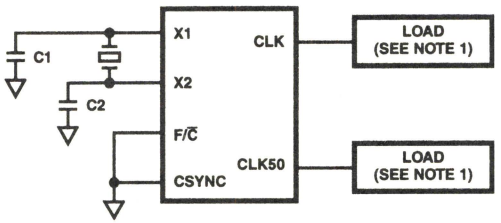


R = 360 at V = 2.25 for CLK and CLK50 outputs
R = 470 at V = 2.87 for all other outputs (Except X2)
NOTES:

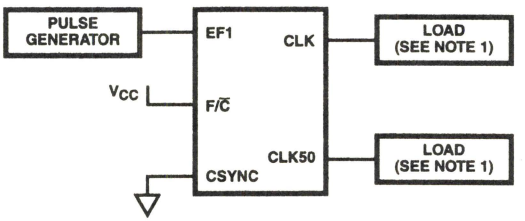
1. C_L = 100pF for CLK and CLK50 output
2. C_L = 50pF minimum for all other outputs
3. C_L = Includes probe and jig capacitance

I_{OL} = 5mA, IOH = -5mA for CLK and CLK50 outputs
I_{OL} = 5mA, IOH = -2.5mA for all other outputs (Except X2)
I_{OL} = 2.5mA, IOH = -1.0mA for X2 output (DC Performance characteristic only)
V_{TRIP} = 1.4V

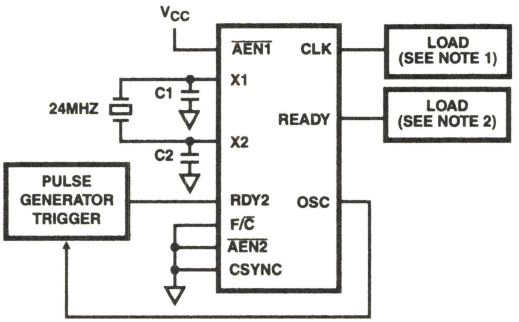
TCHCL, TCLCH LOAD CIRCUIT (USING X1, X2)



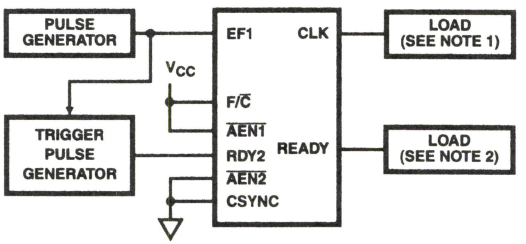
TCHCL, TCLCH LOAD CIRCUIT (USING EFI)



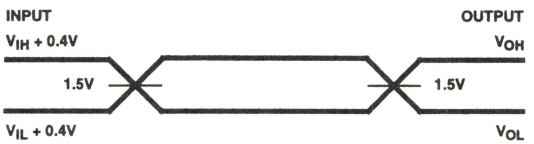
TRYLCL, TRYHCH LOAD CIRCUIT (USING X1, X2)



TRYLCL, TRYHCH LOAD CIRCUIT (USING EFI)

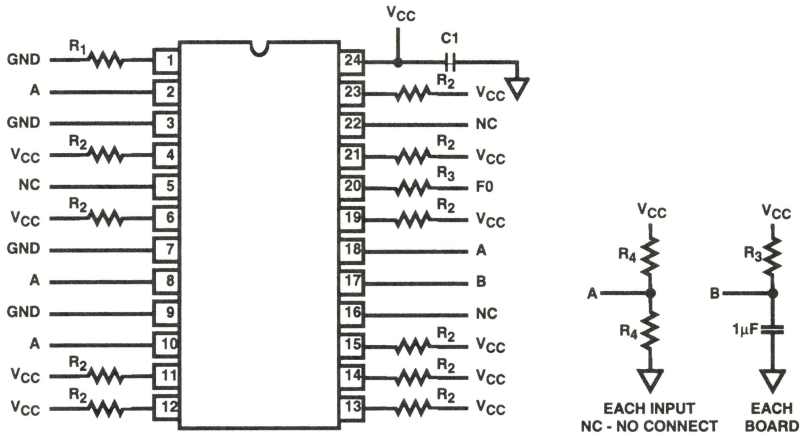


A.C. Testing Input, Output Waveform

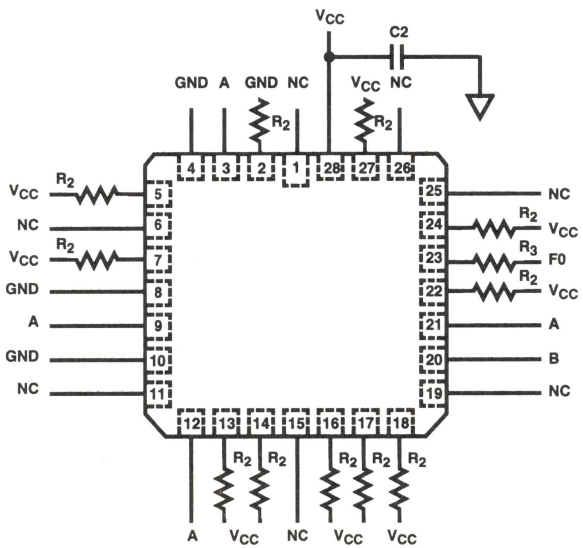


Burn-In Circuits

MD82C85 CERDIP



MR82C85 CLCC
BOTTOM VIEW



NOTES:

1. V_{CC} = 5.5V ±0.5V, GND = 0V
2. V_{IH} = 4.5V ±10%
3. V_{IL} = -0.2 to 0.4V
4. R_1 = 100kΩ, ±5%
5. R_2 = 10kΩ, ±5%
6. R_3 = 47kΩ, ±5%
7. R_4 = 470kΩ, ±5%
8. C1 = 0.01μF (minimum)
9. F0 = 100kHz ±10%

Die Characteristics

DIE DIMENSIONS:
107.9 x 122.0 x 19 ± 1mil

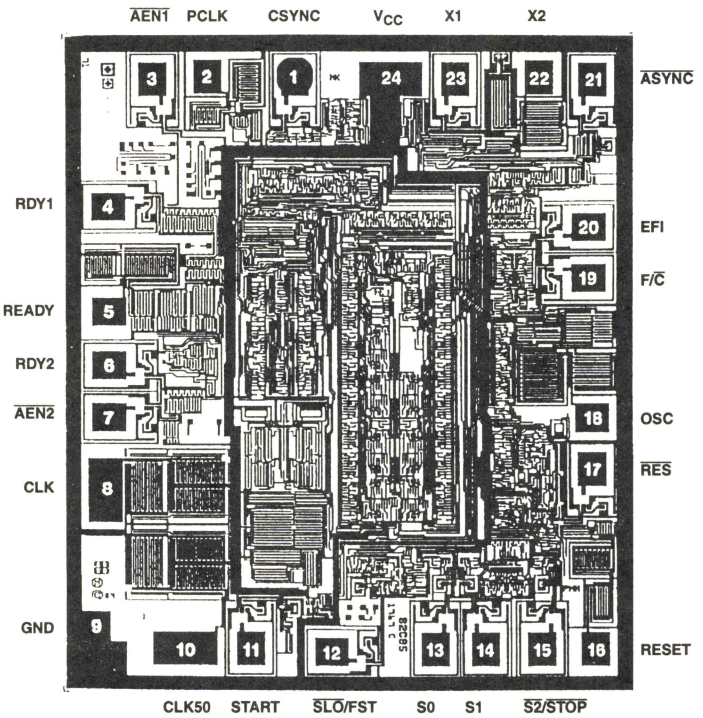
METALLIZATION:
Type: Si - AL
Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
2.26×10^5 A/cm^2
This device meets glassivation integrity test requirements per MIL-STD-883 Method 2021

Metallization Mask Layout

82C85



HARRIS SEMICONDUCTOR

82C86H

March 1997

CMOS Octal Bus Transceiver

Features

- Full Eight Bit Bi-Directional Bus Interface
- Industry Standard 8286 Compatible Pinout
- High Drive Capability
  - B Side I_{OL} 20mA
  - A Side I_{OL} 12mA
- Three-State Outputs
- Propagation Delay ..... 35ns Max.
- Gated Inputs
  - Reduce Operating Power
  - Eliminate the Need for Pull-Up Resistors
- Single 5V Power Supply
- Low Power Operation ..... ICCSB = 10μA
- Operating Temperature Range
  - C82C86H ..... 0°C to +70°C
  - I82C86H ..... -40°C to +85°C
  - M82C86H ..... -55°C to +125°C

Description

The Harris 82C86H is a high performance CMOS Octal Transceiver manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C86H provides a full eight-bit bi-directional bus interface in a 20 lead package. The Transmit (T) control determines the data direction. The active low output enable ($\overline{OE}$) permits simple interface to the 80C86, 80C88 and other microprocessors. The 82C86H has gated inputs, eliminating the need for pull-up/pull-down resistors and reducing overall system operating power dissipation.

Ordering Information

PART NUMBER		PACK-AGE	TEMP. RANGE	PKG. NO.
5MHz	8MHz			
CP82C86H-5	CP82C86H	20 Ld PDIP	0°C to +70°C	E20.3
IP82C86H-5	IP82C86H		-40°C to +85°C	E20.3
CS82C86H-5	CS82C86H	20 Ld PLCC	0°C to +70°C	N20.35
IS82C86H-5	IS82C86H		-40°C to +85°C	N20.35
CD82C86H-5	CD82C86H	20 Ld CERDIP	0°C to +70°C	F20.3
ID82C86H-5	ID82C86H		-40°C to +85°C	F20.3
MD82C86H-5/B	-		-55°C to +125°C	F20.3
5962-8757701RA	-	SMD #		F20.3
MR82C86H-5/B	-	20 Pad CLCC	-55°C to +125°C	J20.A
5962-87577012A	-	SMD #		J20.A

4 CMOS PERIPHERALS

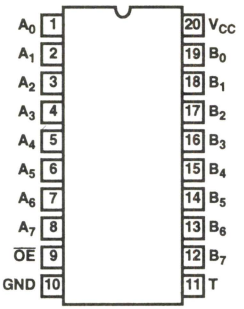
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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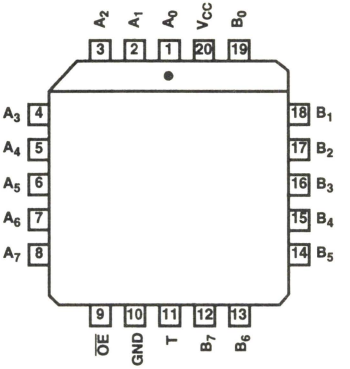
File Number **2977.1**

Pinouts

82C86H (PDIP, CERDIP)
TOP VIEW



82C86H (PLCC, CLCC)
TOP VIEW



TRUTH TABLE

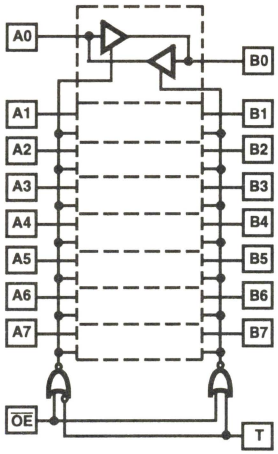
T	$\overline{OE}$	A	B
X	H	Hi-Z	Hi-Z
H	L	I	O
L	L	O	I

H = Logic One
L = Logic Zero
I = Input Mode
O = Output Mode
X = Don't Care
Hi-Z = High Impedance

PIN NAMES

PIN	DESCRIPTION
A_0-A_7	Local Bus Data I/O Pins
B_0-B_7	System Bus Data I/O Pins
T	Transmit Control Input
$\overline{OE}$	Active Low Output Enable

Functional Diagram



Gated Inputs

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between V_{CC} and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance ("float" condition), it could create an indeterminate logic state at the inputs and cause a disruption in device operation.

The Harris 82C8X series of bus drivers eliminates these conditions by turning off data inputs when data is latched (STB = logic zero for the 82C82/83H) and when the device is disabled ($\overline{OE}$ = logic one for the 82C86H/87H). These gated inputs disconnect the input circuitry from the V_{CC} and ground power supply pins by turning off the upper P-channel and lower N-channel (See Figures 1 and 2). No current flow from V_{CC} to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

D.C. input voltage levels can also cause an increase in ICC if these input levels approach the minimum V_{IH} or maximum V_{IL} conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the transparent mode (STB = logic one). ICC remains below the maximum ICC standby specification of 10µA during the time inputs are disabled, thereby greatly reducing the average power dissipation of the 82C8X series devices.

Decoupling Capacitors

The transient current required to charge and discharge the 300pF load capacitance specified in the 82C86H/87H data sheet is determined by:

$$I = C_L(dv/dt) \quad \text{(EQ. 1)}$$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = C_L \frac{(V\,CC \times 80\%)}{tR/tF} \quad \text{(EQ. 2)}$$

where tR = 20ns, V_{CC} = 5.0V, C_L = 300pF on each eight outputs.

$$I = (80 \times 300 \times 10^{-12}) \times (5.0V \times 0.8)/(20 \times 10^{-9}) \quad \text{(EQ. 3)}$$
$$= 480mA$$

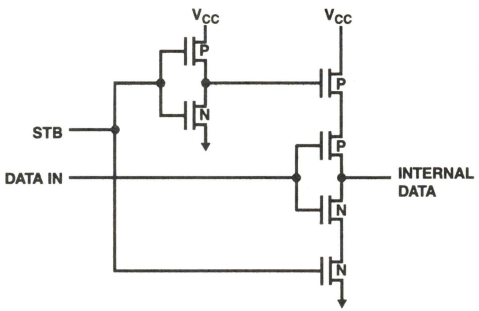


FIGURE 1. 82C82/83H

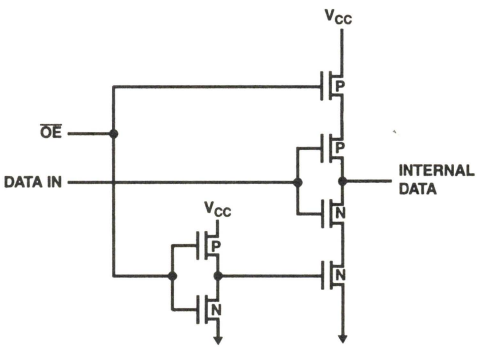


FIGURE 2. 82C86H/87H GATED INPUTS

This current spike may cause a large negative voltage spike on V_{CC} which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1µF ceramic disc capacitor be placed between V_{CC} and GND at each device, with placement being as near to the device as possible.

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C86H . . . . . 0°C to +70°C
I82C86H . . . . . -40°C to +85°C
M82C86H . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	70	16
CLCC Package	80	20
PDIP Package	75	N/A
PLCC Package	75	N/A

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature Hermetic Package . . . . . +175°C
Maximum Junction Temperature Plastic Package . . . . . +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(PLCC - Lead Tips Only)

Die Characteristics

Gate Count . . . . . 265 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5.0V ± 10%; T_A = 0°C to +70°C (C82C86H);
T_A = -40°C to +85°C (I82C86H);
T_A = -55°C to +125°C (M82C86H)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0	-	V	C82C86H, I82C86H
		2.2		V	M82C86H (Note 1)
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
V_{OH}	Logical One Output Voltage				
	B Outputs	3.0		V	I_{OH} = -8mA
	A Outputs	3.0		V	I_{OH} = -4mA
	A or B Outputs	V_{CC} -0.4		V	I_{OH} = -100µA
V_{OL}	Logical Zero Output Voltage				
	B Outputs		0.45	V	I_{OL} = 20mA
	A Outputs		0.45	V	I_{OL} = 12mA
I_I	Input Leakage Current	-10.0	10.0	µA	V_{IN} = GND or V_{CC} DIP Pins 9, 11
IO	Output Leakage Current	-10.0	10.0	µA	VO = GND or V_{CC}, $\overline{OE} \geq V_{CC}$ -0.5V DIP Pins 1 - 8, 12 - 19
ICCSB	Standby Power Supply Current	-	10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs Open
ICCOP	Operating Power Supply Current	-	1	mA/MHz	T_A = +25°C, Typical (See Note 2)

NOTES:

1. V_{IH} is measured by applying a pulse of magnitude = $V_{IH(MIN)}$ to one data input at a time and checking the corresponding device output for a valid logical "1" during valid input high time. Control pins (T, $\overline{OE}$) are tested separately with all device data input pins at V_{CC} -0.4
2. Typical ICCOP = 1mA/MHz of read/ cycle time. (Example: 1.0µs read/write cycle time = 1mA).

Capacitance

T_A = +25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance			
	B Inputs	18	pF	Freq = 1MHz, all measurements are referenced to device GND
	A Inputs	14	pF	

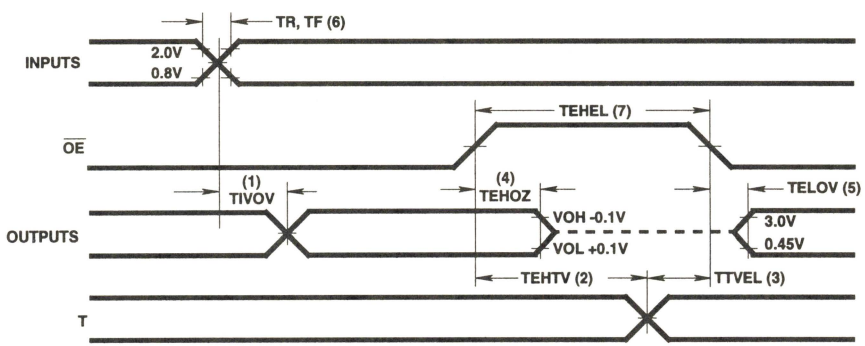
AC Electrical Specifications V_{CC} = 5.0V ± 10%; T_A = 0°C to +70°C (C82C86H);
Freq = 1MHz T_A = -40°C to +85°C (I82C86H);
T_A = -55°C to +125°C (M82C86H)

SYMBOL	PARAMETER	MIN	NOTE 4		UNITS	TEST CONDITIONS
			82C86H MAX	82C86H-5 MAX		
(1) TIVOV	Input to Output Delay					Notes 1, 2
	Inverting	5	30	35	ns	
	Non-Inverting	5	32	35	ns	
(2) TEHTV	Transmit/Receive Hold Time	5	-	-	ns	Notes 1, 2
(3) TTVEL	Transmit/Receive Setup Time	10	-	-	ns	Notes 1, 2
(4) TEHOZ	Output Disable Time	5	30	35	ns	Notes 1, 2
(5) TELOV	Output Enable Time	10	50	65	ns	Notes 1, 2
(6) TR, TF	Input Rise/Fall Times	-	20	20	ns	Notes 1, 2
(7) TEHEL	Minimum Output Enable High Time					Note 3
	82C86H	30	-	-	ns	
	82C86H-5	35	-	-	ns	

NOTES:

1. All AC parameters tested as per test circuits and definitions in timing waveforms and test load circuits. Input rise and fall times are driven at 1ns/V.
2. Input test signals must switch between V_{IL} - 0.4V and V_{IH} +0.4V.
3. A system limitation only when changing direction. Not a measured parameter.
4. 82C86H is available in commercial and industrial temperature ranges only. 82C86H-5 is available in commercial, industrial and military temperature ranges.

Timing Waveform

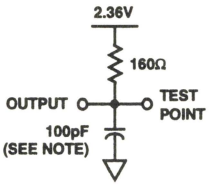


NOTE: All timing measurements are made at 1.5V unless otherwise noted.

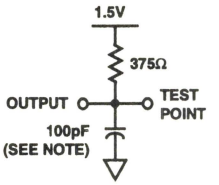
Test Load Circuits

A SIDE OUTPUTS

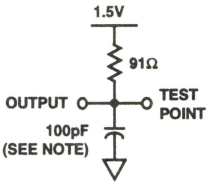
TIVOV LOAD CIRCUIT



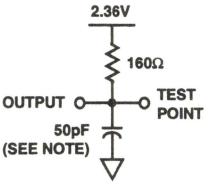
TELOV OUTPUT HIGH ENABLE LOAD CIRCUIT



TELOV OUTPUT LOW ENABLE LOAD CIRCUIT

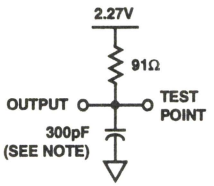


TEHOZ OUTPUT LOW/HIGH DISABLE LOAD CIRCUIT

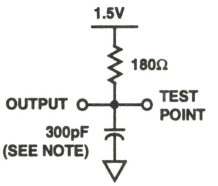


B SIDE OUTPUTS

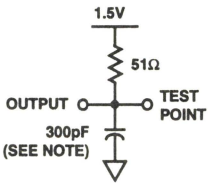
TIVOV LOAD CIRCUIT



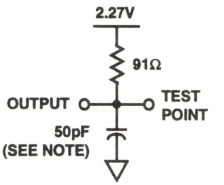
TELOV OUTPUT HIGH ENABLE LOAD CIRCUIT



TELOV OUTPUT LOW ENABLE LOAD CIRCUIT



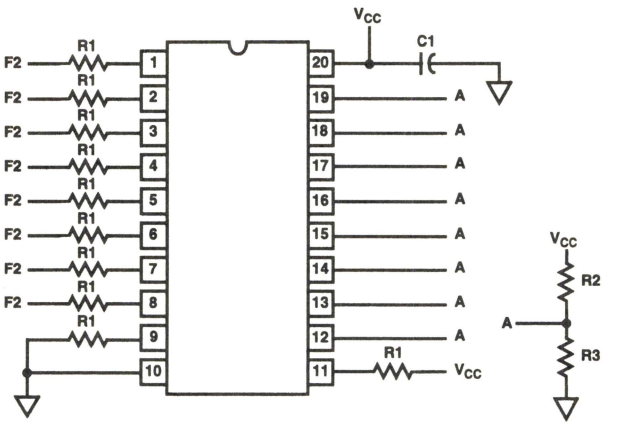
TEHOZ OUTPUT LOW/HIGH DISABLE LOAD CIRCUIT



NOTE: Includes jig and stray capacitance.

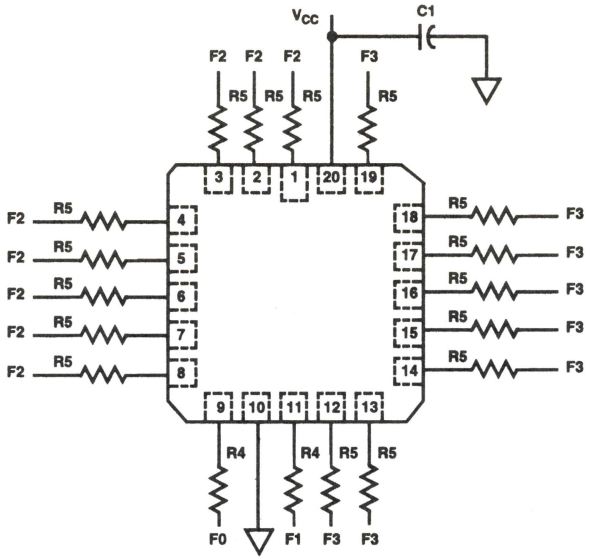
Burn-In Circuits

MD82C86H CERDIP



Burn-In Circuits (Continued)

MR82C86H CLCC



NOTES:

1. V_{CC} = 5.5V ± 0.5V, GND = 0V
2. V_{IH} = 4.5V ± 10%
3. V_{IL} = -0.2V to 0.4V
4. R1 = 47kΩ ± 5%
5. R2 = 2.4kΩ ± 5%
6. R3 = 1.5kΩ ± 5%
7. R4 = 1kΩ ± 5%
8. R5 = 5kΩ ± 5%
9. C1 = 0.01μF minimum
10. F0 = 100kHz ± 10%
11. F1 = F0/2, F2 = F1/2, F3 = F2/2

Die Characteristics

DIE DIMENSIONS:
138.6 x 155.5 x 19 ± 1mils

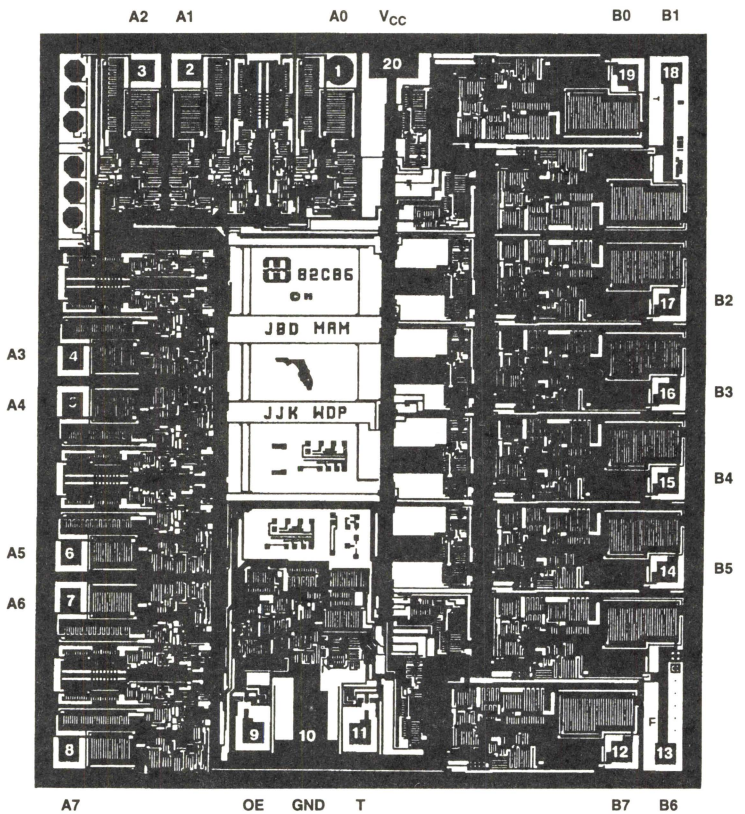
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
1.47 x 10^5 A/cm^2

Metallization Mask Layout

82C86H



HARRIS SEMICONDUCTOR

82C87H

March 1997

CMOS Octal Inverting Bus Transceiver

Features

- Full Eight Bit Bi-Directional Bus Interface
- Industry Standard 8287 Compatible Pinout
- High Drive Capability
  - B Side I_{OL} 20mA
  - A Side I_{OL} 12mA
- Three-State Inverting Outputs
- Propagation Delay . . . . . 35ns Max.
- Gated Inputs
  - Reduce Operating Power
  - Eliminate the Need for Pull-Up Resistors
- Single 5V Power Supply
- Low Power Operation . . . . . ICCSB = 10μA
- Operating Temperature Range
  - C82C87H . . . . . 0°C to +70°C
  - I82C87H . . . . . -40°C to +85°C
  - M82C87H . . . . . -55°C to +125°C

Description

The Harris 82C87H is a high performance CMOS Octal Transceiver manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C87H provides a full eight-bit bi-directional bus interface in a 20 pin package. The Transmit (T) control determines the data direction. The active low output enable ($\overline{OE}$) permits simple interface to the 80C86, 80C88 and other microprocessors. The 82C87H has gated inputs, eliminating the need for pull-up/pull-down resistors and reducing overall system operating power dissipation. The 82C87H provides inverted data at the outputs.

Ordering Information

PART NUMBERS		PACKAGE	TEMP. RANGE	PKG. NO.
5MHz	8MHz			
CP82C87H-5	CP82C87H	20 Ld PDIP	0°C to +70°C	E20.3
IP82C87H-5	IP82C87H		-40°C to +85°C	E20.3
CS82C87H-5	CS82C87H	20 Ld PLCC	0°C to +70°C	N20.35
IS82C87H-5	IS82C87H		-40°C to +85°C	N20.35
CD82C87H-5	CD82C87H	20 Ld CERDIP	0°C to +70°C	F20.3
ID82C87H-5	ID82C87H		-40°C to +85°C	F20.3
MD82C87H-5/B	-		-55°C to +125°C	F20.3
5962-8757702RA	-	SMD #		F20.3
MR82C87H-5/B	-	20 Pad CLCC	-55°C to +125°C	J20.A
5962-87577022A	-	SMD #		J20.A

4 CMOS PERIPHERALS

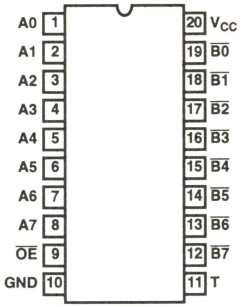
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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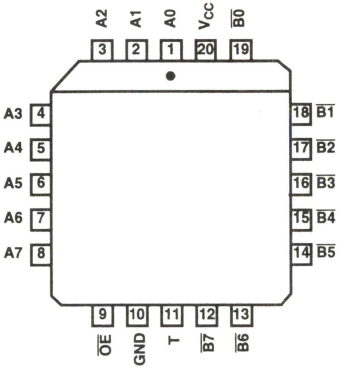
File Number **2978.1**

Pinouts

82C87H (PDIP, CERDIP)
TOP VIEW



82C87H (PLCC, CLCC)
TOP VIEW



TRUTH TABLE

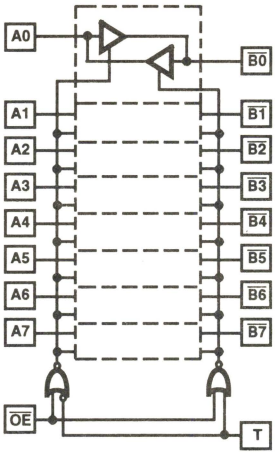
T	$\overline{OE}$	A	B
X	H	Hi-Z	Hi-Z
H	L	I	O
L	L	O	I

H = Logic One
L = Logic Zero
I = Input Mode
O = Output Mode
X = Don't Care
Hi-Z = High Impedance

PIN NAMES

PIN	DESCRIPTION
A_0-A_7	Local Bus Data I/O Pins
B_0-B_7	System Bus Data I/O Pins
T	Transmit Control Input
$\overline{OE}$	Active Low Output Enable

Functional Diagram



Gated Inputs

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between V_{CC} and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance ("float" condition), it could create an indeterminate logic state at the inputs and cause a disruption in device operation.

The Harris 82C8X series of bus drivers eliminates these conditions by turning off data inputs when data is latched (STB = logic zero for the 82C82/83H) and when the device is disabled ($\overline{OE}$ = logic one for the 82C87H/87H). These gated inputs disconnect the input circuitry from the V_{CC} and ground power supply pins by turning off the upper P-Channel and lower N-Channel (See Figures 1 and 2). No current flow from V_{CC} to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

D.C. input voltage levels can also cause an increase in ICC if these input levels approach the minimum V_{IH} or maximum V_{IL} conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the transparent mode (STB = logic one). ICC remains below the maximum ICC standby specification of 10µA during the time inputs are disabled, thereby greatly reducing the average power dissipation of the 82C8X series devices.

Decoupling Capacitors

The transient current required to charge and discharge the 300pF load capacitance specified in the 82C86H/87H data sheet is determined by:

$$I = C_L(dv/dt) \qquad \text{(EQ. 1)}$$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = C_L \frac{(V\,CC \times 80\%)}{tR/tF} \qquad \text{(EQ. 2)}$$

where tR = 20ns, V_{CC} = 5.0V, C_L = 300pF on each eight outputs.

$$I = (80 \times 300 \times 10^{-12}) \times (5.0V \times 0.8)/(20 \times 10^{-9}) = 480mA \qquad \text{(EQ. 3)}$$

This current spike may cause a large negative voltage spike on V_{CC} which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1µF ceramic disc capacitor be placed between V_{CC} and GND at each device, with placement being as near to the device as possible.

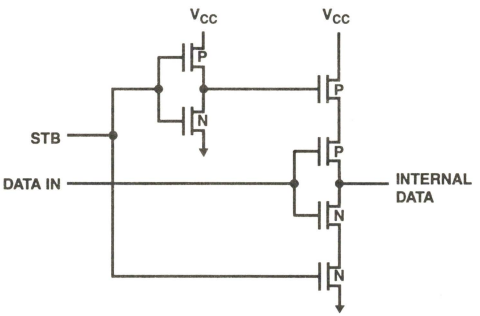


FIGURE 1. 82C82/83H

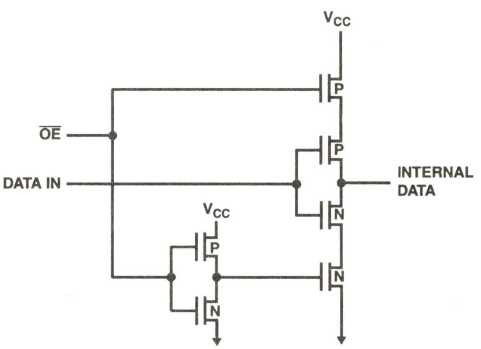


FIGURE 2. 82C86H/87H GATED INPUTS

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C87H . . . . . 0°C to +70°C
I82C87H . . . . . -40°C to +85°C
M82C87H . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	70	16
CLCC Package	80	20
PDIP Package	75	N/A
PLCC Package	75	N/A

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature Hermetic Package . . . . . +175°C
Maximum Junction Temperature Plastic Package . . . . . +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(PLCC - Lead Tips Only)

Die Characteristics

Gate Count . . . . . 265 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5.0V ± 10%; T_A = 0°C to +70°C (C82C87H);
T_A = -40°C to +85°C (I82C87H);
T_A = -55°C to +125°C (M82C87H)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0	-	V	C82C87H, I82C87H
		2.2	-	V	M82C87H (Note 1)
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
V_{OH}	Logical One Output Voltage				
	B Outputs	3.0	-	V	I_{OH} = -8mA
	A Outputs	3.0	-	V	I_{OH} = -4mA
	A or B Outputs	V_{CC} -0.4	-	V	I_{OH} = -100µA
V_{OL}	Logical Zero Output Voltage				
	B Outputs	-	0.45	V	I_{OL} = 20mA
	A Outputs	-	0.45	V	I_{OL} = 12mA
I_I	Input Leakage Current	-10.0	10.0	µA	V_{IN} = GND or V_{CC} DIP Pins 9, 11
IO	Output Leakage Current	-10.0	10.0	µA	VO = GND or V_{CC}, $\overline{OE}$ ≥ V_{CC} -0.5V DIP Pins 1 - 8, 12 - 19
ICCSB	Standby Power Supply Current	-	10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs Open
ICCOP	Operating Power Supply Current	-	1	mA/MHz	T_A = +25°C, Typical (See Note 2)

NOTES:

1. V_{IH} is measured by applying a pulse of magnitude = $V_{IH(MIN)}$ to one data input at a time and checking the corresponding device output for a valid logical "1" during valid input high time. Control pins (T, $\overline{OE}$) are tested separately with all device data input pins at V_{CC} -0.4.
2. Typical ICCOP = 1mA/MHz of read/ cycle time. (Example: 1.0µs read/write cycle time = 1mA).

Capacitance

T_A = +25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance			
	B Inputs	18	pF	Freq = 1MHz, all measurements are referenced to device GND
	A Inputs	14	pF	

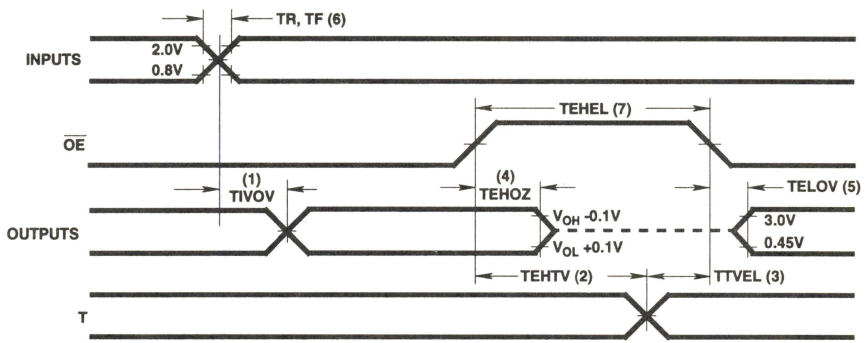
AC Electrical Specifications V_{CC} = 5.0V ± 10%; T_A = 0°C to +70°C (C82C87H);
Freq = 1MHz T_A = -40°C to +85°C (I82C87H);
T_A = -55°C to +125°C (M82C87H)

SYMBOL	PARAMETER	MIN	NOTE 4		UNITS	TEST CONDITIONS
			82C87H MAX	82C87H-5 MAX		
(1) TIVOV	Input to Output Delay					Notes 1, 2
	Inverting	5	30	35	ns	
	Non-Inverting	5	32	35	ns	
(2) TEHTV	Transmit/Receive Hold Time	5	-	-	ns	Notes 1, 2
(3) TTVEL	Transmit/Receive Setup Time	10	-	-	ns	Notes 1, 2
(4) TEHOZ	Output Disable Time	5	30	35	ns	Notes 1, 2
(5) TELOV	Output Enable Time	10	50	65	ns	Notes 1, 2
(6) TR, TF	Input Rise/Fall Times	-	20	20	ns	Notes 1, 2
(7) TEHEL	Minimum Output Enable High Time					Note 3
	82C87H	30	-	-	ns	
	82C87H-5	35	-	-	ns	

NOTES:

1. All AC parameters tested as per test circuits and definitions in timing waveforms and test load circuits. Input rise and fall times are driven at 1ns/V.
2. Input test signals must switch between V_{IL} - 0.4V and V_{IH} +0.4V.
3. A system limitation only when changing direction. Not a measured parameter.
4. 82C87H is available in commercial and industrial temperature ranges only. 82C87H-5 is available in commercial, industrial and military temperature ranges.

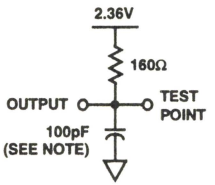
Timing Waveform



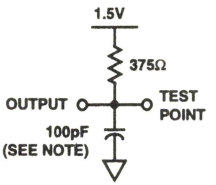
Test Load Circuits

A SIDE OUTPUTS

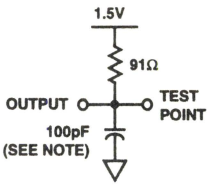
TIVOV LOAD CIRCUIT



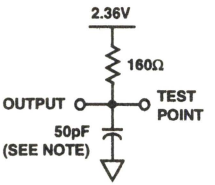
TELOV OUTPUT HIGH ENABLE LOAD CIRCUIT



TELOV OUTPUT LOW ENABLE LOAD CIRCUIT

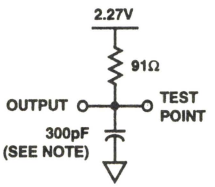


TEHOZ OUTPUT LOW/HIGH DISABLE LOAD CIRCUIT

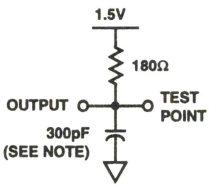


B SIDE OUTPUTS

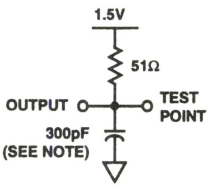
TIVOV LOAD CIRCUIT



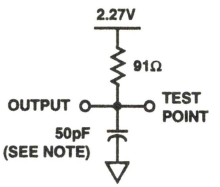
TELOV OUTPUT HIGH ENABLE LOAD CIRCUIT



TELOV OUTPUT LOW ENABLE LOAD CIRCUIT



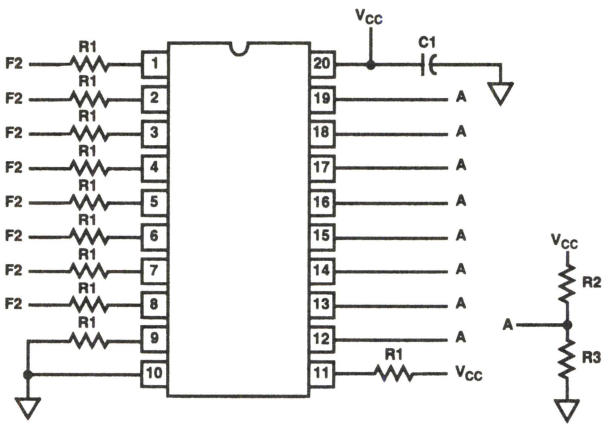
TEHOZ OUTPUT LOW/HIGH DISABLE LOAD CIRCUIT



NOTE: Includes jig and stray capacitance.

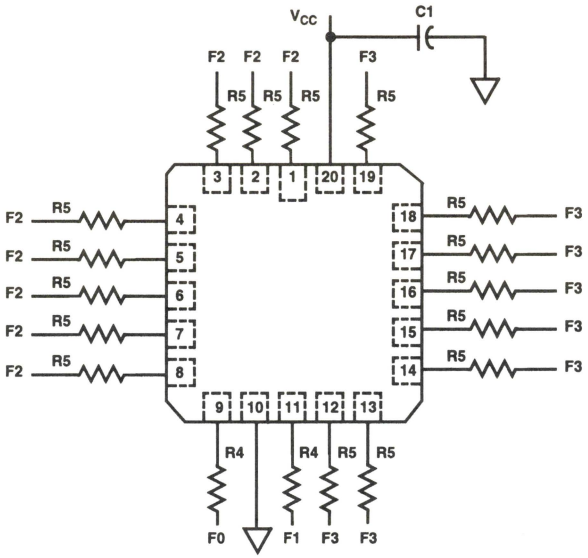
Burn-In Circuits

MD82C87H CERDIP



Burn-In Circuits (Continued)

MR82C87H CLCC



NOTES:

1. V_{CC} = 5.5V ± 0.5V, GND = 0V
2. V_{IH} = 4.5V ± 10%
3. V_{IL} = -0.2V to 0.4V
4. R1 = 47kΩ ± 5%
5. R2 = 2.4kΩ ± 5%
6. R3 = 1.5kΩ ± 5%
7. R4 = 1kΩ ± 5%
8. R5 = 5kΩ ± 5%
9. C1 = 0.01μF minimum
10. F0 = 100kHz ± 10%
11. F1 = F0/2, F2 = F1/2, F3 = F2/2

Die Characteristics

DIE DIMENSIONS:
138.6 x 155.5 x 19 ± 1mils

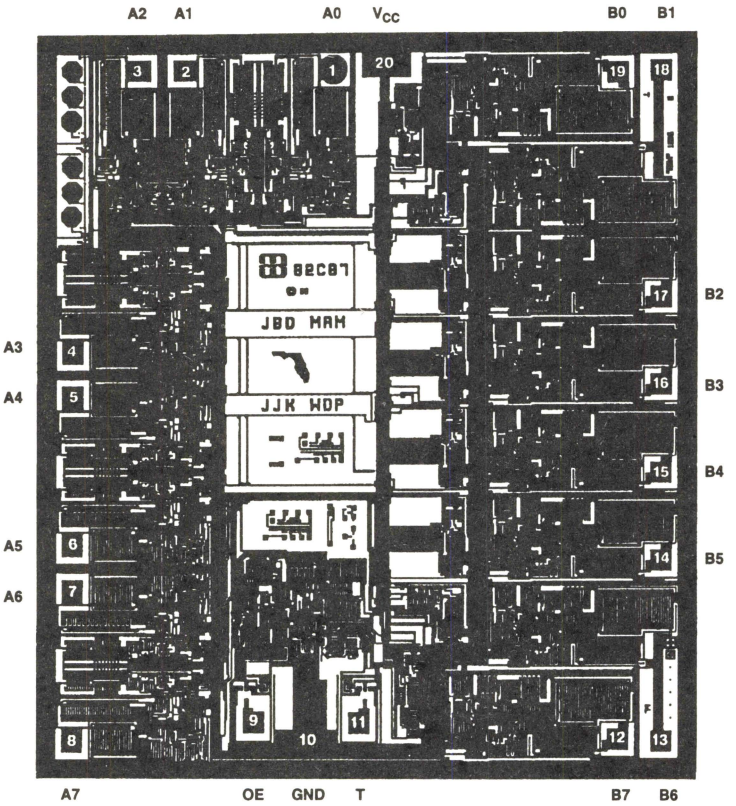
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
1.47 x 10^5 A/cm^2

Metallization Mask Layout

82C87H



March 1997

CMOS Bus Controller

Features

- Compatible with Bipolar 8288
- Performance Compatible with:
  - 80C86/80C88 . . . . . (5/8MHz)
  - 80186/80188 . . . . . (6/8MHz)
  - 8086/8088 . . . . . (5/8MHz)
  - 8089
- Provides Advanced Commands for Multi-Master Busses
- Three-State Command Outputs
- Bipolar Drive Capability
- Scaled SAJI IV CMOS Process
- Single 5V Power Supply
- Low Power Operation
  - ICCSB . . . . . 10μA (Max)
  - ICCOP . . . . . 1mA/MHz (Max)
- Operating Temperature Ranges
  - C82C88 . . . . . 0°C to +70°C
  - I82C88 . . . . . -40°C to +85°C
  - M82C88 . . . . . -55°C to +125°C

Description

The Harris 82C88 is a high performance CMOS Bus Controller manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C88 provides the control and command timing signals for 80C86, 80C88, 8086, 8088, 8089, 80186, and 80188 based systems. The high output drive capability of the 82C88 eliminates the need for additional bus drivers.

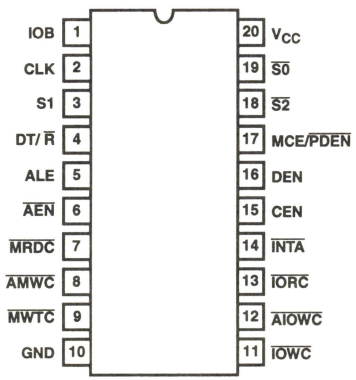
Static CMOS circuit design insures low operating power. The Harris advanced SAJI process results in performance equal to or greater than existing equivalent products at a significant power savings.

Ordering Information

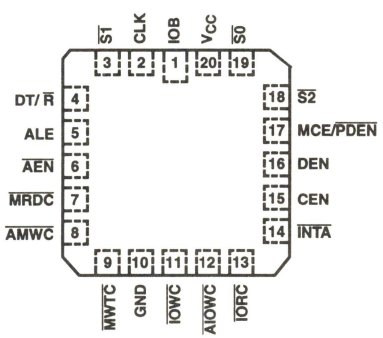
PART NUMBER	PACKAGE	TEMPERATURE RANGE	PKG. NO.
CP82C88	20 Ld PDIP	0°C to +70°C	E20.3
CP82C88-10		0°C to +70°C	E20.3
IP82C88		-40°C to +85°C	E20.3
CS82C88	20 Ld PLCC	0°C to +70°C	N20.35
IS82C88		-40°C to +85°C	N20.35
CD82C88	20 Ld CERDIP	0°C to +70°C	F20.3
ID82C88		-40°C to +85°C	F20.3
MD82C88/B		-55°C to +125°C	F20.3
8406901RA	SMD#		F20.3
MR82C88/B	20 Pad CLCC	-55°C to +125°C	J20.A
84069012A	SMD#		J20.A

Pinouts

20 LEAD PDIP, CERDIP
TOP VIEW



20 LEAD PLCC, CLCC
TOP VIEW

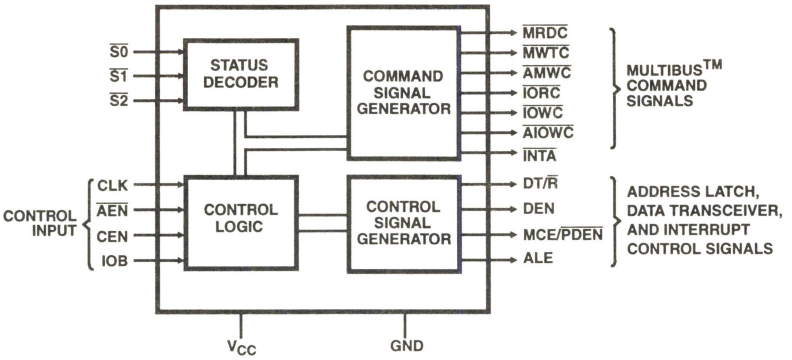


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2979.1**

Functional Diagram



Pin Description

PIN SYMBOL	NUMBER	TYPE	DESCRIPTION
V_{CC}	20		V_{CC}: The +5V power supply pin. A 0.1μF capacitor between pins 10 and 20 is recommended for decoupling.
GND	10		GROUND.
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	19, 3, 18	I	STATUS INPUT PINS: These pins are the input pins from the 80C86, 80C88,8086/88, 8089 processors. The 82C88 decodes these inputs to generate command and control signals at the appropriate time. When Status pins are not in use (passive), command outputs are held HIGH (See Table1).
CLK	2	I	CLOCK: This is a CMOS compatible input which receives a clock signal from the 82C84A or 82C85 clock generator and serves to establish when command/control signals are generated.
ALE	5	O	ADDRESS LATCH ENABLE: This signal serves to strobe an address into the address latches. This signal is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches, such as the 82C82 and 82C83H.
DEN	16	O	DATA ENABLE: This signal serves to enable data transceivers onto either the local or system data bus. This signal is active HIGH.
DT/$\overline{R}$	4	O	DATA TRANSMIT/RECEIVE: This signal establishes the direction of data flow through the transceivers. A HIGH on this line indicates Transmit (write to I/O or memory) and a LOW indicates Receive (read from I/O or memory).
$\overline{AEN}$	6	I	ADDRESS ENABLE: $\overline{AEN}$ enables command outputs of the 82C88 Bus Controller a minimum of 110ns (250ns maximum) after it becomes active (LOW). $\overline{AEN}$ going inactive immediately three-states the command output drivers. $\overline{AEN}$ does not affect the I/O command lines if the 82C88 is in the I/O Bus mode (IOB tied HIGH).
CEN	15	I	COMMAND ENABLE: When this signal is LOW all 82C88 command outputs and the DEN and PDEN control outputs are forced to their Inactive state. When this signal is HIGH, these same outputs are enabled.
IOB	1	I	INPUT/OUTPUT BUS MODE: When the IOB pin is strapped HIGH, the 82C88 functions in the I/O Bus mode. When it is strapped LOW, the 82C88 functions in the System Bus mode (See I/O Bus and System Bus sections).

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Pin Description (Continued)

PIN SYMBOL	NUMBER	TYPE	DESCRIPTION
$\overline{AIOWC}$	12	O	ADVANCED I/O WRITE COMMAND: The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AIOWC}$ is active LOW.
$\overline{IOWC}$	11	O	I/O WRITE COMMAND: This command line instructs an I/O device to read the data on the data bus. The signal is active LOW.
$\overline{IORC}$	13	O	I/O READ COMMAND: This command line instructs an I/O device to drive its data onto the data bus. This signal is active LOW.
$\overline{AMWC}$	8	O	ADVANCED MEMORY WRITE COMMAND: The $\overline{AMWC}$ issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AMWC}$ is active LOW.
$\overline{MWTC}$	9	O	MEMORY WRITE COMMAND: This command line instructs the memory to record the data present on the data bus. This signal is active LOW.
$\overline{MRDC}$	7	O	MEMORY READ COMMAND: This command line instructs the memory to drive its data onto the data bus. $\overline{MRDC}$ is active LOW.
$\overline{INTA}$	14	O	INTERRUPT ACKNOWLEDGE: This command line tells an interrupting device that its interrupt has been acknowledged and that it should drive vectoring information onto the data bus. This signal is active LOW.
MCE/$\overline{PDEN}$	17	O	This is a dual function pin. MCE (IOB IS TIED LOW) Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade Address from a master 82C59A Priority Interrupt Controller onto the data bus. The MCE signal is active HIGH. $\overline{PDEN}$ (IOB IS TIED HIGH): Peripheral Data Enable enables the data bus transceiver for the I/O bus that DEN performs for the system bus. $\overline{PDEN}$ is active LOW.

Functional Description

The command logic decodes the three 80C86, 8086, 80C88, 8088, 80186, 80188 or 8089 status lines ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) to determine what command is to be issued (see Table 1).

TABLE 1. COMMAND DECODE DEFINITION

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	PROCESSOR STATE	82C88 COMMAND
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

I/O Bus Mode

The 82C88 is in the I/O Bus mode if the IOB pin is strapped HIGH. In the I/O Bus mode, all I/O command lines ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (i.e., not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the 82C88 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one 82C88 Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

System Bus Mode

The 82C88 is in the System Bus mode if the IOB pin is strapped LOW. In this mode, no command is issued until a specified time period after the $\overline{AEN}$ line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the $\overline{AEN}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

Command Outputs

The advanced write commands are made available to initiate write procedures early in the machine cycle. This signal can be used to prevent the processor from entering an unnecessary wait state.

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

The command outputs are:

$\overline{MRDC}$ - Memory Read Command

$\overline{MWTC}$ - Memory Write Command

$\overline{IORC}$ - I/O Read Command

$\overline{IOWC}$ - I/O Write Command

$\overline{AMWC}$ - Advanced Memory Write Command

$\overline{AIOWC}$ - Advanced I/O Write Command

$\overline{INTA}$ - Interrupt Acknowledge

Control Outputs

The control outputs of the 82C88 are Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/ Peripheral Data Enable (MCE/$\overline{PDEN}$). The DEN signal determines when the external bus should be enabled onto the local bus and the DT/$\overline{R}$ determines the direction of data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{PDEN}$ pin changes function with the two modes of the 82C88. When the 82C88 is in the IOB mode (IOB HIGH), the $\overline{PDEN}$ signal serves as a dedicated data enable signal for the I/O or Peripheral System bus.

Interrupt Acknowledge and MCE

The MCE signal is used during an interrupt acknowledge cycle if the 82C88 is in the System Bus mode (IOB LOW). During any interrupt sequence, there are two interrupt acknowledge cycles that occur back to back. During the first interrupt cycle no data or address transfers take place. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle, the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, the MCE signal is not used. In this case, the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable and Halt

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the 82C82/82C83H address latches. ALE also serves to strobe the status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) into a latch for halt state decoding.

Command Enable

The Command Enable (CEN) input acts as a command qualifier for the 82C88. If the CEN pin is high, the 82C88 functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not three-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C88. . . . . 0°C to +70°C
I82C88 . . . . . -40°C to +85°C
M82C88 . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	75	18
CLCC Package	85	22
PDIP Package	75	N/A
PLCC Package	75	N/A

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package . . . . . +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(PLCC - Lead Tips Only)

Die Characteristics

Gate Count . . . . . 100 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5.0V ± 10%;
T_A = 0°C to +70°C (C82C88);
T_A = -40°C to +85°C (I82C88);
T_A = -55°C to +125°C (M82C88)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0 2.2	- -	V V	C82C88, I82C88 M82C88
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
VIHC	CLK Logical One Input Voltage	V_{CC} -0.8	-	V	
VILC	CLK Logical Zero Input Voltage	-	0.8	V	
V_{OH}	Output High Voltage Command Outputs	3.0 V_{CC} -0.4	-	V V	I_{OH} = -8.0mA I_{OH} = -2.5mA
	Output High Voltage Control Outputs	3.0 V_{CC} -0.4	-	V V	I_{OH} = -4.0mA I_{OH} = -2.5mA
V_{OL}	Output Low Voltage Command Outputs	-	0.5	V	I_{OL}= +12.0mA
	Output Low Voltage Control Outputs	-	0.4	V	I_{OL} = +8.0mA
I_I	Input Leakage Current	-1.0	1.0	µA	V_{IN} = GND or V_{CC}, except $\overline{S0}$, $\overline{S1}$, $\overline{S2}$, DIP Pins 1-2, 6, 15
IBHH	Input Leakage Current-Status Bus	-50	-300	µA	V_{IN} = 2.0V, $\overline{S0}$, $\overline{S1}$, $\overline{S2}$ (See Note 1)
IO	Output Leakage Current	-10.0	10.0	µA	V_O = GND or V_{CC}, IOB = GND, $\overline{AEN}$ = V_{CC}, DIP Pins 7-9, 11-14
ICCSB	Standby Power Supply	-	10	µA	V_{CC} = 5.5V, V_{IN} = V_{CC} or GND, Outputs Open
ICCOP	Operating Power Supply Current	-	1	mA/MHz	V_{CC} = 5.5V, Outputs Open (See Note 2)

NOTES:

1. IBHH should be measured after raising the V_{IN} on $\overline{S0}$, $\overline{S1}$, $\overline{S2}$ to V_{CC} and then lowering to valid input high level of 2.0V.
2. ICCOP = 1mA/MHz of CLK cycle time (TCLCL)

Capacitance T_A = +25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	10	pF	FREQ = 1MHz, all measurements are referenced to device GND
COUT	Output Capacitance	17	pF	

AC Electrical Specifications

V_{CC} = 5.0V ± 10%;
T_A = 0°C to +70°C (C82C88);
T_A = -40°C to +85°C (I82C88);
T_A = -55°C to +125°C (M82C88)

SYMBOL	PARAMETER	8MHz		10MHz		12MHz		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS									
(1) TCLCL	CLK Cycle Period	125	-	100	-	83	-	ns	
(2) TCLCH	CLK Low Time	55	-	50	-	34	-	ns	
(3) TCHCL	CLK High Time	40	-	37	-	34	-	ns	
(4) TSVCH	Status Active Setup Time	35	-	35	-	35	-	ns	
(5) TCHSV	Status Inactive Hold Time	10	-	10	-	5	-	ns	
(6) TSHCL	Status Inactive Setup Time	35	-	35	-	35	-	ns	
(7) TCLSH	Status Active Hold Time	10	-	10	-	5	-	ns	
TIMING RESPONSES									
(8) TCVNV	Control Active Delay	5	45	5	45	5	45	ns	1
(9) TCVNX	Control Inactive Delay	10	45	10	45	10	35	ns	1
(10) TCLLH	ALE Active Delay (from CLK)	-	20	-	20	-	20	ns	1
(11) TCLMCH	MCE Active Delay (from CLK)	-	25	-	23	-	23	ns	1
(12) TSVLH	ALE Active Delay (from Status)	-	20	-	20	-	20	ns	1
(13) TSVMCH	MCE Active Delay (from Status)	-	30	-	23	-	23	ns	1
(14) TCHLL	ALE Inactive Delay	4	18	4	18	4	18	ns	1
(15) TCLML	Command Active Delay	5	35	5	35	5	35	ns	2
(16) TCLMH	Command Inactive Delay	5	35	5	35	5	35	ns	2
(17) TCHDTL	Direction Control Active Delay	-	50	-	50	-	50	ns	1
(18) TCHDTH	Direction Control Inactive Delay	-	30	-	30	-	30	ns	1
(19) TAELCH	Command Enable Time (Note 1)	-	40	-	40	-	40	ns	3
(20) TAEHCZ	Command Disable Time (Note 2)	-	40	-	40	-	40	ns	4
(21) TAELCV	Enable Delay Time	110	250	110	250	110	250	ns	2
(22) TAEVNV	$\overline{AEN}$ to DEN	-	25	-	25	-	25	ns	1
(23) TCEVNV	CEN to DEN, $\overline{PDEN}$	-	25	-	25	-	25	ns	1
(24) TCELRH	CEN to Command	-	TCLML +10	-	TCLML	-	TCLML	ns	2
(25) TLHLL	ALE High Time	TCLCH - 10	-	TCLCH - 10	-	TCLCH - 10	n	ns	1

NOTES:

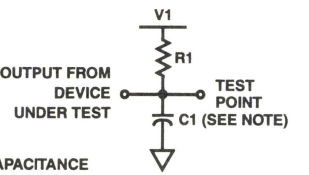
1. TAELCH measurement is between 1.5V and 2.5V.
2. TAEHCZ measured at 0.5V change in VOUT.

AC Testing Input, Output Waveform



A.C. Testing: All input signals (other than CLK) must switch between V_{IL} -0.4V and V_{IH} +0.4. CLK must switch between 0.4V and V_{CC} -0.4V. Input rise and fall times are driven at 1ns/V.

A.C. Test Circuit

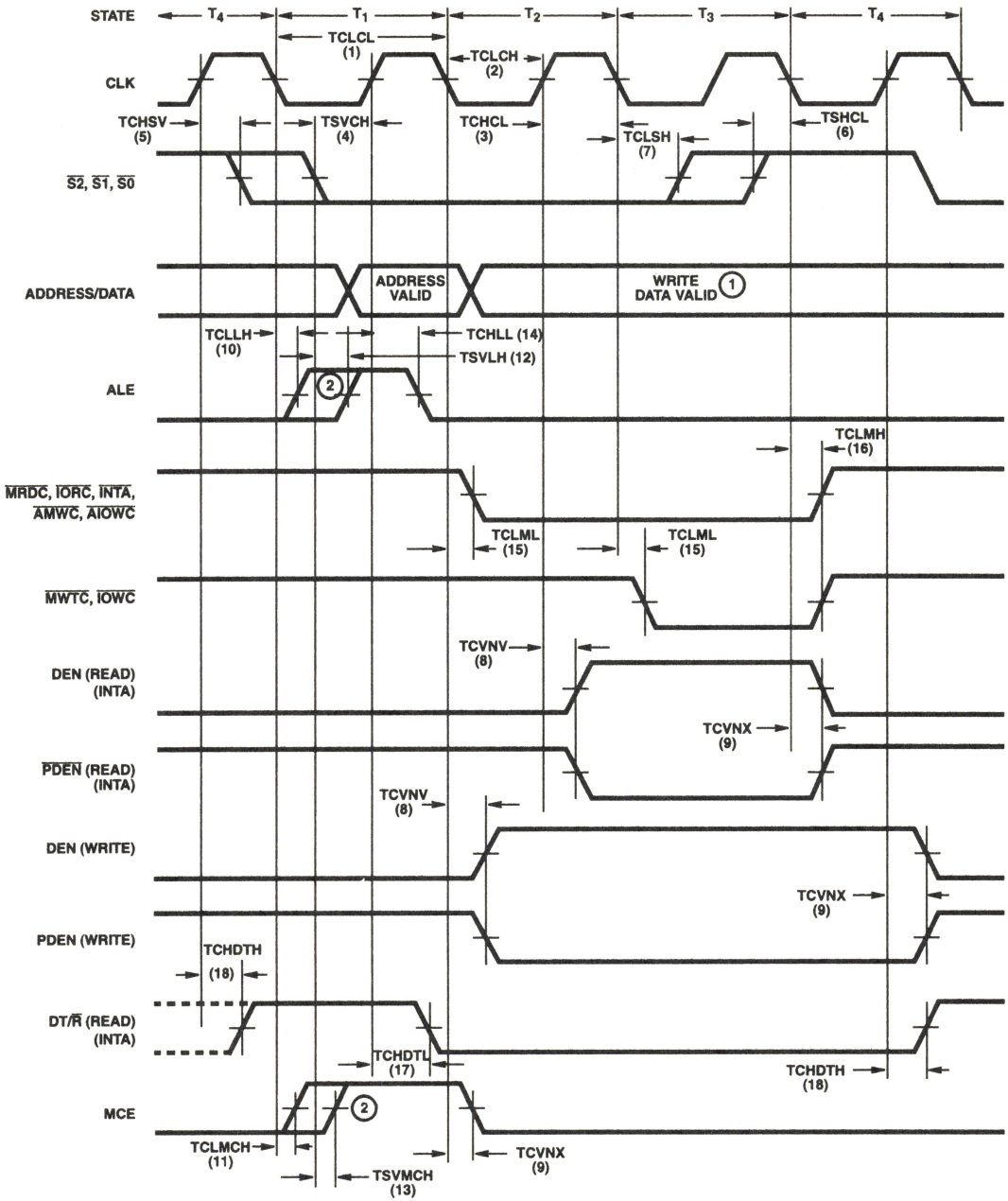


NOTE:
INCLUDES STRAY AND JIG CAPACITANCE

TABLE 2. TEST CONDITION DEFINITION TABLE

TEST CONDITION	V1	R1	C1
1	2.13V	220Ω	80pF
2	2.29V	91Ω	300pF
3	1.5V	187Ω	300pF
4	1.5V	187Ω	50pF

Timing Waveforms (Note 3)



NOTES:

1. Address/Data Bus is shown only for reference purposes.
2. Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active. Whichever occurs last.
3. All timing measurements are made at 1.5V unless otherwise specified.

FIGURE 1.

Timing Waveforms (Note 3) (Continued)

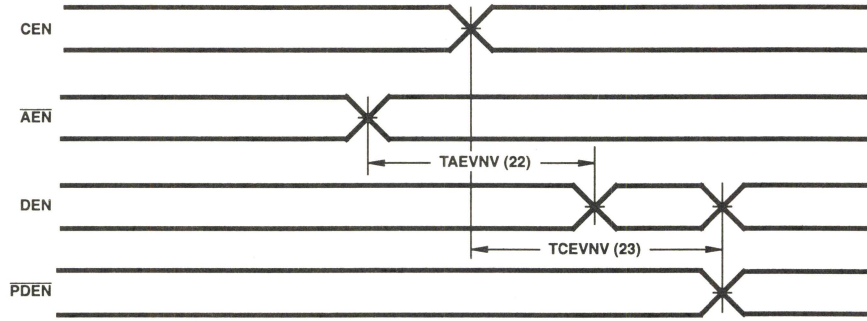
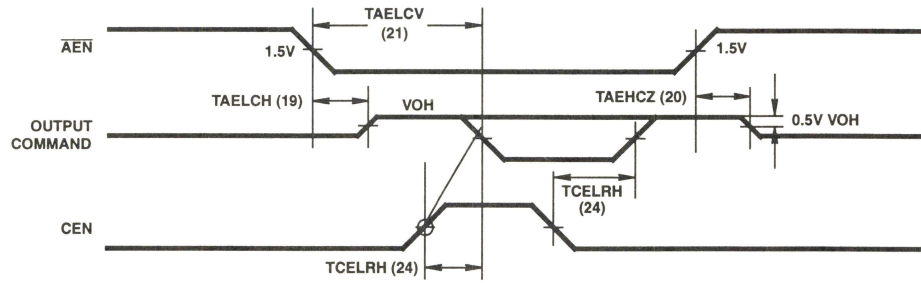


FIGURE 2. DEN, PDEN QUALIFICATION TIMING



CEN MUST BE LOW OR INVALID PRIOR TO T2 TO PREVENT THE COMMAND FROM BEING GENERATED.

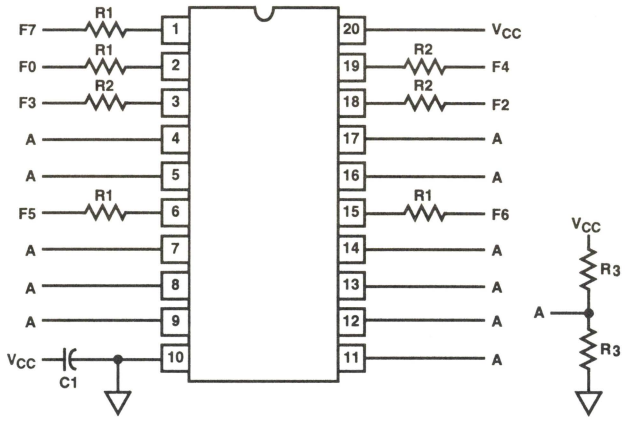
FIGURE 3. ADDRESS ENABLE (AEN) TIMING (THREE-STATE ENABLE/DISABLE)

NOTES:

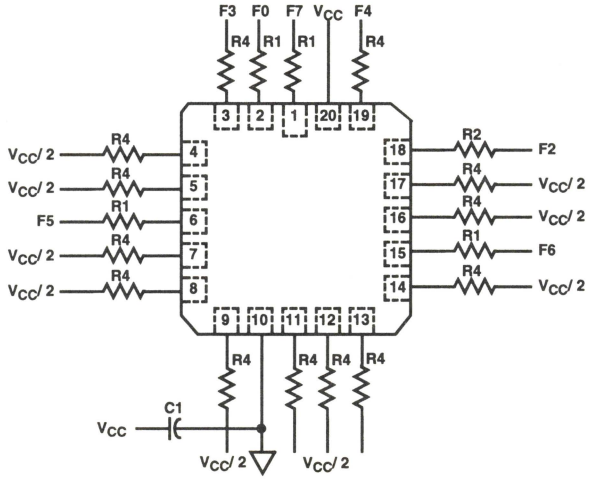
1. Address/Data Bus is shown only for reference purposes.
2. Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active. Whichever occurs last.
3. All timing measurements are made at 1.5V unless otherwise specified.

Burn-In Circuits

MD82C88 CERDIP



MR82C88 CLCC



NOTES:

1. V_{CC} = 5.5V ± 0.5V
   GND = 0V
2. V_{IH} = 4.5V ± 10%
   V_{IL} = -0.2V to +0.4V
3. Component Values:
   R1 = 47kΩ, 1/4W, 5%
   R2 = 1.5kΩ, 1/4W, 5%
   R3 = 10kΩ, 1/4W, 5%
   R4 = 1.2kΩ, 1/4W, 5%
   C1 = 0.01µF (Min)
   F0 = 100kHz ± 10%
   F1 = F0/2
   F2 = F1/2 . . . F7 = F6/2

Die Characteristics

DIE DIMENSIONS:
103.5 x 116.5 x 19 ± 1mils

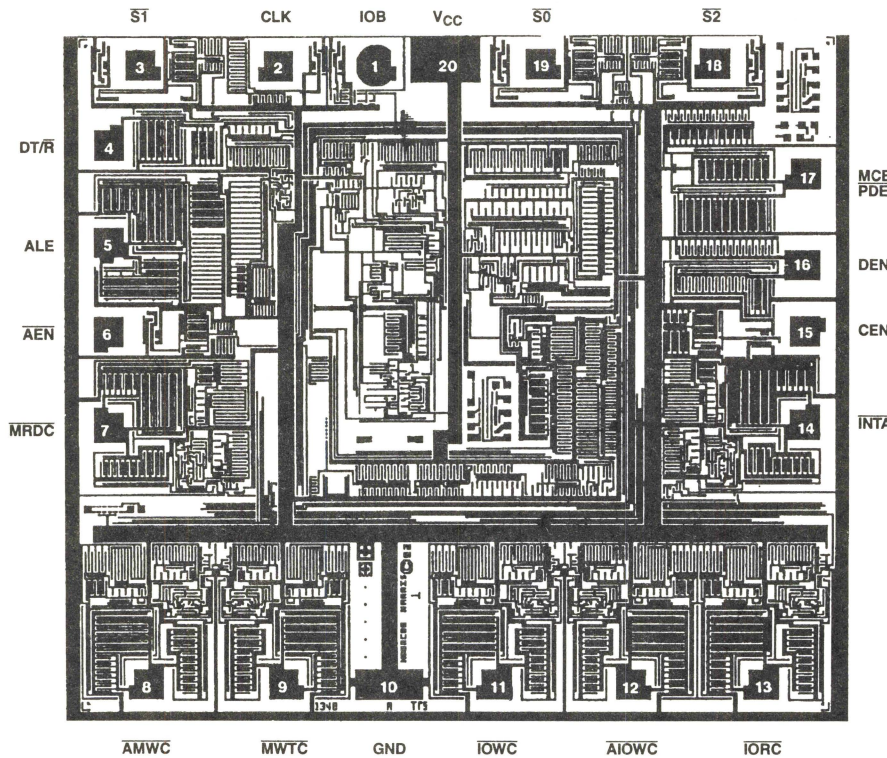
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:
1.9×10^5 A/cm^2

Metallization Mask Layout

82C88



March 1997

CMOS Bus Arbiter

Features

- Pin Compatible with Bipolar 8289
- Performance Compatible with:
  - 80C86/80C88 . . . . . (5/8MHz)
- Provides Multi-Master System Bus Control and Arbitration
- Provides Simple Interface with 82C88/8288 Bus Controller
- Synchronizes 80C86/8086, 80C88/8088 Processors with Multi-Master Bus
- Bipolar Drive Capability
- Four Operating Modes for Flexible System Configuration
- Low Power Operation
  - ICCSB . . . . . 10μA (Max)
  - ICCOP . . . . . 1mA/MHz (Max)
- Operating Temperature Ranges
  - C82C89 . . . . . 0°C to +70°C
  - I82C89 . . . . . -40°C to +85°C
  - M82C89 . . . . . -55°C to +125°C

Description

The Harris 82C89 Bus Arbiter is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). This circuit, along with the 82C88 bus controller, provides full bus arbitration and control for multi-processor systems. The 82C89 is typically used in medium to large 80C86 or 80C88 systems where access to the bus by several processors must be coordinated. The 82C89 also provides high output current and capacitive drive to eliminate the need for additional bus buffering.

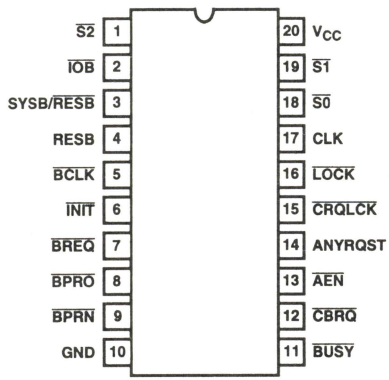
Static CMOS circuit design insures low operating power. The advanced Harris SAJI CMOS process results in performance equal to or greater than existing equivalent products at a significant power savings.

Ordering Information

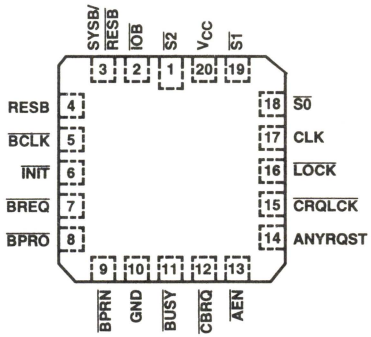
PART NUMBER	PACKAGE	TEMPERATURE RANGE	PKG. NO.
CP82C89	20 Ld PDIP	0°C to +70°C	E20.3
IP82C89		-40°C to +85°C	E20.3
CS82C89	20 Ld PLCC	0°C to +70°C	N20.35
IS82C89		-40°C to +85°C	N20.35
CD82C89	20 Ld CERDIP	0°C to +70°C	F20.3
ID82C89		-40°C to +85°C	F20.3
MD82C89/B		-55°C to +125°C	F20.3
5962-8552801RA	SMD#		F20.3
MR82C89/B	20 Pad CLCC	-55°C to +125°C	J20.A
5962-85528012A	SMD#		J20.A

Pinouts

82C89 (CERDIP)
TOP VIEW

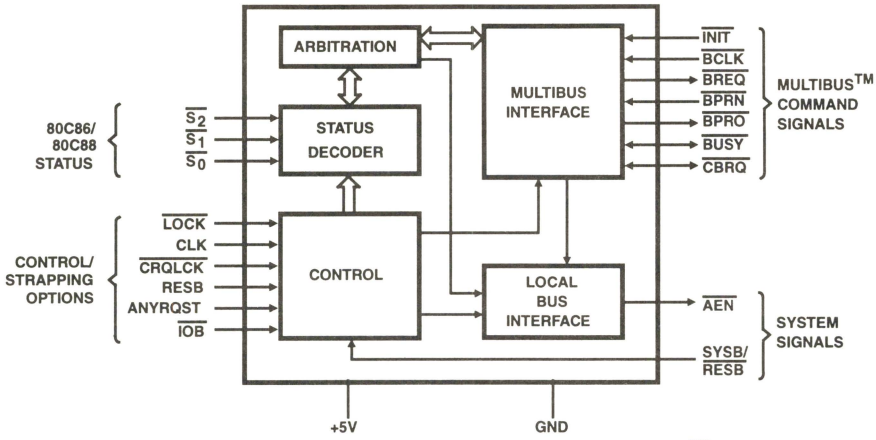


82C89 (PLCC, CLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

Functional Diagram



MULTIBUS™ IS AN INTEL CORP. TRADEMARK

Pin Description

PIN SYMBOL	NUMBER	TYPE	DESCRIPTION
V_{CC}	20		V_{CC}: The +5V Power supply pin. A 0.1µF capacitor between pins 10 and 20 is recommended for decoupling.
GND	10		GROUND.
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	1, 18-19	I	STATUS INPUT PINS: The status input pins from an 80C86, 80C88 or 8089 processor. The 82C89 decodes these pins to initiate bus request and surrender actions. (See Table 1).
CLK	17	I	CLOCK: From the 82C84A or 82C85 clock chip and serves to establish when bus arbiter actions are initiated.
$\overline{LOCK}$	16	I	LOCK: A processor generated signal which when activated (low) prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter, regardless of its priority.
$\overline{CRQLCK}$	15	I	COMMON REQUEST LOCK: An active low signal which prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter requesting the bus through the $\overline{CBRQ}$ input pin.
RESB	4	I	RESIDENT BUS: A strapping option to configure the arbiter to operate in systems having both a multi-master system bus and a Resident Bus. Strapped high, the multi-master system bus is requested or surrendered as a function of the SYSB/$\overline{RESB}$ input pin. Strapped low, the SYSB/$\overline{RESB}$ input is ignored.
ANYRQST	14	I	ANY REQUEST: A strapping option which permits the multi-master system bus to be surrendered to a lower priority arbiter as if it were an arbiter of higher priority (i.e., when a lower priority arbiter requests the use of the multi-master system bus, the bus is surrendered as soon as it is possible). When ANYRQST is strapped low, the bus is surrendered according to Table A in Design Information. If ANYRQST is strapped high and $\overline{CBRQ}$ is activated, the bus is surrendered at the end of the present bus cycle. Strapping $\overline{CBRQ}$ low and ANYRQST high forces the 82C89 arbiter to surrender the multi-master system bus after each transfer cycle. Note that when surrender occurs $\overline{BREQ}$ is driven false (high).

Pin Description (Continued)

PIN SYMBOL	NUMBER	TYPE	DESCRIPTION
$\overline{IOB}$	2	I	IO BUS: A strapping option which configures the 82C89 Arbiter to operate in systems having both an IO Bus (Peripheral Bus) and a multi-master system bus. The arbiter requests and surrenders the use of the multi-master system bus as a function of the status line, $\overline{S2}$. The multi-master system bus is permitted to be surrendered while the processor is performing IO commands and is requested whenever the processor performs a memory command. Interrupt cycles are assumed as coming from the peripheral bus and are treated as an IO command.
$\overline{AEN}$	13	O	ADDRESS ENABLE: The output of the 82C89 Arbiter to the processor's address latches, to the 82C88 Bus Controller and 82C84A or 82C85 Clock Generator. $\overline{AEN}$ serves to instruct the Bus Controller and address latches when to three-state their output drivers.
$\overline{INIT}$	6	I	INITIALIZE: An active low multi-master system bus input signal used to reset all the bus arbiters on the multi-master system bus. After initialization, no arbiters have the use of the multi-master system bus.
SYSB/$\overline{RESB}$	3	I	SYSTEM BUS/RESIDENT BUS: An input signal when the arbiter is configured in the System/Resident Mode ($\overline{RESB}$ is strapped high) which determines when the multi-master system bus is requested and multi-master system bus surrendering is permitted. The signal is intended to originate from a form of address-mapping circuitry, such as a decoder or PROM attached to the resident address bus. Signal transitions and glitches are permitted on this pin from θ1 of T4 to θ1 of T2 of the processor cycle. During the period from θ1 of T2 to θ1 of T4, only clean transitions are permitted on this pin (no glitches). If a glitch occurs, the arbiter may capture or miss it, and the multi-master system bus may be requested or surrendered, depending upon the state of the glitch. The arbiter requests the multi-master system bus in the System/Resident Mode when the state of the SYSB/$\overline{RESB}$ pin is high and permits the bus to be surrendered when this pin is low.
$\overline{CBRQ}$	12	I/O	COMMON BUS REQUEST: An input signal which instructs the arbiter if there are any other arbiters of lower priority requesting the use of the multi-master system bus. The $\overline{CBRQ}$ pins (open-drain output) of all the 82C89 Bus Arbiters which surrender to the multi-master system bus upon request are connected together. The Bus Arbiter running the current transfer cycle will not itself pull the $\overline{CBRQ}$ line low. Any other arbiter connected to the $\overline{CDRQ}$ line can request the multi-master system bus. The arbiter presently running the current transfer cycle drops its $\overline{BREQ}$ signal and surrenders the bus whenever the proper surrender conditions exist. Strapping $\overline{CBRQ}$ low and ANYRQST high allows the multi-master system bus to be surrendered after each transfer cycle. See the pin definition of ANYRQST.
$\overline{BCLK}$	5	I	BUS CLOCK: The multi-master system bus clock to which all multi-master system bus interface signals are synchronized.
$\overline{BREQ}$	7	O	BUS REQUEST: An active low output signal in the Parallel Priority Resolving Scheme which the arbiter activates to request the use of the multi-master system bus.
$\overline{BPRN}$	9	I	BUS PRIORITY IN: The active low signal returned to the arbiter to instruct it that it may acquire the multi-master system bus on the next falling edge of $\overline{BCLK}$. $\overline{BPRN}$ active indicates to the arbiter that it is the highest priority requesting arbiter presently on the bus. The loss of $\overline{BPRN}$ instructs the arbiter that it has lost priority to a higher priority arbiter.
$\overline{BPRO}$	8	O	BUS PRIORITY OUT: An active low output signal used in the serial priority resolving scheme where $\overline{BPRO}$ is daisy-chained to $\overline{BPRN}$ of the next lower priority arbiter.
$\overline{BUSY}$	11	I/O	BUSY: An active low open-drain multi-master system bus interface signal used to instruct all the arbiters on the bus when the multi-master system bus is available. When the multi-master system bus is available the highest requesting arbiter (determined by $\overline{BPRN}$) seizes the bus and pulls $\overline{BUSY}$ low to keep other arbiters off of the bus. When the arbiter is done with the bus, it releases the $\overline{BUSY}$ signal, permitting it to go high and thereby allowing another arbiter to acquire the multi-master system bus.

Functional Description

The 82C89 Bus Arbiter operates in conjunction with the 82C88 Bus Controller to interface 80C86, 80C88 processors to a multi-master system bus (both the 80C86 and 80C88 are configured in their max mode). The processor is unaware of the arbiter's existence and issues commands as though it has exclusive use of the system bus. If the processor does not have the use of the multi-master system bus, the arbiter prevents the Bus Controller (82C88), the data transceivers and the address latches from accessing the system bus (e.g. all bus driver outputs are forced into the high impedance state). Since the command sequence was not issued by the 82C88, the system bus will appear as "Not Ready" and the processor will enter wait states. The processor will remain in Wait until the Bus Arbiter acquires the use of the multi-master system bus whereupon the arbiter will allow the bus controller, the data transceivers, and the address latches to access the system. Typically, once the command has been issued and a data transfer has taken place, a transfer acknowledge (XACK) is returned to the processor to indicate "READY" from the accessed slave device. The processor then completes its transfer cycle. Thus the arbiter serves to multiplex a processor (or bus master) onto a multi-master system bus and avoid contention problems between bus masters.

Arbitration Between Bus Masters

In general, higher priority masters obtain the bus when a lower priority master completes its present transfer cycle. Lower priority bus masters obtain the bus when a higher priority master is not accessing the system bus. A strapping option (ANYRQST) is provided to allow the arbiter to surrender the bus to a lower priority master as though it were a master of higher priority. If there are no other bus masters requesting the bus, the arbiter maintains the bus so long as its processor has not entered the HALT State. The arbiter will not voluntarily surrender the system bus and has to be forced off by another master's bus request, the HALT State being the only exception. Additional strapping options permit other modes of operation wherein the multi-master system bus is surrendered or requested under different sets of conditions.

Priority Resolving Techniques

Since there can be many bus masters on a multi-master system bus, some means of resolving priority between bus masters simultaneously requesting the bus must be provided. The 82C89 Bus Arbiter provides several resolving techniques. All the techniques are based on a priority concept that at a given time one bus master will have priority above all the rest. There are provisions for using parallel priority resolving techniques, serial priority resolving techniques, and rotating priority techniques.

Parallel Priority Resolving

The parallel priority resolving technique uses a separate bus request line $\overline{BREQ}$ for each arbiter on the multi-master system bus, see Figure 1. Each $\overline{BREQ}$ line enters into a priority encoder which generates the binary address of the highest priority $\overline{BREQ}$ line which is active. The binary address is decoded by a decoder to select the corresponding $\overline{BPRN}$ (Bus Priority In) line to be returned to the highest priority requesting arbiter. The arbiter receiving priority ($\overline{BPRN}$ true) then allows its associated bus master onto the multi-master system bus as soon as it becomes available (i.e., the bus is no longer busy). When one bus arbiter gains priority over another arbiter it cannot immediately seize the bus, it must wait until the present bus transaction is complete. Upon completing its transaction the present bus occupant recognizes that it no longer has priority and surrenders the bus by releasing $\overline{BUSY}$. $\overline{BUSY}$ is an active low "OR" tied signal line which goes to every bus arbiter on the system bus. When $\overline{BUSY}$ goes inactive (high), the arbiter which presently has bus priority ($\overline{BPRN}$ true) then seizes the bus and pulls $\overline{BUSY}$ low to keep other arbiters off of the bus. See waveform timing diagram, Figure 2. Note that all multimaster system bus transactions are synchronized to the bus clock ($\overline{BCLK}$). This allows the parallel priority resolving circuitry or any other priority resolving scheme employed to settle.

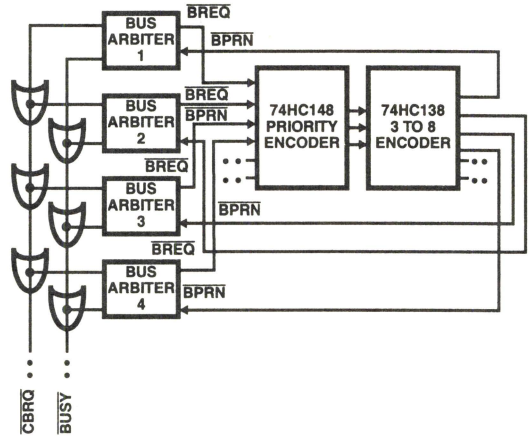


FIGURE 1. PARALLEL PRIORITY RESOLVING TECHNIQUE

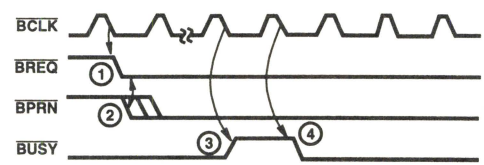


FIGURE 2. HIGHER PRIORITY ARBITER OBTAINING THE BUS FROM A LOWER PRIORITY ARBITER

NOTES:

1. Higher priority bus arbiter requests the Multi-Master system bus.
2. Attains priority.
3. Lower priority bus arbiter releases $\overline{BUSY}$.
4. Higher priority bus arbiter then acquires the bus and pulls $\overline{BUSY}$ down.

Serial Priority Resolving

The serial priority resolving technique eliminates the need for the priority encoder-decoder arrangement by daisychaining the bus arbiters together, connecting the higher priority bus arbiter's $\overline{BPRO}$ (Bus Priority Out) output to the $\overline{BPRN}$ of the next lower priority. See Figure 3.

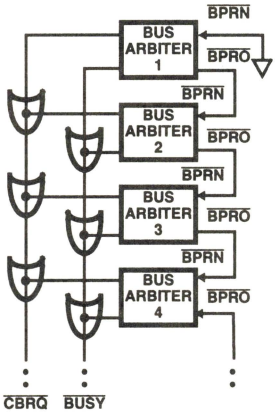


FIGURE 3. SERIAL PRIORITY RESOLVING

NOTE: The number of arbiters that may be daisy-chained together in the serial priority resolving scheme is a function of $\overline{BCLK}$ and the propagation delay from arbiter to arbiter. Normally, at 10MHz only 3 arbiters may be daisychained.

Rotating Priority Resolving

The rotating priority resolving technique is similar to that of the parallel priority resolving technique except that priority is dynamically re-assigned. The priority encoder is replaced by a more complex circuit which rotates priority between requesting arbiters thus allowing each arbiter an equal chance to use the multi-master system bus, over time.

Which Priority Resolving Technique To Use

There are advantages and disadvantages for each of the techniques described above. The rotating priority resolving technique requires substantial external logic to implement while the serial technique uses no external logic but can accommodate only a limited number of bus arbiters before the daisy-chain propagation delay exceeds the multimaster's system bus clock ($\overline{BCLK}$). The parallel priority resolving technique is in general a good compromise between the other two techniques. It allows for many arbiters to be present on the bus while not requiring too much logic to implement.

82C89 Modes Of Operation

There are two types of processors for which the 82C89 will provide support: An Input/Output processor (i.e. an NMOS 8089 IOP) and the 80C86, 80C88. Consequently, there are two basic operating modes in the 82C89 bus arbiter. One, the IOB (I/O Peripheral Bus) mode, permits the processor access to both an I/O Peripheral Bus and a multi-master system bus. The second, the RESB (Resident Bus mode), permits the processor to communicate over both a Resident Bus and a multi-master system bus. An I/O Peripheral Bus is a bus where all devices on that bus, including memory, are treated as I/O devices and are addressed by I/O commands. All memory commands are directed to another bus, the multi-master system bus. A Resident Bus can issue both memory and I/O commands, but it is a distinct and separate bus from the multi-master system bus. The distinction is that the Resident Bus has only one master, providing full availability and being dedicated to that one master.

The $\overline{IOB}$ strapping option configures the 82C89 Bus Arbiter into the $\overline{IOB}$ mode and the strapping option RESB configures it into the RESB mode. It might be noted at this point that if both strapping options are strapped false, the arbiter interfaces the processor to a multi-master system bus only (see Figure 4). With both options strapped true, the arbiter interfaces the processor to a multi-master system bus, a Resident Bus, and an I/O Bus.

In the $\overline{IOB}$ mode, the processor communicates and controls a host of peripherals over the Peripheral Bus. When the I/O Processor needs to communicate with system memory, it does so over the system memory bus. Figure 5 shows a possible I/O Processor system configuration.

The 80C86 and 80C88 processors can communicate with a Resident Bus and a multi-master system bus. Two bus controllers and only one Bus Arbiter would be needed in such a configuration as shown in Figure 6. In such a system configuration the processor would have access to memory and peripherals of both busses. Memory mapping techniques are applied to select which bus is to be accessed. The SYSB/$\overline{RESB}$ input on the arbiter serves to instruct the arbiter as to whether or not the system bus is to be accessed. The signal connected to SYSB/$\overline{RESB}$ also enables or disables commands from one of the bus controllers. A summary of the modes that the 82C89 has, along with its response to its status lines inputs, is shown in Table 1.

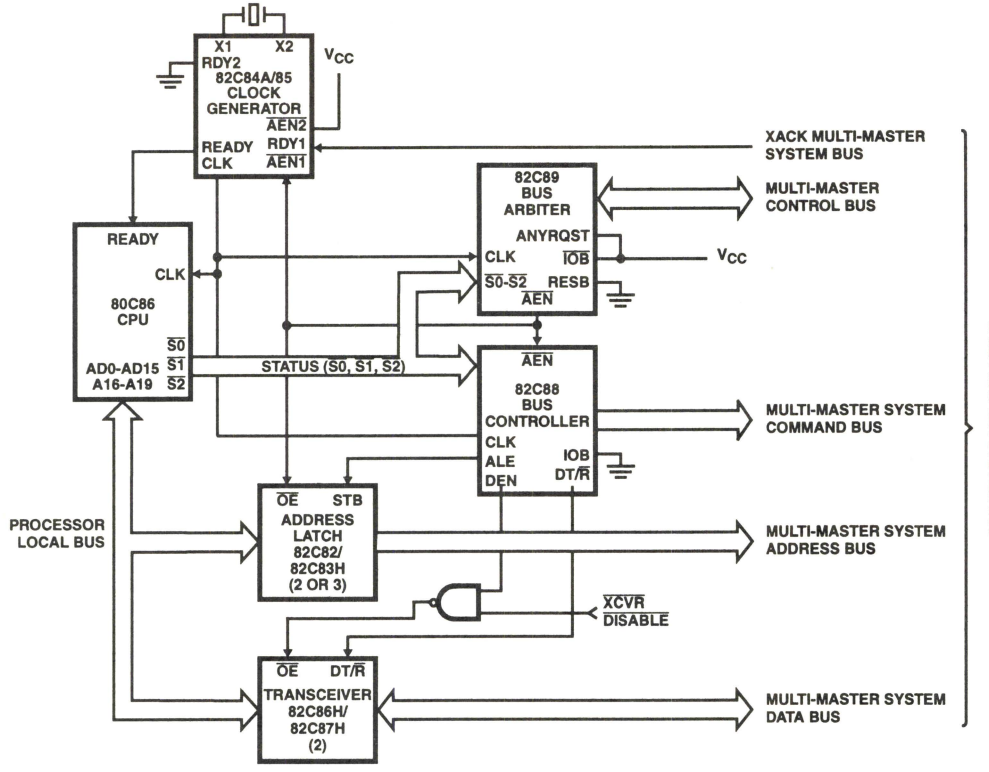


FIGURE 4. TYPICAL MEDIUM COMPLEXITY CPU SYSTEM

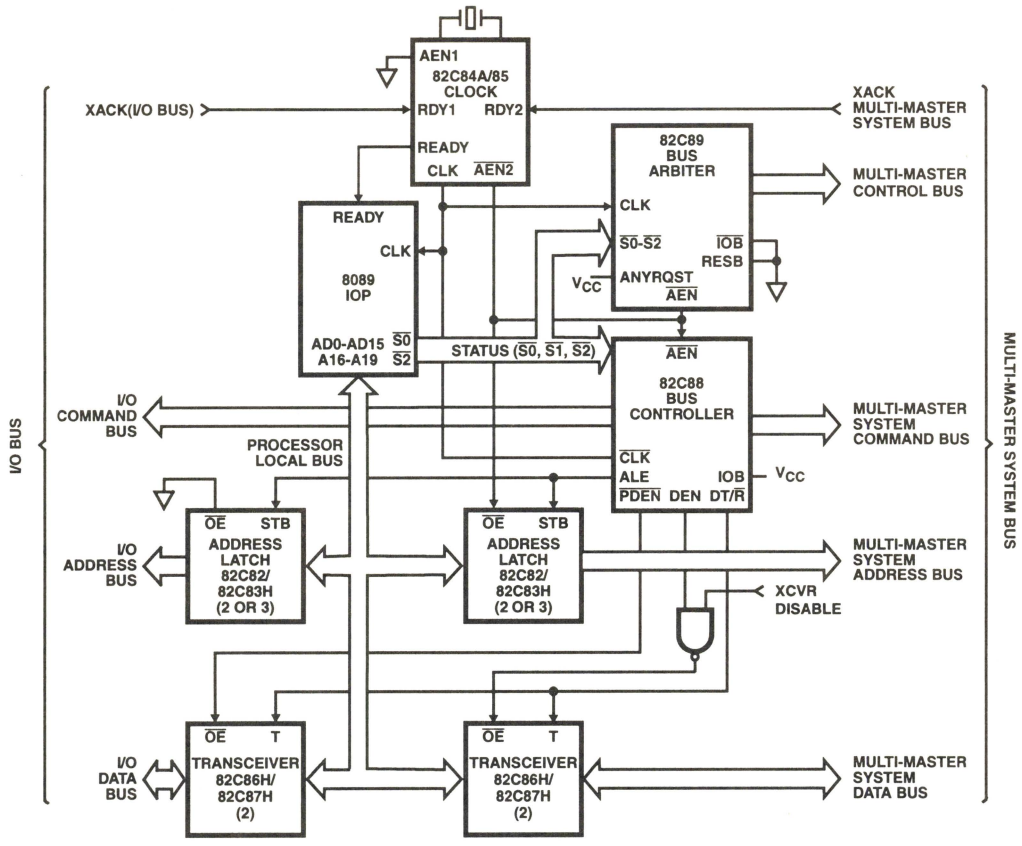


FIGURE 5. TYPICAL MEDIUM COMPLEXITY IOB SYSTEM

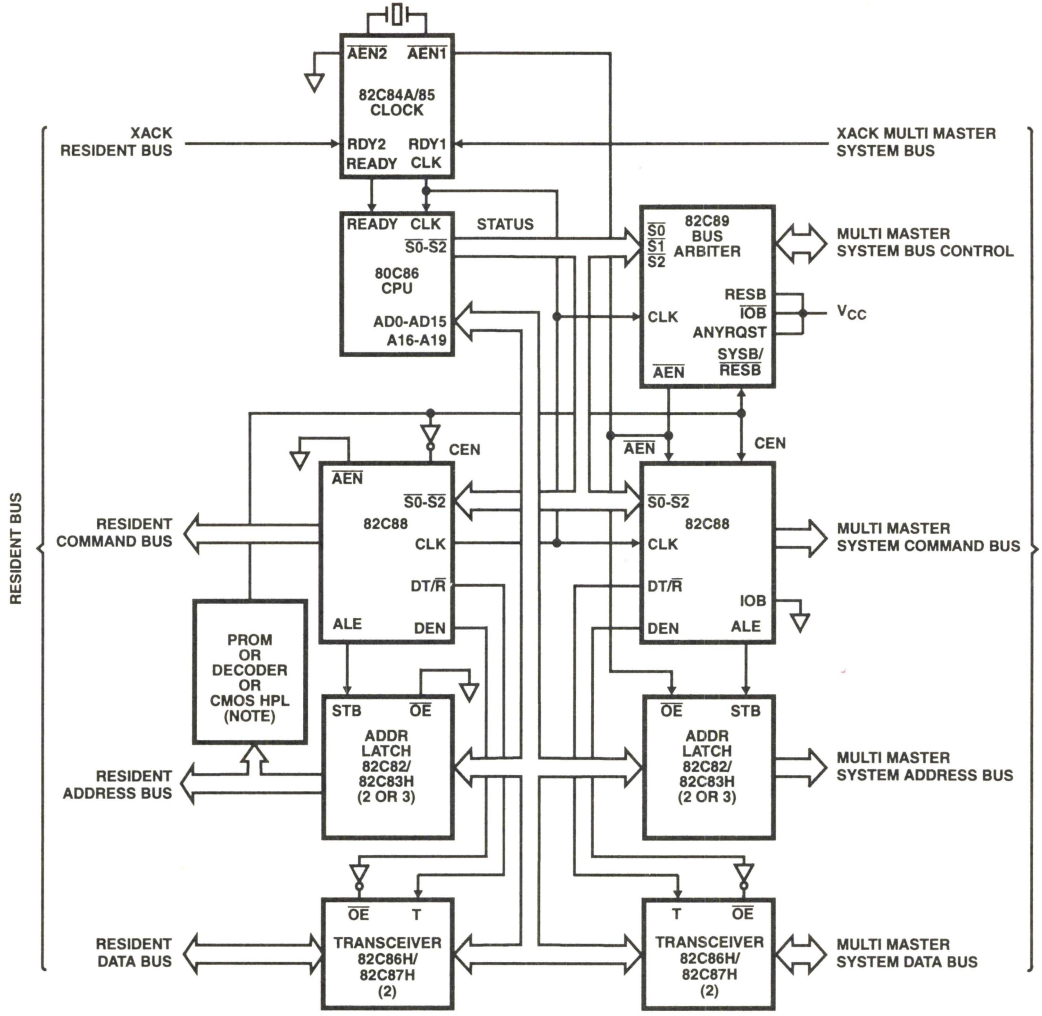


FIGURE 6. 82C89 BUS ARBITER SHOWN IN SYSTEM - RESIDENT BUS CONFIGURATION

NOTE: By adding another 82C89 arbiter and connecting its $\overline{AEN}$ to the 82C88 whose $\overline{AEN}$ is presently grounded, the processor could have access to two multi-master buses.

TABLE 1. SUMMARY OF 82C89 MODES, REQUESTING AND RELINQUISHING THE MULTI-MASTER SYSTEM BUS

SINGLE LINES FROM 80C86 OR 80C88 OR 8088				IOB MODE ONLY $\overline{IOB}$ = LOW RESB = LOW	RESB MODE ONLY $\overline{IOB}$ = HIGH, RESB = HIGH		IOB MODE RESB MODE $\overline{IOB}$ = LOW, RESB = HIGH		SINGLE BUS MODE $\overline{IOB}$ = HIGH RESB = LOW
	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$		SYSB/$\overline{RESB}$ = HIGH	SYSB/$\overline{RESB}$ = LOW	SYSB/$\overline{RESB}$ = HIGH	SYSB/$\overline{RESB}$ = LOW	
I/O Commands	0	0	0	X	†	X	X	X	†
	0	0	1	X	†	X	X	X	†
	0	1	0	X	†	X	X	X	†
Halt	0	1	1	X	X	X	X	X	X
Memory Commands	1	0	0	†	†	X	†	X	†
	1	0	1	†	†	X	†	X	†
	1	1	0†	†	†	X	†	X	†
Idle	1	1	1	X	X	X	X	X	X

NOTES:

1. X = Multi-Master System Bus is allowed to be Surrendered.
2. † = Multi-Master System Bus is Requested.

MODE	PIN STRAPPING	MULTI-MASTER SYSTEM BUS	
		REQUESTED**	SURRENDERED*
Single Bus Multi-Master Mode	$\overline{IOB}$ = High RESB = Low	Whenever the processor's status lines go active	HLT + TI • $\overline{CBRQ}$ + HPBRQ ‡
RESB Mode Only	$\overline{IOB}$ = High RESB = High	SYSB/$\overline{RESB}$ + High • ACTIVE STATUS	(SYSB/$\overline{RESB}$ = Low + TI) • $\overline{CBRQ}$ + HLT + HPBRQ
IOB Mode Only	$\overline{IOB}$ = Low RESB = Low	Memory Commands	(I/O Status + TI) • $\overline{CBRQ}$ + HLT + HPBRQ
IOB Mode RESB Mode	$\overline{IOB}$ = Low RESB = High	(Memory Command) • (SYSB/$\overline{RESB}$ = High)	(I/O Status Commands) + SYSB/$\overline{RESB}$ = Low) • $\overline{CBRQ}$ + HPBRQ + HLT

NOTES:

* $\overline{LOCK}$ prevents surrender of Bus to any other arbiter, $\overline{CRQLCK}$ prevents surrender of Bus to any lower priority arbiter.

** Except for HALT and Passive or IDLE Status.

‡ HPBRQ, Higher priority Bus request or $\overline{BPRN}$ = 1.

1. $\overline{IOB}$ Active Low.
2. RESB Active High.
3. + is read as "OR" and • as "AND"
4. TI = Processor Idle Status $\overline{S2}$, $\overline{S1}$, $\overline{S0}$ = 111
5. HLT = Processor Halt Status $\overline{S2}$, $\overline{S1}$, $\overline{S0}$ = 011

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C89 . . . . . 0°C to +70°C
I82C89 . . . . . -40°C to +85°C
M82C89 . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	80	20
CLCC Package	90	24
PDIP Package	75	N/A
PLCC Package	75	N/A

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package . . . . . +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(PLCC - Lead Tips Only)

Die Characteristics

Gate Count . . . . . 200 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5.0V ± 10%;
T_A = 0°C to +70°C (C82C89);
T_A = -40°C to +85°C (I82C89);
T_A = -55°C to +125°C (M82C89)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0 2.2	- -	V V	C82C89, I82C89 M82C89, Note 1
V_{IL}	Logical Zero Input Voltage	-	0.8	V	Note 1
VIHC	CLK Logical One Input Voltage	0.7 VCC	-	V	
VILC	CLK Logical Zero Input Voltage	-	0.2 VCC	V	
V_{OL}	Output Low Voltage $\overline{BUSY}$, $\overline{CBRQ}$ $\overline{AEN}$ $\overline{BPRO}$, $\overline{BREQ}$	 - - -	 0.45 0.45 0.45	 V V V	 I_{OL} = 20mA I_{OL} = 16mA I_{OL} = 8mA
VOH1	Output High Voltage $\overline{BUSY}$, $\overline{CBRQ}$	Open-Drain			
VOH2	Output High Voltage All Other Outputs	3.0 V_{CC} -0.4	-	V V	I_{OH} = -2.5mA I_{OH} = -100µA
II	Input Leakage Current	-1.0	1.0	µA	V_{IN} = GND or V_{CC}, DIP Pins 1-6, 9, 14-19
IO	I/O Leakage	-10.0	10.0	µA	V_O = GND or V_{CC}, DIP Pins 11-12
ICCSB	Standby Power Supply	-	10	µA	V_{CC} = 5.5V, V_{IN} = V_{CC} or GND, Outputs Open
ICCOP	Operating Power Supply Current	-	1	mA/MHz	V_{CC} = 5.5V, Outputs Open, Note 2

NOTES:

1. Does not apply to $\overline{IOB}$, RESB, or ANYRQST. These are strap options and should be held to VCC or GND.
2. Maximum current defined by CLK or BCLK, whichever has the highest operating frequency

Capacitance

T_A = +25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	10	pF	FREQ = 1MHz, all measurements are referenced to device GND
COUT	Output Capacitance	10	pF	
CIO	I/O Capacitance	15	pF	

AC Electrical Specifications

V_{CC} = 5.0V ± 10%; GND = 0V:
T_A = 0°C to +70°C (C82C89);
T_A = -40°C to +85°C (I82C89);
T_A = -55°C to +125°C (M82C89)

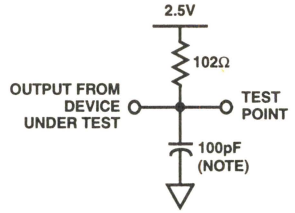
SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
(1) TCLCL	CLK Cycle Period	125	-	ns	Note 3
(2) TCLCH	CLK Low Time	55	-	ns	Note 3
(3) TCHCL	CLK High Time	35	-	ns	Note 3
(4) TSVCH	Status Active Setup	65	TCLCL-10	ns	Note 3
(5) TSHCL	Status Inactive Setup	50	TCLCL-10	ns	Note 3
(6) THVCH	Status Inactive Hold	10	-	ns	Note 3
(7) THVCL	Status Active Hold	10	-	ns	Note 3
(8) TBYSBL	$\overline{BUSY}$↓↑ Setup to $\overline{BCLK}$↓	20	-	ns	Note 3
(9) TCBSBL	$\overline{CBRQ}$↓↑ Setup to $\overline{BCLK}$↓	20	-	ns	Note 3
(10) TBLBL	$\overline{BCLK}$ Cycle Time	100	-	ns	Note 3
(11) TBHCL	$\overline{BCLK}$ High Time	30	0.65 (TBLBL)	ns	Note 3
(12) TCLLL1	$\overline{LOCK}$ Inactive Hold	10	-	ns	Note 3
(13) TCLLL2	$\overline{LOCK}$ Active Setup	40	-	ns	Note 3
(14) TPNBL	$\overline{BPRN}$↓↑ to BCLK Setup Time	20	-	ns	Note 3
(15) TCLSR1	SYSB/$\overline{RESB}$ Setup	0	-	ns	Note 3
(16) TCLSR2	SYSB/$\overline{RESB}$ Hold	30	-	ns	Note 3
(17) TIVIH	Initialization Pulse Width	675	-	ns	Note 3
(18) TBLBRL	$\overline{BCLK}$ to $\overline{BREQ}$ Delay↓↑	-	35	ns	Note 3
(19) TBLPOH	$\overline{BCLK}$ to $\overline{BPRO}$↓↑	-	35	ns	Note 1 and 3
(20) TPNPO	$\overline{BPRN}$↓↑ to $\overline{BPRO}$↓↑ Delay	-	22	ns	Note 1 and 3
(21) TBLBYL	$\overline{BCLK}$ to $\overline{BUSY}$ Low	-	60	ns	Note 3
(22) TBLBYH	$\overline{BCLK}$ to $\overline{BUSY}$ Float	-	35	ns	Note 2 and 3
(23) TCLAEH	CLK to $\overline{AEN}$ High	-	65	ns	Note 3
(24) TBLAEL	$\overline{BCLK}$ to $\overline{AEN}$ Low	-	40	ns	Note 3
(25) TBLCBL	$\overline{BCLK}$ to $\overline{CBRQ}$ Low	-	60	ns	Note 3
(26) TBLCBH	$\overline{BCLK}$ to $\overline{CBRQ}$ Float	-	40	ns	Note 2 and 3
(27) TOLOH	Output Rise Time	-	20	ns	From 0.8V to 2.0V, Note 4
(28) TOHOL	Output Fall Time	-	12	ns	From 2.0V to 0.8V, Note 4
(29) TILIH	Input Rise Time	-	20	ns	From 0.8V to 2.0V
(30) TIHIL	Input Fall Time	-	20	ns	From 2.0V to 0.8V

NOTES:

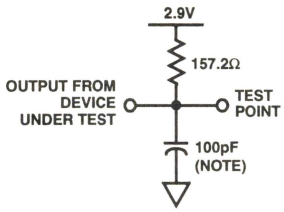
1. $\overline{BCLK}$ generates the first $\overline{BPRO}$ wherein subsequent $\overline{BPRO}$ changes lower in the chain are generated through BPRON.
2. Measured at 0.5V above GND.
3. All AC parameters tested as per AC test load circuits. Input rise and fall times are driven at 1ns/V.
4. Except $\overline{BUSY}$ and $\overline{CBRQ}$

AC Test Load Circuits

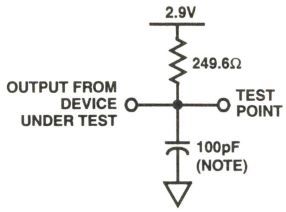
$\overline{BUSY}$, $\overline{CBRQ}$ LOAD CIRCUIT



$\overline{AEN}$ LOAD CIRCUIT



$\overline{BPRO}$, $\overline{BREQ}$ LOAD CIRCUIT



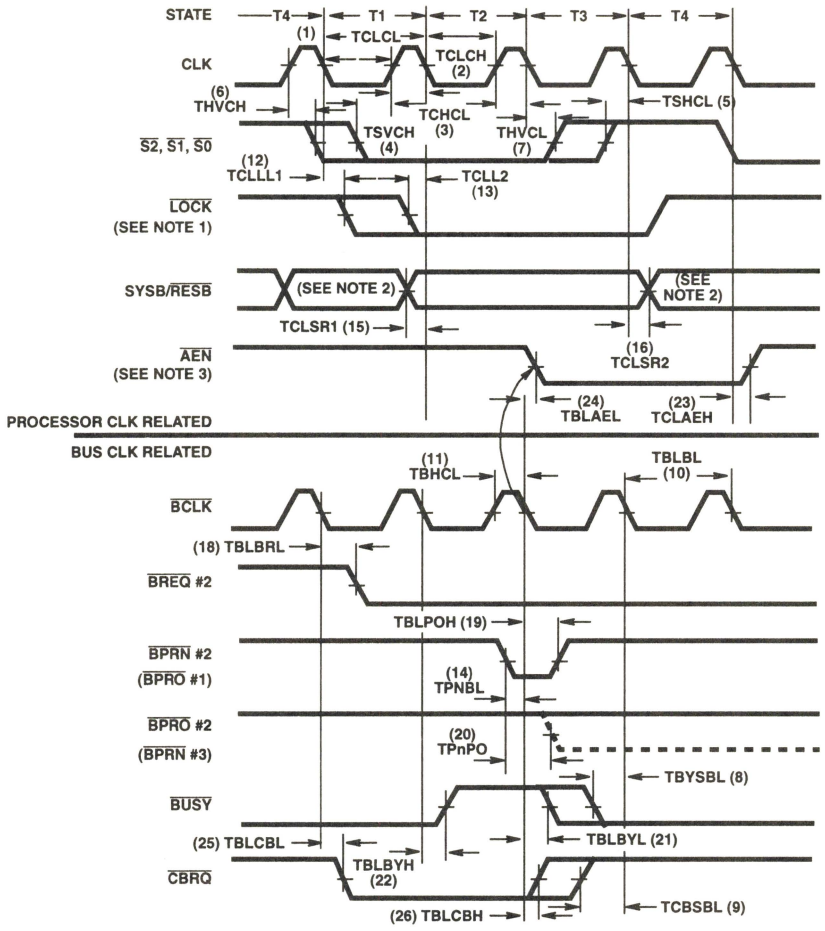
NOTE: Includes Stray and Jig Capacitance

AC Testing Input, Output Waveform



AC Testing: Inputs are driven at V_{IH} +0.4V for a logic "1" and V_{IL} -0.4V for a logic "0". The clock is driven at V_{CC} -0.4V and 0.4V. Timing measurements are made at 1.5V for both a logic "1" and "0".

Timing Waveform



NOTES:

1. LOCK active can occur during any state, as long as the relationships shown above with respect to the CLK are maintained. LOCK inactive has no critical time and can be asynchronous. CRQLCK has no critical timing and is considered an asynchronous input signal.
2. Glitching of SYSB/RESB is permitted during this time. After θ2 of T1, and before θ1 of T4, SYSB/RESB should be stable to maintain system efficiency.
3. AEN leading edge is related to BCLK, trailing edge to CLK. The trailing edge of AEN occurs after bus priority is lost.

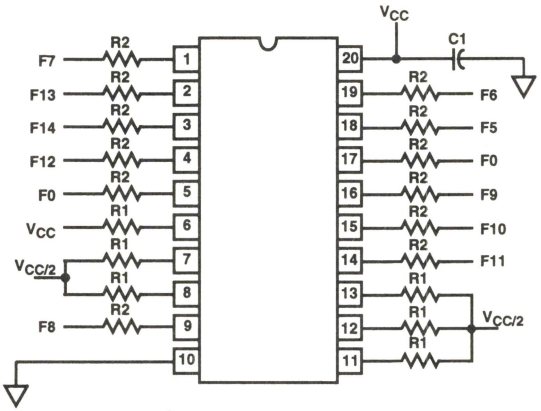
ADDITIONAL NOTES:

The signals related to CLK are typical processor signals, and do not relate to the depicted sequence of events of the signals referenced to BCLK. The signals shown related to the BCLK represent a hypothetical sequence of events for illustration. Assume 3 bus arbiters of priorities 1, 2 and 3 configured in serial priority resolving scheme (as shown in Figure 3). Assume arbiter 1 has the bus and is holding BUSY low. Arbiter #2 detects its processor wants the bus and pulls low BREQ #2. If BPRN #2 is high (as shown), arbiter #2 will pull low CBRQ line. CBRQ signals to the higher priority arbiter #1 that a lower priority arbiter wants the bus. [A higher priority arbiter would be granted BPRN when it makes the bus request rather than having to wait for another arbiter to release the bus through CBRQ]. *Arbiter #1 will relinquish the multi-master system bus when it enters a state not requiring it (see Table 1), by lowering its BPRO #1 (tied to BPRN #2) and releasing BUSY. Arbiter #2 now sees that is has priority from BPRN #2 being low and releases CBRQ. As soon as BUSY signifies the bus is available (high), arbiter #2 pulls BUSY low on next falling edge of BCLK. Note that if arbiter #2 didn't want the bus at the time it received priority, it would pass priority to the next lower priority arbiter by lowering its BPRO #2 [TPNPO].

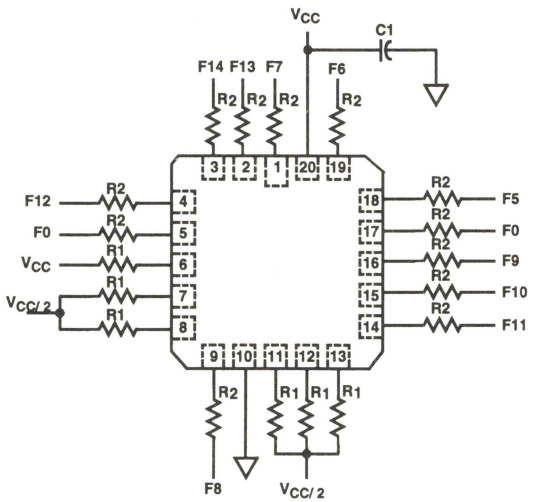
Note that even a higher priority arbiter which is acquiring the bus through BPRN will momentarily drop CBRQ until it has acquired the bus.

Burn-In Circuits

MD82C89 CERDIP



MR82C89 CLCC



NOTES:

1. V_{CC} = 5.5V ± 0.5V, GND = 0V
2. V_{IH} = 4.5V ± 10%, V_{IL} = -0.2V to +0.4V
3. Components Values:
   R1 = 1.2kΩ, 1/4W, 5%
   R2 = 47kΩ, 1/4W, 5%
   C1 = 0.01µF minimum
   F0 = 100kHz ± 10%
   F1 = F0/2
   F2 = F1/2. . . .
   F14 = F13/2

Die Characteristics

DIE DIMENSIONS:
92.9 x 95.7 x 19 ± 1mils

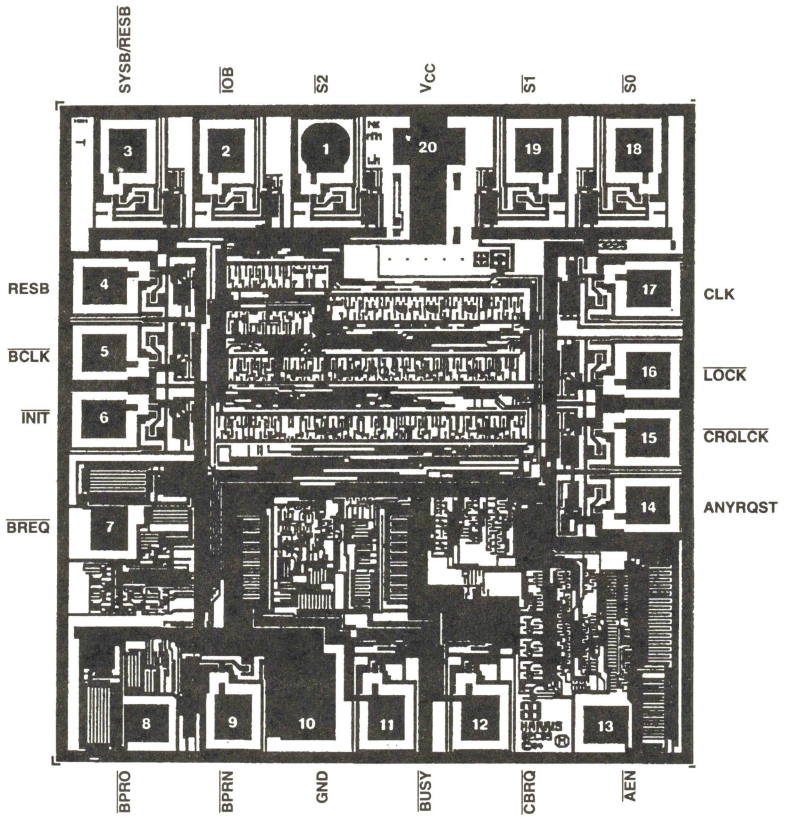
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
1.8×10^5 A/cm^2

Metallization Mask Layout

82C89



MICROPROCESSOR PRODUCTS 5

CMOS DATA COMMUNICATIONS

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HARRIS SEMICONDUCTOR

82C50A

CMOS Asynchronous Communications Element

March 1997

Features

- Single Chip UART/BRG
- DC to 625K Baud (DC to 10MHz Clock)
- Crystal or External Clock Input
- On Chip Baud Rate Generator 1 to 65535 Divisor Generates 16X Clock
- Prioritized Interrupt Mode
- Fully TTL/CMOS Compatible
- Microprocessor Bus Oriented Interface
- 80C86/80C88 Compatible
- Scaled SAJI IV CMOS Process
- Low Power - 1mA/MHz Typical
- Modem Interface
- Line Break Generation and Detection
- Loopback and Echo Modes
- Doubled Buffered Transmitter and Receiver
- Single 5V Supply

Ordering Information

PACKAGE	TEMPERATURE RANGE (^{o}C)	625K BAUD	PKG. NO.
PDIP	0 to +70	CP82C50A-5	E40.6
	-40 to +85	IP82C50A-5	E40.6
PLCC	0 to +70	CS82C50A-5	N44.65
	-40 to +85	IS82C50A-5	N44.65
CERDIP	0 to +70	CD82C50A-5	F40.6
	-40 to +85	ID82C50A-5	F40.6
	-55 to +125	MD82C50A-5/B	F40.6

Description

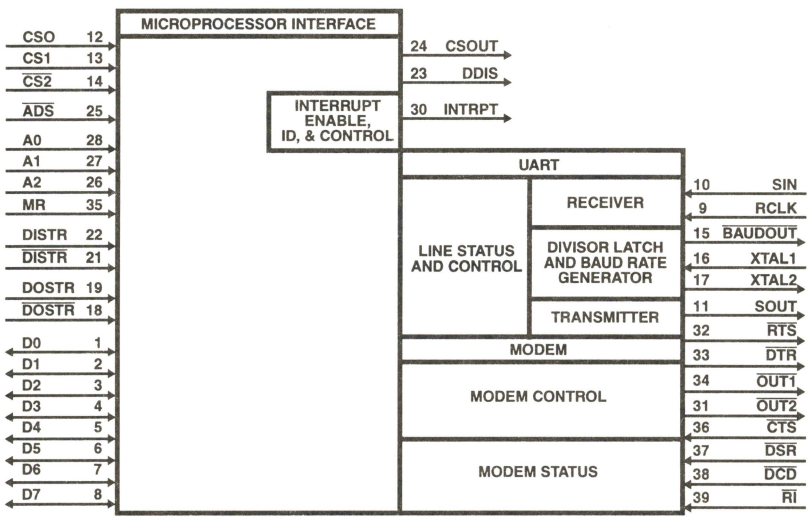
The 82C50A Asynchronous Communication Element (ACE) is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. Using Harris Semiconductor's advanced Scaled SAJI IV CMOS Process, the ACE will support data rates from DC to 625K baud (0-10MHz clock).

The ACE's receiver circuitry converts start, data, stop, and parity bits into a parallel data word. The transmitter circuitry converts a parallel data word into serial form and appends the start, parity, and stop bits. The word length is programmable to 5, 6, 7, or 8 data bits. Stop bit selection provides a choice of 1,1.5, or 2 stop bits.

The Baud Rate Generator divides the clock by a divisor programmable from 1 to 2^{16}-1 to provide standard RS-232C baud rates when using any one of three industry standard baud rate crystals (1.8432MHz, 2.4576MHz, or 3.072MHz). A programmable buffered clock output (BAUDOUT) provides either a buffered oscillator or 16X (16 times the data rate) baud rate clock for general purpose system use.

To meet the system requirements of a CPU interfacing to an asynchronous channel, the modem control signals $\overline{RTS}$, $\overline{CTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, $\overline{DCD}$ are provided. Inputs and outputs have been designed with full TTL/CMOS compatibility in order to facilitate mixed TTL/NMOS/CMOS system design.

Functional Diagram



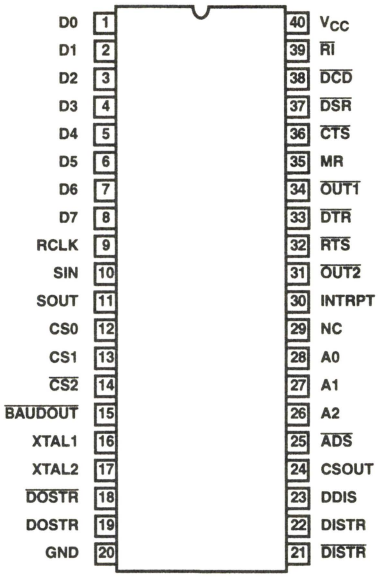
5 CMOS DATA COMMUNICATIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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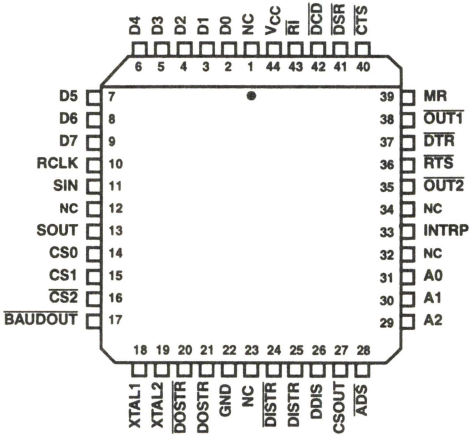
File Number **2958.1**

Pinouts

82C50A (PDIP, CERDIP)
TOP VIEW



82C50A (PLCC)
TOP VIEW



Pin Description

SYMBOL	PIN NUMBER	TYPE	ACTIVE LEVEL	DESCRIPTION
DISTR, $\overline{\text{DISTR}}$	22 21	I I	H L	DATA IN STROBE, DATA IN STROBE: DISTR, $\overline{\text{DISTR}}$ are read inputs which cause the 82C50A to output data to the data bus (D0-D7). The data output depends upon the register selected by the address inputs A0, A1, A2. The chip select inputs CS0, CS1, $\overline{\text{CS2}}$ enable the DISTR, $\overline{\text{DISTR}}$ inputs. Only an active DISTR or $\overline{\text{DISTR}}$, not both, is used to receive data from the 82C50A during a read operation. If DISTR is used as the read input, $\overline{\text{DISTR}}$ should be tied high. If $\overline{\text{DISTR}}$ is used as the active read input, DISTR should be tied low.
DOSTR, $\overline{\text{DOSTR}}$	19 18	I I	H L	DATA OUT STROBE, DATA OUT STROBE: DOSTR, $\overline{\text{DOSTR}}$ are write inputs which cause data from the data bus (D0-D7) to be input to the 82C50A. The data input depends upon the register selected by the address inputs A0, A1, A2. The chip select inputs CS0, CS1, $\overline{\text{CS2}}$ enable the DOSTR, $\overline{\text{DOSTR}}$ inputs. Only an active DOSTR or $\overline{\text{DOSTR}}$, not both, is used to transmit data to the 82C50A during a write operation. If DOSTR is used as the write input, $\overline{\text{DOSTR}}$ should be tied high. If $\overline{\text{DOSTR}}$ is used as the write input, DOSTR should be tied low.
D0-D7	1-8	I/O		DATA BITS 0-7: The Data Bus provides eight, three-state input/output lines for the transfer of data, control and status information between the 82C50A and the CPU. For character formats of less than 8 bits, D7, D6 and D5 are "don't cares" for data write operations and 0 for data read operations. These lines are normally in a high impedance state except during read operations. D0 is the Least Significant Bit (LSB) and is the first serial data bit to be received or transmitted.
A0, A1, A2	28, 27, 26	I I	H	REGISTER SELECT: The address lines select the internal registers during CPU bus operations. See Table 1.
XTAL1, XTAL2	16 17	I O		CRYSTAL/CLOCK: Crystal connections for the internal Baud Rate Generator. XTAL1 can also be used as an external clock input, in which case XTAL2 should be left open.
SOUT	11	O		SERIAL DATA OUTPUT: Serial data output from the 82C50A transmitter circuitry. A Mark (1) is a logic one (high) and Space (0) is a logic zero (low). SOUT is held in the Mark condition when the transmitter is disabled, MR is true, the Transmitter Register is empty, or when in the Loop Mode. SOUT is not affected by the $\overline{\text{CTS}}$ input.
GND	20		L	GROUND: Power supply ground connection (V_{SS}).
$\overline{\text{CTS}}$	36	I	L	CLEAR TO SEND: The logical state of the $\overline{\text{CTS}}$ pin is reflected in the CTS bit of the (MSR) Modem Status Register (CTS is bit 4 of the MSR, written MSR (4)). A change of state in the $\overline{\text{CTS}}$ pin since the previous reading of the MSR causes the setting of DCTS (MSR(O)) of the Modem Status Register. When $\overline{\text{CTS}}$ pin is ACTIVE (low), the modem is indicating that data on SOUT can be transmitted on the communications link. If $\overline{\text{CTS}}$ pin goes INACTIVE (high), the 82C50A should not be allowed to transmit data out of SOUT. $\overline{\text{CTS}}$ pin does not affect Loop Mode operation.
$\overline{\text{DSR}}$	37	I	L	DATA SET READY: The logical state of the $\overline{\text{DSR}}$ pin is reflected in MSR(5) of the Modem Status Register. DDSR (MSR(1)) indicates whether the $\overline{\text{DSR}}$ pin has changed state since the previous reading of the MSR. When the $\overline{\text{DSR}}$ pin is ACTIVE (low), the modem is indicating that it is ready to exchange data with the 82C50A, while the $\overline{\text{DSR}}$ Pin INACTIVE (high) indicates that the modem is not ready for data exchange. The ACTIVE condition indicates only the condition of the local Data Communications Equipment (DCE), and does not imply that a data circuit as been established with remote equipment.
$\overline{\text{DTR}}$	33	O	L	DATA TERMINAL READY: The $\overline{\text{DTR}}$ pin can be set (low) by writing a logic 1 to MCR(0), Modem Control Register bit 0. This signal is cleared (high) by writing a logic 0 to the DTR bit (MCR(0)) or whenever a MR ACTIVE (high) is applied to the 82C50A. When ACTIVE (low), $\overline{\text{DTR}}$ pin indicates to the DCE that the 82C50A is ready to receive data. In some instances, $\overline{\text{DTR}}$ pin is used as a power on indicator. The INACTIVE (high) state causes the DCE to disconnect the modem from the telecommunications circuit.

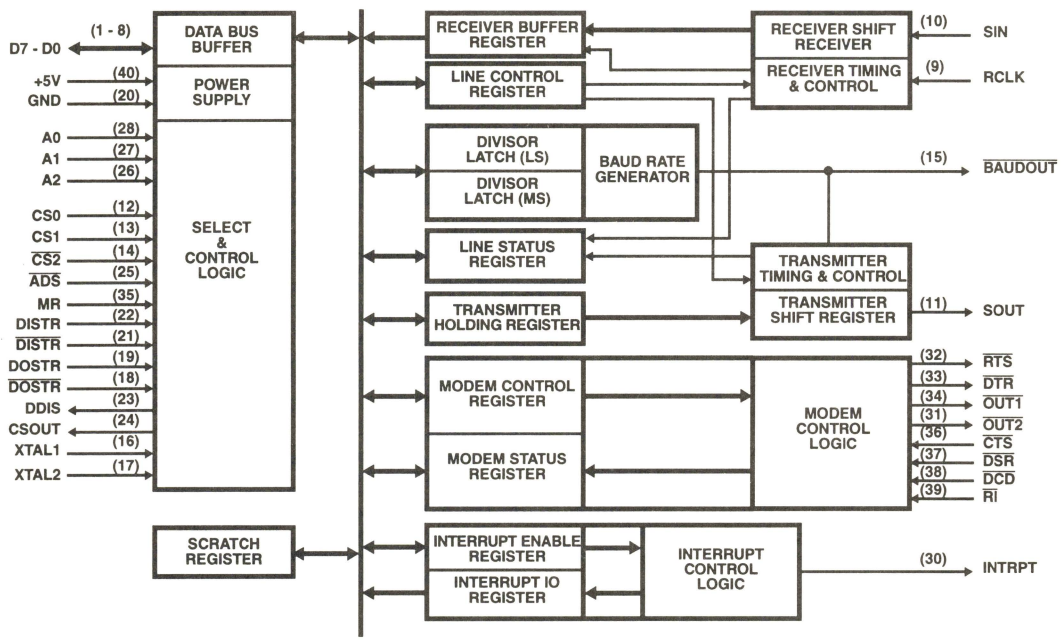
Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	ACTIVE LEVEL	DESCRIPTION
$\overline{RTS}$	32	O	L	REQUEST TO SEND: The $\overline{RTS}$ signal is an output used to enable the modem. The $\overline{RTS}$ pin is set low by writing a logic 1 to MCR (1) bit 1 of the Modem Control Register. The $\overline{RTS}$ pin is reset high by Master Reset. When ACTIVE, the $\overline{RTS}$ pin indicates to the DCE that the 82C50A has data ready to transmit. In half duplex operations, $\overline{RTS}$ is used to control the direction of the line.
$\overline{BAUDOUT}$	15	O		BAUDOUT: This output is a 16X clock out used for the transmitter section (16X = 16 times the data rate). The $\overline{BAUDOUT}$ clock rate is equal to the reference oscillator frequency divided by the specified divisor in the Baud Rate Generator Divisor Latches DLL and DLM. $\overline{BAUDOUT}$ may be used by the Receiver section by tying this output to RCLK.
$\overline{OUT1}$	34	O	L	OUTPUT 1: This is a general purpose output that can be programmed ACTIVE (low) by settingVCR(2) (OUT1) of the Modem Control Register to a high level. The $\overline{OUT1}$ pin is set high by Master Reset. The $\overline{OUT1}$ pin is INACTIVE (high) during loop mode operation.
$\overline{OUT2}$	31	O	L	OUTPUT 2: This is a general purpose output that can be programmed ACTIVE (low) by setting MCR(3) (OUT1) of the Modem Control Register to a high level. The $\overline{OUT2}$ pin is set high by Master Reset. The $\overline{OUT2}$ signal is INACTIVE (high) during loop mode operation.
$\overline{RI}$	39	I	L	RING INDICATOR: When low, $\overline{RI}$ indicates that a telephone ringing signal has been received by the modem or data set. The $\overline{RI}$ signal is a modem control input whose condition is tested by reading MSR(6) (RI). The Modem Status Register output TERI (MSR(2)) indicates whether the $\overline{RI}$ input has changed from a Low to High since the previous reading of the MSR. If the interrupt is enabled (IER (3) = 1) and $\overline{RI}$ changes from a Low to High, an interrupt is generated. The ACTIVE (low) state of $\overline{RI}$ indicates that the DCE is receiving a ringing signal. $\overline{RI}$ will appear ACTIVE for approximately the same length of time as the ACTIVE segment of the ringing cycle. The INACTIVE state of $\overline{RI}$ will occur during the INACTIVE segments not detected by the DCE. This circuit is not disabled by the INACTIVE condition of $\overline{DTR}$.
$\overline{DCD}$	38	I	L	DATA CARRIER DETECT: When ACTIVE (low), $\overline{DCD}$ indicates that the data carrier has been detected by the modem or data set. $\overline{DCD}$ is a modem input whose condition can be tested by the CPU by reading MSR(7) (DCD) of the Modem Status Register. MSR(3) (DDCD) of the Modem Status Register indicates whether the $\overline{DCD}$ input has changed since the previous reading of the MSR. $\overline{DOD}$ has no effect on the receiver. If the $\overline{DCD}$ changes state with the modem status interrupt enabled, an interrupt is generated. When $\overline{DCD}$ is ACTIVE (low), the received line signal from the remote terminal is within the limits specified by the DCE manufacturer. The INACTIVE (high) signal indicates that the signal is not within the specified limits, or is not present.
MR	35	I	H	MASTER RESET: The MR input forces the 82C50A into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. The 82C50A remains in an idle state until programmed to resume serial data activities. The MR input is a Schmitt trigger input. See the DC Electrical Characteristics for Schmitt trigger logic input voltage levels. See Table 7 for a summary of Master Reset's effect on 82C50A operation.
INTRPT	30	O	H	INTERRUPT REQUEST: The INTRPT output goes ACTIVE (high) when one of the following interrupts has an ACTIVE (high) condition and is enabled by the Interrupt Enable Register: Receiver Error flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. The INTRPT is reset low upon appropriate service or a MR operation. See Figure 1. Interrupt Control Structure.
SIN	10	I	H	SERIAL DATA INPUT: The SIN input is the serial data input from the communication line or modem to the 82C50A receiver circuits. A mark (1) is high, and a space (0) is low. Data inputs on SIN are disabled when operating in the loop mode.

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	ACTIVE LEVEL	DESCRIPTION
V_{CC}	40		H	V_{CC}: +5V positive power supply pin. A 0.1µA decoupling capacitor from V_{CC} (pin 40) to GND (pin 20) is recommended.
CS0, CS1, $\overline{CS2}$	12,13, 14	I I	H, H, L	CHIP SELECT: The Chip Select inputs act as enable signals for the write (DOSTR, $\overline{DOSTR}$) and read (DISTR, $\overline{DISTR}$) input signals. The Chip Select inputs are latched by the $\overline{ADS}$ input.
NC	29			Do Not Connect
CSOUT	24	O	H	CHIP SELECT OUT: When ACTIVE (high), this pin indicates that the chip has been selected by active CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until CSOUT is a logic 1, ACTIVE (high).
DDIS	23	O	H	DRIVER DISABLE: This output is INACTIVE (low) when the CPU is reading data from the 82C50A. An ACTIVE (high) Dells output can be used to disable an external transceiver when the CPU is reading data.
$\overline{ADS}$	25	I	L	ADDRESS STROBE: When ACTIVE (low), $\overline{ADS}$ latches the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) inputs. An active $\overline{ADS}$ is required when the Register Select pins are not stable for the duration of the read or write operation, multiplexed mode. If not required, the $\overline{ADS}$ input should be tied low, non-multiplexed mode.
RCLK	9	I		This input is the 16X Baud Rate Clock for the receiver section of the 82C50A. This input may be provided from the $\overline{BAUDOUT}$ output or an external clock.

Block Diagram



Accessible Registers

The three types of internal registers in the 82C50A used in the operation of the device are control, status, and data registers. The control registers are the Bit Rate Select Register DLL and DLM, Line Control Register, Interrupt Enable Register and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register (LCR(7)) to select the register to be written or read (see Table 1.). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example, LCR(7) refers to Line Control Register Bit 7.

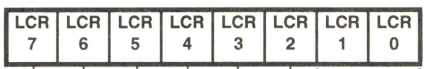
The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from 5-8 data bits. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The 82C50A data registers are double buffered so that read and write operations can be performed at the same time the UART is performing the parallel to serial and serial to parallel conversion. This provides the microprocessor with increased flexibility in its read and write timing.

TABLE 1. ACCESSING 82C50A INTERNAL REGISTERS

DLAB	A2	A1	A0	MNEMONIC	REGISTER
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

NOTE: X = "Don't Care", 0 = Logic Low, 1 = Logic High

Line Control Register (LCR)



Word Length Select	0 0 = 5 Data Bits 0 1 = 6 Data Bits 1 0 = 7 Data Bits 1 1 = 8 Data Bits
Stop Bit Select	0 = 1 Stop Bit 1 = 1.5 Stop Bits if 5 Data Bit Word Length is Selected 2 Stop Bits if 6, 7, or 8 Data Bit Word Length is Selected
Parity Enable	0 = Parity Disabled 1 = Parity Enabled (Generated & Checked)
Even Parity Select	0 = Odd Parity When Parity is Enabled 1 = Even Parity When Parity is Enabled
Stick Parity	0 = Stick Parity Disabled 1 = When Parity is Enabled Forces the Transmission and Checking of a Parity Bit of a Known State. Parity Bit Forced to a Logic 1 if LCR (4) = 0 or to a Logic 0 If LCR (4) = 1.
Break Control	0 = Break Disabled 1 = Break Enabled. The Serial Output (SOUT) is Forced to the Spacing (Logic 0) State.
Divisor Latch Access Bit	0 = Must be Low to Access the Receiver Buffer. Transmitter Holding Register or the Interrupt Enable Register. 1 = Must be High to Access the Divisor Latches DLL and DLM of the Baud Rate Generator During a Read or Write Operation.

LINE CONTROL REGISTER (LCR)

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described below.

LCR Bits 0 thru 7

LCR (0) Word Length Select Bit 0 (WLS0)
LCR (1) Word Length Select Bit 1 (WLS1)
LCR (2) Stop Bit Select (STB)
LOR (3) Parity Enable (PEN)
LCR (4) Even Parity Select (EPS)
LOR (5) Stick Parity
LOR (6) Set Break
LCR (7) Divisor Latch Access Bit (DLAB)

LCR(0) and LCR(1) Word Length Select Bit 0, Word Length Select Bit 1: The number of bits in each transmitted or received serial character is programmed as follows:

LCR(1)	LCR(0)	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. If LCR(2) is a logic 0, one stop bit is generated in the transmitted data. If LCR(2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR(2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR(3) Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select: When parity is enabled (LCR(3) = 1), LCR(4) = 0 selects odd parity, and LCR(4) = 1 selects even parity.

LCR(5) Stick Parity: When parity is enabled (LCR(3) = 1), LCR(5) = 1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by LCR(4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to logic-1, the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR(6) to a logic-0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all Os pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored.

During the break, the transmitter can be used as a character timer to accurately establish the break duration.

LCR(7) Divisor Latch Access Bit (DLAB): LCR(7) must be set high (logic 1) to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR(7) must be input low to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

LINE STATUS REGISTER (LSR)

The LSR is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the 82C50A.

Three error flags OE, FE, and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurred. The Overrun Error (OE) indicates that a character in the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The character is lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received contained a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character, with the entire character, including parity and stop bits, logic zero.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and ready to receive another character. The Transmission Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty, and the 82C50A has completed transmission of the last character. If the interrupt is enabled (IER(1)), an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Reading the LSR clears LSR (1) - LSR (4). (OE, PE, FE and BI).

LSR BITS 0 THRU 7

		LOGIC 1	LOGIC 0
LSR	(0) Data Ready (DR)	Ready	Not Ready
LSR	(1) Overrun Error (OE)	Error	No Error
LSR	(2) Parity Error (PE)	Error	No Error
LSR	(3) Framing Error (FE)	Error	No Error
LSR	(4) Break Interrupt (BI)	Break	No Break
LSR	(5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR	(6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR	(7) Not Used		

The contents of the Line Status Register are indicated in the above table and are described below.

LSR(0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR(0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR (4)). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The B indicator is reset when the CPU reads the contents of the Line Status Register.

LSR(1) - LSR(4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER (2) = 1 in the Interrupt Enable Register.

LSR(5) Transmitter Holding Register Empty (THRE): THRE indicates that the 82C50A is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled (IER(1) = 1), THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR(7): This bit is permanently set to logic 0.

MODEM CONTROL REGISTER (MCR)

The MCR controls the interface with the modem or data set as described below. The MCR can be written and read. The $\overline{RTS}$, $\overline{DTR}$, $\overline{OUT1}$ and $\overline{OUT2}$ outputs are directly controlled by their control bits in this register. **A high input asserts a low (true) at the output pins.**

MCR BITS 0 THRU 7

		MCR BIT LOGIC 1	MCR BIT LOGIC 0
MCR	(0) Data Terminal Ready (DTR)	$\overline{DTR}$ Output Low	$\overline{DTR}$ Output High
MCR	(1) Request to Send (RTS)	$\overline{RTS}$ Output Low	$\overline{RTS}$ Output High
MCR	(2) OUT1	$\overline{OUT1}$ Output Low	$\overline{OUT1}$ Output High
MCR	(3) OUT2	$\overline{OUT2}$ Output Low	$\overline{OUT2}$ Output High
MCR	(4) LOOP	LOOP Enabled	LOOP Disabled
MCR	(5) 0		
MCR	(6) 0		
MCR	(7) 0		

MCR(0): When MCR(0) is set high, the $\overline{DTR}$ output is forced low. When MCR(0) is reset low, the $\overline{DTR}$ output is forced high. The $\overline{DTR}$ output of the 82C50A may be input into an EIA inverting line driver as the 1488 to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the $\overline{RTS}$ output is forced low. When MCR(1) is reset low, the $\overline{RTS}$ output is forced high. The $\overline{RTS}$ output of the 82C50A may be input into an EIA inverting line driver as the 1488 to obtain the proper polarity input at the modem or data set.

MCR(2): When MCR(2) is set high, the $\overline{OUT1}$ output is forced low. When MCR(2) is reset low, the $\overline{OUT1}$ output is forced high. $\overline{OUT1}$ is an user designated output.

MCR(3): When MCR(3) is set high, the $\overline{OUT2}$ output is forced low. When MCR(3) is reset low, the $\overline{OUT2}$ output is forced high. $\overline{OUT2}$ is an user designated output.

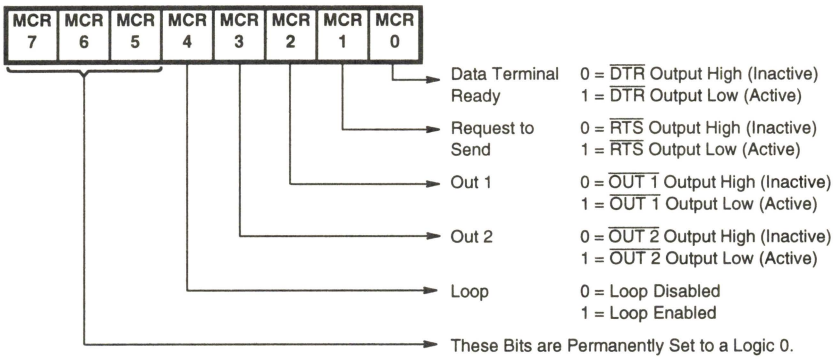
MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the 62C50A. When MCR(4) is set high,

Serial Output (SOUT) is set to the marking (logic 1) state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, DC, and $\overline{RI}$) are disconnected. The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$ and $\overline{OUT2}$) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high). In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the 82C50A.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the interrupt sources are now the lower four bits of the MCR instead of the four modem control inputs. The interrupts are still controlled by the Interrupt Enable Register.

MCR(5) - MCR(7): These bits are permanently set to logic 0.

Modem Control Register (MCR)



MODEM STATUS REGISTER (MSR)

The MSR provides the CPU with status of the modem input lines from the modem or peripheral device. The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the 82C50A. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines are $\overline{CTS}$ (pin 36), $\overline{DSR}$ (pin 37), $\overline{RI}$ (pin 39), and $\overline{DCD}$ (pin 38). MSR(4) - MSR(7) are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled (IER(3)), a change of state in a modem input signals will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described below:

Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

MSR BITS 0 THRU 7

MSR BIT	MNEMONIC	DESCRIPTION
MSR (1)	DDSR	Delta Data Set Ready
MSR (2)	TERI	Trailing Edge of Ring Indicator
MSR (0)	DCTS	Delta Clear To Send
MSR (3)	DDCD	Delta Data Carrier Detect
MSR (4)	CTS	Clear To Send
MSR (5)	DSR	Data Set Ready
MSR (6)	RI	Ring Indicator
MSR (7)	DCD	Data Carrier Detect

MSR(0) Delta Clear to Send (DCTS): DCTS indicates that the $\overline{CTS}$ input (Pin-36) to the 82C50A has changed state since the last time it was read by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the $\overline{DSR}$ input (Pin-37) to the 62C50A has changed state since the last time it was read by the CPU.

MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the $\overline{RI}$ input (Pin-39) to the 82C50A has Changed state from Low to High since the last time it was read by the CPU. High to Low transitions on $\overline{RI}$ do not activate TERI.

MSR(3) Delta Data Carrier Detect (DDCD): DDCD indicates that the $\overline{DCD}$ input (Pin-36) to the 82C50A has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS): Clear to Send (CTS) is the status of the $\overline{CTS}$ input (Pin-36) from the modem indicating to the 82C50A that the modem is ready to receive data from the 62C50A transmitter output (SOUT). If the 82C50A is in

the loop mode (MCR(4)=1), MSR(4) is equivalent to RTS in the MCR.

MSR(5) Data Set Ready (DSR): Data Set Ready (DSR) is a status of the $\overline{DSR}$ input (Pin-37) from the modem to the 82C50A which indicates that the modem is ready to provide received data to the 82C50A receiver circuitry. If the 82C50A is in the loop mode (MCR(4) = 1), MSR(5) is equivalent to DTR in the MCR.

MSR(6) Ring Indicator MSR(6): Indicates the status of the RI input (Pin-39). If the 82C50A is in the loop mode (MCR(4) = 1), MSR(6) is equivalent to OUT1 in the MCR.

MSR(7) Data Carrier Detect (MSR(7)): Data Carrier Detect indicates the status of the Data Carrier Detect ($\overline{DCD}$) input (Pin-38). If the 82C50A is in the loop mode (MCR(4) = 1), MSR(4) is equivalent to OUT2 of the MCR.

The modem status inputs (RI, DCD, DSR and CTS) reflect the modem input lines with any change of status. **Reading the MSR register will clear the delta modem status indications but has no effect on the status bits.** The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI, or DDCD are true and a state change occurs during a read operation (DISTR, $\overline{DISTR}$), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DDCD are false and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read (DISTR, $\overline{DISTR}$) operations. If a status condition is generated during a read (DISTR, $\overline{DISTR}$) operation, the status bit is not set until the trailing edge of the read (DISTR, $\overline{DISTR}$).

If a status bit is set during a read (DISTR, $\overline{DISTR}$) operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read (DISTR, $\overline{DISTR}$) instead of being set again.

BAUD RATE SELECT REGISTER (BRSR)

The 82C50A contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 10MHz) by any divisor from 1 to 2^{16}-1 (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = frequency input ÷ (baud rate x 16)]. **Two 8-bit divisor latch registers store the divisor in a 16-bit binary format.** These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Sample Divisor Number Calculation:

Given: Desired Baud Rate 1200 Baud
Frequency Input 1.8432MHz

Formula: Divisor # = Frequency Input ÷ (Baud Rate x 16)
Divisor # = 1843200 ÷ (1200 x 16)

Answer: Divisor # = 96 = 60_{HEX} → DLL = 01100000
DLM = 00000000

Check: The Divisor # 96 will divide the input frequency 1.8432MHz down to 19200 which is 16 times the desired baud rate.

Divisor Latch Least Significant BYTE

DLL (0)	Bit 0
DLL (1)	Bit 1
DLL (2)	Bit 2
DLL (3)	Bit 3
DLL (4)	Bit 4
DLL (5)	Bit 5
DLL (6)	Bit 6
DLL (7)	Bit 7

Divisor Latch Most Significant BYTE

DLM (0)	Bit 8
DLM (1)	Bit 9
DLM (2)	Bit 10
DLM (3)	Bit 11
DLM (4)	Bit 12
DLM (5)	Bit 13
DLM (6)	Bit 14
DLM (7)	Bit 15

RECEIVER BUFFER REGISTER (RBR)

The receiver circuitry in the 82C50A is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit (LSB = Data Bit 0 (RBR(0)). Data Bit 0 of a data word (RBR(0)) is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the 82C50A.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the 82C50A, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character result in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

RBR Bits 0 thru 7

RBR (0)	Data Bit 0
RBR (1)	Data Bit 1
RBR (2)	Data Bit 2
RBR (3)	Data Bit 3
RBR (4)	Data Bit 4
RBR (5)	Data Bit 5
RBR (6)	Data Bit 6
RBR (7)	Data Bit 7

TRANSMITTER HOLDING REGISTER (THR)

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 (THR(0)) is the first serial data bit transmitted. The THRE flag (LSR(5)) reflect the status of the THR. The TEMT flag (LSR(6)) indicates if both the THR and TSR are empty.

THR Bits 0 thru 7

THR (0)	Data Bit 0
THR (1)	Data Bit 1
THR (2)	Data Bit 2
THR (3)	Data Bit 3
THR (4)	Data Bit 4
THR (5)	Data Bit 5
THR (6)	Data Bit 6
THR (7)	Data Bit 7

SCRATCHPAD REGISTER (SCR)

This 8-bit Read/Write register has no effect on the 82C50A. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

SCR Bits 0 thru 7

SCR (0)	Data Bit 0
SCR (1)	Data Bit 1
SCR (2)	Data Bit 2
SCR (3)	Data Bit 3
SOR (4)	Data Bit 4
SCR (5)	Data Bit 5
SOR (6)	Data Bit 6
SCR (7)	Data Bit 7

Interrupt Structure

INTERRUPT IDENTIFICATION REGISTER (IIR)

The 82C50A has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the 82C50A prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (Priority 1)
2. Received Data Ready (Priority 2)
3. Transmitter Holding Register Empty (Priority 3)
4. Modem Status (Priority 4).

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 2 and are described below.

IIR(0): IIR(0) can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending, and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When IIR(0) is high, no interrupt is pending.

IIR(1) and IIR(2): IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 2.

IIR(3) - IIR(7): These five bits of the IIR are logic 0.

TABLE 2. INTERRUPT IDENTIFICATION REGISTER

INTERRUPT IDENTIFICATION				INTERRUPT SET AND RESET FUNCTIONS		
BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT FLAG	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Receiver Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	Fourth	Modem Status	$\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, $\overline{DCD}$	MSR Read

NOTE: X = Not Defined, May Be 0 or 1

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) is a Write register used to independently enable the four 82C50A interrupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER(0) - IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and

Modem Status Registers. The contents of the Interrupt Enable Register are indicated in Table 3 and are described below.

IER(0): When programmed high (IER(0) = Logic 1), IER(0) enables Received Data Available interrupt.

IER(1): When programmed high (IER(1) = Logic 1), IER(1) enables the Transmitter Holding Register Empty interrupt.

IER(2): When Programmed high (IER(2) = Logic 1), IER(2) enables the Receiver Line Status interrupt.

IER(3): When programmed high (IER(3) = Logic 1), IER(3) enables the Modem Status interrupt.

IER(4) - IER(7): These four bits of the IER are logic 0.

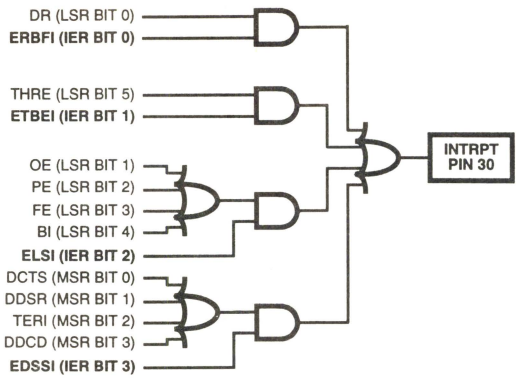


FIGURE 1. 82C50A INTERRUPT CONTROL STRUCTURE

TABLE 3. 82C50A ACCESSIBLE REGISTER SUMMARY
(NOTE: See Table 1 for how to access these registers.)

REGISTER MNEMONIC	REGISTER BIT NUMBER							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)†
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" 1F Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request to Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Set Ready	(CTS) Clear to Send	(DDCD) Delta Data Carrier Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

†LSB, Data Bit 0 is the first bit transmitted or received.

Transmitter

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5-8 bit word, the word is written through D0-D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, both THRE and TEMT are high. The first word written causes THRE to be reset to 0. After completion of the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed transmission of the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSR transfer time later.

Receiver

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid bit sample of the start bit. Verifying the start bit prevents the receiver from assembling an incorrect data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR(0), LCR(1)), number of stop bits LCR(2), if parity is used LCR(3), and the polarity of parity LCR(4). Status information for the receiver is provided in the Line Status Register. When a character is transferred from the Receiver Shift Register to the Receiver Buffer Register, the Data Received indication in LSR(0) is set high. The CPU reads the Receiver Buffer Register through D0-D7. This read resets LSR(0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR (2). There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR(3).

The center of the start bit is defined as clock count 7 1/2. If the data into SIN is a symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

Baud Rate Generator (BRG)

The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG may be provided either with the addition of an external crystal to the XTAL1 and XTAL2 inputs, or an external clock into XTAL1. In either case, a buffered clock output, $\overline{\text{BAUDOUT}}$, is provided for other system clocking. If two 82C50As are used on the same board, one can use a crystal, and the buffered clock output can be routed directly into the XTAL1 of the second 82C50A.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency or crystal input, with the $\overline{\text{BAUDOUT}}$ providing an output 16X the data rate. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL = 1 and DLM = 0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at XTAL1). The on-chip oscillator is optimized for a 10MHz crystal. Usually, higher frequency are less expensive than lower frequency crystals.

The BRG can use any of three different popular crystals to provide standard baud rates. The frequency of these three common crystals on the market are 1.8432MHz, 2.4576MHz, and 3.072MHz. With these standard crystals, standard bit rates from 50 to 38.5kbps are available. The following tables illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

TABLE 4. BAUD RATES USING 1.8432MHz CRYSTAL

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

TABLE 5. BAUD RATES USING 2.4576MHz CRYSTAL

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3072	-
75	2048	-
110	1396	0.026
134.5	1142	0.0007
150	1024	-
300	512	-
600	256	-
1200	128	-
1800	85	0.392
2000	77	0.260
2400	64	-
3600	43	0.775
4800	32	-
7200	21	1.587
9600	16	-
19200	8	-
38400	4	-

TABLE 6. BAUD RATES USING 3.072MHz CRYSTAL

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

Reset

After powerup, the 82C50A Master Reset Schmitt trigger input (MR) should be held high for TMRW ns to reset the 82C50A circuits to an idle mode until initialization. A high on MR causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TE MT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not effected.

Following removal of the reset condition (MR low), the 82C50A remains in the idle mode until programmed.

A hardware reset of the 82C50A sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a Master Reset on the 82C50A is given in Table 7.

TABLE 7. 82C50A RESET OPERATIONS

REGISTER/SIGNAL	RESET CONTROL	RESET
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 are High
MODEM Status Register	Master Reset	Bit 0-3 Low Bits 4-7 Input Signal
SOUT	Master Reset	High
Intrpt (RCVR Errs)	Read LSR/MR	Low
Intrpt (RCVR Data Ready)	Read RBR/MR	Low
Intrpt (THRE)	Read IIR/Write THR/MR	Low
Intrpt (Modem Status Changes)	Read MSR/MR	Low

TABLE 7. 82C50A RESET OPERATIONS (Continued)

REGISTER/SIGNAL	RESET CONTROL	RESET
$\overline{Out2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{Out1}$	Master Reset	High

Programming

The 82C50A is programmed by the control registers LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control registers can be written in any order, the IER should be written to last because it controls the interrupt enables. Once the 82C50A is programmed and operational, these registers can be updated any time the 82C50A is not transmitting or receiving data.

The control signals required to access 82C50A internal registers are shown below.

Software Reset

A software reset of the 82C50A is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

Crystal Operation

The 82C50A crystal oscillator circuitry is designed to operate with a fundamental mode, parallel resonant crystal. Table 8 shows the required crystal parameters and crystal circuit configuration, respectively.

When using an external clock source, the XTAL1 input is driven and the XTAL2 output is left open. Power consumption when using an external clock is typically 50% of that required when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

The maximum frequency of the 82C50A is 10MHz with an external clock or a crystal attached to XTAL1 and XTAL2. Using the external clock or crystal, and a divide by one divisor, the maximum $\overline{BAUDOUT}$ is 10MHz, and the maximum data rate is 625Kbps.

TABLE 8. TYPICAL CRYSTAL OSCILLATOR CIRCUIT

PARAMETER	
Frequency	1.0 to 10MHz
Type of Operation	Parallel Resonant, Fundamental Mode
Load Capacitance (CL)	20 or 32pF (Typ)
R_{SERIES} (Max)	100Ω (f = 10MHz, CL = 32pF) 200Ω (f = 10MHz, CL = 20pF)

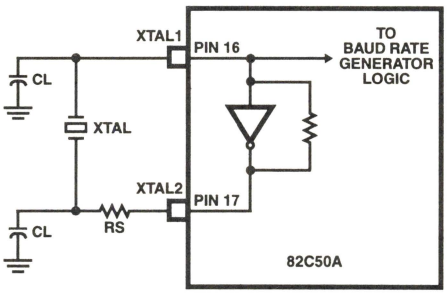


FIGURE 2. TYPICAL CRYSTAL OSCILLATOR CIRCUIT

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C50A-5 . . . . . 0^oC to $+70^oC$
I82C50A-5 . . . . . -40^oC to $+85^oC$
M82C50A-5 . . . . . -55^oC to $+125^oC$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	35	10
Plastic DIP Package	50	N/A
Plastic LCC Package	46	N/A

Maximum Junction Temperature
Ceramic Package . . . . . $+175^oC$
Plastic Package . . . . . $+150^oC$
Max Storage Temperature Range . . . . . -65^oC to $+150^oC$
Max Lead Temperature (Soldering 10s) . . . . . $+300^oC$
(Lead Tips Only for Surface Mount Packages)

Die Characteristics

Gate Count . . . . . 1788 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 5.0V ±10%, T_A = 0^oC to $+70^oC$ (C82C50A-5)
T_A = -40^oC to $+85^oC$ (I82C50A-5)
T_A = -55^oC to $+125^oC$ (M82C50A-5)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0	-	V	I82C50A-5, C82C50A-5
		2.2	-	V	M82C50A-5
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
VTH	Schmitt Trigger Logic One Input Voltage	2.0	-	V	MR Input 82C50A-5, C82C50A-5
		2.2	-	V	M82C50A-5
VTL	Schmitt Trigger Logic Zero Input Voltage	-	0.8	V	MR Input
VIH (CLK)	Logical One Clock Voltage	V_{CC}-0.8	-	V	External Clock
VIL (CLK)	Logical Zero Clock Voltage	-	0.8	V	External Clock
V_{OH}	Output High Voltage	3.0	-	V	I_{OH} = -2.5mA
		V_{CC}-0.4	-	V	I_{OH} = -100µA
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = +2.5mA,
II	Input Leakage Current	-1.0	+1.0	µA	V_{IN} = GND or V_{CC}, DIP Pins 9,10,12, 13, 14, 18, 19, 21, 22, 25-28, 35-39
IO	Input/Output Leakage Current	-10.0	+10.0	µA	V_O = GND or V_{CC}, DIP Pins 1-8
ICCOP	Operating Power Supply Current	-	6	mA	External Clock F = 2.4576MHz, V_{CC} = 5.5V, V_{IN} = V_{CC} or GND, Outputs Open
ICCSB	Standby Supply Current	-	100	µA	V_{CC} = 5.5V, V_{IN} = V_{CC} or GND, Outputs Open

Capacitance

T_A = 25^oC

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	15	pF	FREQ = 1MHz, all measurements are referenced to device GND
COUT	Output Capacitance	15	pF	
CI/O	I/O Capacitance	20	pF	

AC Electrical Specifications

V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C (C82C50A-5)
T_A = -40°C to +85°C (I82C50A-5)
T_A = -55°C to +125°C (M82C50A-5)

Timing Requirements

SYMBOL		PARAMETER	82C50A-5 MIN	82C50A-5 MAX	UNITS	TEST CONDITIONS
(1)	TAW	Address Strobe Width	50	-	ns	
(2)	TAS	Address Setup Time	60	-	ns	Note 1
(3)	TAH	Address Hold Time	0	-	ns	
(4)	TCS	Chip Select Setup Time	60	-	ns	Note 1
(5)	TCH	Chip Select Hold Time	0	-	ns	
(6)	TDIW	DISTR $\overline{\text{DISTR}}$ Strobe Width	150	-	ns	
(7)	TRC	Read Cycle Delay	270	-	ns	Note 1
(8)	RC	Read Cycle = TAR + TDIW + TRC	500	-	ns	
(9)	TDD	DISTR $\overline{\text{DISTR}}$ to Driver Disable Delay	-	75	ns	
(10)	TDDD	Delay From DISTR $\overline{\text{DISTR}}$ to Data	-	120	ns	
(11)	THZ	DISTR $\overline{\text{DISTR}}$ to Floating Data Delay	10	75	ns	
(12)	TDOW	DOSTR $\overline{\text{DOSTR}}$ Strobe Width	150	-	ns	
(13)	TWC	Write Cycle Delay	270	-	ns	Note 1
(14)	WC	Write Cycle = TAW + TDOW + TWC	500	-	ns	
(15)	TDS	Data Setup Time	90	-	ns	
(16)	TDH	Data Hold Time	60	-	ns	

NOTE:

1. "When using the 82C50A in the multiplexed mode ($\overline{\text{ADS}}$ operational), it will operate in 80C86/88 systems with a maximum 3MHz operating frequency."

AC Electrical Specifications

V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C (C82C50A-5)
T_A = -40°C to +85°C (I82C50A-5)
T_A = -55°C to +125°C (M82C50A-5)

Timing

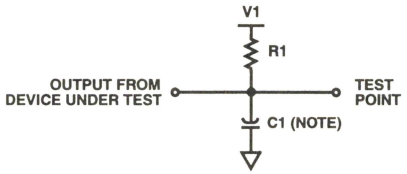
SYMBOL		PARAMETER	82C50A-5 MIN	82C50A-5 MAX	UNITS	TEST CONDITIONS
DEMULTIPLEXED OPERATION						
(17)	TCSC	Chip Select Output Delay from Select	-	125	ns	
(18)	TRA	Address Hold Time from DISTR $\overline{\text{DISTR}}$	20	-	ns	
(19)	TRCS	Chip Select Hold Time from DISTR $\overline{\text{DISTR}}$	20	-	ns	
(20)	TAR	DISTR $\overline{\text{DISTR}}$ Delay from Address	80	-	ns	
(21)	TCSR	DISTR $\overline{\text{DISTR}}$ Delay from Chip Select	80	-	ns	
(22)	TWA	Address Hold Time from DOSTR $\overline{\text{DOSTR}}$	20	-	ns	
(23)	TWCS	Chip Select Hold Time from DOSTR $\overline{\text{DOSTR}}$	20	-	ns	
(24)	TAW	DOSTR $\overline{\text{DOSTR}}$ Delay from Address	80	-	ns	
(25)	TCSW	DOSTR $\overline{\text{DOSTR}}$ Delay from Select	80	-	ns	
(26)	TMRW	Master Reset Pulse Width	500	-	ns	
(27)	TXH	Duration of Clock High Pulse	40	-	ns	
(28)	TXL	Duration of Clock Low Pulse	40		ns	

AC Electrical Specifications V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C (C82C50A-5)
T_A = -40°C to +85°C (I82C50A-5)
T_A = -55°C to +125°C (M82C50A-5)

Timing (Continued)

SYMBOL		PARAMETER	82C50A-5 MIN	82C50A-5 MAX	UNITS	TEST CONDITIONS
BAUD GENERATOR						
(29)	N	Baud Divisor	1	2^{16}-1		
(30)	TBLD	Baud Output Negative Edge Delay	-	250	ns	
(31)	TBHD	Baud Output Positive Edge Delay	-	250	ns	
(32)	TLW	Baud Output Down Time	40	-	ns	T_{XL} = 50ns
(33)	THW	Baud Output Up Time	40	-	ns	T_{XH} = 50ns
RECEIVER						
(34)	TSCD	Delay from RCLK to Sample Time	-	250	ns	
(35)	TSINT	Delay from Stop to Set Interrupt	1	1	$\overline{\text{BAUDOUT}}$ Cycles	
(36)	TRINT	Delay from DISTR $\overline{\text{DISTR}}$ (RD RBR) to Reset Interrupt	-	250	ns	
TRANSMITTER						
(37)	THR	Delay from DOSTR $\overline{\text{DOSTR}}$ to Reset Interrupt	-	250	ns	
(38)	TIRS	Delay from Initial INTR Reset to Transmit Start	8	24	$\overline{\text{BAUDOUT}}$ Cycles	
(39)	TS1	Delay from Initial Write to Interrupt	16	32	$\overline{\text{BAUDOUT}}$ Cycles	
(40)	TSTI	Delay from Stop to Interrupt (THRE)	8	24	$\overline{\text{BAUDOUT}}$ Cycles	
(41)	TIR	Delay from DISTR $\overline{\text{DISTR}}$ (RD IIR) to Reset Interrupt (THRE)	-	250	ns	
MODEM CONTROL						
(42)	TMDO	Delay from DOSTR $\overline{\text{DOSTR}}$ to Output	-	500	ns	
(43)	TSIM	Delay to Set Interrupt from Modem Input	-	500	ns	
(44)	TRIM	Delay to Reset Interrupt from DISTR $\overline{\text{DISTR}}$ (RD MSR)	-	500	ns	

AC Test Circuit



NOTE: Includes stay and jig capacitance.

TEST CONDITION DEFINITION TABLE

IOH	IOL	V1	R1	C1
-2.5mA	+2.5mA	1.7V	520Ω	100pF

AC Testing Input, Output Waveform



AC Testing: All input signals must switch between V_{IL} -0.4V and V_{IH} +0.4V. Input rise and fall times are driven at 1ns/V.

Timing Waveforms

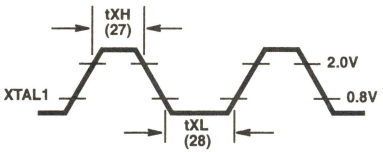


FIGURE 3. EXTERNAL CLOCK INPUT

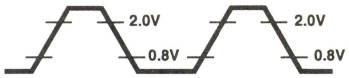
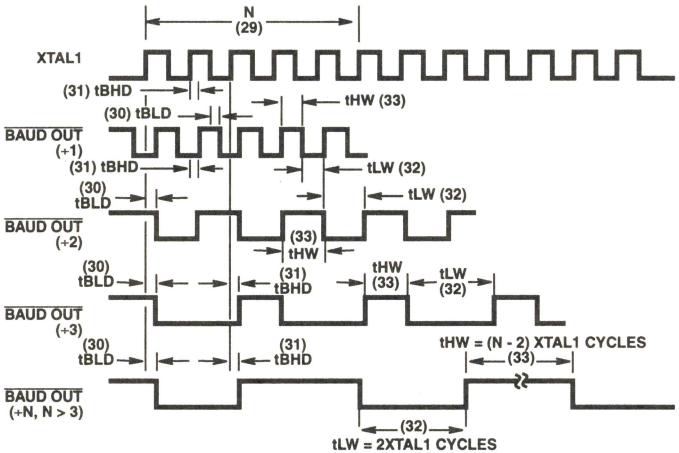


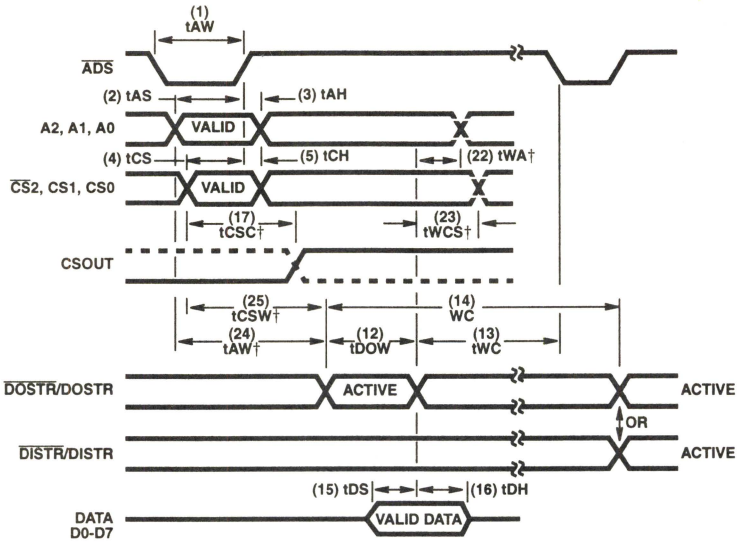
FIGURE 4. AC TEST POINTS



NOTE: tBLD (÷1) is the only spec measure from XTL1 falling edge. All other tBLD's and tBHD's are measured from XTAL1 rising edge.

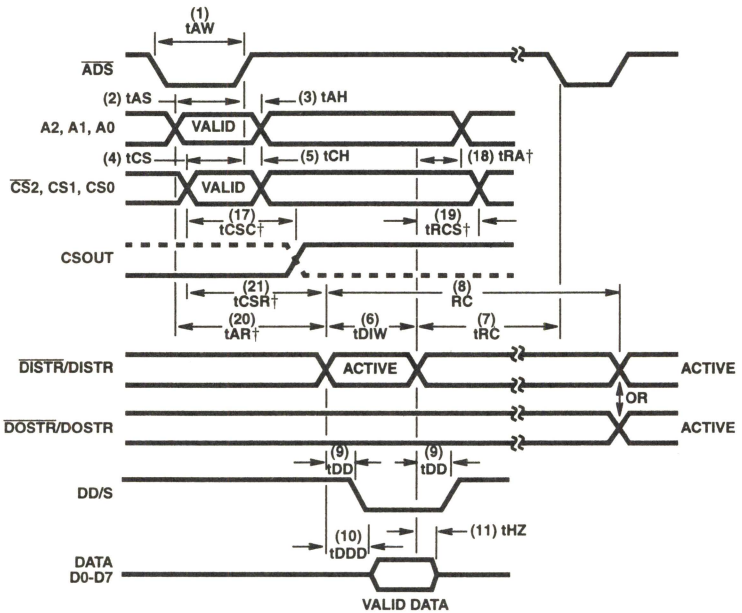
FIGURE 5. $\overline{\text{BAUDOUT}}$ TIMING

Timing Waveforms (Continued)



† Applicable only when $\overline{ADS}$ is tied low.

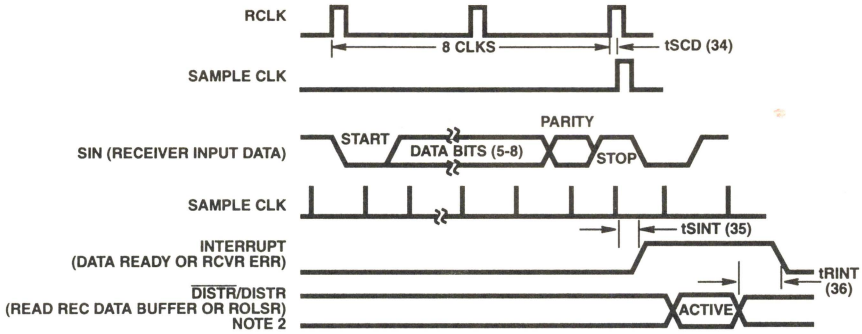
FIGURE 6. WRITE CYCLE



† Applicable only when $\overline{ADS}$ is tied low.

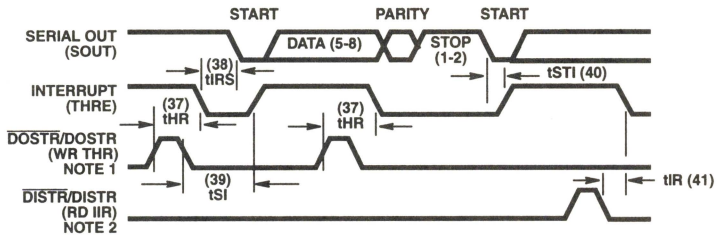
FIGURE 7. READ CYCLE

Timing Waveforms (Continued)



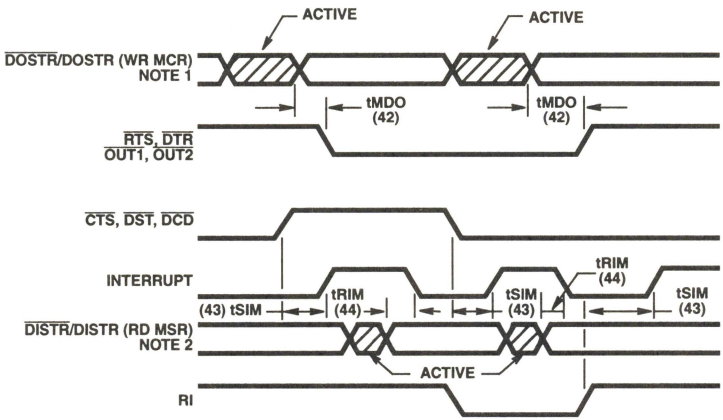
NOTES:
1. See Write Cycle Timing.
2. See Read Cycle Timing.

FIGURE 8. RECEIVER TIMING



NOTES:
1. See Write Cycle Timing.
2. See Read Cycle Timing.

FIGURE 9. TRANSMITTER TIMING



NOTES:
1. See Write Cycle Timing.
2. See Read Cycle Timing.

FIGURE 10. MODEM CONTROLS TIMING

HARRIS SEMICONDUCTOR

82C52

March 1997

CMOS Serial Controller Interface

Features

- Single Chip UART/BRG
- DC to 16MHz (1M Baud) Operation
- Crystal or External Clock Input
- On-Chip Baud Rate Generator - 72 Selectable Baud Rates
- Interrupt Mode with Mask Capability
- Microprocessor Bus Oriented Interface
- 80C86 Compatible
- Single +5V Power Supply
- Low Power Operation . . . . . 1mA/MHz Typ
- Modem Interface
- Line Break Generation and Detection
- Operating Temperature Range:
  - C82C52 . . . . . $0^{o}C$ to $+70^{o}C$
  - I82C52 . . . . . $-40^{o}C$ to $+85^{o}C$
  - M82C52 . . . . . $-55^{o}C$ to $+125^{o}C$

Description

The Harris 82C52 is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. Utilizing the Harris advanced Scaled SAJI IV CMOS process, the 82C52 will support data rates up to 1M baud asynchronously with a 16X clock (16MHz clock frequency).

The on-chip Baud Rate Generator can be programmed for any one of 72 different baud rates using a single industry standard crystal or external frequency source. A unique pre-scale divide circuit has been designed to provide standard RS-232-C baud rates when using any one of three industry standard crystals (1.8432MHz, 2.4576MHz, or 3.072MHz).

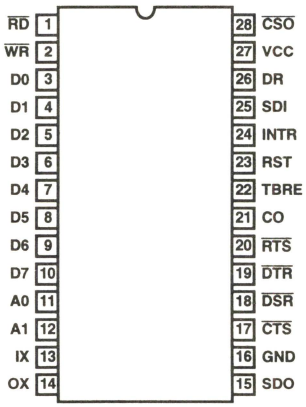
A programmable buffered clock output (CO) is available and can be programmed to provide either a buffered oscillator or 16X baud rate clock for general purpose system usage.

Ordering Information

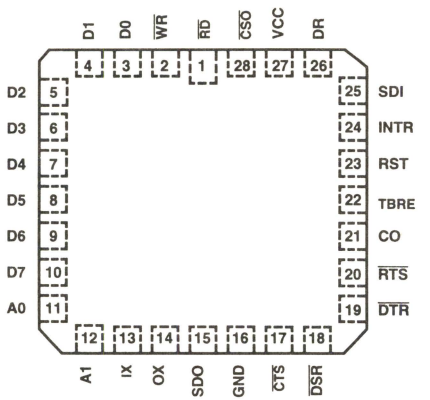
PACKAGE	TEMPERATURE RANGE	1M BAUD	PKG. NO.
PDIP	$0^{o}C$ to $+70^{o}C$	CP82C52	E28.6
	$-40^{o}C$ to $+85^{o}C$	IP82C52	E28.6
PLCC	$0^{o}C$ to $+70^{o}C$	CS82C52	N28.45
	$-40^{o}C$ to $+85^{o}C$	IS82C52	N28.45
CERDIP	$0^{o}C$ to $+70^{o}C$	CD82C52	F28.6
	$-40^{o}C$ to $+85^{o}C$	ID82C52	F28.6
	$-55^{o}C$ to $+125^{o}C$	MD82C52/B	F28.6
SMD#		8501501XA	F28.6
CLCC	$-55^{o}C$ to $+125^{o}C$	MR82C52/B	J28.A
SMD#		85015013A	J28.A

Pinouts

82C52 (PDIP, CERDIP)
TOP VIEW



82C52 (PLCC, CLCC)
TOP VIEW

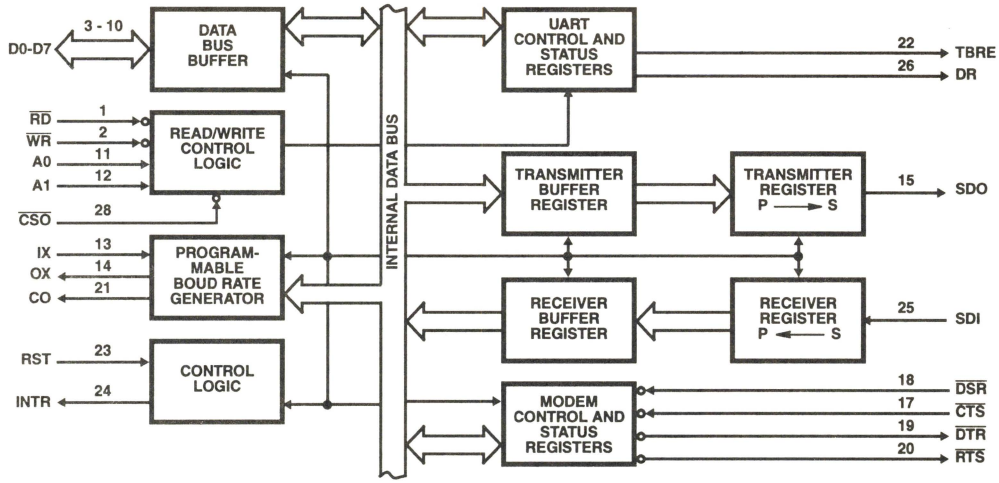


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2950.1**

Block Diagram



Pin Description

SYMBOL	PIN NO.	TYPE	ACTIVE LEVEL	DESCRIPTION
$\overline{RD}$	1	I	Low	READ: The $\overline{RD}$ input causes the 82C52 to output data to the data bus (D0-D7). The data output depends upon the state of the address inputs (A0-A1). $\overline{CS0}$ enables the $\overline{RD}$ input.
$\overline{WR}$	2	I	Low	WRITE: The $\overline{WR}$ input causes data from the data bus (D0-D7) to be input to the 82C52. Addressing and chip select action is the same as for read operations.
D0-D7	3-10	I/O	High	DATA BITS 0-7: The Data Bus provides eight, three-state input/output lines for the transfer of data, control and status information between the 82C52 and the CPU. For character formats of less than 8 bits, the corresponding D7, D6 and D5 are considered "don't cares" for data WRITE operations and are 0 for data READ operations. These lines are normally in a high impedance state except during read operations. D0 is the Least Significant Bit (LSB) and is the first serial data bit to be received or transmitted.
A0, A1	11, 12	I	High	ADDRESS INPUTS: The address lines select the various internal registers during CPU bus operations.
IX, OX	13, 14	I/O		CRYSTAL/CLOCK: Crystal connections for the internal Baud Rate Generator. IX can also be used as an external clock input in which case OX should be left open.
SDO	15	O	High	SERIAL DATA OUTPUT: Serial data output from the 82C52 transmitter circuitry. A Mark (1) is a logic one (high) and Space (0) is logic zero (low). SD0 is held in the Mark condition when $\overline{CTS}$ is false, when RST is true, when the Transmitter Register is empty, or when in the Loop Mode.
GND	16		Low	GROUND: Power supply ground connection.
$\overline{CTS}$	17	I	Low	CLEAR TO SEND: The logical state of the $\overline{CTS}$ line is reflected in the $\overline{CTS}$ bit of the Modem Status Register. Any change of state in $\overline{CTS}$ causes INTR to be set true when INTEN and MIEN are true. A false level on $\overline{CTS}$ will inhibit transmission of data on the SD0 output and will hold SD0 in the Mark (high) state. If $\overline{CTS}$ goes false during transmission, the current character being transmitted will be completed. $\overline{CTS}$ does not affect Loop Mode operation.

Pin Description (Continued)

SYMBOL	PIN NO.	TYPE	ACTIVE LEVEL	DESCRIPTION
$\overline{DSR}$	18	I	Low	DATA SET READY: The logical state of the $\overline{DSR}$ line is reflected in the Modem Status Register. Any change of state of $\overline{DSR}$ will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the 82C52.
$\overline{DTR}$	19	O	Low	DATA TERMINAL READY: The $\overline{DTR}$ signal can be set (low) by writing a logic 1 to the appropriate bit in the Modem Control Register (MCR). This signal is cleared (high) by writing a logic 0 in the $\overline{DTR}$ bit in the MCR or whenever a reset (RST = high) is applied to the 82C52.
$\overline{RTS}$	20	O	Low	REQUEST TO SEND: The $\overline{RTS}$ signal can be set (low) by writing a logic 1 to the appropriate bit in the MCR. This signal is cleared (high) by writing a logic 0 to the $\overline{RTS}$ bit in the MCR or whenever a reset (RST = high) is applied to the 82C52.
CO	21	O		CLOCK OUT: This output is user programmable to provide either a buffered IX output or a buffered Baud Rate Generator (16X) clock output. The buffered IX (Crystal or external clock source) output is provided when the Baud Rate Select Register (BRSR) bit 7 is set to a zero. Writing a logic one to BRSR bit 7 causes the CO output to provide a buffered version of the internal Baud Rate Generator clock which operates at sixteen times the programmed baud rate. On reset D7 (CO select) is reset to 0.
TBRE	22	O	High	TRANSMITTER BUFFER REGISTER EMPTY: The TBRE output is set (high) whenever the Transmitter Buffer Register (TBR) has transferred its data to the Transmit Register. Application of a reset (RST) to the 82C52 will also set the TBRE output. TBRE is cleared (low) whenever data is written to the TBR.
RST	23	I	High	RESET: The RST input forces the 82C52 into an "Idle" mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The UART Status Register (USR) is cleared except for the TBRE and TC bits, which are set. The 82C52 remains in an "Idle" state until programmed to resume serial data activities. The RST input is a Schmitt triggered input.
INTR	24	O	High	INTERRUPT REQUEST: The INTR output is enabled by the INTEN bit in the Modem Control Register (MCR). The MIEN bit selectively enables modem status changes to provide an input to the INTR logic. Figure 9 in Design Information shows the overall relationship of these interrupt control signals.
SDI	25	I	High	SERIAL DATA INPUT: Serial data input to the 82C52 receiver circuits. A Mark (1) is high, and a Space (0) is low. Data inputs on SDI are disabled when operating in the loop mode or when RST is true.
DR	26	O	High	DATA READY: A true level indicates that a character has been received, transferred to the RBR, and is ready for transfer to the CPU. DR is reset on a data READ of the Receiver Buffer Register (RBR) or when RST is true.
V_{CC}	27		High	V_{CC}: +5V positive power supply pin. A 0.1µF decoupling capacitor from V_{CC} (Pin 27) to GND (Pin 16) is recommended.
$\overline{CS0}$	28	I	Low	CHIP SELECT: The chip select input acts as an enable signal for the $\overline{RD}$ and $\overline{WR}$ input signals.

Reset

During and after power-up, the 82C52 Reset Input (RST) must be held high for at least two IX clock cycles in order to initialize and drive the 82C52 circuits to an idle mode until proper programming can be done. A high on RST causes the following events to occur

- Resets the internal Baud Rate Generator (BRG) circuit clock counters and bit counters. The Baud Rate Select Register (BRSR) is not affected (except for bit 7 which is reset to 0).
- Clears the UART Status Register (USR) except for Transmission Complete (TC) and Transmit Buffer Register Empty (TBRE) which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. Note that the UART Control Register (UCR) is not affected.

Following removal of the reset condition (RST = low), the 82C52 remains in the idle mode until programmed to its desired system configuration.

Programming The 82C52

The complete functional definition of the 82C52 is programmed by the systems software. A set of control words (UCR, BRSR and MCR) must be sent out by the CPU to initialize the 82C52 to support the desired communication format. These control words will program the character length, number of stop bits, even/odd/no parity, baud rate, etc. Once programmed, the 82C52 is ready to perform its communication functions.

The control registers can be written to in any order. However, the MCR should be written to last because it controls the interrupt enables, modem control outputs and the receiver enable bit. Once the 82C52 is programmed and operational, these registers can be updated any time the 82C52 is not immediately transmitting or receiving data.

Table 1. Shows the control signals required to access 82C52 internal registers.

UART Control Register (UCR)

The UCR is a write only register which configures the UART transmitter and receiver circuits. Data bits D7 and D6 are not used but should always be set to a logic zero (0) in order to insure software compatibility with future product upgrades. During the Echo Mode, the transmitter always repeats the received word and parity, even when the UCR is programmed with different or no parity. See Figure 1.

TABLE 1.

$\overline{CS0}$	A1	A0	$\overline{WR}$	$\overline{RD}$	OPERATION
0	0	0	0	1	Data Bus → Transmitter Buffer Register (TBR)
0	0	0	1	0	Receiver Buffer Register (RBR) → Data Bus
0	0	1	0	1	Data Bus → UART Control Register (UCR)
0	0	1	1	0	UART Status Register (USR) → Data Bus
0	1	0	0	1	Data Bus → Modem Control Register (MCR)
0	1	0	1	0	MCR → Data Bus
0	1	1	0	1	Data Bus → Bit Rate Select Register (BRSR)
0	1	1	1	0	Modem Status Register (MSR) → Data Bus

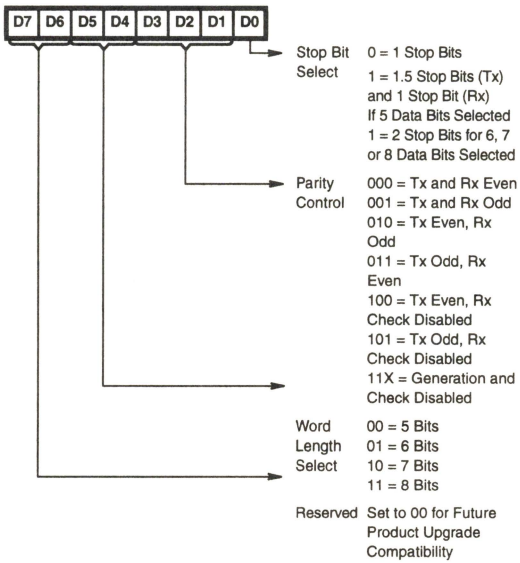


FIGURE 1. UCR

Baud Rate Select Register (BRSR)

The 82C52 is designed to operate with a single crystal or external clock driving the IX input pin. The Baud Rate Select Register is used to select the divide ratio (one of 72) for the internal Baud Rate Generator circuitry. The internal circuitry is separated into two separate counters, a Prescaler and a Divisor Select. The Prescaler can be set to any one of four division rates, ÷1, ÷3, ÷4, or ÷5.

The Prescaler design has been optimized to provide standard baud rates using any one of three popular crystal frequencies. By using one of these common system clock frequencies, 1.8432MHz, 2.4576MHz or 3.072MHz and Prescaler divide ratios of ÷3, ÷4, or ÷5 respectively, the Prescaler output will provide a constant 614.4KHz. When this frequency is further divided by the Divisor Select counter, any of the standard baud rates from 50 Baud to 38.4Kbaud can be selected (see Table 2). Non-standard baud rates up to 1Mbaud can be selected by using different input frequencies (crystal or an external frequency input up to 16MHz) and/or different Prescaler and Divisor Select ratios.

Regardless of the baud rate, the baud rate generator provides a clock which is 16 times the desired baud rate. For example, in order to operate at a 1Mbaud data rate, a 16MHz crystal, a Prescale rate of ÷1, and a Divisor Select rate of "external" would be used. This would provide a 16MHz clock as the output of the Baud Rate Generator to the Transmitter and Receiver circuits.

The CO select bit in the BRSR selects whether a buffered version of the external frequency input (IX input) or the Baud Rate Generator output (16x baud rate clock) will be output on the CO output (pin 21). The Baud Rate Generator output will always be a 50% nominal duty cycle except when "external" is selected and the Prescaler is set to ÷3 or ÷5.

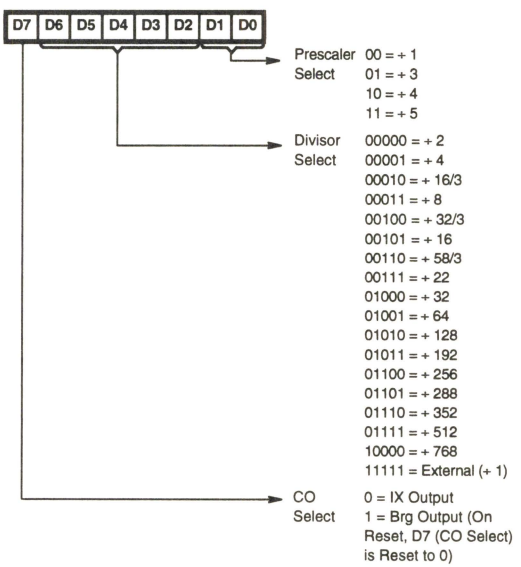


FIGURE 2. BRSR

TABLE 2.

BAUD RATE	DIVISOR
38.4K	External
19.2K	2
9600	4
7200	16/3
4800	8
3600	32/3
2400	16
2000†	58/3
1800†	22
1200	32
600	64
300	128
200	192
150	256
134.5†	288
110†	352
75	512
50	768

NOTE: These baud rates are based upon the following input frequency/ Prescale divisor combinations.
1.8432MHz and Prescale = ÷ 3
2.4576MHz and Prescale = ÷ 4
3.072MHZ and Prescale = ÷ 5

† All baud rates are exact except for:

BAUD RATE	ACTUAL	PERCENT ERROR
1800	1745.45	3.03%
2000	1986.2	0.69%
134.5	133.33	0.87%
110	109.09	0.83%

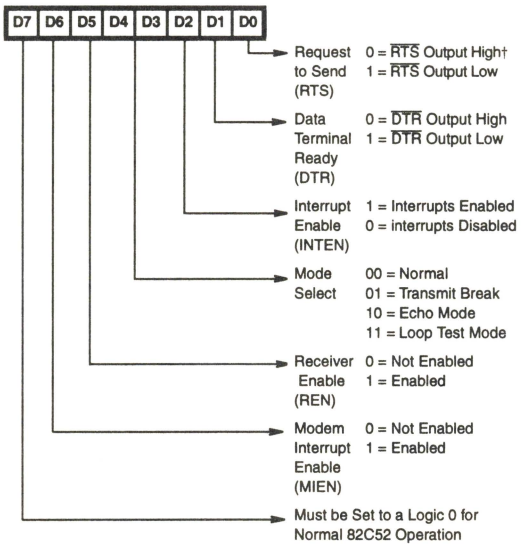
Modem Control Register

The MCR is a general purpose control register which can be written to and read from. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their associated bits in this register. Note that a logic one asserts a true logic level (low) at these output pins. The Interrupt Enable (INTEN) bit is the overall control for the INTR output pin. When INTEN is false, INTR is held false (low).

The Operating Mode bits configure the 82C52 into one of four possible modes. "Normal" configures the 82C52 for normal full or half duplex communications. "Transmit Break"' enables the transmitter to only transmit break characters (Start, Data and Stop bits all are logic zero). The Echo Mode causes any data that is received on the SDI input pin to be retransmitted on the SDO output pin. Note that this output is a buffered version of the data seen on the SDI input and is not a resynchronized output. Also note that normal UART transmission via the Transmitter Register is disabled when operating in the Echo mode (see Figure 4). The Loop Test Mode internally routes transmitted data to the receiver circuitry for the purpose of self test. The transmit data is

disabled from the SDO output pin. The Receiver Enable bit gates off the input to the receiver circuitry when in the false state.

Modem Interrupt Enable will permit any change in modem status line inputs ($\overline{CTS}$, $\overline{DSR}$) to cause an interrupt when this bit is enabled. Bit D7 must always be written to with a logic zero to insure correct 82C52 operation.



† See Modem Status Register description for a description of register flag images with respect to output pins.

FIGURE 3. MCR

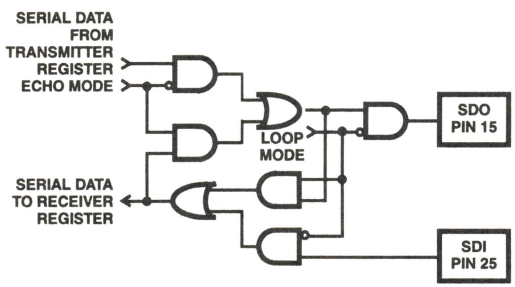


FIGURE 4. LOOP AND ECHO MODE FUNCTIONALITY

UART Status Register (USR)

The USR provides a single register that the controlling sys tem can examine to determine if errors have occurred or if other status changes in the 82C52 require attention. For this reason, the USR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the 82C52.

Three error flags OE, FE and PE report the status of any error conditions detected in the receiver circuitry. These error flags are updated with every character received during reception of the stop bits. The Overrun Error (OE) indicates that a character in the Receiver Register has been received and cannot be transferred to the Receiver Buffer Register (RBR) because the RBR was not read by the CPU. Framing Error (FE) indicates that the last character received in the RBR contained improper stop bits. This could be caused by the absence of the required stop bit(s) or by a stop bit(s) that was too short to be properly detected. Parity Error (PE) indicates that the last character received in the RBR contained a parity error based on the programmed parity of the receiver and the calculated parity of the received character data and parity bits.

The Received Break (RBRK) status bit indicates that the last character received was a break character. A break character would be considered to be an invalid data character in that the entire character including parity and stop bits are a logic zero.

The Modem Status bit is set whenever a transition is detected on any of the Modem input lines ($\overline{CTS}$ or $\overline{DSR}$). A subsequent read of the Modem Status Register will show the state of these two signals. Assertion of this bit will cause an interrupt (INTR) to be generated if the MIEN and INTEN bits in the MCR register are enabled.

The Transmission Complete (TC) bit indicates that both the TBR and Transmitter Registers are empty and the 82C52 has completed transmission of the last character it was commanded to transmit. The assertion of this bit will cause an interrupt (INTR) if the INTEN bit in the MCR register is true.

The Transmitter Buffer Register Empty (TBRE) bit indicates that the TBR register is empty and ready to receive another character.

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Assertion of the TBRE or DR bits do not affect the INTR logic and associated INTR output pin since the 82C52 has been designed to provide separate requests via the DR and TBRE output pins. If a single interrupt for any status change in the 82C52 is desired this can be accomplished by using an 82C59A Interrupt controller with DR, TBRE, and INTR as inputs. (See Figure 11).

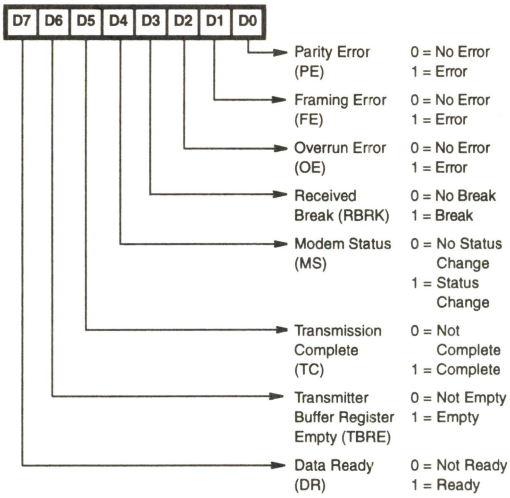


FIGURE 5. USR

Modem Status Register (MSR)

The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the 82C52. Like all of the register images of external pins in the 82C52, true logic levels are represented by a high (1) signal level. By following this consistent definition, the system software need not be concerned with whether external signals are high or low true. In particular, the modem signal inputs are low true, thus a 0 (true assertion) at a modem input pin is represented by a 1 (true) in the MSR.

Any change of state in any modem input signals will set the Modem Status (MS) bit in the USR register. When this happens, an interrupt (INTR) will be generated if the MIEN and INTEN bits of the MCR are enabled.

The Data Set Ready (DSR) input is a status indicator from the modem to the 82C52 which indicates that the modem is ready to provide received data to the 82C52 receiver circuitry.

Clear to Send (CTS) is both a status and control signal from the modem that tells the 82C52 that the modem is ready to receive transmit data from the 82C52 transmitter output (SDO). A high (false) level on this input will inhibit the 82C52 from beginning transmission and if asserted in the middle of a transmission will only permit the 82C52 to finish transmission of the current character.

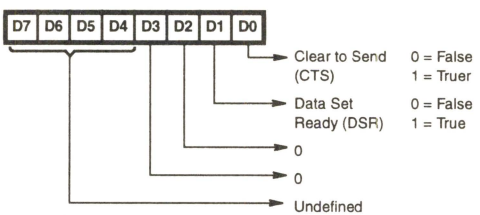


FIGURE 6. MSR

Receiver Buffer Register (RBR)

The receiver circuitry in the 82C52 is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the Least Significant Bit (LSB = D0). Bit D0 of a data word is always the first data bit received. The unused bits in a less than 8-bit word, at the parallel interface, are set to a logic zero (0) by the 82C52.

Received data at the SDI input pin is shifted into the Receiver Register by an internal 1x clock which has been synchronized to the incoming data based on the position of the start bit. When a complete character has been shifted into the Receiver Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. Both the DR output pin and DR flag in the USR register are set. This double buffering of the received data permits continuous reception of data without losing any of the received data.

While the Receiver Register is shifting a new character into the 82C52, the Receiver Buffer Register is holding a previously received character for the system CPU to read. Failure to read the data in the RBR before complete reception of the next character can result in the loss of the data in the Receiver Register. The OE flag in the USR register indicates the overrun condition.

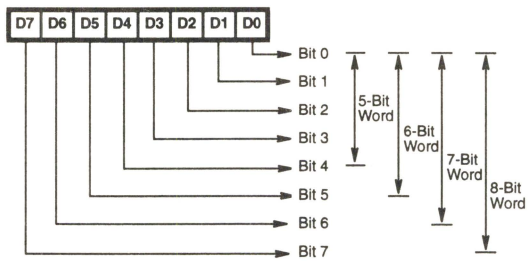


FIGURE 7. RBR

Transmitter Buffer Register (TBR)

The Transmitter Buffer Register (TBR) accepts parallel data from the data bus (D0-D7) and holds it until the Transmitter Register is empty and ready to accept a new character for transmission. The transmitter always has the same word length and number of stop bits as the receiver. For words of less than 8 bits the unused bits at the microprocessor data bus are ignored by the transmitter.

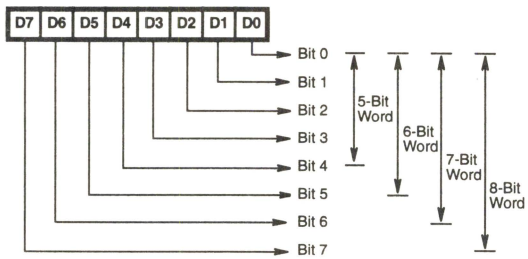


FIGURE 8. TBR

Bit 0, which corresponds to D0 at the data bus, is always the first serial data bit transmitted. Provision is made for the transmitter parity to be the same or different from the receiver. The TBRE output pin and flag (USR register) reflect the status of the TBR. The TC flag (USR register) indicates when both TBR and TR are empty.

82C52 Interrupt Structure

The 82C52 has provisions for software masking of interrupts generated for the INTR output pin. Two control bits in the MCR register, MIEN and INTEN, control modem status interrupts and overall 82C52 interrupts respectively. Figure 9 illustrates the logical control function provided by these signals.

The modem status inputs ($\overline{DSR}$ and $\overline{CTS}$) will trigger the edge detection circuitry with any change of status. Reading the MSR register will clear the detect circuit but has no effect on the status bits themselves. These status bits always reflect the state of the input pins regardless of the mask control signals. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

The edge detection circuits for the USR register signals will trigger only for a positive edge (true assertion) of these status bits. Reading the USR register not only clears the edge detect circuit but also clears (sets to 0) all of the status bits. The output pins associated with these status bits are not affected by reading the USR register.

A hardware reset of the 82C52 sets the TC status bit in the USR. When interrupts are subsequently enabled an interrupt can occur due to the fact that the positive edge detection circuitry in the interrupt logic has detected the setting of the TC bit. If this interrupt is not desired the USR should be read prior to enabling interrupts. This action resets the positive edge detection circuitry in the interrupt control logic (Figure 9).

NOTE: For USR and MSR, the setting of status bits is inhibited during status register READ operations. If a status condition is generated during a READ operation, the status bit is not set until the trailing edge of the $\overline{RD}$ pulse.

If the bit was already set at the time of the READ operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the $\overline{RD}$ pulse instead of being set again.

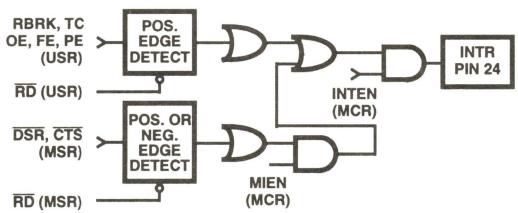


FIGURE 9. 82C52 INTERRUPT STRUCTURE

Software Reset

A software reset of the 82C52 is a useful method for returning to a completely known state without exercising a complete system reset. Such a reset would consist of writing to the UCR, BRSR and MCR registers. The USR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

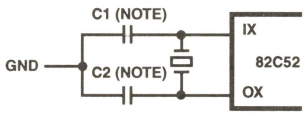
Crystal Operation

The 82C52 crystal oscillator circuitry is designed to operate with a fundamental mode, parallel resonant crystal. This circuit is the same one used in the Harris 82C84A clock generator/driver. To summarize, Table 3 and Figure 10 show the required crystal parameters and crystal circuit configuration respectively.

When using an external clock source, the IX input is driven and the OX output is left open. Power consumption when using an external clock is typically 50% of that required when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

TABLE 3.

PARAMETER	TYPICAL CRYSTAL SPECIFICATION
Frequency	1.0 to 16MHz
Type of Operation	Parallel Resonant, Fundamental Mode
Load Capacitance (CL)	20 or 32pF (Typ)
R_{SERIES}(Max)	100Ω (f = 16MHz, CL = 32pF) 200Ω (f = 16MHz, CL = 20pF)



NOTE: C1 = C2 = 20pF For CL = 20pF
C1 = C2 = 47pF For CL = 32pF

FIGURE 10.

82C52 - 80C86 Interfacing

The following example (Figure 11) shows the interface for an 82C52 in an 80C86 system.

Use of the Harris CMOS Interrupt Controller (82C59A) is optional and necessary only if an interrupt driven system is desired.

By using the Harris CMOS 82C84A clock generator, the system can be built with a single crystal providing both the processor clock and the clock for the 82C52. The 82C52 has special divider circuitry which is designed to supply industry standard baud rates with a 2.4576MHz input frequency. Using a 15MHz crystal as shown, results in less than a 2% frequency error which is adequate for many applications. For more precise baud rate requirements, a 14.7456MHz crystal will drive the 80C86 at 4.9MHz and provide the 82C52 with the standard baud rate input frequency of 2.4576MHz. If baud rates above 156Kbaud are desired, the OSC output can be used instead of the PCLK (÷6) output for asynchronous baud rates up to 1Mbaud.

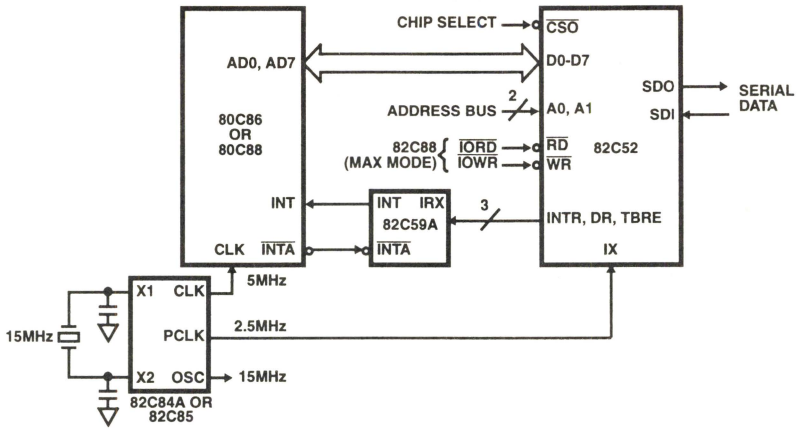


FIGURE 11. 80C86/82C52 INTERFACE

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND-0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C52 . . . . . 0^oC to $+70^oC$
I82C52 . . . . . -40^oC to $+85^oC$
M82C52 . . . . . -55^oC to $+125^oC$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	45	8.4
CLCC Package	60	14
PDIP Package	55	N/A
PLCC Package	46	N/A

Maximum Junction Temperature
Ceramic Package . . . . . $+175^oC$
Plastic Package . . . . . $+150^oC$
Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$
(Lead Tips Only For Surface Mount Packages)

Die Characteristics

Gate Count . . . . . 1500 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 5.0V ±10%, T_A = 0^oC to $+70^oC$ (C82C52), T_A = -40^oC to $+85^oC$ (I82C52)
T_A = -55^oC to $+125^oC$ (M82C52)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0	-	V	I82C52, C82C52
		2.2	-	V	M82C52
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
VTH	Schmitt Trigger Logic One Input Voltage	V_{CC} -0.5	-	V	Reset Input
VTL	Schmitt Trigger Logic Zero Input Voltage	-	GND +0.5	V	Reset Input
VIH (CLK)	Logical One Clock Input Voltage	V_{CC} -0.5	-	V	External Clock
VIL (CLK)	Logical Zero Clock Input Voltage	-	GND +0.5	V	External Clock
VOH	Output High Voltage	3.0	-	V	I_{OH} = -2.5mA, Except OX
		V_{CC} -0.4	-	V	I_{OH} = -100µA, For OX - I_{OH} = -1.0mA
VOL	Output Low Voltage	-	0.4	V	I_{OL} = +2.5mA
II	Input Leakage Current	-1.0	+1.0	µA	V_{IN} = GND or V_{CC}, DIP Pins 1, 2, 11, 12, 17, 18, 23, 25, 28
IO	Input/Output Leakage Current	-10.0	+10.0	µA	V_O = GND or V_{CC}, DIP Pins 3-10
ICCOP	Operating Power Supply Current (Note 1)	-	4	mA	External Clock F = 2.4576MHz, V_{CC} = 5.5V, V_{IN} = V_{CC} or GND, Outputs Open
ICCSB	Standby Supply Current	-	100	µA	V_{CC} = 5.5V, V_{IN} = V_{CC} or GND, Outputs Open

NOTE:

1. Guaranteed and sampled, but not 100% tested. ICCOP is typically ≤ 1.5mA/MHz.

Capacitance

T_A = 25^oC

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	12	pF	FREQ = 1MHz, all measurements are referenced to device GND
COUT	Output Capacitance	15	pF	
CI/O	I/O Capacitance	15	pF	

AC Electrical Specifications V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C (C82C52), T_A = -40°C to +85°C (I82C52)
T_A = -55°C to +125°C (M82C52)

Timing Requirements and Responses

SYMBOL		PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1)	TSVCTL	Select Setup to Control Leading Edge	30	-	ns	
(2)	TCTHSX	Select Hold from Control Trailing Edge	50	-	ns	
(3)	TCTLCTH	Control Pulse Width	150	-	ns	Control Consists of $\overline{RD}$ or $\overline{WR}$
(4)	TCTHCTL	Control Disable to Control Enable	190	-	ns	
(5)	TRLDV	Read Low to Data Valid	-	120	ns	1, See AC Test Circuit
(6)	TRHDZ	Read Disable	0	60	ns	2, See AC Test Circuit
(7)	TDVWH	Data Setup Time	50	-	ns	
(8)	TWHDX	Data Hold Time	20	-	ns	
(9)	FC	Clock Frequency	0	16	MHz	TCHCL + TCLCH must be ≥ 62.5ns
(10)	TCHCL	Clock High Time	25	-	ns	
(11)	TCLCH	Clock Low Time	25	-	ns	
(12)	TR/TF	IX Input Rise/Fall Time (External Clock)	-	tx	ns	$tx \geq \frac{1}{6FC}$ or 50ns Whichever is smaller
(13)	TFCO	Clock Output Fall Time	-	15	ns	CL = 50pf
(14)	TRCO	Clock Output Rise Time	-	15	ns	CL = 50pf

AC Testing Input, Output Waveforms



FIGURE 12. PROPAGATION DELAY

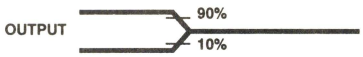


FIGURE 13. ENABLE/DISABLE DELAY

AC TESTING: All input signals (except IX and RST) must switch between V_{IL} -0.4V and V_{IH} +0.4V. Input rise and fall times are driven at 1ns/V.

Timing Waveform

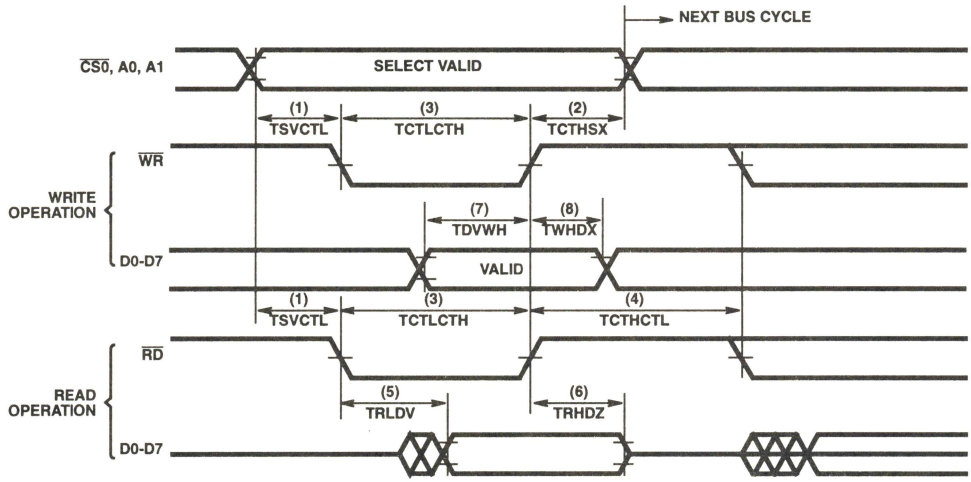
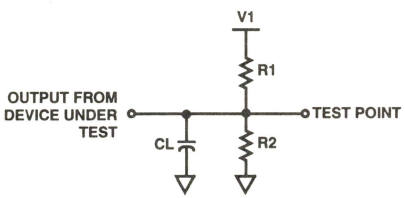


FIGURE 14. BUS OPERATION

AC Test Circuit



TEST CONDITION		V1	R1	R2	CL
1	Propagation Delay	1.7V	520	∞	100pF
2	Disable Delay	V_{CC}	5K	5K	50pF

UART Timing Characterization

All parameters listed in this table were laboratory bench characterized at room temperature on a small sample of parts. No guarantee is implied. The main intent here is to clarify functional operation of the 82C52.

82C52 UART Timing Characterized with IX = External Clock

SYMBOL		PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(15)	TS1	CO(IX) Delay from IX	-	30	ns	BRSR Bit D7 = 0 (IX Output)
(16)	TS2	CO (BRG) Delay from IX	-	80	ns	BRSR Bit D7 = 1 (BRG Output)
(17)	TCY	CO (BRG) Clock Cycle Time	62.5	-	ns	BRSR Bit D7 = 1 (BRG Output), Note 1
(18)	TDTX	SDO Delay from CO(BRG) Low	-	30	ns	Note 2
(19)	TWLTL	$\overline{WR}$ Low to TBRE Low	-	50	ns	Note 3
(20)	TCLTH	CO (BRG) Low to TBRE HIgh	-	50	ns	Notes 3, 4
(21)	TIHF	INTR High on Flag	-	50	ns	Note 5A, 5B
(22)	TIHM	INTR High on MS	-	50	ns	Note 5
(23)	TRLIL	$\overline{RD}$ Low to INTR Low	-	60	ns	
(24)	TCTHX	$\overline{CTS}$ High to Disable Transmit	4TCY + 10	-	ns	TBR Full, Note 6
(25)	TDRH	CO (BRG) Low to DR High	-	40	ns	Note 7
(26)	TRLDL	$\overline{RD}$ Low to DR Low	-	50	ns	Note 7
(27)	TWHO	$\overline{WR}$ High to $\overline{RTS}/\overline{DTR}$ Active	-	50	ns	

NOTES:

1. Prescaler rate of divide by 1, Divisor Select rate of "external" (divide by 1). The Baud Rate Clock (CO-BRG) operates at 16 times the user programmed bit rate. For example, at 1200 baud: TCY = 1/(16 x 1200) = 52.1µs.
2. A. With TR (Transmitter Register) initially empty, TDTX occurs from the 5th falling edge of CO(BRG) after $\overline{WR}$ goes high.
   B. With TR initially full, TDTX occurs from the trailing edge of the 16th CO(BRG) in the last Stop bit provided $\overline{WR}$ went high by the trailing edge of the 12th CO(BRG) in the last Stop bit.
   C. With $\overline{CTS}$ high (disable transmit) and TBR full, TDTX occurs from the 5th falling edge of CO(BRG) after $\overline{CTS}$ goes low.
3. TBRE bit D6 in USR is updated each time TBRE changes state.
4. A. With TR initially empty, TCLTH(TBRE) occurs from the 4th falling edge of CO(BRG) after $\overline{WR}$ goes high.
   B. With TR initially full, TCLTH(TBRE) occurs from the trailing edge of the 15th CO(BRG) in the last Stop bit provided $\overline{WR}$ went high by the trailing edge of the 12th CO(BRG) in the last Stop bit.
   C. With $\overline{CTS}$ high (disable transmit) and TBR full, TCLTH(TBRE) occurs from the 4th falling edge of CO(BRG) after $\overline{CTS}$ goes low.
5. A. INT on TC: INTEN enabled; USR bit D5(TC) is updated at this time regardless of interrupt configuration.
      - INT on TC occurs from the trailing edge of the 11th CO(BRG) in the last Stop bit if TBR empty at that time.
   B. INTR on receive flags OE, FE, PE, and RBRK: INTEN enabled; Respective USR bits updated at this time regardless of interrupt configuration.
      - INT on OE, FE, PE, RBRK occurs from the trailing edge of the 11th CO(BRG) in the last Stop bit. To avoid OE, $\overline{RD}$(RBR) must go low by the trailing edge of the 8th CO(BRG) in the last Stop bit.
   C. INTR on MS: INTEN and MIEN enabled; USR bit D4(MS) is updated at this time regardless of INTEN/MIEN.
      - INTR on MS occurs whenever $\overline{CTS}$ or $\overline{DSR}$ input changes state.
6. TCTHX is time before end of last Stop bit by which $\overline{CTS}$ must be inactive (high) to prevent transmission of the character waiting in TBR.
7. DR bit D7 in USR is updated each time DR changes state. TDRH always from trailing edge of 11th CO(BRG) in last Stop bit.

UART Timing Characterization

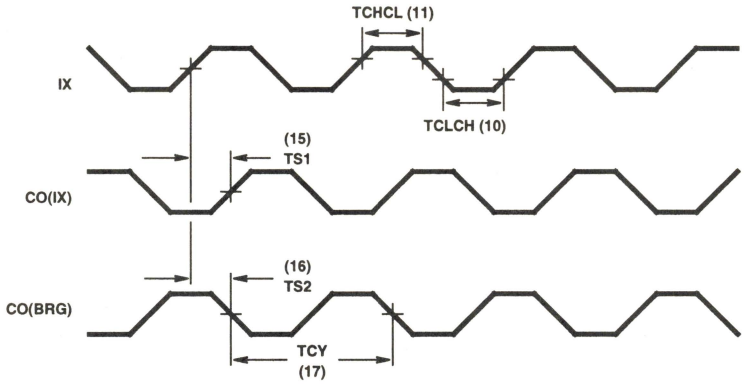


FIGURE 15. CLOCK (IX) AND CO TIMING

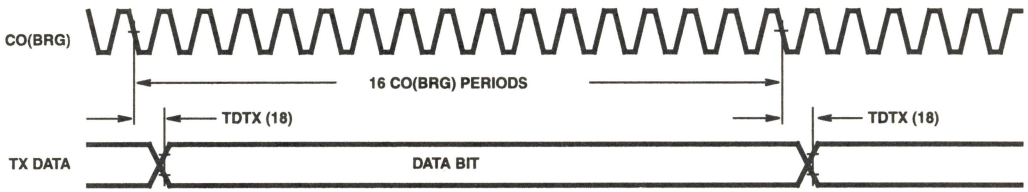


FIGURE 16. TRANSMITTER DATA

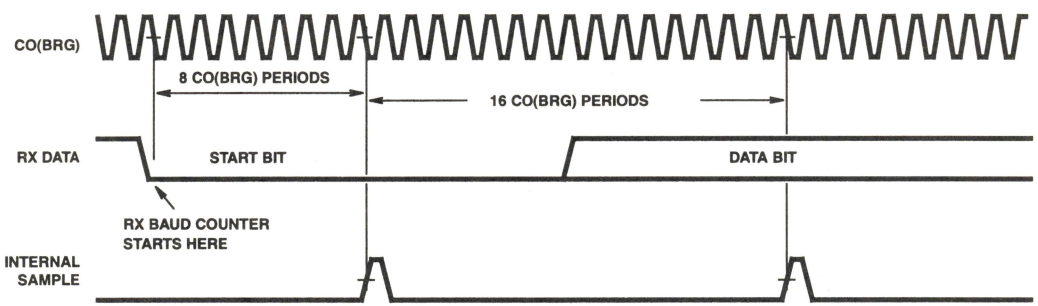


FIGURE 17. RECEIVER DATA

UART Timing Characterization (Continued)

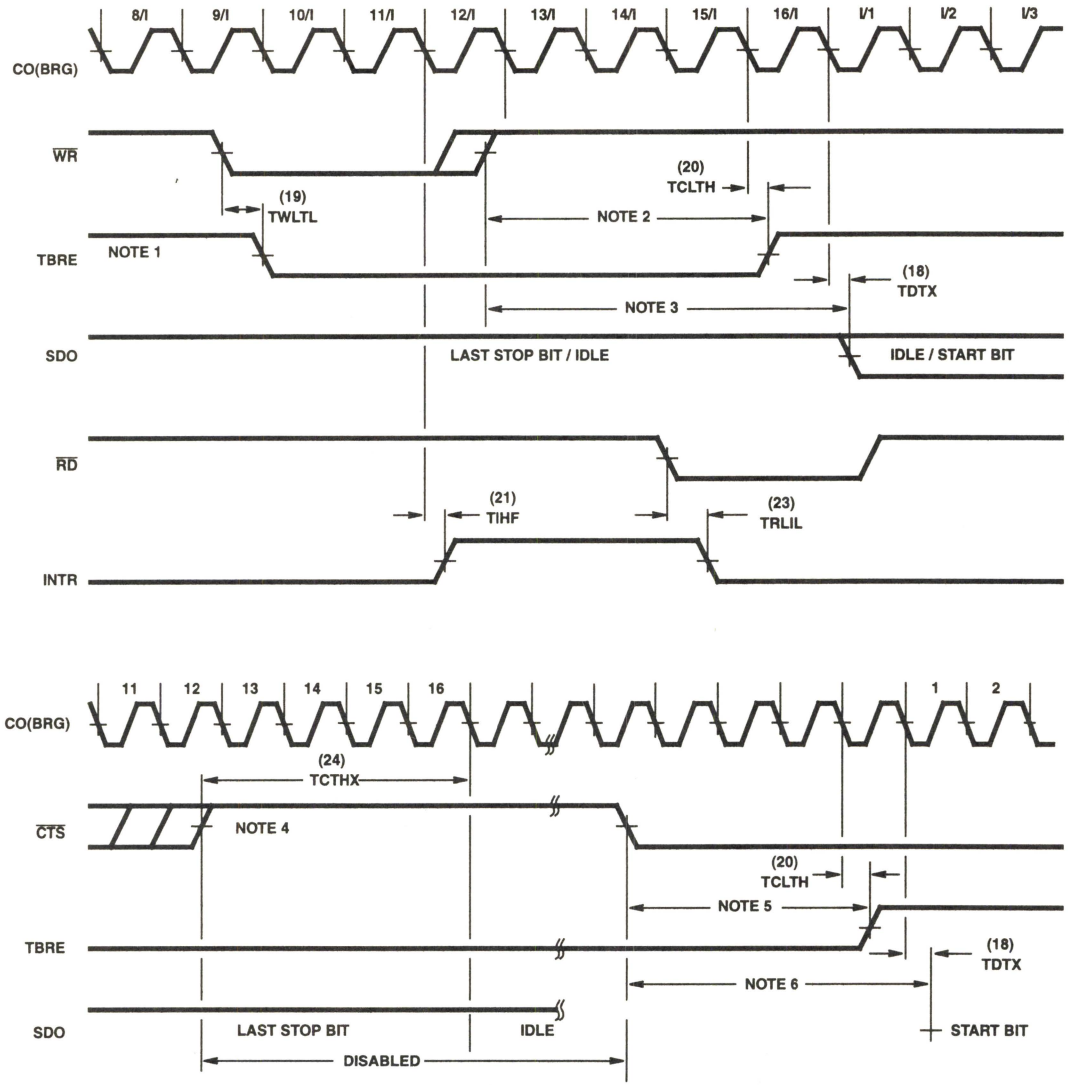


FIGURE 18. TRANSMIT TIMING

NOTES:

1. TBRE bit D6 in USR is updated each time TBRE changes state.
2. A. With TR initially empty, TCLTH(TBRE) occurs from the 4th falling edge of CO(BRG) after $\overline{WR}$ goes high.
   B. With TR initially full, TCLTH(TBRE) occurs from the trailing edge of the 15th CO(BRG) in the last Stop bit provided $\overline{WR}$ went high by the trailing edge of the 12th CO(BRG) in the last Stop bit.
3. A. With TR (Transmitter Register) initially empty, TDTX occurs from the 5th falling edge of CO(BRG) after $\overline{WR}$ goes high.
   B. With TR initially full, TDTX occurs from the trailing edge of the 16th CO(BRG) in the last Stop bit provided $\overline{WR}$ went high by the trailing edge of the 12th CO(BRG) in the last Stop bit.
4. TCTHX is time before end of last Stop bit by which $\overline{CTS}$ must be inactive (high) to prevent transmission of the character waiting in TBR.
5. With $\overline{CTS}$ high (disable transmit) and TBR full, TCLTH(TBRE) occurs from the 4th falling edge of CO(BRG) after $\overline{CTS}$ goes low.
6. With $\overline{CTS}$ high (disable transmit) and TBR full, TDTX occurs from the 5th falling edge of CO(BRG) after $\overline{CTS}$ goes low.

UART Timing Characterization (Continued)

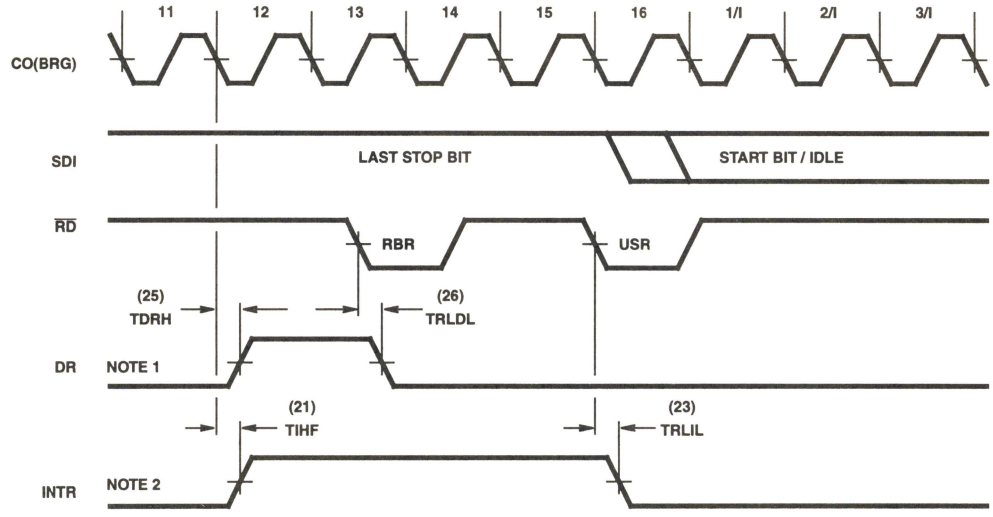


FIGURE 19. RECEIVE TIMING

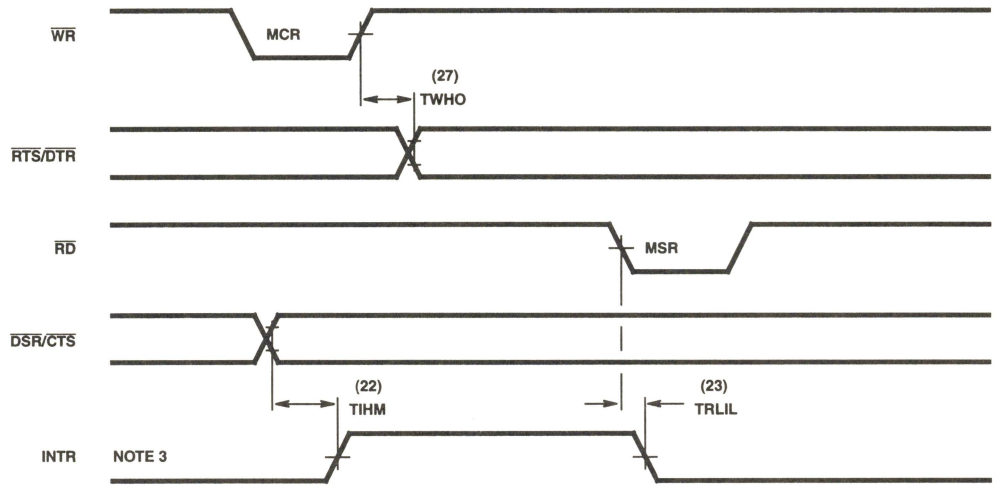


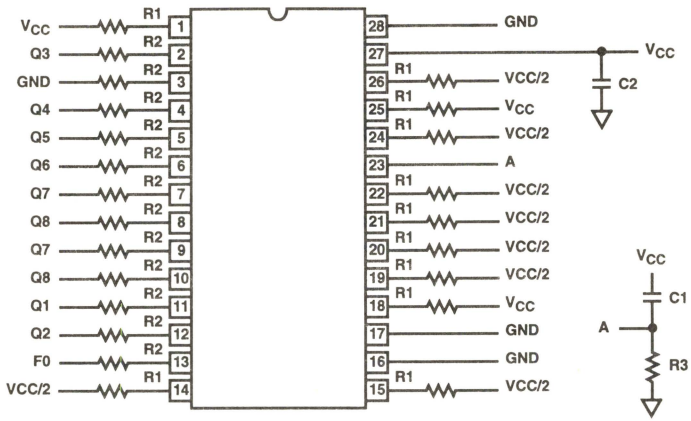
FIGURE 20. OTHER TIMING

NOTES:

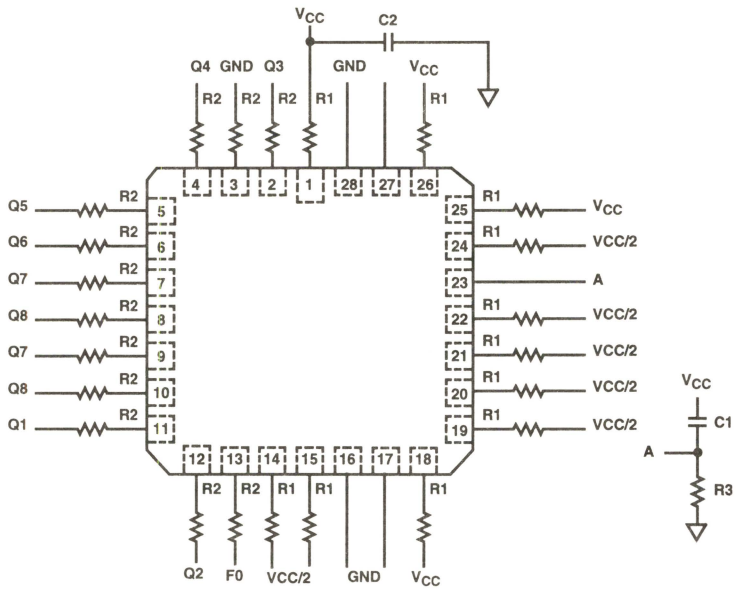
1. DR bit D7 in USR is updated each time DR changes state. TDRH always from trailing edge of 11th CO(BRG) in last Stop bit.
2. INTR on receive flags OE, FE, PE, and RBRK: INTEN enabled; Respective USR bits updated at this time regardless of interrupt configuration.
   - INT on OE, FE, PE, RBRK occurs from the trailing edge of the 11th CO(BRG) in the last Stop bit. To avoid OE, $\overline{RD}$(RBR) must go low by the trailing edge of the 8th CO(BRG) in the last Stop bit.
3. INTR on MS: INTEN and MIEN enabled; USR bit D4(MS) is updated at this time regardless of INTEN/MIEN.
   - INTR on MS occurs whenever $\overline{CTS}$ or $\overline{DSR}$ input changes state.

Burn-In Circuits

MD 82C52 CERDIP



MR 82C52 CLCC



NOTES:

1. V_{CC} = 5.5V ±0.5V
   GND = 0V
2. V_{IH} = 4.5V ±10%
   V_{IL} = -0.2V to +0.4V
3. Component Values:
   R1 = 1.2KΩ, 1/4W, 5%
   R2 = 47KΩ, 1/4W, 5%
   R3 = 10KΩ, 1/4W, 5%
   C1 = 1.0μF nominal
   C2 = 0.01μF minimum
   F0 = 100KHz ±10%, F1 = F0/2, F2 = F1/2 . . . F12 = F11/2

Die Characteristics

DIE DIMENSIONS:
178.7 x 187.0 x 19 ±1mils

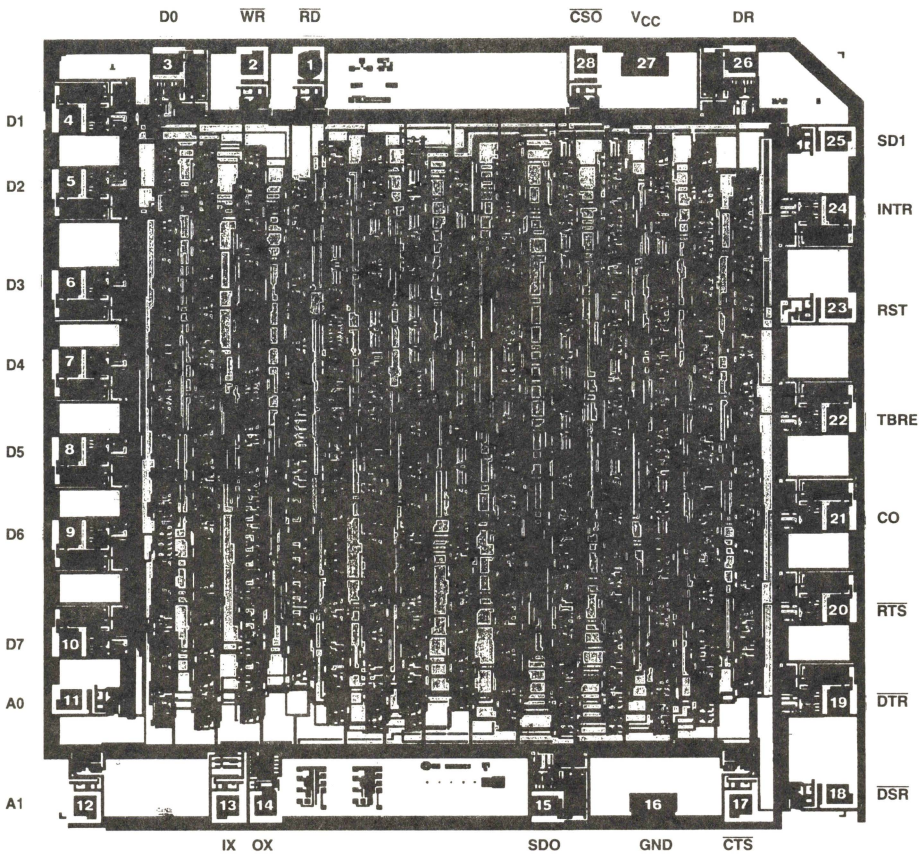
METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:
2.07×10^4 A/cm^2

Metallization Mask Layout

82C52



HARRIS SEMICONDUCTOR

CDP1854A, CDP1854AC

Programmable Universal Asynchronous Receiver/Transmitter (UART)

March 1997

Features

- Two Operating Modes
  - Mode 0 - Functionally Compatible with Industry Types Such as the TR1602A and CDP6402
  - Mode 1 - Interfaces Directly with CDP1800-Series Microprocessors without Additional Components
- Full or Half Duplex Operation
- Parity, Framing and Overrun Error Detection
- Baud Rate
  - DC to 200K Bits/s at V_{DD} 5V
  - DC to 400K Bits/s at V_{DD} 10V
- Fully Programmable with Externally Selectable Word Length (5-8 Bits), Parity Inhibit, Even/Odd Parity, and 1, 1-1/2, or 2 Stop Bits
- False Start Bit Detection

Ordering Information

PACKAGE	TEMP. RANGE	5V/200K BAUD	10V/400K BAUD	PKG. NO.
PDIP	-40°C to +85°C	CDP1854ACE	CDP1854AE	E40.6
Burn-In		CDP1854ACEX	CDP1854AEX	E40.6
PLCC	-40°C to +85°C	CDP1854ACQ	CDP1854AQ	N44.65
SBDIP	-40°C to +85°C	CDP1854ACD	CDP1854AD	D40.6
Burn-In		CDP1854ACDX	-	D40.6

Description

The CDP1854A and CDP1854AC are silicon-gate CMOS Universal Asynchronous Receiver/Transmitter (UART) circuits. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data. For example, these UARTs can be used to interface between a peripheral or terminal with serial I/O ports and the 8-bit CDP1800-series microprocessor parallel data bus system. The CDP1854A is capable of full duplex operation, i.e., simultaneous conversion of serial input data to parallel output data and parallel input data to serial output data.

The CDP1854A UART can be programmed to operate in one of two modes by using the mode control input. When the input is high (MODE = 1), the CDP1854A is directly compatible with the CDP1800-series microprocessor system without additional interface circuitry. When the mode input is low (MODE = 0), the device is functionally compatible with industry standard UART's such as the TR1602A and CDP6402. It is also pin compatible with these types, except that pin 2 is used for the mode control input.

The CDP1854A and the CDP1854AC are functionally identical. The CDP1854A has a recommended operating voltage range of 4V to 10.5V, and the CDP1854AC has a recommended operating voltage range of 4V to 6.5V.

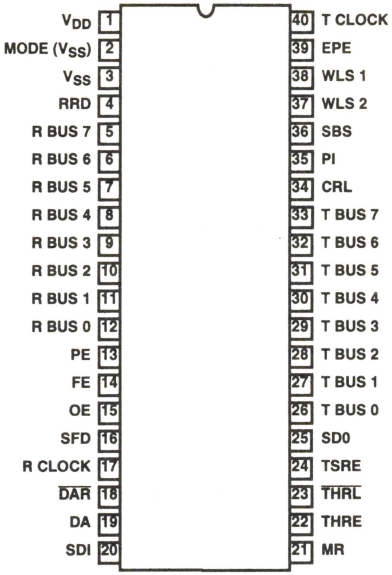
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Copyright © Harris Corporation 1997

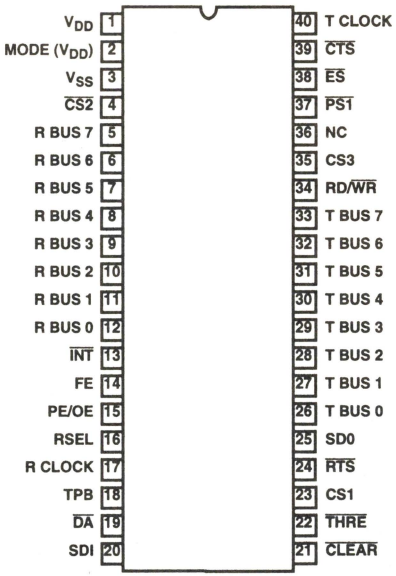
File Number **1193.2**

Pinouts

40 LEAD SBDIP, PDIP (MODE 0)
TOP VIEW

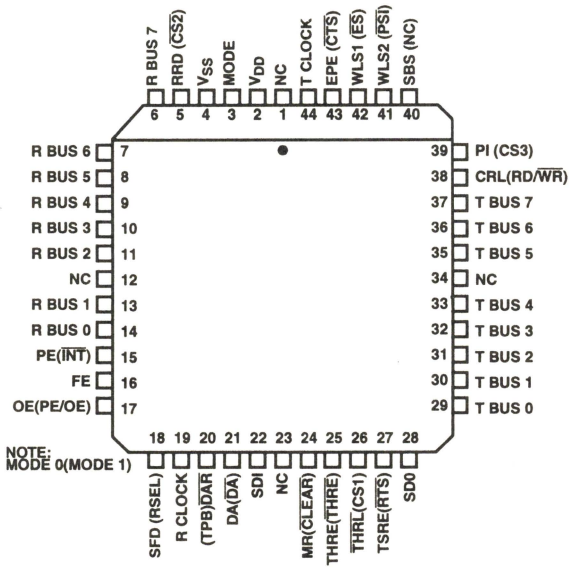


40 LEAD SBDIP, PDIP (MODE 1)
TOP VIEW



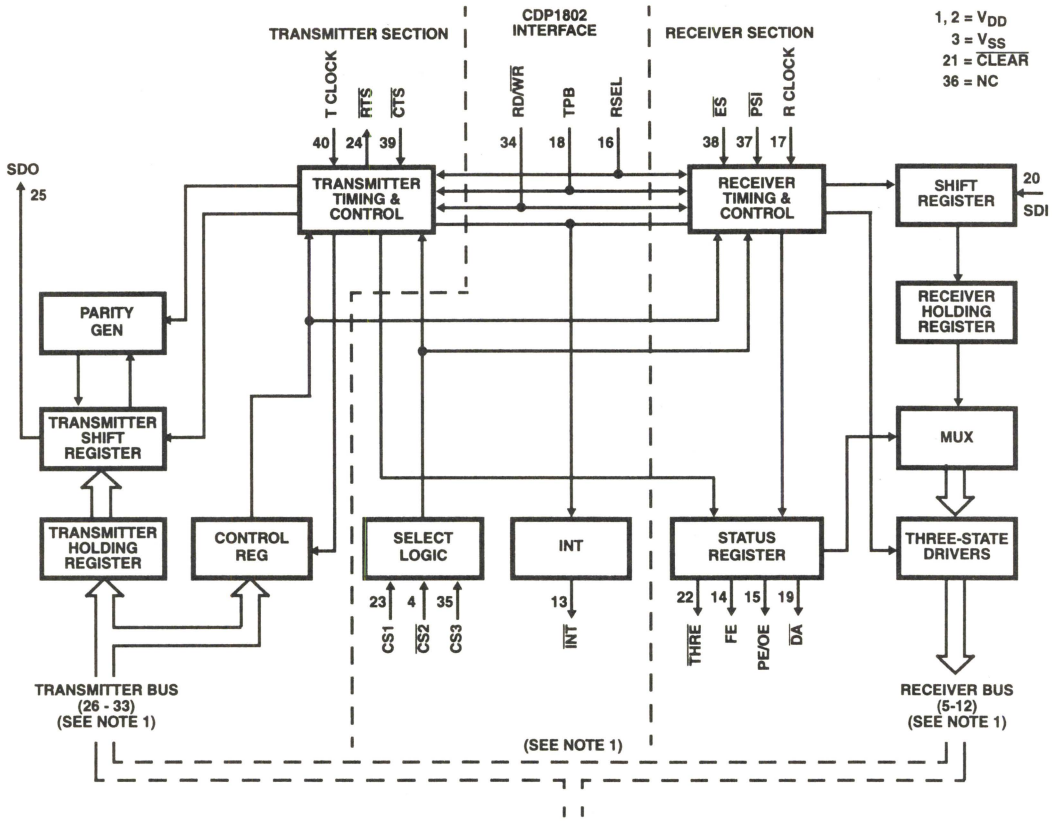
NC = NO CONNECT

44 LEAD PLCC (Q SUFFIX)
TOP VIEW



Block Diagram

Mode Input High (Mode = 1)



NOTE: 1. User Interconnect

FIGURE 1. MODE 1 BLOCK DIAGRAM (CDP1800-SERIES MICROPROCESSOR COMPATIBLE)

Absolute Maximum Ratings

DC Supply-Voltage Range, (V_{DD})
(Voltages Referenced to V_{SS} Terminal)
CDP1854A . . . . . -0.5 to +11V
CDP1854AC . . . . . -0.5 to +7V
Input Voltage Range, All Inputs . . . . . -0.5 to V_{DD} + 0.5V
DC Input Current, Any One Input. . . . . ±10mA
Device Dissipation Per Output Transistor
T_A = Full Package-Temperature Range 100mW
Operating-Temperature Range (T_A)
Package Type D . . . . . -55°C to +125°C
Package Type E and Q . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	55	15
PDIP Package	50	N/A
PLCC Package	46	N/A

Maximum Junction Temperature
Plastic Package . . . . . +150°C
Ceramic Package . . . . . +175°C
Maximum Storage Temperature Range (T_{STG}) . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s):
At Distance 1/16 ±1/32 inch (1.59 ±0.79mm) . . . . . +265°C
NOTE: Printed circuit board mount: 57mm x 57mm minimum area x 1.6mm thick G10 epoxy glass, or equivalent.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Static Electrical Specifications at T_A = -40°C to +85°C, Unless Otherwise Noted

PARAMETER		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS CDP1854A MIN	LIMITS CDP1854A (NOTE 1) TYP	LIMITS CDP1854A MAX	LIMITS CDP1854AC MIN	LIMITS CDP1854AC (NOTE 1) TYP	LIMITS CDP1854AC MAX	UNITS
Quiescent Device Current	I_{DD}	-	0, 5	5	-	0.01	50	-	0.02	200	µA
		-	0, 10	10	-	1	200	-	-	-	µA
Output Low Drive (Sink) Current (Except pins 24 and 25)	I_{OL}	0.4	0, 5	5	1	2	-	1	2	-	mA
		0.5	0, 10	10	2	4	-	-	-	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-0.55	-1.1	-	-0.55	-1.1	-	mA
		9.5	0, 10	10	-1.3	-2.6	-	-	-	-	mA
Output Low Drive (Sink) Current (Pins 24 and 25)	I_{OL}	0.4	0, 5	5	1.6	3.5	-	1.6	3.5	-	mA
		0.5	0, 10	10	3.2	7	-	-	-	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High-Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 9.5	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Current	I_{IN}	-	0, 5	5	-	-	±1	-	-	±1	µA
		-	0, 10	10	-	-	±2	-	-	-	µA

Static Electrical Specifications at T_A = -40°C to +85°C, Unless Otherwise Noted **(Continued)**

PARAMETER		CONDITIONS			LIMITS						UNITS
					CDP1854A			CDP1854AC			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	-	±1	-	-	±1	µA
		0, 10	0, 10	10	-	-	±10	-	-	-	µA
Operating Current (Note 3)	I_{DD1}	-	0, 5	5	-	1.5	-	-	1.5	-	mA
		-	0, 10	10	-	6	-	-	-	-	mA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = 25°C.
2. $I_{OL} = I_{OH}$ = 1µA.
3. Operating current is measured at 200kHz or V_{DD} = 5V and 400kHz for V_{DD} = 10V in a CDP1800-series microprocessor system, with open outputs.

Operating Conditions At T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	CONDITIONS	LIMITS				UNITS
		CDP1854A		CDP1854AC		
	V_{DD} (V)	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	-	4	10.5	4	6.5	V
Input Voltage Range	-	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Baud Rate (Receive or Transmit)	5	-	200	-	200	K bits/s
	10	-	400	-	-	K bits/s

Functional Definitions for CDP1854A Terminals Mode 1 CDP1800-Series Microprocessor Compatible

SIGNAL: FUNCTION

V_{DD}:

Positive supply voltage.

MODE SELECT (MODE):

A high-level voltage at this input selects CDP1800-series microprocessor Mode operation.

V_{SS}:

Ground

CHIP SELECT 2 ($\overline{CS2}$):

A low-level voltage at this input together with CS1 and CS3 selects the CDP1854A UART.

RECEIVER BUS (R BUS 7 - R BUS 0):

Receiver parallel data outputs (may be externally connected to corresponding transmitter bus terminals).

INTERRUPT ($\overline{INT}$):

A low-level voltage at this output indicates the presence of one or more of the interrupt conditions listed in Table 1.

FRAMING ERROR (FE):

A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register.

PARITY ERROR or OVERRUN ERROR (PE/OE):

A high-level voltage at this output indicates that either the PE or OE bit in the Status Register has been set (see Status Register Bit Assignment, Table 2).

REGISTER SELECT (RSEL):

This input is used to choose either the Control/Status Registers (high input) or the transmitter/receiver data registers (low input) according to the truth table in Table 3.

RECEIVER CLOCK (RCLOCK):

Clock input with a frequency 16 times the desired receiver shift rate.

TPB:

A positive input pulse used as a data load or reset strobe.

DATA AVAILABLE ($\overline{DA}$):

A low-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

SERIAL DATA IN (SDI):

Serial data received on this input line enters the Receiver Shift Register at a point determined by the character length. A high-level input voltage must be present when data is not being received.

CLEAR ($\overline{CLEAR}$):

A low-level voltage at this input resets the Interrupt Flip-Flop, Receiver Holding Register, Control Register, and Status Register, and sets SERIAL DATA OUT (SDO) high.

TRANSMITTER HOLDING REGISTER EMPTY ($\overline{THRE}$):

A low-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.

CHIP SELECT 1 (CS1):

A high-level voltage at this input together with $\overline{CS2}$ and CS3 selects the UART.

REQUEST TO SEND ($\overline{RTS}$):

This output signal tells the peripheral to get ready to receive data. $\overline{CLEAR\ TO\ SEND}$ ($\overline{CTS}$) is the response from the peripheral. $\overline{RTS}$ is set to a low-level voltage when data is latched in the Transmitter Holding Register or TR is set high, and is reset high when both the Transmitter Holding Register and Transmitter Shift Register are empty and TR is low.

SERAL DATA OUTPUT (SDO):

The contents of the Transmitter Shift Register [start bit, data bits, parity bit, and stop bit(s)] are serially shifted out on this output. When no character is being transmitted, a high level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.

TRANSMITTER BUS (T BUS 0 - T BUS 7):

Transmitter parallel data input. These may be externally connected to corresponding Receiver bus terminals.

RD/$\overline{WR}$:

A low-level voltage at this input gates data from the transmitter bus to the Transmitter Holding Register or the Control Register as chosen by register select. A high-level voltage gates data from the Receiver Holding Register or the Status Register, as chosen by register select, to the receiver bus.

CHIP SELECT 3 (CS3):

With high-level voltage at this input together with CS1 and $\overline{CS2}$ selects the UART.

PERIPHERAL STATUS INTERRUPT ($\overline{PSI}$):

A high-to-low transition on this input line sets a bit in the Status Register and causes an $\overline{INTERRUPT}$ ($\overline{INT}$ = low).

EXTERNAL STATUS ($\overline{ES}$):

A low-level voltage at this input sets a bit in the Status Register.

CLEAR TO SEND ($\overline{CTS}$):

When this input from peripheral is high, transfer of a character to the Transmitter Shift Register and shifting of serial data out is inhibited.

TRANSMITTER CLOCK (TCLOCK):

Clock input with a frequency 16 times the desired transmitter shift rate.

TABLE 1. INTERRUPT SET AND RESET CONDITIONS

(NOTE 1) SET (INT = LOW)	RESET (INT = HIGH)	
CAUSE	**CONDITION**	**TIME**
DA (Receipt of Data)	Read of Data	TPB Leading Edge
THRE (Note 2) (Ability to Reload)	Read of Status or Write of Character	TPB Leading Edge
THRE • TSRE (Transmitter Done)	Read of Status or Write of Character	TPB Leading Edge
$\overline{PSI}$ (Negative Edge)	Read of Status	TPB Trailing Edge
$\overline{CTS}$ (Positive Edge when $\overline{THRE \bullet TSRE}$)	Read of Status	TPB Leading Edge

NOTES:

1. Interrupts will occur only after the IE bit in the Control Register (see Table 4) has been set.
2. THRE will cause an interrupt only after the TR bit in the Control Register (see Table 4) has been set.

TABLE 2. STATUS REGISTER BIT ASSIGNMENT

BIT	7	6	5	4	3	2	1	0
SIGNAL	THRE	TSRE	PSI	ES	FE	PE	OE	DA
ALSO AVAILABLE AT TERMINAL † Polarity reversed at output terminal.	22†	-	-	-	14	15	15	19†

BIT SIGNAL: FUNCTION

0	DATA AVAILABLE (DA): When set high, this bit indicates that an entire character has been received and transferred to the Receiver Holding Register. This signal is also available at Term. 19 but with its polarity reversed.
1	OVERRUN ERROR (OE): When set high, this bit indicates that the Data Available bit was not reset before the next character was transferred to the Receiver Holding Register. This signal OR'ed with PE is output at Term. 15.
2	PARITY ERROR (PE): When set high, this bit indicates that the received parity bit does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal OR'ed with OE is output at Term. 15.
3	FRAMING ERROR (FE): When set high, this bit indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal is also available at Term. 14.
4	EXTERNAL STATUS (ES): This bit is set high by a low-level input at Term. 38 ($\overline{ES}$).
5	PERIPHERAL STATUS INTERRUPT (PSI): This bit is set high by a high-to-low voltage transition of Term. 37 ($\overline{PSI}$). The INTERRUPT output (Term. 13) is also asserted ($\overline{INT}$ = low) when this bit is set.
6	TRANSMITTER SHIFT REGISTER EMPTY (TSRE): When set high, this bit indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains set until the start of transmission of the next character.
7	TRANSMITTER HOLDING REGISTER EMPTY (THRE): When set high, this bit indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character. Setting this bit also sets the $\overline{THRE}$ output (Term. 22) low and causes an INTERRUPT ($\overline{INT}$ = low), if TR is high.

Description of Mode 1 Operation CDP1800-Series Microprocessor Compatible (Mode Input = V_{DD})

Initialization and Controls

In the CDP1800-series microprocessor compatible mode, the CDP1854A is configured to receive commands and send status via the microprocessor data bus. The register connected to the transmitter bus or the receiver bus is determined by the RD/$\overline{WR}$ and RSEL inputs as follows:

TABLE 3. REGISTER SELECTION SUMMARY

RSEL	RD/$\overline{WR}$	FUNCTION
Low	Low	Load Transmitter Holding Register from Transmitter Bus
Low	High	Read Receiver Holding Register from Receiver Bus
High	Low	Load Control Register from Transmitter Bus
High	High	Read Status Register from Receiver Bus

In this mode the CDP1854A is compatible with a bidirectional bus system. The receiver and transmitter buses are connected to the bus. CDP1800-series microprocessor I/O control output signals can be connected directly to the CDP1854A inputs as shown in Figure 2. The CLEAR input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting SERIAL DATA OUT (SDO) high. The Control Register is loaded from the Transmitter Bus in order to determine the operating configuration for the UART. Data is transferred from the Transmitter Bus inputs to the Control Register during TPB when the UART is selected (CS1• $\overline{CS2}$ • CS3 = 1) and the Control Register is designated (RSEL = H, RD/$\overline{WR}$ = L). The CDP1854A also has a Status Register which can be read onto the Receiver Bus (R BUS 0 - R BUS 7) in order to determine the status of the UART. Some of these status bits are also available at separate terminals as indicated in Table 2.

Transmitter Operation

Before beginning to transmit, the TRANSMIT REQUEST (TR) bit in the Control Register (see bit assignment, Table 4) is set. Loading the Control Register with TR = 1 (bit 7 = high) inhibits changing the other control bits. Therefore two loads are required: one to format the UART, the second to set TR. When TR has been set, a $\overline{TRANSMITTER\ HOLDING\ REGISTER\ EMPTY}$ ($\overline{THRE}$) interrupt will occur, signalling the microprocessor that the Transmitter Holding Register is empty and may be loaded. Setting TR also causes assertion of a low-level on the REQUEST TO SEND ($\overline{RTS}$) output to the peripheral. It is not necessary to set TR for proper operation for the UART. If desired, it can be used to enable $\overline{THRE}$ interrupts and to generate the $\overline{RTS}$ signal. The Transmitter Holding Register is loaded from the bus by TPB during execution of an output instruction. The CDP1854A is selected by CS1 • $\overline{CS2}$ • CS3 = 1, and the Holding Register is selected by RSEL = L and RD/$\overline{WR}$ = L. When the $\overline{CLEAR\ TO\ SEND}$ ($\overline{CTS}$) input, which can be connected to a peripheral device output, goes low, the Transmitter Shift Register will be loaded from the Transmitter Holding Register and data transmission will begin. If $\overline{CTS}$ is always low, the Transmitter Shift Register will be loaded on the first high-to-low edge of the clock which occurs at least 1/2 clock period after the trailing edge of TPB and transmission of a start bit will occur 1/2 clock period later (see Figure 3). Parity (if programmed) and stop bit(s) will be transmitted following the last data bit. If the word length selected is less than 8 bits, the most significant unused bits in the transmitter shift register will not be transmitted.

One transmitter clock period after the Transmitter Shift Register is loaded from the Transmitter Holding Register, the $\overline{THRE}$ signal will go low and an interrupt will occur ($\overline{INT}$ goes low). The next character to be transmitted can then be loaded into the Transmitter Holding Register for transmission with its start bit immediately following the last stop bit of the previous character. This cycle can be repeated until the last character is transmitted, at which time a final THRE • TSRE interrupt will occur. This interrupt signals the microprocessor that TR can be turned off. This is done by reloading the original control byte in the Control Register with the TR bit 0, thus terminating the $\overline{REQUEST\ TO\ SEND}$ ($\overline{RTS}$) signal.

SERIAL DATA OUT (SDO) can be held low by setting the BREAK bit in the Control Register (see Table 4). SDO is held low until the BREAK bit is reset.

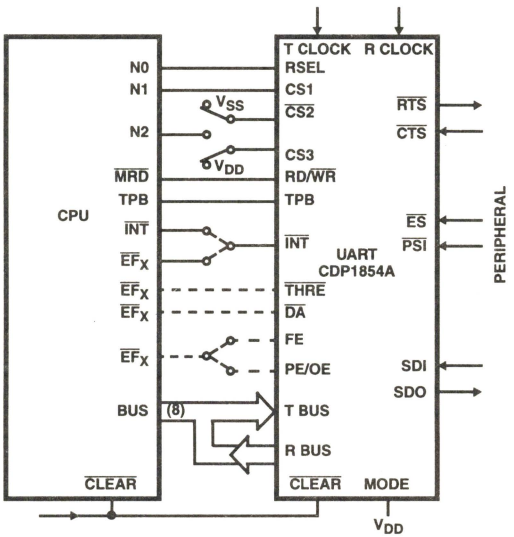


FIGURE 2. RECOMMENDED CDP1800-SERIES CONNECTION, MODE 1 (NON-INTERRUPT DRIVEN SYSTEM)

Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After detection of the first high-to-low transition on the SDI line, a valid start bit is verified by checking for a low-level input 7-1/2 receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed) and stop bit(s) are shifted into the Receiver Shift Register by clock pulse 7-1/2

in each bit time. The parity bit (if programmed) is checked and receipt of a valid stop bit is verified. On count 7-1/2 of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output level) are loaded into the unused most significant bits. If DATA AVAILABLE (DA) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) status bit is set. One half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) status bits become valid for the character in the Receiver Holding Register. At this time, the Data Available status bit is also set and the DATA AVAILABLE (DA) and INTERRUPT (INT) outputs go low, signalling the microprocessor that a received character is ready. The microprocessor responds by executing an input instruction. The UART's three-state bus drivers are enabled when the UART is selected (CS1 • $\overline{CS2}$ • CS3 = 1) and RD/$\overline{WR}$ = high. Status can be read when RSEL = high. Data is read when RSEL = low. When reading data, TPB latches data in the microprocessor and resets $\overline{DATA\ AVAILABLE}$ ($\overline{DA}$) in the UART. The preceding sequence is repeated for each serial character which is received from the peripheral.

Peripheral Interface

In addition to serial data in and out, four signals are provided for communication with a peripheral. The $\overline{REQUEST\ TO\ SEND}$ ($\overline{RTS}$) output signal alerts the peripheral to get ready to receive data. The $\overline{CLEAR\ TO\ SEND}$ ($\overline{CTS}$) input signal is the response, signalling that the peripheral is ready. The $\overline{EXTERNAL\ STATUS}$ ($\overline{ES}$) input latches a peripheral status level, and the $\overline{PERIPHERAL\ STATUS\ INTERRUPT}$ ($\overline{PSI}$) input senses a status edge (high-to-low) and also generates an interrupt. For example, the modem $\overline{DATA\ CARRIER\ DETECT}$ line could be connected to the $\overline{PSI}$ input on the UART in order to signal the microprocessor that transmission failed because of loss of the carrier on the communications line. The PSI and ES bits are stored in the Status Register (see Table 2).

TABLE 4. CONTROL REGISTER BIT ASSIGNMENT

BIT	7	6	5	4	3	2	1	0
SIGNAL	TR	BREAK	IE	WLS2	WLS1	SBS	EPE	PI

BIT SIGNAL: FUNCTION

0	PARITY INHIBIT (PI): When set high parity generation and verification are inhibited and the PE Status bit is held low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission, and EPE is ignored.
1	EVEN PARITY ENABLE (EPE): When set high, even parity is generated by the transmitter and checked by the receiver. When low, odd parity is selected.
2	STOP BIT SELECT (SBS): See table below.
3	WORD LENGTH SELECT 1 (WLS1): See table below.
4	WORD LENGTH SELECT 2 (WLS2): See table below.
5	INTERRUPT ENABLE (IE): When set high $\overline{THRE}$, DA, THRE • TSRE, $\overline{CTS}$, and PSI interrupts are enabled (see Interrupt Conditions, Table 1).
6	TRANSMIT BREAK (BREAK): Holds SDO low when set. Once the break bit in the control register has been set high, SDO will stay low until the break bit is reset low and one of the following occurs: $\overline{CLEAR}$ goes low; $\overline{CTS}$ goes high; or a word is transmitted. (The transmitted word will not be valid since there can be no start bit if SDO is already low. SDO can be set high without intermediate transitions by transmitting a word consisting of all zeros).
7	TRANSMIT REQUEST (TR): When set high, $\overline{RTS}$ is set low and data transfer through the transmitter is initiated by the initial $\overline{THRE}$ interrupt. (When loading the Control Register from the bus, this (TR) bit inhibits changing of other control flip-flops).

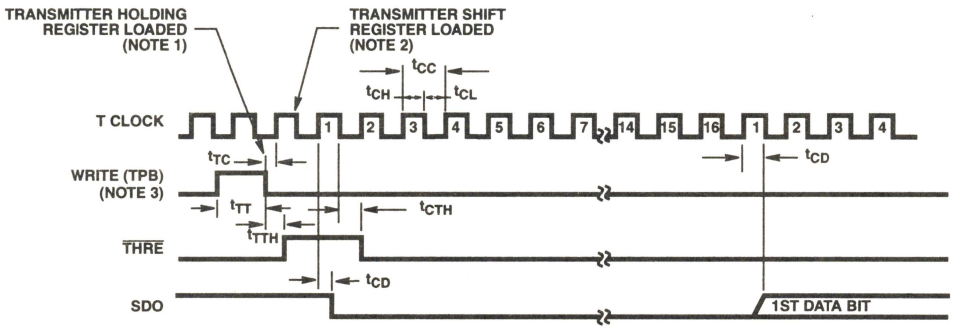
BIT 4 WLS2	BIT 3 WLS1	BIT 2 SBS	FUNCTION
0	0	0	5 data bits, 1 stop bit
0	0	1	5 data bits, 1.5 stop bits
0	1	0	6 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
1	0	1	7 data bits, 2 stop bits
1	1	0	8 data bits, 1 stop bit
1	1	1	8 data bits, 2 stop bits

Dynamic Electrical Specifications T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, (See Figure 3)

PARAMETER		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP1854AC		
			(NOTE 1) TYP	(NOTE 2) MAX	(NOTE 1) TYP	(NOTE 2) MAX	
TRANSMITTER TIMING - MODE 1							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	-	-	ns
Minimum Pulse Width							
Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	-	-	ns
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	-	-	ns
TPB	t_{TT}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Minimum Setup Time							
TPB to Clock	t_{TC}	5	175	225	175	225	ns
		10	90	150	-	-	ns
Propagation Delay Time							
Clock to Data Start Bit	t_{CD}	5	300	450	300	450	ns
		10	150	225	-	-	ns
TPB to $\overline{THRE}$	t_{TTH}	5	200	300	200	300	ns
		10	100	150	-	-	ns
Clock to $\overline{THRE}$	t_{CTH}	5	200	300	200	300	ns
		10	100	150	-	-	ns

NOTES:

1. Typical values for T_A = 25°C and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.



NOTES:

1. The holding register is loaded on the trailing edge of TPB.
2. The Transmitter Shift Register is loaded on the first high-to-low transition of the clock which occurs at least 1/2 clock period + t_{TC} after the trailing edge of TPB and transmission of a start bit occurs 1/2 clock period + t_{CD} later.
3. Write is the overlap of TPB, CS1, and CS3 = 1 and $\overline{CS3}$, RD/$\overline{WR}$ = 0.

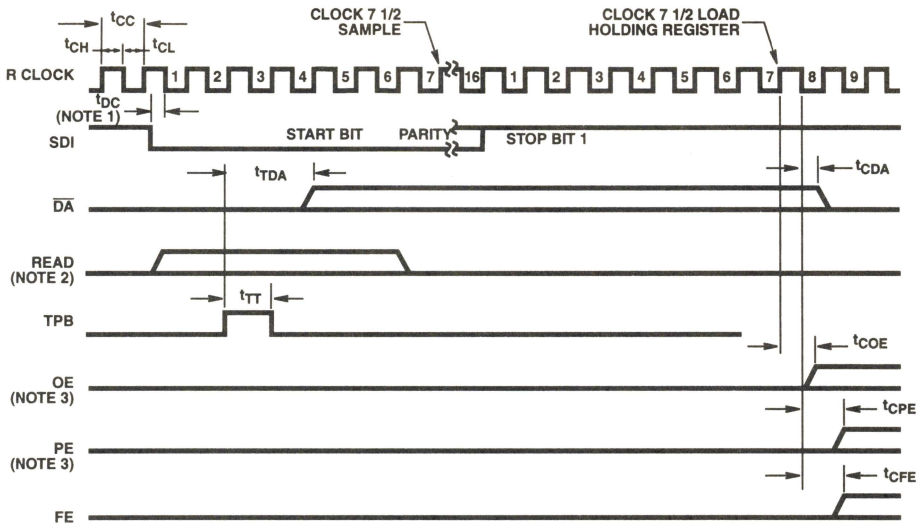
FIGURE 3. TRANSMITTER TIMING DIAGRAM - MODE 1

Dynamic Electrical Specifications T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, (See Figure 4)

PARAMETER		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP1854AC		
			(NOTE 1) TYP	(NOTE 2) MAX	(NOTE 1) TYP	(NOTE 2) MAX	
RECEIVER TIMING - MODE 1							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	-	-	ns
Minimum Pulse Width							
Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	-	-	ns
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	-	-	ns
TPB	t_{TT}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Minimum Setup Time							
Data Start Bit to Clock	t_{DC}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Propagation Delay Time							
TPB to $\overline{\text{DATA AVAILABLE}}$	t_{TDA}	5	220	325	220	325	ns
		10	110	175	-	-	ns
Clock to $\overline{\text{DATA AVAILABLE}}$	t_{CDA}	5	220	325	220	325	ns
		10	110	175	-	-	ns
Clock to Overrun Error	t_{COE}	5	210	300	210	300	ns
		10	105	150	-	-	ns
Clock to Parity Error	t_{CPE}	5	240	375	240	375	ns
		10	120	175	-	-	ns
Clock to Framing Error	t_{CFE}	5	200	300	200	300	ns
		10	100	150	-	-	ns

NOTES:

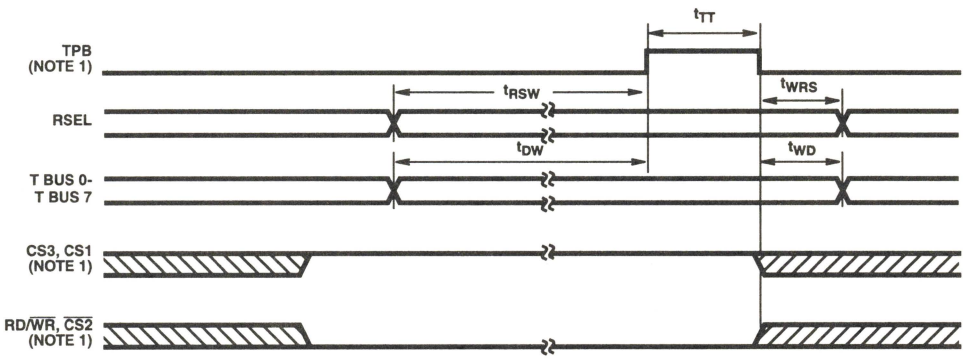
1. Typical values for T_A = 25°C and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.



NOTES:

1. If a start bit occurs at a time less than t_{DC} before a high-to-low transition of the clock, the start bit may not be recognized until the next high-to-low transition of the clock. The start bit may be completely asynchronous with the clock.
2. Read is the overlap of CS1, CS3, RD/$\overline{WR}$ = 1 and $\overline{CS2}$ = 0. If a pending DA has not been cleared by a read of the Receiver Holding Register by the time a new word is loaded into the Receiver Holding Register, the OE signal will come true.
3. OE and PE share terminal 15 and are also available as two separate bits in the status register.

FIGURE 4. MODE 1 RECEIVER TIMING DIAGRAM



NOTE:

1. Write is the overlap of TPB, CS1, CS3 = 1 and $\overline{CS2}$, RD/$\overline{WR}$ = 0.

FIGURE 5. MODE 1 CPU INTERFACE (WRITE) TIMING DIAGRAM

Dynamic Electrical Specifications T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, (See Figure 5)

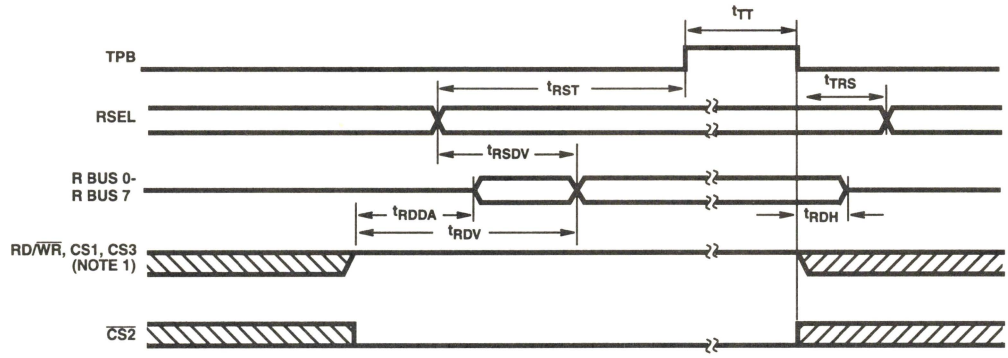
PARAMETER		V_{DD} (V)	LIMITS CDP1854A (NOTE 1) TYP	CDP1854A (NOTE 2) MAX	CDP1854AC (NOTE 1) TYP	CDP1854AC (NOTE 2) MAX	UNITS
CPU INTERFACE - WRITE TIMING - MODE 1							
Minimum Pulse Width TPB	t_{TT}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Minimum Setup Time RSEL to Write	t_{RSW}	5	50	75	50	75	ns
		10	25	40	-	-	ns
Data to Write	t_{DW}	5	-30	0	-30	0	ns
		10	-15	0	-	-	ns
Minimum Hold Time RSEL after Write	t_{WRS}	5	50	75	50	75	ns
		10	25	40	-	-	ns
Data after Write	t_{WD}	5	75	125	75	125	ns
		10	40	60	-	-	ns

NOTES:
1. Typical values for T_A = 25°C and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.

Dynamic Electrical Specifications T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, (See Figure 6)

PARAMETER		V_{DD} (V)	LIMITS CDP1854A MIN	CDP1854A (NOTE 1) TYP	CDP1854A (NOTE 2) MAX	CDP1854AC MIN	CDP1854AC (NOTE 1) TYP	CDP1854AC (NOTE 2) MAX	UNITS
CPU INTERFACE - READ TIMING - MODE 1									
Minimum Pulse Width TPB	t_{TT}	5	-	100	150	-	100	150	ns
		10	-	50	75	-	-	-	ns
Minimum Setup Time RSEL to TPB	t_{RST}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Minimum Hold Time RSEL after TPB	t_{TRS}	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
Read to Data Access Time	t_{RDDA}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	ns
Read to Data Valid Time	t_{RDV}	5	-	200	300	-	200	300	ns
		10	-	100	150	-	-	-	
RESEL to Data Valid Time	t_{RSDV}	5	-	150	225	-	150	225	ns
		10	-	75	125	-	-	-	ns
Hold Time Data after Read	t_{RDH}	5	50	150	-	50	150	-	ns
		10	25	75	-	-	-	-	ns

NOTES:
1. Typical values for T_A = 25°C and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.



NOTE:

1. Read is the overlap of CS1, CS3, RD/$\overline{WR}$ = 1 and $\overline{CS2}$ = 0.

FIGURE 6. MODE 1 CPU INTERFACE (READ) TIMING DIAGRAM

Mode Input Low (Mode = 0)

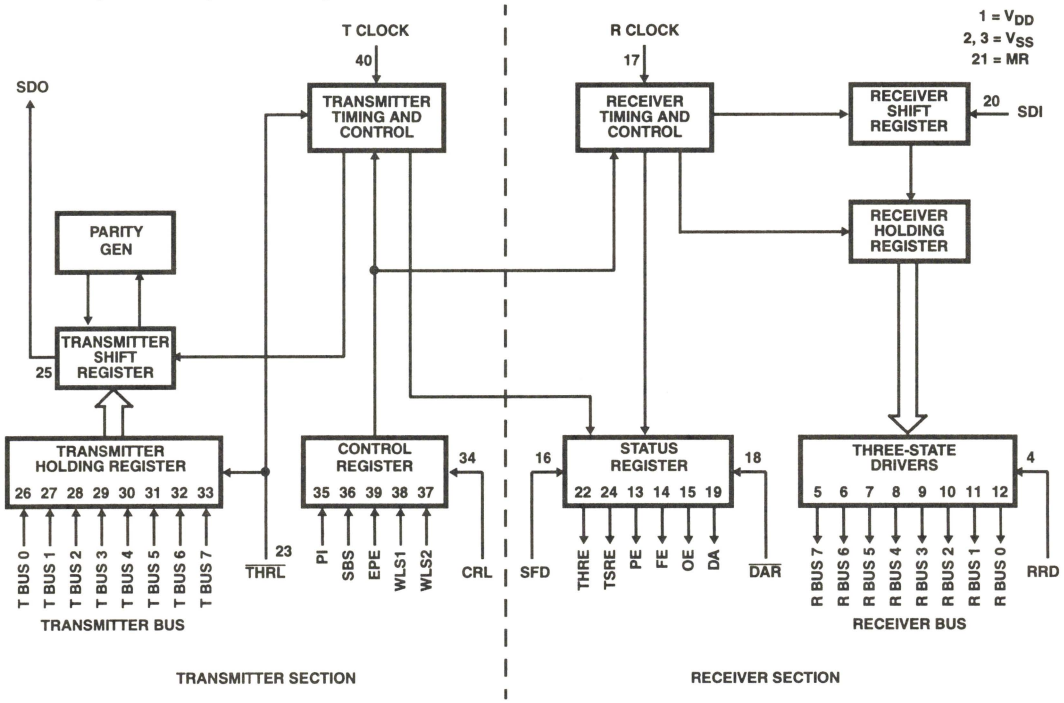


FIGURE 7. MODE 0 BLOCK DIAGRAM (INDUSTRY STANDARD COMPATIBLE)

Functional Definitions for CDP1854A Terminals Standard Mode 0

SIGNAL: FUNCTION

V_{DD}:

Positive supply voltage.

MODE SELECT (MODE):

A low-level voltage at this input selects Standard Mode 0 Operation.

V_{SS}:

Ground.

RECEIVER REGISTER DISCONNECT (RRD):

A high-level voltage applied to this input disconnects the Receiver Holding Register from the Receiver Bus.

RECEIVER BUS (R BUS 7 - R BUS 0):

Receiver parallel data outputs.

PARITY ERROR (PE):

A high-level voltage at this output indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This output is updated each time a character is transferred to the Receiver Holding Register. PE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

FRAMING ERROR (FE):

A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

OVERRUN ERROR (OE):

A high-level voltage at this output indicates that the DATA AVAILABLE (DA) flag was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

STATUS FLAG DISCONNECT (SFD):

A high-level voltage applied to this input disables the three-state output drivers for PE, FE, OE, DA, and THRE, allowing these status outputs to be bus connected.

RECEIVER CLOCK (RCLOCK):

Clock input with a frequency 16 times the desired receiver shift rate.

$\overline{\text{DATA AVAILABLE RESET}}$ ($\overline{\text{DAR}}$):

A low-level voltage applied to this input resets the DA flip-flop.

DATA AVAILABLE (DA):

A high-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

SERIAL DATA IN (SDI):

Serial data received at this input enters the receiver shift register at a point determined by the character length. A high-level voltage must be present when data is not being received.

MASTER RESET (MR):

A high-level voltage at this input resets the Receiver Holding Register, Control Register, and Status Register, and sets the serial data output high.

TRANSMITTER HOLDING REGISTER EMPTY (THRE):

A high-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.

$\overline{\text{TRANSMITTER HOLDING REGISTER LOAD}}$ ($\overline{\text{THRL}}$):

A low-level voltage applied to this input enters the character on the bus into the Transmitter Holding Register. Data is latched on the trailing edge of this signal.

TRANSMITTER SHIFT REGISTER EMPTY (TSRE):

A high-level voltage at this output indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains at this level until the start of transmission of the next character.

SERIAL DATA OUTPUT (SDO):

The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop bit(s)) are serially shifted out on this output. When no character is being transmitted, a high-level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.

TRANSMITTER BUS (T BUS 0 - T BUS 7):

Transmitter parallel data inputs.

CONTROL REGISTER LOAD (CRL):

A high-level voltage at this input loads the Control Register with the control bits (PI, EPE, SBS, WLS1, WLS2). This line may be strobed or hardwired to a high-level input voltage.

PARITY INHIBIT (PI):

A high-level voltage at this input inhibits the parity generation and verification circuits and will clamp the PE output low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission.

STOP BIT SELECT (SBS):

This input selects the number of stop bits to be transmitted after the parity bit. A high-level selects two stop bits, a low-level selects one stop bit. Selection of two stop bits with five data bits programmed selects 1.5 stop bits.

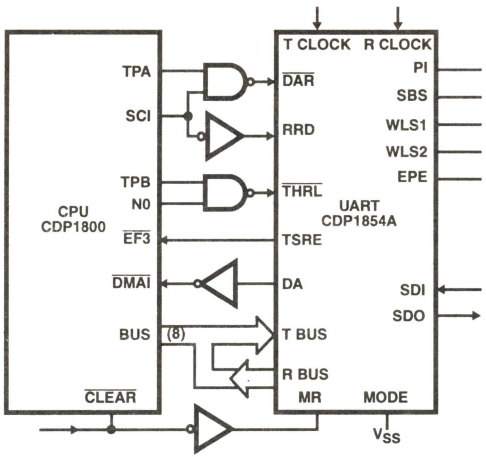


FIGURE 8. MODE 0 CONNECTION DIAGRAM

WORD LENGTH SELECT 2 (WLS2):

WORD LENGTH SELECT 1 (WLS1):

These two inputs select the character length (exclusive of parity) as follows:

WLS2	WLS1	WORD LENGTH
Low	Low	5 Bits
Low	High	6 Bits
High	Low	7 Bits
High	High	8 Bits

EVEN PARITY ENABLE (EPE):

A high-level voltage at this input selects even parity to be generated by the transmitter and checked by the receiver. A low-level input selects odd parity.

TRANSMITTER CLOCK (TCLOCK):

Clock input with a frequency 16 times the desired transmitter shift rate.

Description of Standard Mode 0 Operation (Mode Input = V_{SS})

Initialization and Controls

The MASTER RESET (MR) input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting the SERIAL DATA OUTPUT (SDO) signal high. Timing is generated from the clock inputs, Transmitter Clock (TCLOCK) and Receiver Clock (RCLOCK), at a frequency equal to 16 times the serial data bit rate. When the receiver data input rate and the transmitter data output rate are the same, the TCLOCK and RCLOCK inputs may be connected together. The CONTROL REGISTER LOAD (CRL) input is pulsed to store the control inputs PARITY INHIBIT (PI), EVEN PARITY ENABLE (EPE), STOP BIT SELECT (SBS), and WORD LENGTH SELECTs (WLS1 and WLS2). These inputs may be hardwired to the proper voltage levels (V_{SS} or V_{DD}) instead of being dynamically set and CRL may be hardwired to V_{DD}. The CDP1854A is then ready for transmitter and/or receiver operation.

Transmitter Operation

For the transmitter timing diagram refer to Figure 10. At the beginning of a typical transmitting sequence the Transmitter Holding Register is empty (THRE is HIGH). A character is transferred from the transmitter bus to the Transmitter Holding Register by applying a low pulse to the TRANSMITTER HOLDING REGISTER LOAD ($\overline{THRL}$) input causing THRE to go low. If the Transmitter Shift Register is empty (TSRE is HIGH) and the clock is low, on the next high-to-low transition of the clock the character is loaded into the Transmitter Shift Register preceded by a start bit. Serial data transmission begins 1/2 clock period later with a start bit and 5-8 data bits followed by the parity bit (if programmed) and stop bit(s). The THRE output signal goes high 1/2 clock period later on the high-to-low transition of the clock. When THRE goes high, another character can be loaded into the Transmitter Holding Register for transmission beginning with a start bit immediately following the last stop bit of the previous character. This process is repeated until all characters have been transmitted. When transmission is complete, THRE and Transmitter Shift Register Empty (TSRE) will both be high. The format of serial data is shown in Figure 12. Duration of each serial output data bit is determined by the transmitter clock frequency (^{f}CLOCK) and will be 16/f CLOCK.

Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After the detection of a high-to-low transition on the SD line, a divide-by-16 counter is enabled and a valid start bit is verified by checking for a low-level input 7-1/2 receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed), and stop bit(s) are shifted into the Receiver Shift Register at clock pulse 7-1/2 in each bit time. If programmed, the parity bit is checked, and receipt of a valid stop bit is verified. On count 7-1/2 of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output voltage level) are loaded into the unused most significant bits. If DATA AVAILABLE (DA) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) signal is raised. One-half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) signals become valid for the character in the Receiver Holding Register. The DA signal is also raised at this time. The three-state output drivers for DA, OE, PE and FE are enabled when STATUS FLAG DISCONNECT (SFD) is low. When RECEIVER REGISTER DISCONNECT (RRD) goes low, the receiver bus three-state output drivers are enabled and data is available at the RECEIVER BUS (R BUS 0 - R BUS 7) outputs. Applying a negative pulse to the DATA AVAILABLE RESET ($\overline{DAR}$) resets DA. The preceding sequence of operation is repeated for each serial character received. A receiver timing diagram is shown in Figure 11.

Dynamic Electrical Specifications T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, (See Figure 9)

PARAMETER		V_{DD} (V)	LIMITS CDP1854A (NOTE 1) TYP	LIMITS CDP1854A (NOTE 2) MAX	LIMITS CDP1854AC (NOTE 1) TYP	LIMITS CDP1854AC (NOTE 2) MAX	UNITS
INTERFACE TIMING - MODE 0							
Minimum Pulse Width CRL	t_{CRL}	5	100	150	100	150	ns
		10	50	75	-	-	ns
MR	t_{MR}	5	200	400	200	400	ns
		10	100	200	-	-	ns
Minimum Setup Time Control Word to CRL	t_{CWC}	5	40	80	40	80	ns
		10	20	50	-	-	ns
Minimum Hold Time Control Word after CRL	t_{CCW}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Propagation Delay Time SFD High to SOD	t_{SFDH}	5	200	300	200	300	ns
		10	100	150	-	-	ns
SFD Low to SOD	t_{SFDL}	5	75	120	75	120	ns
		10	40	60	-	-	ns
RRD High to Receiver Register High Impedance	t_{RRDH}	5	200	300	200	300	ns
		10	100	150	-	-	ns
RRD Low to Receiver Register Active	t_{RRDL}	5	100	150	100	150	ns
		10	50	75	-	-	ns

NOTES:

1. Typical values for T_A = 25°C and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.

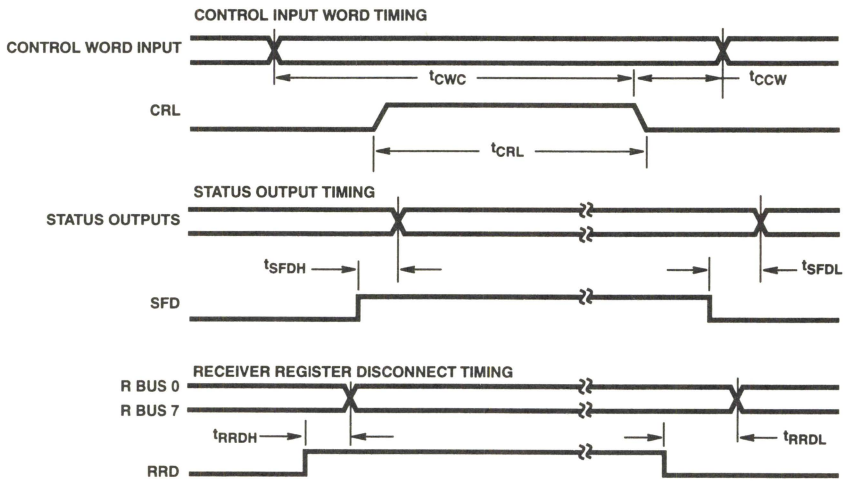


FIGURE 9. MODE 0 INTERFACE TIMING DIAGRAM

Dynamic Electrical Specifications $T_A = -40^oC$ to $+85^oC$, $V_{DD} \pm 5\%$, t_R, $t_F = 20ns$, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100pF$, (See Figure 10)

PARAMETER		V_{DD} (V)	LIMITS CDP1854A (NOTE 1) TYP	LIMITS CDP1854A (NOTE 2) MAX	LIMITS CDP1854AC (NOTE 1) TYP	LIMITS CDP1854AC (NOTE 2) MAX	UNITS
TRANSMITTER TIMING - MODE 0							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	-	-	ns
Minimum Pulse Width							
Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	-	-	ns
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	-	-	ns
$\overline{THRL}$	t_{THTH}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Minimum Setup Time							
$\overline{THRL}$ to Clock	t_{THC}	5	175	275	175	275	ns
		10	90	150	-	-	ns
Data to $\overline{THRL}$	t_{DT}	5	20	50	20	50	ns
		10	0	40	-	-	ns
Minimum Hold Time							
Data after $\overline{THRL}$	t_{TD}	5	80	120	80	120	ns
		10	40	60	-	-	ns
Propagation Delay Time							
Clock to Data Start Bit	t_{CD}	5	300	450	300	450	ns
		10	150	225	-	-	ns
Clock to THRE	t_{CT}	5	200	300	200	300	ns
		10	100	150	-	-	ns
$\overline{THRL}$ to THRE	t_{TTHR}	5	200	300	200	300	ns
		10	100	150	-	-	ns
Clock to TSRE	t_{TTS}	5	200	300	200	300	ns
		10	100	150	-	-	ns

NOTES:

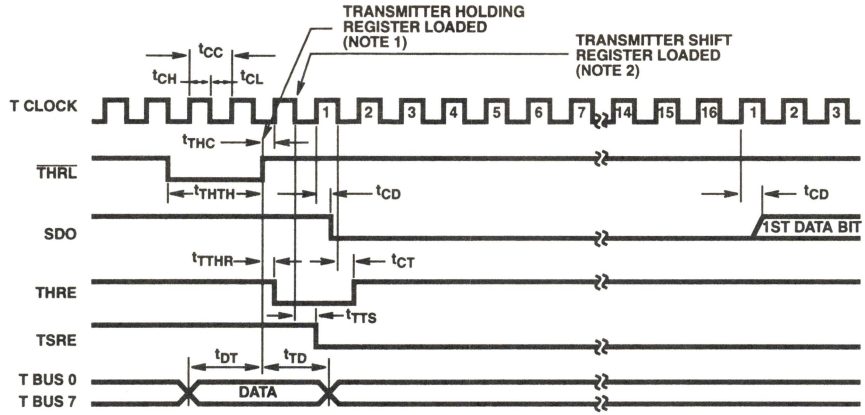
1. Typical values for $T_A = 25^oC$ and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.

Dynamic Electrical Specifications T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, (See Figure 11)

PARAMETER		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP1854AC		
			(NOTE 1) TYP	(NOTE 2) MAX	(NOTE 1) TYP	(NOTE 2) MAX	
RECEIVER TIMING - MODE 0							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	-	-	ns
Minimum Pulse Width							
Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	-	-	ns
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	-	-	ns
$\overline{\text{DATA AVAILABLE RESET}}$	t_{DD}	5	50	75	50	75	ns
		10	25	40	-	-	ns
Minimum Setup Time							
Data Start Bit to Clock	t_{DC}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Propagation Delay Time							
$\overline{\text{DATA AVAILABLE RESET}}$ to Data Available	t_{DDA}	5	150	225	150	225	ns
		10	75	125	-	-	ns
Clock to Data Valid	t_{CDV}	5	225	325	225	325	ns
		10	110	175	-	-	ns
Clock to Data Available	t_{CDA}	5	225	325	225	325	ns
		10	110	175	-	-	ns
Clock to Overrun Error	t_{COE}	5	210	300	210	300	ns
		10	100	150	-	-	ns
Clock to Parity Error	t_{CPE}	5	240	375	240	375	ns
		10	120	175	-	-	ns
Clock to Framing Error	t_{CFE}	5	200	300	200	300	ns
		10	100	150	-	-	ns

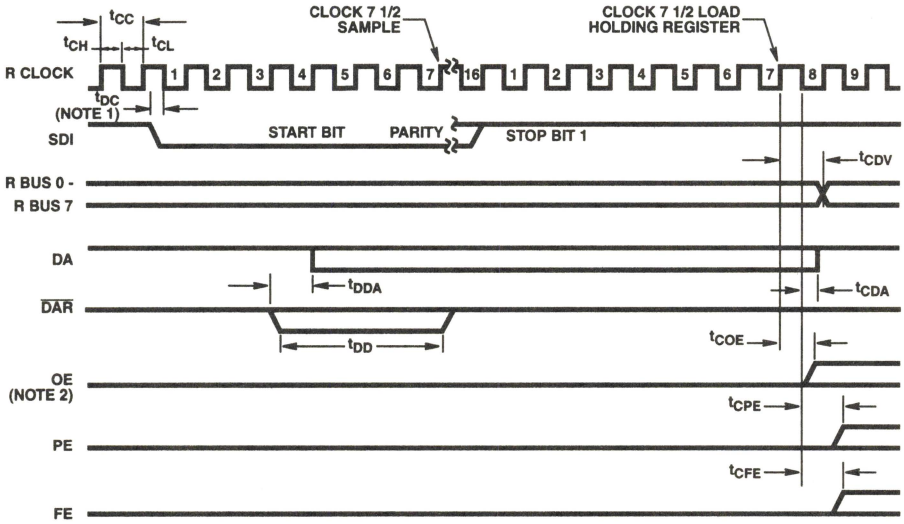
NOTES:

1. Typical values for T_A = 25°C and nominal voltages.
2. Maximum limits of minimum characteristics are the values above which all devices function.



NOTES:
1. The holding register is loaded on the trailing edge of $\overline{THRL}$.
2. The transmitter shift register, if empty, is loaded on the first high-to-low transition of the clock which occurs at least 1/2 clock period + t_{THC} after the trailing edge of $\overline{THRL}$ and transmission of a start bit occurs 1/2 clock period + t_{CD} later.

FIGURE 10. MODE 0 TRANSMITTER TIMING DIAGRAM



NOTES:
1. If a start bit occurs at a time less than t_{DC} before a high-to-low transition of the clock, the start bit may not be recognized until the next high-to-low transition of the clock. The start bit may be completely asynchronous with the clock.
2. If a pending DA has not been cleared by a read of the receiver holding register by the time a new word is loaded into the receiver holding register, the OE signal will come true.

FIGURE 11. MODE 0 RECEIVER TIMING DIAGRAM

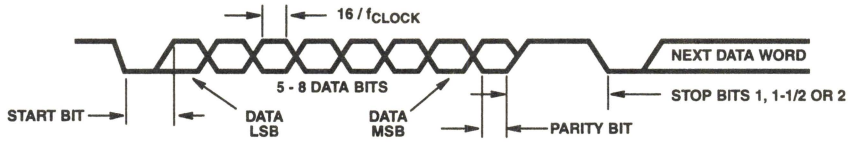


FIGURE 12. SERIAL DATA WORD FORMAT

HARRIS SEMICONDUCTOR

CDP1854A/3, CDP1854AC/3

High Reliability CMOS Programmable Universal Asynchronous Receiver/Transmitter (UART)

March 1997

Features

- Two Operating Modes
  - Mode 0 - Functionally Compatible with Industry Types Such as the TR1602A and CDP6402
  - Mode 1 - Interfaces Directly with CDP1800 Series Microprocessors without Additional Components
- Full or Half-Duplex Operation
- Parity, Framing, and Overrun Error Detection
- Fully Programmable with Externally Selectable Word Length (5-8 Bits), Parity Inhibit, Even/Odd Parity, and 1, 1-1/2, or 2 Stop Bits

Ordering Information

PACK-AGE	TEMP. RANGE	5V/200K BAUD	10V/400K BAUD	PKG. NO.
SBDIP	-55°C to +125°C	CDP1854ACD3	CDP1854ACD3	D40.6

Description

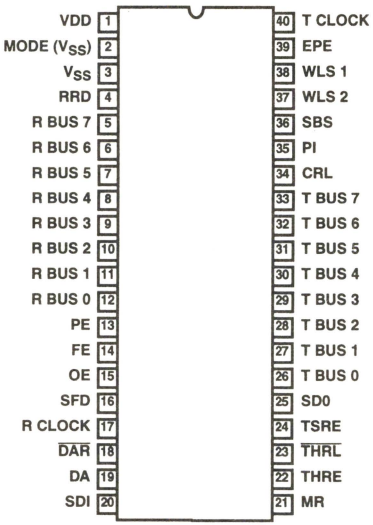
The CDP1854A/3 and CDP1854AC/3 are high reliability silicon gate CMOS Universal Asynchronous Receiver/Transmitter (UART) circuits. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data. For example, these UARTs can be used to interface between a peripheral or terminal with serial I/O ports and the 8-bit CDP1800-series microprocessor parallel data bus system. The CDP1854A/3 is capable of full duplex operation, i.e., simultaneous conversion of serial input data to parallel output data and parallel input data to serial output data.

The CDP1854A/3 UART can be programmed to operate in one of two modes by using the mode control input. When the mode input is high (MODE = 1), the CDP1854A/3 is directly compatible with the CDP1800 series microprocessor system without additional interface circuitry. When the mode input is low (MODE = 0), the device is functionally compatible with industry standard UARTs such as the TR1602A and CDP6402. It is also pin compatible with these types, except that pin 2 is used for the mode control input.

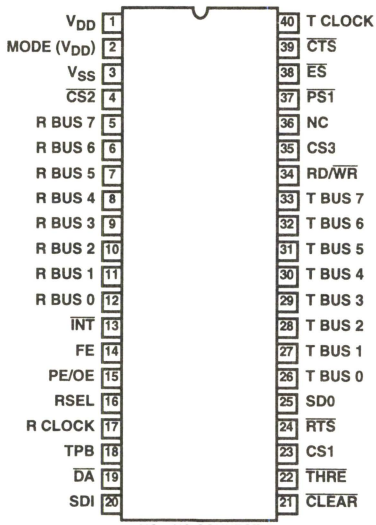
The CDP1854A/3 and the CDP1854AC/3 are functionally identical. The CDP1854A/3 has a recommended operating voltage range of 4V to 10.5V, and the CDP1854AC/3 has a recommended operating voltage range of 4V to 6.5V.

Pinouts

CDP1854A/3, CDP1854AC/3 (SBDIP) (MODE 0)
TOP VIEW



CDP1854A/3, CDP1854AC/3 (SBDIP) (MODE 1)
TOP VIEW



NC = NO CONNECT

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

File Number 1715.2

Absolute Maximum Ratings

DC Supply-Voltage Range, (V_{DD})
(All voltages referenced to V_{SS} terminal)
CDP1854A/3 . . . . . -0.5 to +11V
CDP1854AC/3 . . . . . -0.5 to +7V
Input Voltage Range, All Inputs . . . . . -0.5 to V_{DD} +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Device Dissipation Per Output Transistor
For T_A = Full Package-Temperature Range 100mW
Operating-Temperature Range (T_A)
Package Type D . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	55	15

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range (T_{STG}) . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s)
At Distance 1/16 ±1/32 inch (1.59 ±0.79mm) . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Static Electrical Specifications

PARAMETER		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS -55°C, +25°C MIN	LIMITS -55°C, +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
Quiescent Device Current	I_{DD}	-	0, 5	5	-	500	-	1000	µA
		-	0, 10	10	-	500	-	1000	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	0.75	-	0.5	-	mA
		0.5	0, 10	10	1.80	-	1.2	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-	-0.5	-	-0.35	mA
		9.5	0, 10	10	-	-1.0	-	-0.70	mA
Output Voltage Low-Level (Note 1)	V_{OL}	-	0, 5	5	-	0.1	-	0.2	V
		-	0, 10	10	-	0.1	-	0.2	V
Output Voltage High Level (Note 1)	V_{OH}	-	0, 5	5	4.9	-	4.9	-	V
		-	0, 10	10	9.9	-	9.8	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	1.5	-	1.5	V
		0.5, 9.5	-	10	-	3	-	3	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	V
		0.5, 9.5	-	10	7	-	7	-	V
Input Leakage Current	I_{IN}	-	0, 5	5	-	±1	-	±5	µA
		-	0, 10	10	-	±1	-	±5	µA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	±1	-	±10	µA
		0, 10	0, 10	10	-	±1	-	±10	µA
Input Capacitance (Note 1)	C_{IN}	-	-	-	-	10	-	10	pF
Output Capacitance (Note 1)	C_{OUT}	-	-	-	-	15	-	15	pF

NOTE:

1. Guaranteed but not tested.

Operating Conditions At T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

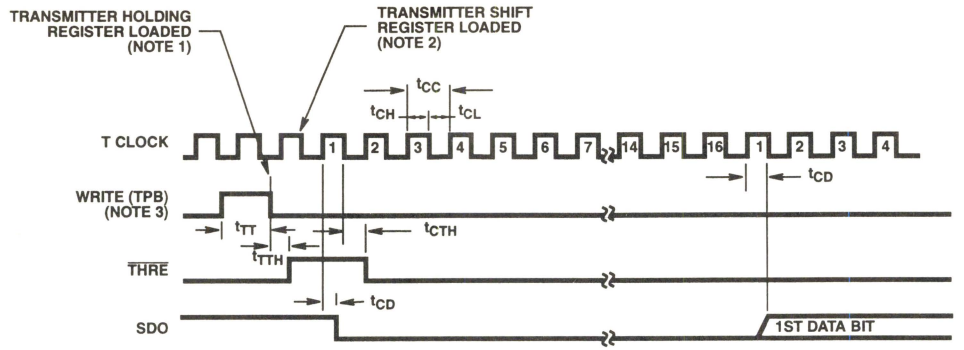
PARAMETER	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	-55°C, +25°C		+125°C		
		MIN	MAX	MIN	MAX	
DC Operating Voltage Range	-	4	10.5	4	6.5	V
Input Voltage Range	-	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Baud Rate (Receive or Transmit)	5	-	250	-	215	K bits/s
	10	-	520	-	430	K bits/s

Dynamic Electrical Specifications t_R, t_F = 15ns, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, C_L = 100pF, (See Figure 1)

PARAMETER		V_{DD} (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			MIN	MAX	MIN	MAX	
TRANSMITTER TIMING - MODE 1							
Clock Period	t_{CC}	5	240	-	280	-	ns
		10	120	-	145	-	ns
Pulse Width Clock Low Level	t_{CL}	5	105	-	125	-	ns
		10	55	-	65	-	ns
Clock High Level	t_{CH}	5	135	-	155	-	ns
		10	65	-	80	-	ns
TPB	t_{TT}	5	125	-	165	-	ns
		10	70	-	80	-	ns
Propagation Delay Time Clock to Data Start Bit	t_{CD}	5	-	425	-	485	ns
		10	-	205	-	235	ns
TPB to $\overline{THRE}$	t_{TTH}	5	-	315	-	380	ns
		10	-	155	-	185	ns
Clock to $\overline{THRE}$	t_{CTH}	5	-	335	-	390	ns
		10	-	160	-	190	ns

Dynamic Electrical Specifications t_R, t_F = 15ns, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, C_L = 100pF, (See Figure 2)

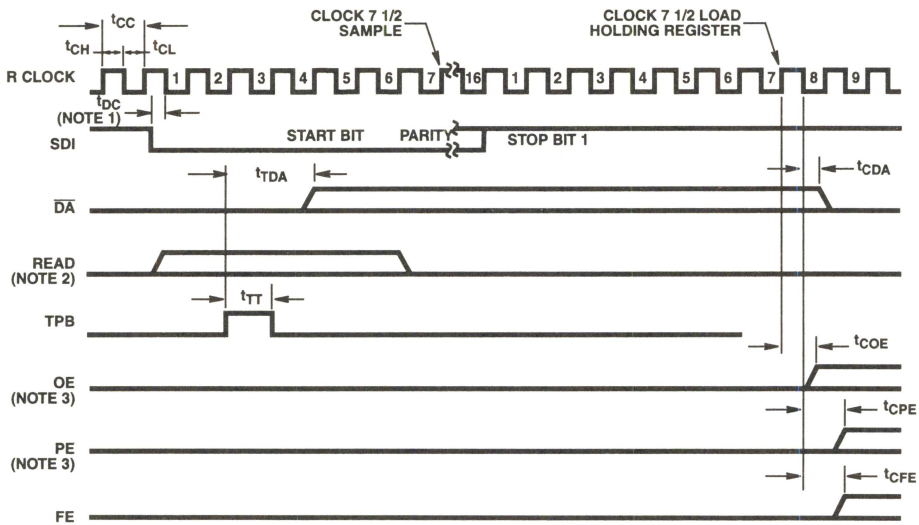
PARAMETER		V_{DD} (V)	LIMITS -55°C, +25°C MIN	LIMITS -55°C, +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
RECEIVER TIMING - MODE 1							
Clock Period	t_{CC}	5	240	-	280	-	ns
		10	120	-	145	-	ns
Pulse Width							
Clock Low Level	t_{CL}	5	105	-	125	-	ns
		10	55	-	65	-	ns
Clock High Level	t_{CH}	5	135	-	155	-	ns
		10	65	-	80	-	ns
TPB	t_{TT}	5	125	-	165	-	ns
		10	70	-	80	-	ns
Setup Time							
Data Start Bit to Clock	t_{DC}	5	105	-	120	-	ns
		10	65	-	70	-	ns
Propagation Delay Time							
TPB to $\overline{\text{DATA AVAILABLE}}$	t_{TDA}	5	-	295	-	340	ns
		10	-	150	-	170	ns
Clock to $\overline{\text{DATA AVAILABLE}}$	t_{CDA}	5	-	305	-	355	ns
		10	-	150	-	170	ns
Clock to Overrun Error	t_{COE}	5	-	305	-	330	ns
		10	-	150	-	175	ns
Clock to Parity Error	t_{CPE}	5	-	305	-	330	ns
		10	-	150	-	175	ns
Clock to Framing Error	t_{CFE}	5	-	280	-	330	ns
		10	-	145	-	165	ns



NOTES:

1. The holding register is loaded on the trailing edge of TPB.
2. The transmitter shift register, if empty, is loaded on the first high-to-low transition of the clock which occurs at least 1/2 clock period + t_{TC} after the trailing edge of TPB and transmission of a start bit occurs 1/2 clock period + t_{CD} later.
3. Write is the overlap of TPB, CS1, and CS3 = 1 and $\overline{CS3}$, RD/$\overline{WR}$ = 0

FIGURE 1. TRANSMITTER TIMING DIAGRAM - MODE 1



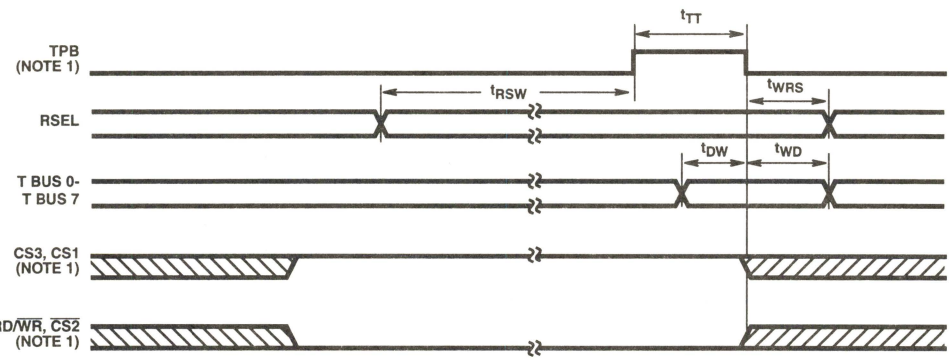
NOTES:

1. If a start bit occurs at a time less than t_{DC} before a high-to-low transition of the clock, the start bit may not be recognized until the next high-to-low transition of the clock. The start bit may be completely asynchronous with the clock.
2. Read is the overlap of CS1, CS3, RD/$\overline{WR}$ = 1 and $\overline{CS2}$ = 0. If a pending DA has not been cleared by a read of the receiver holding register by the time a new word is loaded into the receiver holding register, the OE signal will come true.
3. OE and PE share terminal 15 and are also available as two separate bits in the status register.

FIGURE 2. MODE 1 RECEIVER TIMING DIAGRAM

Dynamic Electrical Specifications t_R, t_F = 15ns, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, C_L = 100pF, (See Figure 3)

PARAMETER		V_{DD} (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			MIN	MAX	MIN	MAX	
CPU INTERFACE - WRITE TIMING - MODE 1							
Pulse Width							
TPB	t_{TT}	5	125	-	165	-	ns
		10	70	-	80	-	ns
Setup Time							
RSEL to Write	t_{RSW}	5	20	-	10	-	ns
		10	25	-	25	-	ns
Data to Write	t_{DW}	5	65	-	75	-	ns
		10	45	-	50	-	ns
Hold Time							
RSEL after Write	t_{WRS}	5	-10	-	-20	-	ns
		10	5	-	5	-	ns
Data after Write	t_{WD}	5	95	-	105	-	ns
		10	55	-	55	-	ns



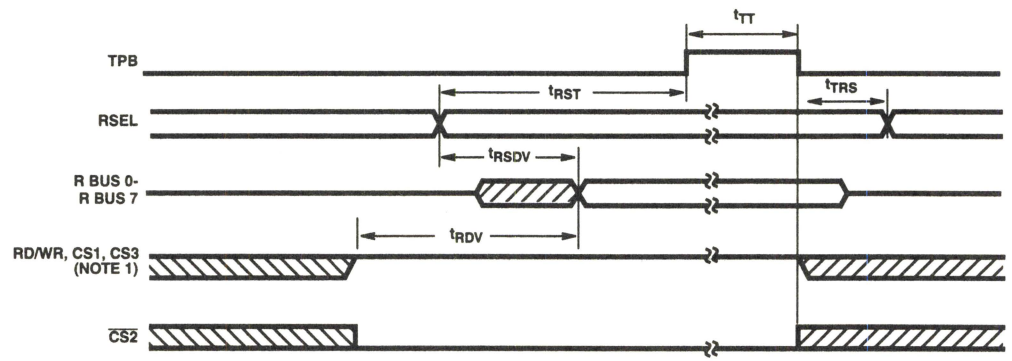
NOTE:

1. Write is the overlap of TPB, CS1, CS3 = 1 and $\overline{CS2}$, RD/$\overline{WR}$ = 0.

FIGURE 3. MODE 1 CPU INTERFACE (WRITE) TIMING DIAGRAM

Dynamic Electrical Specifications t_R, t_F = 15ns, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, C_L = 100pF, (See Figure 4)

PARAMETER		V_{DD} (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			MIN	MAX	MIN	MAX	
CPU INTERFACE - READ TIMING - MODE 1							
Pulse Width							
TPB	t_{TT}	5	125	-	165	-	ns
		10	70	-	80	-	ns
Setup Time							
RSEL to TPB	t_{RST}	5	15	-	0	-	ns
		10	20	-	10	-	ns
Hold Time							
RSEL after TPB	t_{TRS}	5	-10	-	-25	-	ns
		10	5	-	0	-	ns
Propagation Delay Time							
Read to Data Valid Time	t_{RDV}	5	-	360	-	420	ns
		10	-	165	-	195	ns
RESEL to Data Valid Time	t_{RSDV}	5	-	250	-	295	ns
		10	-	125	-	145	ns



NOTE:

1. Read is the overlap of CS1, CS3, RD/$\overline{WR}$ = 1 and $\overline{CS2}$ = 0.

FIGURE 4. MODE 1 CPU INTERFACE (READ) TIMING DIAGRAM

Dynamic Electrical Specifications t_R, t_F = 15ns, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, C_L = 100pF, (See Figure 5)

PARAMETER		V_{DD} (V)	LIMITS -55°C, +25°C MIN	LIMITS -55°C, +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
INTERFACE TIMING - MODE 0							
Pulse Width CRL	t_{CRL}	5	105	-	125	-	ns
		10	55	-	65	-	ns
MR	t_{MR}	5	340	-	385	-	ns
		10	160	-	175	-	ns
Setup Time Control Word to CRL	t_{CWC}	5	80	-	85	-	ns
		10	40	-	60	-	ns
Hold Time Control Word after CRL	t_{CCW}	5	65	-	65	-	ns
		10	45	-	45	-	ns
Propagation Delay Time SFD High to SOD	t_{SFDH}	5	-	175	-	195	ns
		10	-	105	-	115	ns
SFD Low to SOD	t_{SFDL}	5	165	-	195	-	ns
		10	90	-	105	-	ns
RRD High to Receiver Register High Impedance	t_{RRDH}	5	-	185	-	205	ns
		10	-	110	-	130	ns
RRD Low to Receiver Register Active	t_{RRDL}	5	165	-	195	-	ns
		10	90	-	105	-	ns

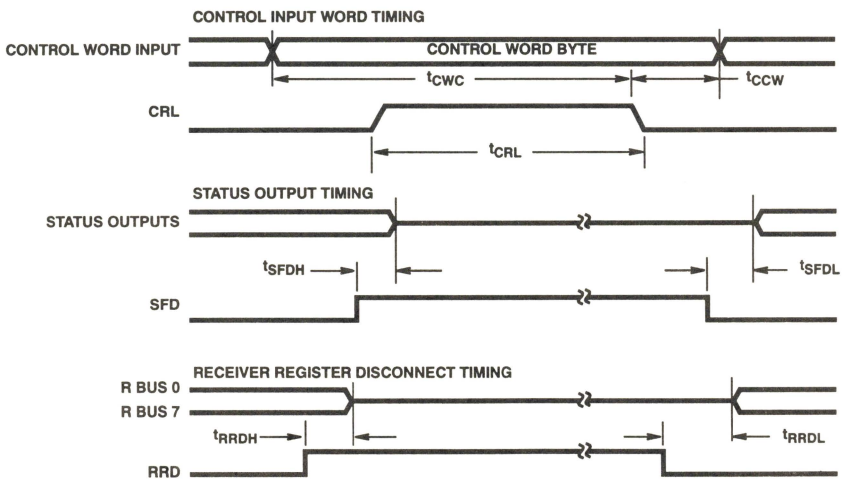
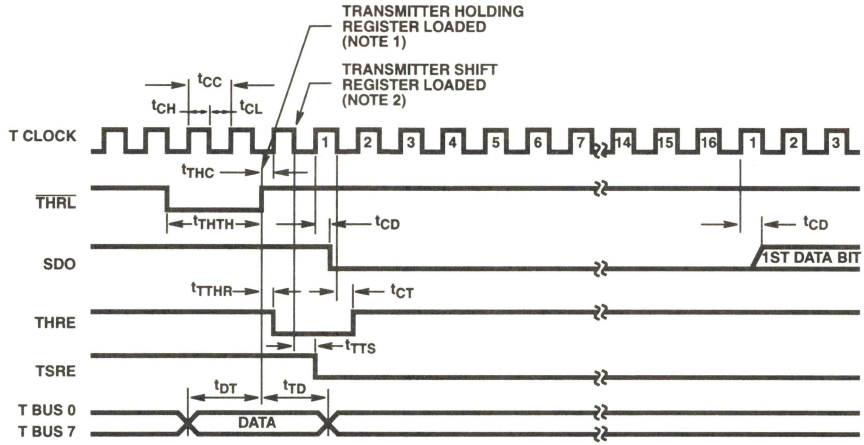


FIGURE 5. MODE 0 INTERFACE TIMING DIAGRAM

Dynamic Electrical Specifications t_R, t_F = 15ns, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, C_L = 100pF, (See Figure 6)

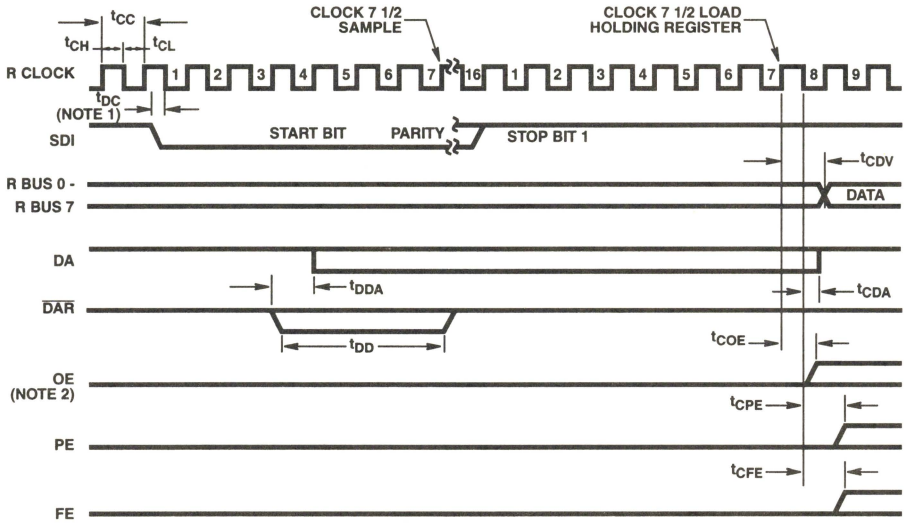
PARAMETER		V_{DD} (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			MIN	MAX	MIN	MAX	
TRANSMITTER TIMING - MODE 0							
Clock Period	t_{CC}	5	240	-	280	-	ns
		10	120	-	145	-	ns
Pulse Width							
Clock Low Level	t_{CL}	5	105	-	125	-	ns
		10	55	-	65	-	ns
Clock High Level	t_{CH}	5	135	-	155	-	ns
		10	65	-	80	-	ns
$\overline{THRL}$	t_{THTH}	5	140	-	165	-	ns
		10	80	-	85	-	ns
Setup Time							
$\overline{THRL}$ to Clock	t_{THC}	5	205	-	235	-	ns
		10	120	-	140	-	ns
Data to $\overline{THRL}$	t_{DT}	5	25	-	30	-	ns
		10	20	-	25	-	ns
Hold Time							
Data after $\overline{THRL}$	t_{TD}	5	60	-	95	-	ns
		10	45	-	75	-	ns
Propagation Delay Time							
Clock to Data Start Bit	t_{CD}	5	-	435	-	505	ns
		10	-	205	-	235	ns
Clock to THRE	t_{CT}	5	-	345	-	420	ns
		10	-	175	-	200	ns
$\overline{THRL}$ to THRE	t_{TTHR}	5	-	275	-	325	ns
		10	-	145	-	165	ns
Clock to TSRE	t_{TTS}	5	-	345	-	405	ns
		10	-	165	-	190	ns



NOTES:

1. The holding register is loaded on the trailing edge of $\overline{THRL}$.
2. The transmitter shift register, if empty, is loaded on the first high-to-low transition of the clock which occurs at least 1/2 clock period + t_{THC} after the trailing edge of $\overline{THRL}$ and transmission of a start bit occurs 1/2 clock period + t_{CD} later.

FIGURE 6. MODE 0 TRANSMITTER TIMING DIAGRAM



NOTES:

1. If a start bit occurs at a time less than t_{DC} before a high-to-low transition of the clock, the start bit may not be recognized until the next high-to-low transition of the clock. The start bit may be completely asynchronous with the clock.
2. If a pending DA has not been cleared by a read of the receiver holding register by the time a new word is loaded into the receiver holding register, the OE signal will come true.

FIGURE 7. MODE 0 RECEIVER TIMING DIAGRAM

Dynamic Electrical Specifications t_R, t_F = 15ns, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, C_L = 100pF, (See Figure 7)

PARAMETER		V_{DD} (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			MIN	MAX	MIN	MAX	
RECEIVER TIMING - MODE 0							
Clock Period	t_{CC}	5	240	-	280	-	ns
		10	120	-	145	-	ns
Pulse Width							
Clock Low Level	t_{CL}	5	105	-	125	-	ns
		10	55	-	65	-	ns
Clock High Level	t_{CH}	5	135	-	155	-	ns
		10	65	-	80	-	ns
$\overline{\text{DATA AVAILABLE RESET}}$	t_{DD}	5	75	-	90	-	ns
		10	45	-	50	-	ns
Setup Time							
Data Start Bit to Clock	t_{DC}	5	105	-	130	-	ns
		10	65	-	85	-	ns
Propagation Delay Time							
$\overline{\text{DATA AVAILABLE RESET}}$ to Data Available	t_{DDA}	5	-	240	-	280	ns
		10	-	130	-	145	ns
Clock to Data Valid	t_{CDV}	5	-	360	-	420	ns
		10	-	175	-	195	ns
Clock to Data Available	t_{CDA}	5	-	320	-	375	ns
		10	-	155	-	180	ns
Clock to Overrun Error	t_{COE}	5	-	365	-	415	ns
		10	-	170	-	190	ns
Clock to Parity Error	t_{CPE}	5	-	275	-	320	ns
		10	-	135	-	155	ns
Clock to Framing Error	t_{CFE}	5	-	270	-	320	ns
		10	-	135	-	165	ns

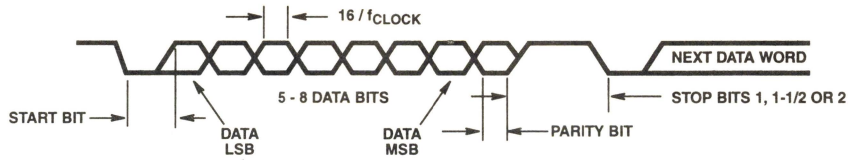
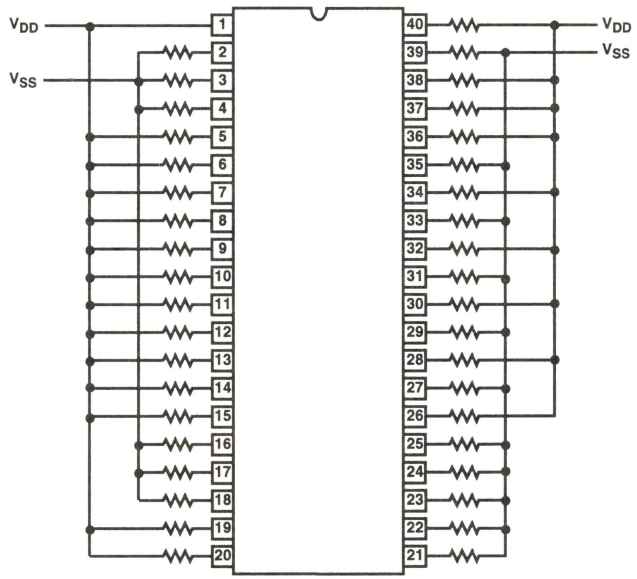


FIGURE 8. SERIAL DATA WORD FORMAT

Burn-In Circuit



ALL RESISTORS ARE 47kΩ ±20%

TYPE	V_{DD}	TEMPERATURE	TIME
CDP1854A/3	11	+125°C	160 hrs.
CDP1854AC/3	7	+125°C	160 hrs.

FIGURE 9. BIAS/STATIC BURN-IN CIRCUIT

HARRIS SEMICONDUCTOR

CDP6402, CDP6402C

CMOS Universal Asynchronous Receiver/Transmitter (UART)

March 1997

Features

- Low Power CMOS Circuitry . . . . . 7.5mW (Typ) at 3.2MHz (Max Freq.) at V_{DD} = 5V
- Baud Rate
  - DC to 200K Bits/s (Max) at . . . . . 5V, 85°C
  - DC to 400K Bits/s (Max) at . . . . . 10V, 85°C
- 4V to 10.5 Operation
- Automatic Data Formatting and Status Generation
- Fully Programmable with Externally Selectable Word Length (5 - 8 Bits), Parity Inhibit, Even/Odd Parity, and 1, 1-1/2, or 2 Stop Bits
- Operating Temperature Range
  - CDP6402D, CD . . . . . -55°C to +125°C
  - CDP6402E, CE . . . . . -40°C to +85°C
- Replaces Industry Type IM6402 and Compatible with HD6402

Ordering Information

PACK-AGE	TEMP. RANGE	5V/200K BAUD	10V/400K BAUD	PKG. NO.
PDIP	-40°C to +85°C	CDP6402CE	CDP6402E	E40.6
Burn-In		CDP6402CEX	-	
SBDIP	-40°C to +85°C	CDP6402CD	CDP6402D	D40.6
Burn-In		CDP6402CDX	CDP6402DX	

Description

The CDP6402 and CDP6402C are silicon gate CMOS Universal Asynchronous Receiver/Transmitter (UART) circuits for interfacing computers or microprocessors to asynchronous serial data channels. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data channels. The receiver converts serial start, data, parity, and stop bits to parallel data verifying proper code transmission, parity and stop bits. The transmitter converts parallel data into serial form and automatically adds start parity and stop bits.

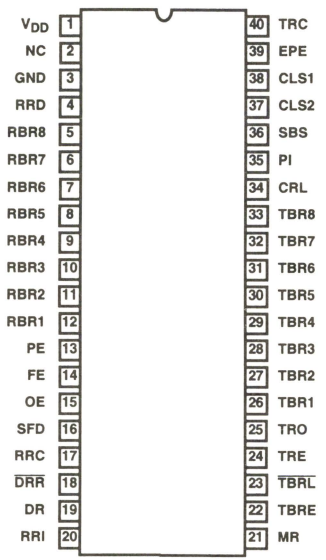
The data word can be 5, 6, 7 or 8 bits in length. Parity may be odd, even or inhibited. Stop bits can be 1, 1-1/2, or 2 (when transmitting 5-bit code).

The CDP6402 and CDP6402C can be used in a wide range of applications including modems, printers, peripherals, video terminals, remote data acquisition systems, and serial data links for distributed processing systems.

The CDP6402 and CDP6402C are functionally identical. They differ in that the CDP6402 has a recommended operating voltage range of 4V to 10.5V, and the CDP6402C has a recommended operating voltage range of 4V to 6.5V.

Pinout

CDP6402, CDP6402C (PDIP, SBDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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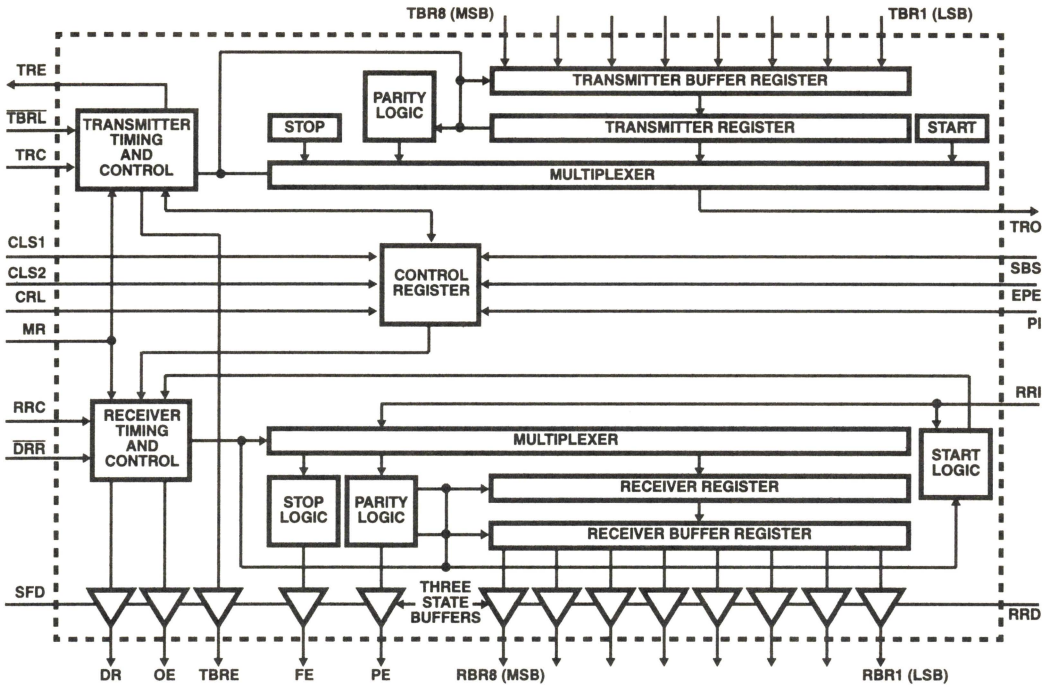


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

Absolute Maximum Ratings

DC Supply-Voltage Range, (V_{DD})
- CDP6402 . . . . . -0.5 to +11V
- CDP6402C . . . . . -0.5 to +7V

Input Voltage Range, All Inputs . . . . . -0.5 to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±100µA
Device Dissipation Per Output Transistor
- For T_A = Full Package-Temperature Range (All Package Types) 100mW

Operating-Temperature Range (T_A)
- Package Type D (SBDIP) . . . . . -55°C to +125°C
- Package Type E (PDIP) . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	50	N/A
SBDIP Package	55	15

Maximum Junction Temperature
- Plastic Package . . . . . +150°C
- Ceramic Package . . . . . +175°C

Maximum Storage Temperature Range (T_{STG}) . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s):
- At Distance 1/16 ±1/32 inch (1.59 ±0.79mm) . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Operating Conditions At T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS				UNITS
	CDP6402		CDP6402C		
	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Static Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ±10%, Except as noted

PARAMETER		CONDITIONS			LIMITS						UNITS
					CDP6402			CDP6402C			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	0.01	50	-	0.02	200	µA
		-	0,10	10	-	1	200	-	-	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0,5	5	2	4	-	1.2	2.4	-	mA
		0.5	0,10	10	5	7	-	-	-	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-0.55	-1.1	-	-0.55	-1.1	-	mA
		9.5	0,10	10	-1.3	-2.6	-	-	-	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	0.8	-	-	0.8	V
		0.5, 9.5	-	10	-	-	0.2 V_{DD}	-	-	-	V

Static Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ±10%, Except as noted **(Continued)**

PARAMETER		CONDITIONS			LIMITS						UNITS
					CDP6402			CDP6402C			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Input High Voltage	V_{IH}	0.5, 4.5	-	5	V_{DD}-2	-	-	V_{DD}-2	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	Any Input	0,5	5	-	$\pm10^{-4}$	±1	-	-	±1	µA
			0,10	10	-	$\pm10^{-4}$	±2	-	-	-	µA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	$\pm10^{-4}$	±1	-	$\pm10^{-4}$	±1	µA
		0, 10	0,10	10	-	$\pm10^{-4}$	±10	-	-	-	µA
Operating Current (Note 3)	I_{DD1}	-	0, 5	5	-	1.5	–	-	1.5	-	mA
		-	0,10	10	-	10	–	-	-	-	mA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = 25°C and nominal V_{DD}
2. $I_{OL} = I_{OH}$ = 1µA.
3. Operating current is measured at 200kHz or V_{DD} = 5V and 400kHz for V_{DD} = 10V, with open outputs (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2MHz).

Description of Operation

Initialization and Controls

A positive pulse on the MASTER RESET (MR) input resets the control, status, and receiver buffer registers, and sets the serial output (TRO) High. Timing is generated from the clock inputs RRC and TRC at a frequency equal to 16 times the serial data bit rate. The RRC and TRC inputs may be driven by a common clock, or may be driven independently by two different clocks. The CONTROL REGISTER LOAD (CRL) input is strobed to load control bits for PARITY INHIBIT (PI), EVEN PARITY ENABLE (EPE), STOP BIT SELECTS (SBS), and CHARACTER LENGTH SELECTS (CLS1 and CLS2). These inputs may be hand wired to V_{SS} or V_{DD} with CRL to V_{DD}. When the initialization is completed, the UART is ready for receiver and/or transmitter operations.

Transmitter Operation

The transmitter section accepts parallel data, formats it, and transmits it in serial form (Figure 2) on the TRO terminal.

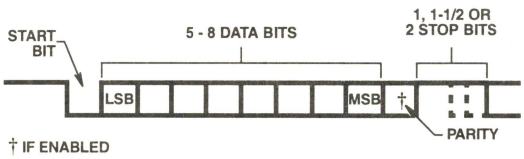


FIGURE 2. SERIAL DATA FORMAT

Transmitter timing is shown in Figure 3. (A) Data is loaded into the transmitter buffer register from the inputs TBR1 through TBR8 by a logic low on the $\overline{TBRL}$ input. Valid data must be present at least t_{DT} prior to, and t_{TD} following, the rising edge of $\overline{TBRL}$. If words less than 8-bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. (B) The rising edge of $\overline{TBRL}$ clears TBRE. 1/2 to 11/2 cycles later, depending on when the $\overline{TBRL}$ pulse occurs with respect to TRC, data is transferred to the transmitter register and TRE is cleared. TBRE is set to a logic High one cycle after that.

Output data is clocked by TRC. The clock rate is 16 times the data rate. (C) A second pulse on $\overline{TBRL}$ loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. (D) Data is automatically transferred to the transmitter register and transmission of that character begins.

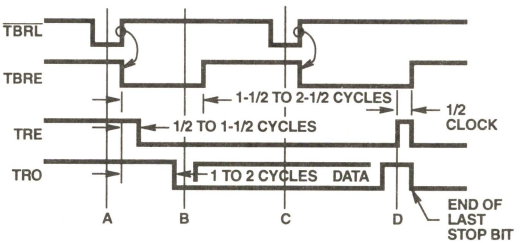


FIGURE 3. TRANSMITTER TIMING WAVEFORMS

Receiver Operation

Data is received in serial form at the RRI input. When no data is being received, RRI input must remain high. The data is clocked through the RRC. The clock rate is 16 times the data rate. Receiver timing is shown in Figure 4.

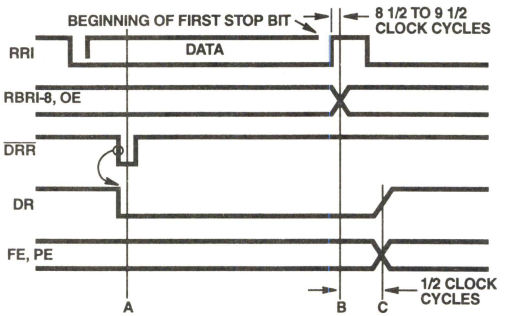


FIGURE 4. RECEIVER TIMING WAVEFORMS

(A) A low level on $\overline{DRR}$ clears the DR line. (B) During the first stop bit data is transferred from the receiver register to the RB Register. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OE indicates overruns. An overrun occurs when DR has not been cleared before the present character was transferred to the RBR. (C) 1/2 clock cycle later DR is set to a logic high and FE is evaluated. A logic high on FE indicates an invalid stop bit was received. A logic high on PE indicates a parity error.

Start Bit Detection

The receiver uses a 16X clock for timing (Figure 5). The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7 1/2. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±1/2 clock cycle ±1/32 bit or ±3.125%. The receiver begins searching for the next start bit at 9 clocks into the first stop bit.

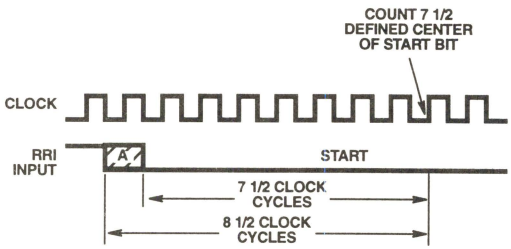


FIGURE 5. START BIT TIMING WAVEFORMS

TABLE 1. CONTROL WORD FUNCTION

CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT (S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

NOTE: X = Don't Care

TABLE 2. FUNCTION PIN DEFINITION

PIN	SYMBOL	DESCRIPTION
1	V_{DD}	Positive Power Supply
2	N/C	No Connection
3	GND	Ground (V_{SS})
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register ouputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 - RBR8
7	RBR6	
8	RBR5	
9	RBR4	
10	RBR3	
11	RBR2	
12	RBR1	
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits. The output is active until parity matches on a succeeding character. When parity is inhibited, this output is low.
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE will stay active until the next valid character's stop bit is received.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. The Error is reset at the next character's stop bit if DRR has been performed (i.e., DRR; active low).
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	RRC	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	$\overline{DRR}$	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE and DR, and sets TRE, TBRE, and TRO. TRE is actually set on the first rising edge of TRC after MR goes high. MR should be strobed after power-up.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	$\overline{TBRL}$	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on $\overline{TBRL}$ requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.

TABLE 2. FUNCTION PIN DEFINITION (Continued)

PIN	SYMBOL	DESCRIPTION
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8 bits, the TBR8, 7, and 6 Inputs are ignored corresponding to the programmed word length.
27	TBR2	See Pin 26 - TBR1
28	TBR3	
29	TBR4	
30	TBR5	
31	TBR6	
32	TBR7	
33	TBR8	
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI†	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS†	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
37	CLS2†	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits).
38	CLS1†	See Pin 37 - CLS2
39	EPE†	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

† See Table 1 (Control Word Function)

Dynamic Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF

(NOTE 1) PARAMETER		V_{DD} (V)	LIMITS CDP6402 (NOTE 2) TYP	LIMITS CDP6402 (NOTE 3) MAX	LIMITS CDP6402C (NOTE 2) TYP	LIMITS CDP6402C (NOTE 3) MAX	UNITS
SYSTEM TIMING (See Figure 6)							
Minimum Pulse Width CRL	t_{CRL}	5	50	150	50	150	ns
		10	40	100	-	-	ns
Minimum Setup Time Control Word to CRL	t_{CWC}	5	20	50	20	50	ns
		10	0	40	-	-	ns
Minimum Hold Time Control Word after CRL	t_{CCW}	5	40	60	40	60	ns
		10	20	30	-	-	ns
Propagation Delay Time SFD High to SOD	t_{SFDH}	5	130	200	130	200	ns
		10	100	150	-	-	ns
SFD Low to SOD	t_{SFDL}	5	130	200	130	200	ns
		10	40	60	-	-	ns
RRD High to Receiver Register High Impedance	t_{RRDH}	5	80	150	80	150	ns
		10	40	70	-	-	ns
RRD Low to Receiver Register Active	t_{RRDL}	5	80	150	80	150	ns
		10	40	70	-	-	ns
Minimum Pulse Width MR		5	200	400	200	400	ns
		10	100	200	-	-	ns

NOTES:

1. All measurements are made at the 50% point of the transition except three-state measurements.
2. Typical values for T_A = 25°C and nominal V_{DD}.
3. Maximum limits of minimum characteristics are the values above which all devices function.

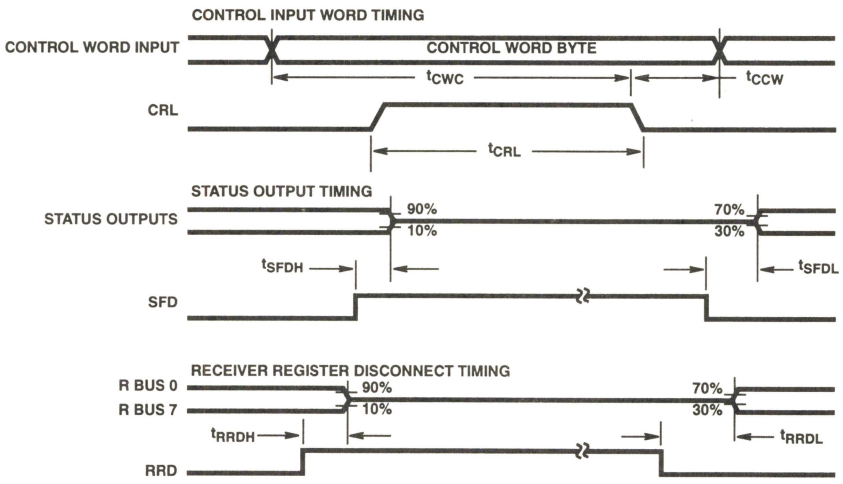


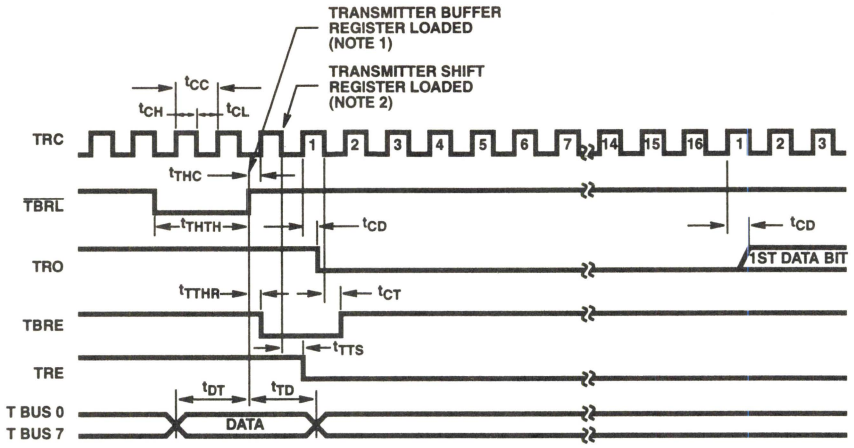
FIGURE 6. SYSTEM TIMING WAVEFORMS

Dynamic Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF

(NOTE 1) PARAMETER		V_{DD} (V)	LIMITS				UNITS
			CDP6402		CDP6402C		
			(NOTE 2) TYP	(NOTE 3) MAX	(NOTE 2) TYP	(NOTE 3) MAX	
TRANSMITTER TIMING (See Figure 7)							
Minimum Clock Period (TRC)	t_{CC}	5	250	310	250	310	ns
		10	125	155	-	-	ns
Minimum Pulse Width							
Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	-	-	ns
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	-	-	ns
$\overline{TBRL}$	t_{THTH}	5	80	200	80	200	ns
		10	40	100	-	-	ns
Minimum Setup Time							
$\overline{TBRL}$ to Clock	t_{THC}	5	175	275	175	275	ns
		10	90	150	-	-	ns
Data to $\overline{TBRL}$ ↗	t_{DT}	5	20	50	20	50	ns
		10	0	40	-	-	ns
Minimum Hold-Time							
Data after $\overline{TBRL}$ ↗	t_{TD}	5	40	60	40	60	ns
		10	20	30	-	-	ns
Propagation Delay Time							
Clock to Data Start Bit	t_{CD}	5	300	450	300	450	ns
		10	150	225	-	-	ns
Clock to TBRE	t_{CT}	5	330	400	330	400	ns
		10	100	150	-	-	ns
$\overline{TBRL}$ to TBRE	t_{TTHR}	5	200	300	200	300	ns
		10	100	150	-	-	ns
Clock to TRE	t_{TTS}	5	330	400	330	400	ns
		10	100	150	-	-	ns

NOTES:

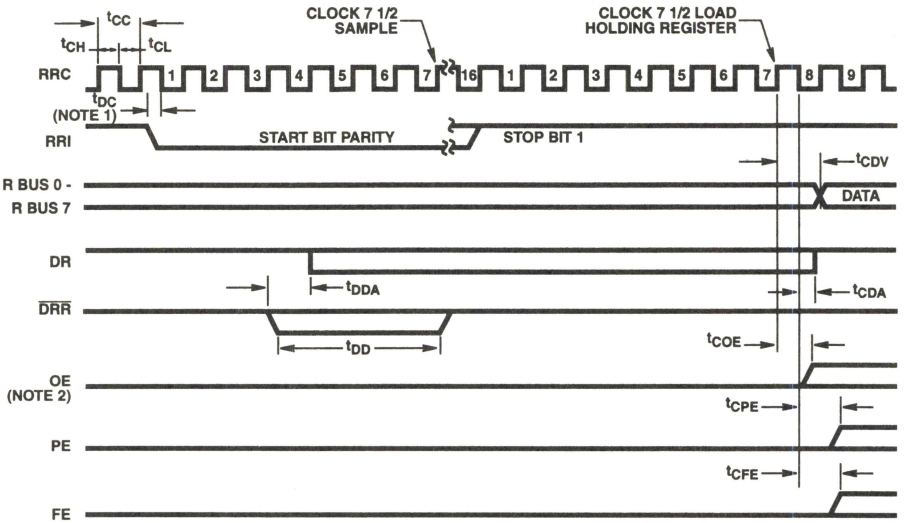
1. All measurements are made at the 50% point of the transition except three-state measurements.
2. Typical values for T_A = 25°C and nominal V_{DD}.
3. Maximum limits of minimum characteristics are the values above which all devices function.



NOTES:

1. The holding register is loaded on the trailing edge of $\overline{TBRL}$.
2. The transmitter shift register, if empty, is loaded on the first high-to-low transition of the clock which occurs at least 1/2 clock period + t_{THC} after the trailing edge of $\overline{TBRL}$ and transmission of a start bit occurs 1/2 clock period + t_{CD} later.

FIGURE 7. TRANSMITTER TIMING WAVEFORMS



NOTES:

1. If a start bit occurs at a time less than t_{DC} before a high-to-low transition of the clock, the start bit may not be recognized until the next high-to-low transition of the clock. The start bit may be completely asynchronous with the clock.
2. If a pending DA has not been cleared by a read of the receiver holding register by the time a new word is loaded into the receiver holding register, the OE signal will come true.

FIGURE 8. RECEIVER TIMING WAVEFORMS

Dynamic Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF

(NOTE 1) PARAMETERS		V_{DD} (V)	LIMITS				UNITS
			CDP6402		CDP6402C		
			(NOTE 2) TYP	(NOTE 3) MAX	(NOTE 2) TYP	(NOTE 3) MAX	
RECEIVER TIMING (See Figure 8)							
Minimum Clock Period (RRC)	t_{CC}	5	250	310	250	310	ns
		10	125	155	-	-	ns
Minimum Pulse Width							
Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	-	-	ns
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	-	-	ns
$\overline{\text{Data Received Reset}}$	t_{DD}	5	50	75	50	75	ns
		10	25	40	-	-	ns
Minimum Setup Time							
Data Start Bit to Clock	t_{DC}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Propagation Delay Time							
$\overline{\text{Data Received Reset}}$ to Data Received	t_{DDA}	5	150	250	150	250	ns
		10	75	125	-	-	ns
Clock to Data Valid	t_{CDV}	5	275	400	275	400	ns
		10	110	175	-	-	ns
Clock to DR	t_{CDA}	5	275	400	275	400	ns
		10	110	175	-	-	ns
Clock to Overrun Error	t_{COE}	5	275	400	275	400	ns
		10	100	150	-	-	ns
Clock to Parity Error	t_{CPE}	5	240	375	240	375	ns
		10	120	175	-	-	ns
Clock to Framing Error	t_{CFE}	5	200	300	200	300	ns
		10	100	150	-	-	ns

NOTES:

1. All measurements are made at the 50% point of the transition except three-state measurements.
2. Typical values for T_A = 25°C and nominal V_{DD}.
3. Maximum limits of minimum characteristics are the values above which all devices function.

HARRIS SEMICONDUCTOR

HD-4702

March 1997

CMOS Programmable Bit Rate Generator

Features

- HD-4702 Provides 13 Commonly Used Bit Rates
- Uses a 2.4576MHz Crystal/Input for Standard Frequency Output (16 Times Bit Rate)
- Low Power Dissipation
- Conforms to EIA RS-404
- One HD-4702 Controls up to Eight Transmission Channels
- Initialization Circuit Facilitates Diagnostic Fault Isolation
- On-Chip Input Pull-Up Circuit

Ordering Information

PACKAGE	TEMP. RANGE (°C)	PART NUMBER	PKG. NO.
PDIP	-40 to +85	HD3-4702-9	E16.3
CERDIP	-40 to +85	HD1-4702-9	F16.3
SMD#	-55 to +125	5962-9051801MEA	F16.3

Description

The HD-4702 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as a UART. It generates 13 commonly used bit rates using an on-chip crystal oscillator or an external input. For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 Baud x 16 x 16, since there is an internal ÷ 16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The HD-4702 can provide multi-channel operation with a minimum of external logic by having the clock frequency CO and the ÷ 8 prescaler outputs Q0, Q1, Q2 available externally. All signals have a 50% duty cycle except 1800 Baud, which has less than 0.39% distortion.

The four rate select inputs (S0-S3) select which bit rate is at the output (Z). See Truth Table for Rate Select Inputs for select code and output bit rate. Two of the 16 select codes for the HD-4702 do not select an internally generated frequency, but select an input into which the user can feed either a different frequency, or a static level (High or Low) to generate "ZERO BAUD".

The bit rates most commonly used in modern data terminals (110, 150, 300, 1200, 2400 Baud) require that no more than one input be grounded for the HD-4702, which is easily achieved with a single 5-position switch.

The HD-4702 has an initialization circuit which generates a master reset for the scan counter. This signal is derived from a digital differentiator that senses the first high level on the CP input after the $\overline{E}_{CP}$ input goes low. When $\overline{E}_{CP}$ is high, selecting the crystal input, CP must be low. A high level on CP would apply a continuous reset. See Clock Modes and Initialization below.

Truth Table

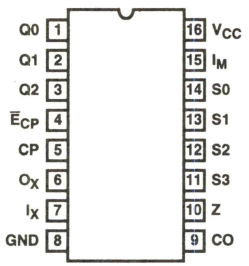
TRUTH TABLE FOR RATE SELECT INPUTS
(Using 2.4576MHz Crystal)

S3	S2	S1	S0	OUTPUT RATE (Z)
L	L	L	L	MUX Input (IM)
L	L	L	H	MUX Input (IM)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

NOTE: 19200 Baud by connecting Q2 to IM.

Pinout

HD-4702 (CERDIP, PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2954.1**

Pin Description

PIN NUMBER	TYPE	SYMBOL	DESCRIPTION
16		V_{CC}	V_{CC}: Is the +5V power supply pin. A 0.1µF capacitor between pins 16 and 8 is recommended for decoupling.
8		GND	GROUND
5	I	CP	EXTERNAL CLOCK INPUT
4	I	$\overline{E}_{CP}$	EXTERNAL CLOCK ENABLE: A low signal on this input allows the baud rate to be generated from the CP input.
7	I	I_X	CRYSTAL INPUT
6	O	O_X	CRYSTAL DRIVE OUTPUT
15	I	I_M	MULTIPLEXED INPUT
11, 12, 13, 14	I	S0 - S3	BAUD RATE SELECT INPUTS
9	O	CO	CLOCK OUTPUT
1, 2, 3	O	Q_0 - Q_2	SCAN COUNTER OUTPUTS
10	O	Z	BIT RATE OUTPUT

CLOCK MODES AND INITIALIZATION

IX	$\overline{E}_{CP}$	CP	OPERATION
	H	L	Clocked from I_X
X	L		Clocked from CP
X	H	H	Continuous Reset
X	L		Reset During 1st CP = High Time

H = HIGH Level

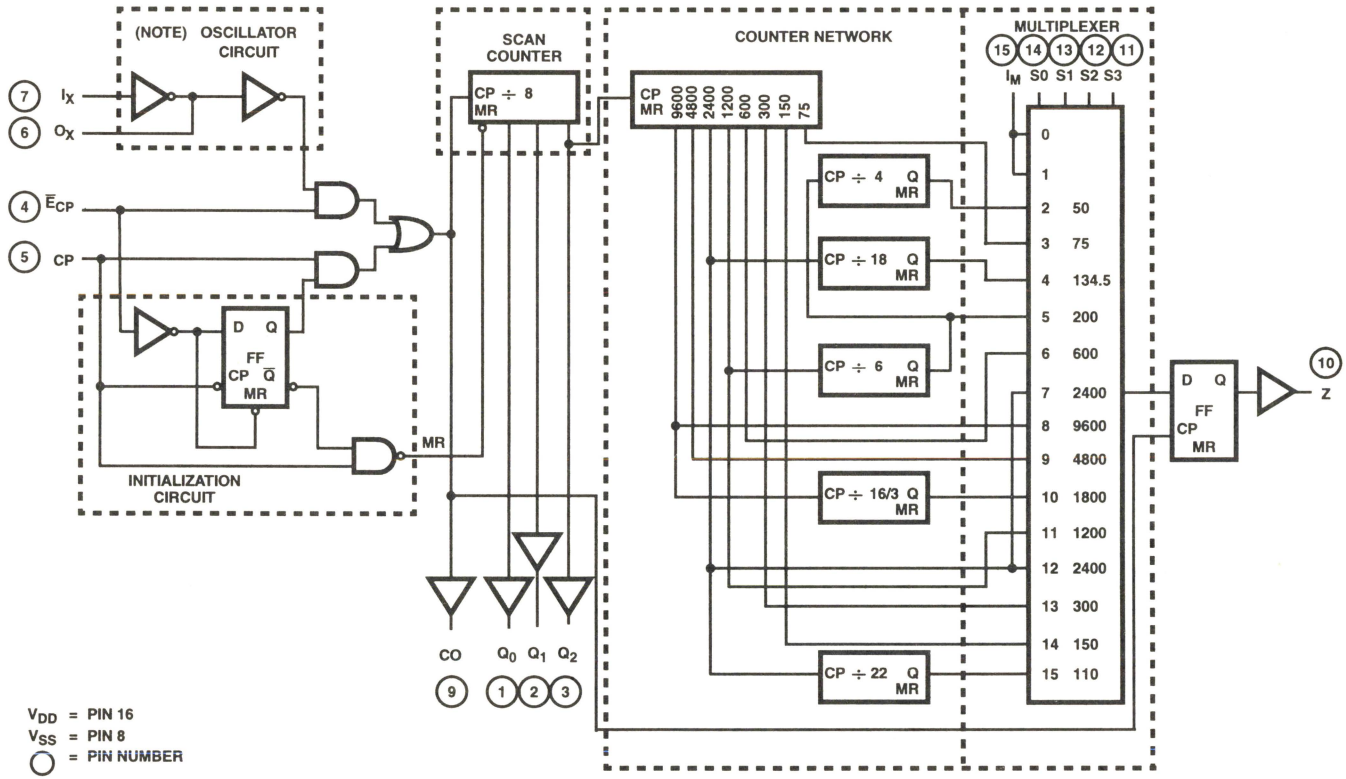
L = LOW Level

X = Don't Care

 = Clock Pulse

 = 1st HIGH Level Clock Pulse after $\overline{E}_{CP}$ goes LOW

NOTE: Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576MHz.

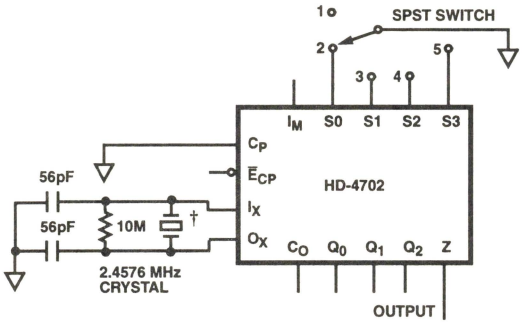


NOTE: See Figure 4 in Design Information for Crystal Specifications.

Application Information

Single Channel Bit Rate Generator

Figure 1 shows the simplest application of the HD-4702. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 Baud. For many low cost terminals, these five bit rates are adequate.



† See Table 1.

SWITCH POSITION	HD-4702 BIT RATE
1	110 Baud
2	150 Baud
3	300 Baud
4	1200 Baud
5	2400 Baud

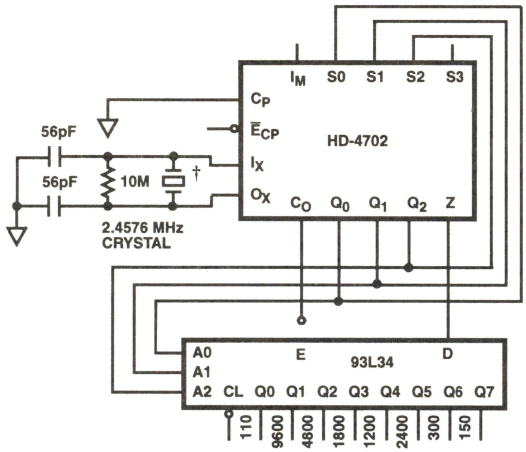
FIGURE 1. SWITCH SELECTABLE BIT RATE GENERATOR CONFIGURATION PROVIDING FIVE BIT RATES

Simultaneous Generation of Several Bit Rates

Figure 2 shows a simple scheme that generates eight bit rates on eight output lines, using one HD-4702 and one 93L34 Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select Inputs of the multiplexer causes the HD-4702 to interrogate sequentially eight different frequency signals. The 93L34 8-bit addressable Latch, addressed by the same Scan Counter Outputs, re-converts the multiplexed single Output (Z) of the HD-4702 into eight parallel output frequency signals. In the simple scheme of Figure 2, input S3 is left open (HIGH) and the following bit rates are generated:

Q0: 110 Baud Q1: 9600 Baud Q2: 4800 Baud
Q3: 1800 Baud Q4: 1200 Baud Q5: 2400 Baud
Q6: 300 Baud Q7: 150 Baud

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.

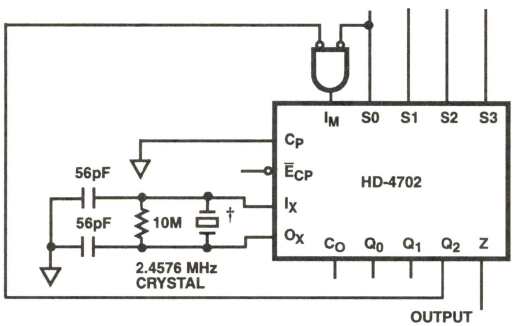


† See Table 1.

FIGURE 2. BIT RATE GENERATOR CONFIGURATION WITH EIGHT SIMULTANEOUS FREQUENCIES

19200 Baud Operation

Though a 19200 Baud signal is not internally routed to the multiplexer, the HD-4702 can be used to generate this bit rate by connecting the Q_2 output to IM input and applying select code. An additional 2-input NOR gate can be used to retain the "Zero Baud" feature on select code 1 for the HD-4702 (See Figure 3).



† See Table 1.

FIGURE 3. 19200 BAUD OPERATION

TABLE 1. CRYSTAL SPECIFICATIONS

PARAMETERS	TYPICAL CRYSTAL SPEC
Frequency	2.4576MHz "AT" Cut
Series Resistance (Max)	250
Unwanted Modes	-6.0dB (Min)
Type of Operation	Parallel
Load Capacitance	32pF +0.5

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1
Typical Derating Factor . . . . . 1mA/MHz Increase in ICCOP

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package	78°C/W	23°C/W
PDIP Package	90°C/W	N/A

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . .
Ceramic Package . . . . . +175°C
Plastic Package . . . . . +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 720 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V

Operating Temperature Range
HD-4702-9 . . . . . -40°C to +85°C
HD-4702-8 . . . . . -55°C to +125°C

DC Electrical Specifications

V_{CC} = 5V ±10%, T_A = -40°C to +85°C (HD-4702-9), T_A = -55°C to +125°C (HD-4702-8)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input High Voltage	V_{CC} 70%	-	V	V_{CC} = 4.5V
V_{IL}	Input Low Voltage	-	V_{CC} 30%	V	V_{CC} = 4.5V
V_{OH1}	Output High Voltage	V_{CC} -0.1	-	V	$I_{OH} \leq$ -1µA, V_{CC} = 4.5V, (Note 1)
V_{OL1}	Output Low Voltage	-	0.1	V	$I_{OL} \leq$ +1µA, V_{CC} = 4.5V, (Note 1)
I_{IH}	Input High Current	-1	+1	µA	$V_{IN} = V_{CC}$, All 0ther Pins = 0V, V_{CC} = 5.5V
I_{ILX}	Input Low Current (I_X Input)	-1	+1	µA	V_{IN} = 0V, All Other Pins = V_{CC}, V_{CC} = 5.5V
I_{IL}	Input Low Current (All Other Inputs)	-	-100	µA	V_{IN} = 0V, All Other Pins = V_{CC}, V_{CC} = 5.5V (Note 2)
I_{OHX}	Output High Current (O_X)	-0.1	-	mA	$V_{OUT} = V_{CC}$ - 0.5, V_{CC} = 4.5V, Input at 0V or V_{CC} per Logic Function or Truth Table
I_{OH1}	Output High Current (All Other Outputs)	-1.0	-	mA	V_{OUT} = 2.5V, V_{CC} = 4.5V, Input at 0V or V_{CC} per Logic Function or Truth Table
I_{OH2}	Output High Current (All Other Outputs)	-0.3	-	mA	$V_{OUT} = V_{CC}$ -0.5, V_{CC} = 4.5V, Input at 0V or V_{CC} per Logic Function or Truth Table
I_{OLX}	Output Low Current (O_X)	0.1	-	mA	V_{OUT} = 0.4V, V_{CC} = 4.5V, Input at 0V or V_{CC} per Logic Function or Truth Table
I_{OL}	Output Low Current (All Other Outputs)	1.6	-	mA	V_{OUT} = 0.4V, V_{CC} = 4.5V Input, at 0V or V_{CC} per Logic Function or Truth Table
I_{CC}	Supply Current (Static)	-	1500	µA	$\overline{E}_{CP} = V_{CC}$, CP = 0V, V_{CC} = 5.5V, All Other Inputs = GND, (Note 2)
		-	1000	µA	$\overline{E}_{CP} = V_{CC}$, CP = 0V, V_{CC} = 5.5V, All Other Inputs = V_{CC}, (Note 2)

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except I_X.

AC Electrical Specifications V_{CC} = 5V ±10%, T_A = -40°C to +85°C (HD-4702-9), T_A = -55°C to +125°C (HD-4702-8)

SYMBOL	AC PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, I_X to CO	-	350	ns	V_{CC} = 4.5V $C_L \leq$ 7pF on O_X C_L = 50pF (Note 1)
t_{PHL}		-	275	ns	
t_{PLH}	Propagation Delay, CP to CO	-	260	ns	
t_{PHL}		-	220	ns	
t_{PLH}	Propagation Delay, CO to Qn	-	(Note 2)	ns	
t_{PHL}		-	(Note 2)	ns	
t_{PLH}	Propagation Delay, CO to Z	-	85	ns	
t_{PHL}		-	75	ns	
t_{TLH}	Output Transition Time (Except O_X)	-	160	ns	
t_{THL}		-	75	ns	
t_s	Set-Up Time, Select to CO	350	-	ns	
t_h	Hold Time, Select to CO	0	-	ns	
t_s	Set-Up Time, I_M to CO	350	-	ns	
t_h	Hold Time, I_M to CO	0	-	ns	
$t_{wCP}(L)$	Minimum Clock Pulse Width, Low (Notes 3, 4)	120	-	ns	
$t_{wCP}(H)$	Minimum Clock Pulse Width, High (Notes 3, 4)	120	-	ns	
$t_{wCP}(L)$	Minimum I_X Pulse Width, Low (Note 4)	160	-	ns	
$t_{wCP}(H)$	Minimum I_X Pulse Width, High (Note 4)	160	-	ns	
t_{PLH}	Propagation Delay I_X to CO	-	300	ns	V_{CC} = 4.5V $C_L \leq$ 7pF on O_X C_L = 15pF (Note 1)
t_{PHL}		-	250	ns	
t_{PLH}	Propagation Delay CP to CO	-	215	ns	
t_{PHL}		-	195	ns	
t_{PLH}	Propagation Delay CO to Qn	-	(Note 2)	ns	
t_{PHL}		-	(Note 2)	ns	
t_{PLH}	Propagation Delay CO to Z	-	75	ns	
t_{PHL}		-	65	ns	
t_{TLH}	Output Transition Time (Except O_X)	-	80	ns	
t_{THL}		-	40	ns	

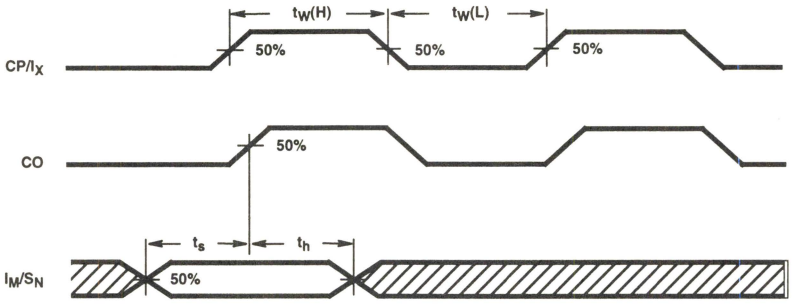
NOTES:

1. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Setup Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
2. For multichannel operation, Propagation Delay (CO to Qn) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 367ns.
3. The first High Level Clock Pulse after $\overline{E}_{CP}$ goes Low must be at least 350ns long to guarantee reset of all Counters.
4. It is recommended that input rise and fall times to the clock inputs (CP, I_X) be less than 15ns.

Capacitance $T_A = +25^oC$; Frequency = 1MHz

SYMBOL	PARAMETER	TYPICAL	UNITS	CONDITIONS
C_{IN}	Input Capacitance	7	pF	All measurements are referenced the device GND
C_{OUT}	Output Capacitance	15	pF	

Switching Waveforms



NOTE:

1. Setup and Hold times are shown as positive values but may be specified as negative values.

AC Testing Input, Output Waveform



NOTE:

1. AC Testing: All input signals must switch between V_{IL} and V_{IH}. Input rise and fall times are driven at 1ns per volt.

HD-4702/883

March 1997

CMOS Programmable Bit Rate Generator

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1. 2. 1.**
- **HD-4702/883 Provides 13 Commonly Used Bit Rates**
- **Uses a 2.4576MHz Crystal/Input for Standard Frequency Output (16 Times Bit Rate)**
- **Low Power Dissipation**
- **Conforms to EIA RS-404**
- **One HD-4702/883 Controls up to Eight Transmission Channels**
- **Initialization Circuit Facilitates Diagnostic Fault Isolation**
- **On-Chip Input Pull-Up Circuit**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PKG. NO.
HD1-4702R/883	-55°C to +125°C	CERDIP	F16.3

Description

The HD-4702/883 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as a UART. It generates 13 commonly used bit rates using an on-chip crystal oscillator or an external input. For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e., 9600 Baud x 16 x 16, since there is an internal ÷ 16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The HD-4702/883 can provide multi-channel operation with a minimum of external logic by having the clock frequency CO and the ÷ 8 prescaler outputs Q0, Q1, Q2 available externally. All signals have a 50% duty cycle except 1800 Baud, which has less than 0.39% distortion.

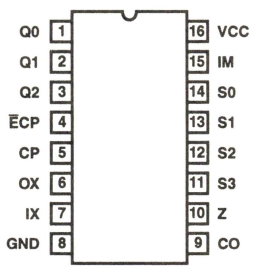
The four rate select inputs (S0-S3) select which bit rate is at the output (Z). See Truth Table for Rate Select Inputs for select code and output bit rate. Two of the 16 select codes for the HD-4702/883 do not select an internally generated frequency, but select an input into which the user can feed either a different frequency, or a static level (High or Low) to generate "ZERO BAUD".

The bit rates most commonly used in modern data terminals (110,150, 300,1200, 2400 Baud) require that no more than one input be grounded for the HD-4702/883, which is easily achieved with a single 5-position switch.

The HD-4702/883 has an initialization circuit which generates a master reset for the scan counter. This signal is derived from a digital differentiator that senses the first high level on the CP input after the $\overline{ECP}$ input goes low. When $\overline{ECP}$ is high, selecting the crystal input, CP must be low. A high level on CP would apply a continuous reset. See Clock Modes and Initialization below.

Pinout

HD-4702/883 (CERDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Truth Table

TRUTH TABLE FOR RATE SELECT INPUTS
(Using 2.4576MHz Crystal)

S3	S2	S1	S0	OUTPUT RATE (Z)
L	L	L	L	MUX Input (IM)
L	L	L	H	MUX Input (IM)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

NOTE:

1. 19200 Baud by connecting Q2 to IM.

CLOCK MODES AND INITIALIZATION

IX	$\overline{ECP}$	CP	OPERATION
	H	L	Clocked from IX
X	L		Clocked from CP
X	H	H	Continuous Reset
X	L		Reset During First CP = High Time

NOTE: Actual output frequency is 16 times the indicated output rate, assuming a clock frequency of 2.4576MHz.

H = HIGH Level
L = LOW Level
X = Don't Care
 = ClockPulse
 = First HIGH Level Clock Pulse after $\overline{ECP}$ goes LOW

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1
Typical Derating Factor . . . . . 1mA/MHz Increase in ICCOP

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance, (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	78	23

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering, 10s . . . . . +300°C

Die Characteristics

Gate Count . . . . . 720 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

DC PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input High Voltage	VIH	VCC = 4.5V	1, 2, 3	-55°C ≤ TA ≤ +125°C	VCC 70%	-	V
Input Low Voltage	VIL	VCC = 4.5V	1, 2, 3	-55°C ≤ TA ≤ +125°C	-	VCC 30%	V
Output High Voltage	VOH1	IOH ≤ -1µA, VCC = 4.5V, (Note 1)	1, 2, 3	-55°C ≤ TA ≤ +125°C	VCC -0.1	-	V
Output Low Voltage	VOL1	IOL ≤ +1µA, VCC = 4 5V, (Note 1)	1, 2, 3	-55°C ≤ TA ≤ +125°C	-	0.1	V
Input High Current	IIH	VIN = VCC. All Other Pins = 0V, VCC = 5.5V	1, 2, 3	-55°C ≤ TA ≤ +125°C	-1	+1	µA
Input Low Current (IX Input)	IILX	VIN = 0V, All Other Pins = VCC, VCC = 5.5V	1, 2, 3	-55°C ≤ TA ≤ +125°C	-1	+1	µA
Input Low Current (All Other Inputs)	IIL	VIN = 0V All Other Pins = VCC, VCC = 5.5V (Note 2)	1, 2, 3	-55°C ≤ TA ≤ +125°C	-	-100	µA
Output High Current (OX)	IOHX	VOUT = VCC -0.5, VCC = 4.5V Input at 0V or VCC per Logic Function or Truth Table	1, 2, 3	-55°C ≤ TA ≤ +125°C	-0.1	-	mA
Output High Current (All Other Outputs)	IOH1	VOUT = 2.5V, VCC = 4.5V Input at 0V or VCC per Logic Function or Truth Table	1, 2, 3	-55°C ≤ TA ≤ +125°C	-1.0	-	mA
Output High Current (All Other Outputs)	IOH2	VOUT = VCC -0.5,VCC = 4.5V Input at 0V or VCC per Logic Function or Truth Table	1, 2, 3	-55°C ≤ TA ≤ +125°C	-0.3	-	mA
Output Low Current (OX)	IOLX	VOUT = 0.4V, VCC = 4.5V Input at 0V or VCC per Logic Function or Truth Table	1, 2, 3	-55°C ≤ TA ≤ +125°C	0.1	-	mA
Output Low Current (All Other Outputs)	IOL	VOUT = 0.4V, VCC = 4.5V Input at 0V or VCC per Logic Function or Truth Table	1, 2, 3	-55°C ≤ TA ≤ +125°C	1.6	-	mA

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested

DC PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current (Static)	ICC	$\overline{E}CP$ = VCC, CP = 0V, VCC = 5.5V All Other Inputs = GND, (Note 2)	1, 2, 3	$-55^oC \leq TA \leq +125^oC$	-	1500	µA
		$\overline{E}CP$ = VCC, CP = 0V, VCC = 5.5V All Other Inputs = VCC, (Note 2)	1, 2, 3	$-55^oC \leq TA \leq +125^oC$	-	1000	µA

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except IX.

TABLE 2. AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested.

AC PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay, IX to CO	tPLH	VCC = 4.5V CL ≤ 7pF on OX CL = 50pF (Note 1)	9, 10, 11	$-55^oC \leq TA \leq +125^oC$	-	350	ns
Propagation Delay, IX to CO	tPHL		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	-	275	ns
Propagation Delay, CP to CO	tPLH		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	-	260	ns
Propagation Delay, CP to CO	tPHL		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	-	220	ns
Propagation Delay, CO to Qn	tPLH		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	-	(Note 2)	ns
Propagation Delay, CO to Qn	tPHL		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	-	(Note 2)	ns
Propagation Delay, CO to Z	tPLH		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	-	85	ns
Propagation Delay, CO to Z	tPHL		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	-	75	ns
Output Transition Time (Except OX)	tTLH		9, 10, 11	$-55^oC \leq TA \leq +125^oC$		160	ns
Output Transition Time (Except OX)	tTHL		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	-	75	ns
Set-UpTime Select to CO	ts		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	350	-	ns
Hold Time, Select to CO	th		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	0	-	ns
Set-UpTime, IM to CO	ts		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	350	-	ns
Hold Time, IM to CO	th		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	0	-	ns
Minimum Clock Pulse Width, Low (Notes 3, 4)	twCP(L)		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	120		ns
Minimum Clock Pulse Width, High (Notes 3, 4)	twCP(H)		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	120	-	ns
Minimum IX Pulse Width, Low (Note 4)	twCP(L)		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	160	-	ns
Minimum IX Pulse Width, High (Note 4)	twCP(H)		9, 10, 11	$-55^oC \leq TA \leq +125^oC$	160	-	ns

NOTES:

1. Propagation Delays (tPLH and tPHL) and Output Transition Times (tTLH and tTHL) will change with Output Load Capacitance (CL). Set-Up Times (ts), Hold Times (th), and Minimum Pulse Widths (tw) do not vary with load capacitance.
2. For multichannel operation, Propagation Delay (CO to Qn), plus Set-Up Time, Select to CO, is guaranteed to be ≤ 367ns.
3. The first High Level Clock Pulse alter $\overline{E}CP$ goes Low must be at least 350ns long to guarantee reset of all Counters.
4. It is recommended that input rise and fall times to the clock inputs (CP, IX) be less than 15ns.

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

AC PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CIN	All Measurements are referenced to device ground, f = 1MHz.	1	TA = +25°C	-	7.0	pF
Output Capacitance	CO		1	TA = +25°C	-	15.0	pF
Propagation Delay IX to CO	tPLH	VCC = 4.5V CL ≤ 7pF on OX CL = 15pF	1, 3	-55°C ≤ TA ≤ +125°C	-	300	ns
Propagation Delay IX to CO	tPHL		1, 3	-55°C ≤ TA ≤ +125°C	-	250	ns
Propagation Delay CP to CO	tPLH		1, 3	-55°C ≤ TA ≤ +125°C	-	215	ns
Propagation Delay CP to CO	tPHL		1, 3	-55°C ≤ TA ≤ +125°C	-	195	ns
Propagation Delay CO to Qn	tPLH		1, 3	-55°C ≤ TA ≤ +125°C	-	(Note 2)	ns
Propagation Delay CO to Qn	tPHL		1, 3	-55°C ≤ TA ≤ +125°C	-	(Note 2)	ns
Propagation Delay CO to Z	tPLH		1, 3	-55°C ≤ TA ≤ +125°C	-	75	ns
Propagation Delay CO to Z	tPHL		1, 3	-55°C ≤ TA ≤ +125°C	-	65	ns
Output Transition Time (Except OX)	tTLH		1, 3	-55°C ≤ TA ≤ +125°C	-	80	ns
Output Transition Time (Except OX)	tTHL		1, 3	-55°C ≤ TA ≤ +125°C	-	40	ns

NOTES:

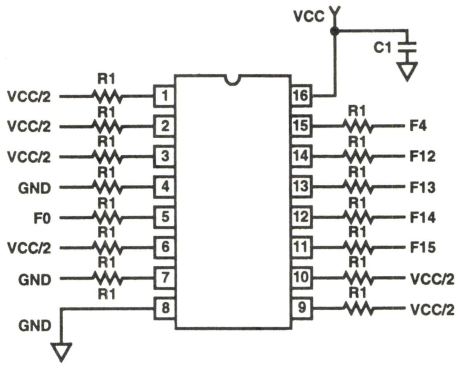
1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. For multichannel operation, Propagation Delay (CO to Qn) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 367ns.
3. Propagation Delays (tPLH and tPHL) and Output Transition Times (tTLH and tTHL) will change with Output Load Capacitance (CL). Set-Up Times (ts), Hold Times (th), and Minimum Pulse Widths (tw) do not vary with load capacitance.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Burn-In Circuit

HD-4702/883 CERDIP



NOTES:

1. F0 = 100kHz ±10%, F1 = F0/2, F2 = F1/2., ...
2. R1 = 10kΩ, 1/4W, ±10%.
3. VCC = 5.5V ±0.5V, GND = 0V.
4. C1 = 0.01µF minimum.

Die Characteristics

DIE DIMENSIONS:
100 x 97 x 19 mils

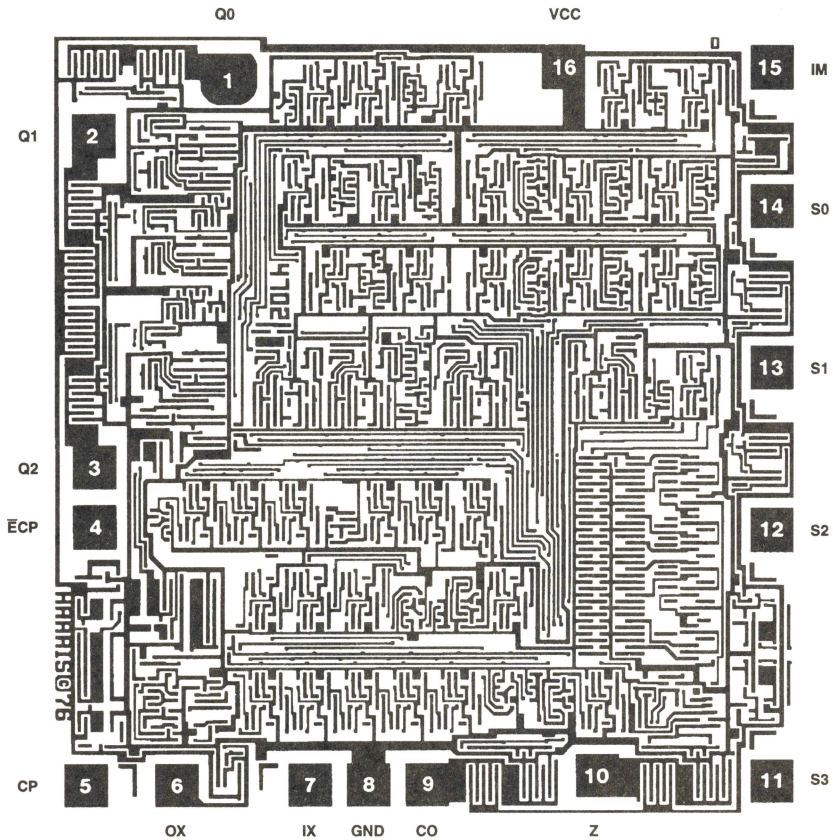
METALLIZATION:
Type: Si - Al
Thickness: 10kÅ - 12kÅ

GLASSIVATION:
Type: SiO2
Thickness: 7kÅ - 9kÅ

WORST CASE CURRENT DENSITY:
$7.1 \times 10^4 A/cm^2$

Metallization Mask Layout

HD-4702/883



HARRIS SEMICONDUCTOR

HD-6402

CMOS Universal Asynchronous Receiver Transmitter (UART)

March 1997

Features

- 8.0MHz Operating Frequency (HD-6402B)
- 2.0MHz Operating Frequency (HD-6402R)
- Low Power CMOS Design
- Programmable Word Length, Stop Bits and Parity
- Automatic Data Formatting and Status Generation
- Compatible with Industry Standard UARTs
- Single +5V Power Supply
- CMOS/TTL Compatible Inputs

Description

The HD-6402 is a CMOS UART for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5-bit code.

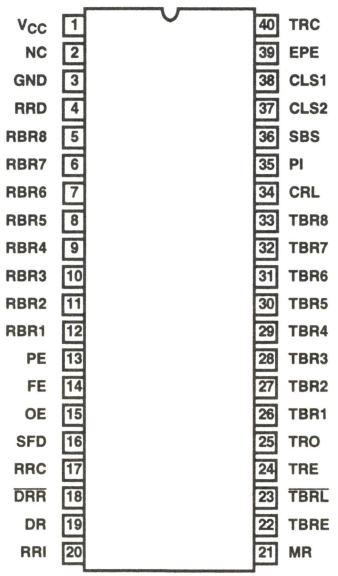
The HD-6402 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. Utilizing the Harris advanced scaled SAJI IV CMOS process permits operation clock frequencies up to 8.0MHz (500K Baud). Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

Ordering Information

PACKAGE	TEMPERATURE RANGE	2MHz = 125K BAUD	8MHz = 500K BAUD	PKG. NO.
Plastic DIP	-40°C to +85°C	HD3-6402R-9	HD3-6402B-9	E40.6
CERDIP	-40°C to +85°C	HD1-6402R-9	HD1-6402B-9	F40.6
SMD#	-55°C to +125°C	5962-9052501MQA	5962-9052502MQA	F40.6

Pinout

HD-6402 (PDIP, CERDIP)
TOP VIEW

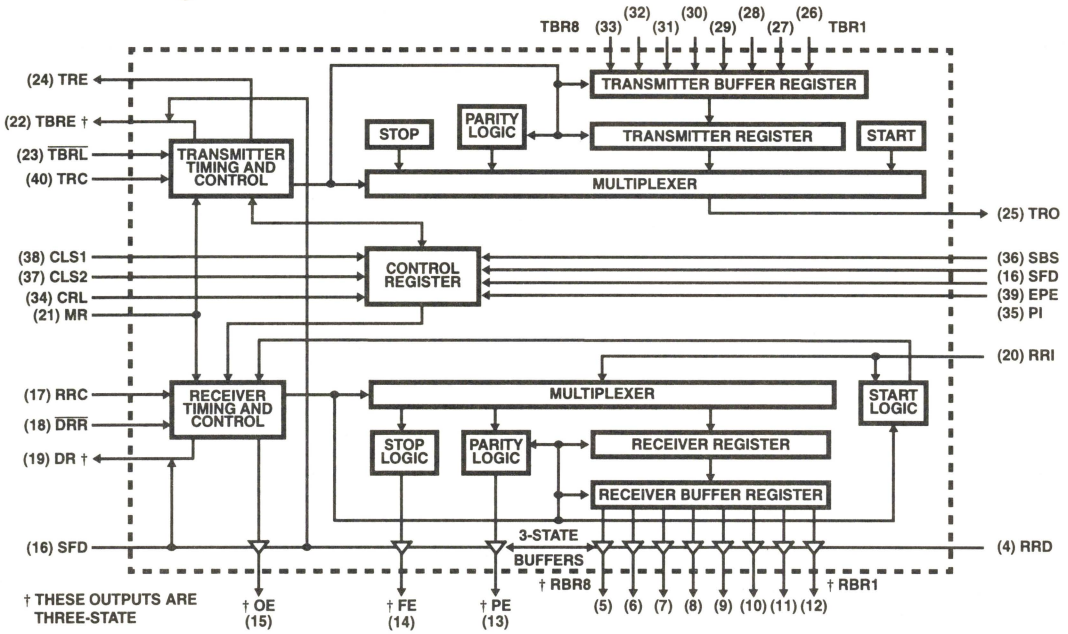


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2956.1**

Functional Diagram



Control Definition

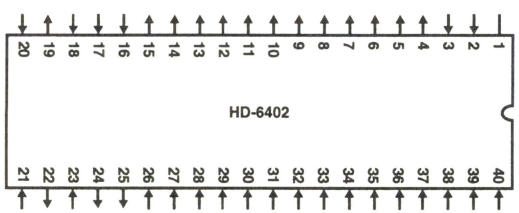
CONTROL WORD					CHARACTER FORMAT			
CLS 2	CLS 1	PI	EPE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	X	0	1	5	NONE	1
0	0	1	X	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	X	0	1	6	NONE	1
0	1	1	x	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	X	0	1	7	NONE	1
1	0	1	x	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	X	0	1	8	NONE	1
1	1	1	x	1	1	8	NONE	2

Pin Description

PIN	TYPE	SYMBOL	DESCRIPTION
1		V_{CC} †	Positive Voltage Supply
2		NC	No Connection
3		GND	Ground
4	I	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding out-puts RBR1-RBR8 to high impedance state.
5	O	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	O	RBR7	See Pin 5-RBR8
7	O	RBR6	See Pin 5-RBR8
8	O	RBR5	See Pin 5-RBR8
9	O	RBR4	See Pin 5-RBR8
10	O	RBR3	See Pin 5-RBR8
11	O	RBR2	See Pin 5-RBR8
12	O	RBR1	See Pin 5-RBR8
13	O	PE	A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low.
14	O	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.
15	O	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register.
16	I	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	I	RRC	The Receiver register clock is 16X the receiver data rate.
18	I	$\overline{DRR}$	A low level on DATA RECEIVED RESET clears the data received output DR to a low level.
19	O	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	I	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	I	MR	A high level on MASTER RESET clears PE, FE, OE and DR to a low level and sets the transmitter register empty (TRE) to a high level 18 clock cycles after MR falling edge. MR does not clear the receiver buffer register. This input must be pulsed at least once after power up. The HD-6402 must be master reset after power up. The reset pulse should meet V_{IH} and t_{MR}. Wait 18 clock cycles after the falling edge of MR before beginning operation.

PIN	TYPE	SYMBOL	DESCRIPTION
22	O	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	I	$\overline{TBRL}$	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on $\overline{TBRL}$ initiates data transfer to the transmitter register. If busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	O	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	O	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	I	TRB1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8 bits the TBR8, 7 and 6 inputs are ignored corresponding to their programmed word length.
27	I	TBR2	See Pin 26-TBR1.
28	I	TBR3	See Pin 26-TBR1.
29	I	TBR4	See Pin 26-TBR1.
30	I	TBR5	See Pin 26-TBR1.
31	I	TBR6	See Pin 26-TBR1.
32	I	TBR7	See Pin 26-TBR1.
33	I	TBR8	See Pin 26-TBR1.
34	I	CRL	A high level on CONTROL REGISTER LOAD loads the control register with the control word. The control word is latched on the falling edge of CRL. CRL may be tied high.
35	I	PI	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	I	SBS	A high level on STOP BIT SELECT selects 1.5 stop bits for 5 character format and 2 stop bits for other lengths.
37	I	CLS2	These inputs program the CHARACTER LENGTH SELECTED (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits.)
38	I	CLS1	See Pin 37-CLS2.
39	I	EPE	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	I	TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

† A 0.1µF decoupling capacitor from the V_{CC} pin to the GND is recommended.



Transmitter Operation

The transmitter section accepts parallel data, formats the data and transmits the data in serial form on the Transmitter Register Output (TRO) terminal (See serial data format). Data is loaded from the inputs TBR1-TBR8 into the Transmitter Buffer Register by applying a logic low on the Transmitter Buffer Register Load ($\overline{TBRL}$) input (A). Valid data must be present at least t_{set} prior to and t_{hold} following the rising edge of $\overline{TBRL}$. If words less than 8 bits are used, only the least significant bits are transmitted. The character is right justified, so the least significant bit corresponds to TBR1 (B).

The rising edge of $\overline{TBRL}$ clears Transmitter Buffer Register Empty (TBRE). 0 to 1 Clock cycles later, data is transferred to the transmitter register, the Transmitter Register Empty (TRE) pin goes to a low state, TBRE is set high and serial data information is transmitted. The output data is clocked by Transmitter Register Clock (TRC) at a clock rate 16 times the data rate. A second low level pulse on $\overline{TBRL}$ loads data into the Transmitter Buffer Register (C). Data transfer to the transmitter register is delayed until transmission of the current data is complete (D). Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.

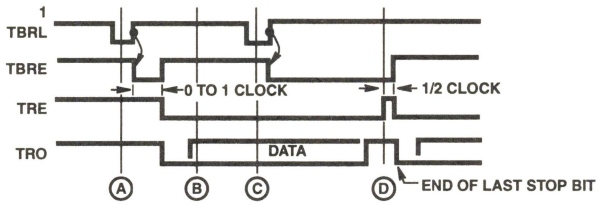


FIGURE 1. TRANSMITTER TIMING (NOT TO SCALE)

Receiver Operation

Data is received in serial form at the Receiver Register Input (RRI). When no data is being received, RRI must remain high. The data is clocked through the Receiver Register Clock (RRC). The clock rate is 16 times the data rate. A low level on Data Received Reset ($\overline{DRR}$) clears the Data Receiver (DR) line (A). During the first stop bit data is transferred from the Receiver Register to the Receiver Buffer Register (RBR) (B). If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on Overrun Error (OE) indicates overruns. An overrun occurs when DR has not been cleared before the present character was transferred to the RBR. One clock cycle later DR is reset to a logic high, and Framing Error (FE) is evaluated (C). A logic high on FE indicates an invalid stop bit was received, a framing error. A logic high on Parity Error (PE) indicates a parity error.

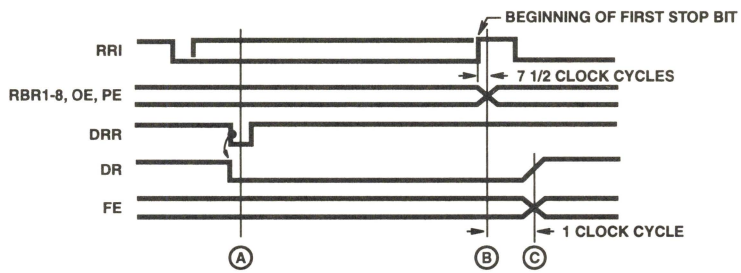


FIGURE 2. RECEIVER TIMING (NOT TO SCALE)

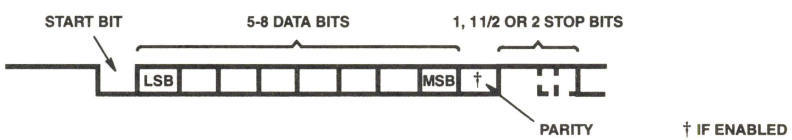


FIGURE 3. SERIAL DATA FORMAT

Start Bit Detection

The receiver uses a 16X clock timing. The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion (A). The center of the start bit is defined as clock count 7 1/2. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±1/2 clock cycle, ±1/32 bit or 3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.

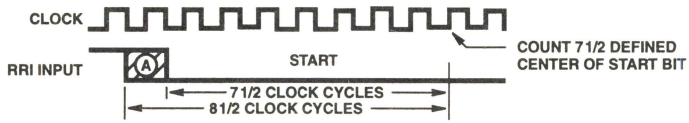


FIGURE 4.

Interfacing with the HD-6402

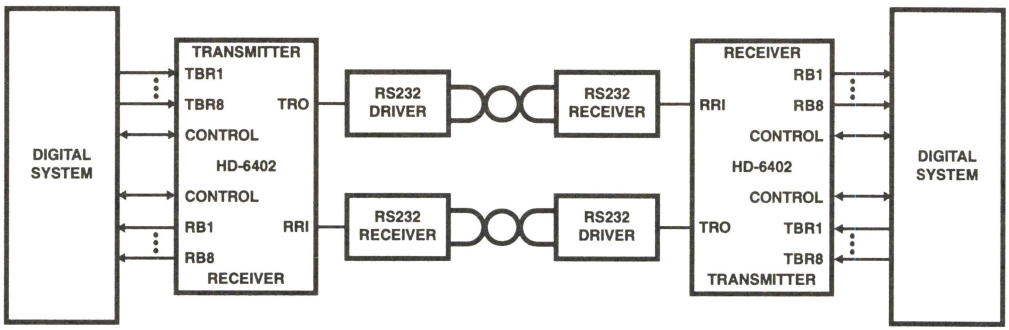


FIGURE 5. TYPICAL SERIAL DATA LINK

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage Applied . . . . . GND -0.5V to V_{CC} +0.5V
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Temperature (Soldering 10s) . . . . . +300°C
ESD Classification . . . . . Class 1
Typical Derating Factor . . . . . 1mA/MHz Increase in ICCOP

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package	50°C/W	12°C/W
PDIP Package	50°C/W	N/A

Gate Count . . . . . 1643 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V

Operating Temperature Range
HD-6402R-9, HD6402B-9 . . . . . -40°C to +85°C

DC Electrical Specifications V_{CC} = 5.0V ± 10%, T_A = -40°C to +85°C (HD-6402R-9, HD-6402B-9)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	CONDITIONS
V_{IH}	Logical "1" Input Voltage	2.0	-	V	V_{CC} = 5.5V
V_{IL}	Logical "0" Input Voltage	-	0.8	V	V_{CC} = 4.5V
II	Input Leakage Current	-1.0	1.0	µA	V_{IN} = GND or V_{CC}, V_{CC} = 5.5V
V_{OH}	Logical "1" Output Voltage	3.0 V_{CC} -0.4	- -	V	I_{OH} = -2.5mA, V_{CC} = 4.5V I_{OH} = -100µA
V_{OL}	Logical "0" Output Voltage	-	0.4	V	I_{OL} = +2.5mA, V_{CC} = 4.5V
I_O	Output Leakage Current	-1.0	1.0	µA	V_O = GND or V_{CC}, V_{CC} = 5.5V
ICCSB	Standby Supply Current	-	100	µA	V_{IN} = GND or V_{CC}; V_{CC} = 5.5V, Output Open
ICCOP	Operating Supply Current (See Note)	-	2.0	mA	V_{CC} = 5.5V, Clock Freq. = 2MHz, V_{IN} = V_{CC} or GND, Outputs Open

NOTE: Guaranteed, but not 100% tested

Capacitance T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	LIMIT TYPICAL	UNITS
Input Capacitance	CIN	Freq. = 1MHz, all measurements are referenced to device GND	25	pF
Output Capacitance	COUT		25	pF

AC Electrical Specifications V_{CC} = 5.0V ± 10%, T_A = -40°C to +85°C (HD-6402R-9, HD6402B-9)

SYMBOL	PARAMETER	LIMITS HD-6402R MIN	LIMITS HD-6402R MAX	LIMITS HD-6402B MIN	LIMITS HD-6402B MAX	UNITS	CONDITIONS
(1) fCLOCK	Clock Frequency	D.C.	2.0	D.C.	8.0	MHz	C_L = 50pF See Switching Waveform
(2) t_{PW}	Pulse Widths, CRL, DRR, TBRL	150	-	75	-	ns	
(3) t_{MR}	Pulse Width MR	150	-	150	-	ns	
(4) t_{SET}	Input Data Setup Time	50	-	20	-	ns	
(5) t_{HOLD}	Input Data Hold Time	60	-	20	-	ns	
(6) t_{EN}	Output Enable Time	-	160	-	35	ns	

Switching Waveforms

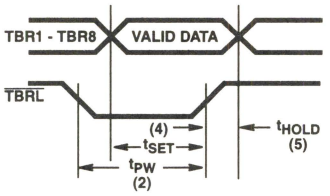


FIGURE 6. DATA INPUT CYCLE

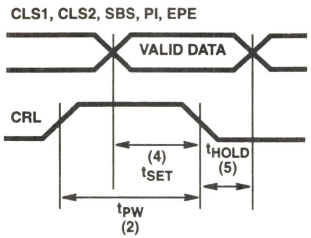


FIGURE 7. CONTROL REGISTER LOAD CYCLE

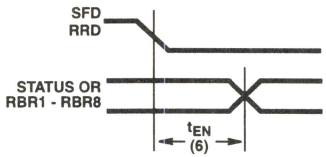


FIGURE 8. STATUS FLAG OUTPUT ENABLE TIME OR DATA OUTPUT ENABLE TIME

A.C. Testing Input, Output Waveform

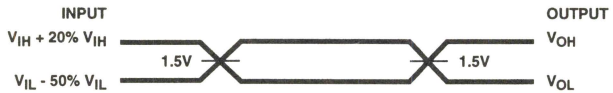


FIGURE 9.

NOTE: A.C. Testing: All input signals must switch between V_{IL} - 50% V_{IL} and V_{IH} + 20% V_{IH}. Input rise and fall times are driven at 1ns/V.

Test Circuit

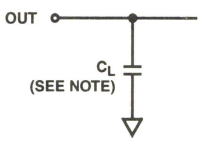


FIGURE 10.

NOTE: Includes stray and jig capacitance, C_L = 50pF.

HARRIS SEMICONDUCTOR

HD-6402/883

CMOS Universal Asynchronous Receiver Transmitter (UART)

March 1997

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **8.0MHz Operating Frequency (HD-6402/883B)**
- **2.0MHz Operating Frequency (HD-6402/883R)**
- **Low Power CMOS Design**
- **Programmable Word Length, Stop Bits and Parity**
- **Automatic Data Formatting and Status Generation**
- **Compatible with Industry Standard UARTs**
- **Single +5V Power Supply**
- **CMOS/TTL Compatible Inputs**

Description

The HD-6402/883 is a CMOS UART for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5-bit code.

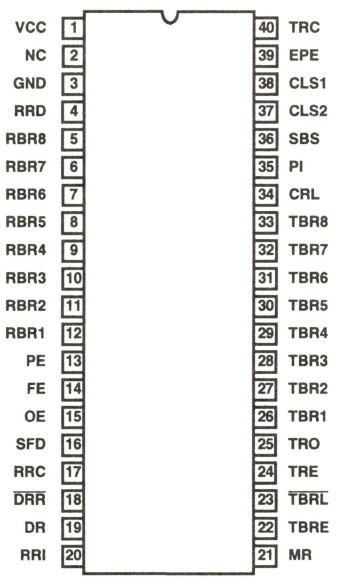
The HD-6402/883 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. Utilizing the Harris advanced scaled SAJI IV CMOS process permits operation clock frequencies up to 8.0MHz (500K Baud). Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

Ordering Information

PACKAGE	TEMPERATURE RANGE	2MHz = 125K BAUD	8MHz = 500K BAUD	PKG. NO.
CERDIP	-55°C to +125°C	HD1-6402R/883	HD1-6402B/883	F40.6

Pinout

HD-6402/883 (CERDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2953.1**

Control Definition

CONTROL WORD					CHARACTER FORMAT			
CLS 2	CLS 1	PI	EPE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	X	0	1	5	NONE	1
0	0	1	X	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	X	0	1	6	NONE	1
0	1	1	x	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	X	0	1	7	NONE	1
1	0	1	x	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	X	0	1	8	NONE	1
1	1	1	x	1	1	8	NONE	2

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage Applied. . . . . GND -0.5V to V_{CC} +0.5V
Storage Temperature Range . . . . . $-65^{o}C$ to $+150^{o}C$
Junction Temperature . . . . . $+175^{o}C$
Lead Temperature (Soldering 10s) . . . . . $+300^{o}C$
ESD Classification . . . . . Class 1
Typical Derating Factor . . . . . 1mA/MHz Increase in ICCOP

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	$50^{o}C/W$	$12^{o}C/W$

Gate Count . . . . . 1643 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V Operating Temperature Range . . . . . $-55^{o}C$ to $+125^{o}C$

TABLE 1. HD-6402/883 D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

D.C. PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical "1" Input Voltage	VIH	VCC = 5.5V	1, 2, 3	$-55^{o}C \le T_A \le +125^{o}C$	2.3	-	V
Logical "0" Input Voltage	VIL	VCC = 4.5V	1, 2, 3	$-55^{o}C \le T_A \le +125^{o}C$	-	0.8	V
Input Leakage Current	IID	VIN = GND or VCC, VCC = 5.5V	1, 2, 3	$-55^{o}C \le T_A \le +125^{o}C$	-1.0	1.0	µA
Logical "1" Output Voltage	VOH	IOH = -2.5mA, VCC = 4.5V (Note 1)	1, 2, 3	$-55^{o}C \le T_A \le +125^{o}C$	3.0	-	V
Logical "1" Output Voltage	VOH	IOH = -100µA VCC = 4.5V (Note 1)	1, 2, 3	$-55^{o}C \le T_A \le +125^{o}C$	VCC -0.4	-	V
Logical "0" Output Voltage	VOL	IOL = +2.5mA, VCC = 4.5V (Note 1)	1, 2, 3	$-55^{o}C \le T_A \le +125^{o}C$	-	0.4	V
Output Leakage Current	IO	VO = GND or VCC, VCC = 5.5V	1, 2, 3	$-55^{o}C \le T_A \le +125^{o}C$	-1.0	1.0	µA
Standby Supply Current	ICCSB	VIN = GND or VCC; VCC = 5.5V, Output Open	1, 2, 3	$-55^{o}C \le T_A \le +125^{o}C$	-	100	µA

TABLE 2. HD-6402/883 A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

A.C. PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS HD-6402/883R MIN	LIMITS HD-6402/883R MAX	LIMITS HD-6402/883B MIN	LIMITS HD-6402/883B MAX	UNITS
Clock Frequency	(1) fCLOCK	VCC = 4.5V CL = 50pF	9, 10, 11	$-55^{o}C \le T_A \le +125^{o}C$	-	2.0	-	8.0	MHz
Pulse Widths, CRL, $\overline{DRR}$, $\overline{TBRL}$	(2) tPW		9, 10, 11	$-55^{o}C \le T_A \le +125^{o}C$	150	-	75	-	ns
Pulse Width MR	(3) tMR		9, 10, 11	$-55^{o}C \le T_A \le +125^{o}C$	150	-	150	-	ns
Input Data Setup Time	(4) tSET		9, 10, 11	$-55^{o}C \le T_A \le +125^{o}C$	50	-	20	-	ns
Input Data Hold Time	(5) tHOLD		9, 10, 11	$-55^{o}C \le T_A \le +125^{o}C$	60	-	20	-	ns
Output Enable Time	(6) tEN		9, 10, 11	$-55^{o}C \le T_A \le +125^{o}C$	-	160	-	35	ns

NOTE:

1. Interchanging of force and sense conditions is permitted.
2. Tested with input levels of VIH = 2.76V and VIL = 0.4V. Rise and fall times are driven at 1ns/V.

TABLE 3. HD-6402/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

A.C. PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CIN	f = 1Mhz All Measurements are Referenced to Device GND	1	$T_A = +25^oC$	-	25.0	pF
Output Capacitance	CO		1	$T_A = +25^oC$	-	25.0	pF
Operating Supply Current	ICCOP	VCC = 5.5V, Clock Freq. = 2MHz, VIN = VCC or GND, Outputs Open	1	$-55^oC \leq T_A \leq +125^oC$	-	2.0	mA

NOTE:

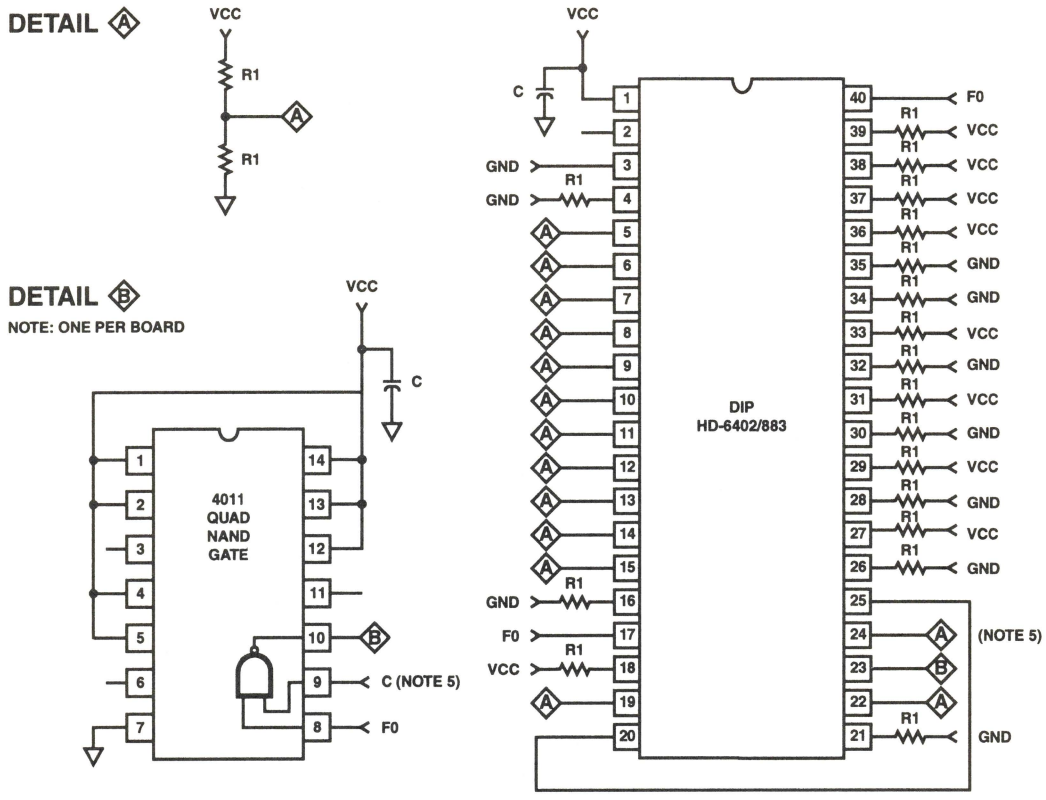
1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C and D	Samples/5005	1, 7, 9

Burn-In Circuits

HD-6402/883 CERDIP



NOTES:

1. VCC = 5.5V ± 0.5V
2. F0 = 100kHz ± 10%
3. R1 = 47kΩ, 1/4W ± 10%
4. C = 0.01µF minimum
5. One socket per board should not be loaded, but rather have pin 24 go the "C" of the 4011.

Die Characteristics

DIE DIMENSIONS:
126.4 mils x 134.3 mils x 19 mils

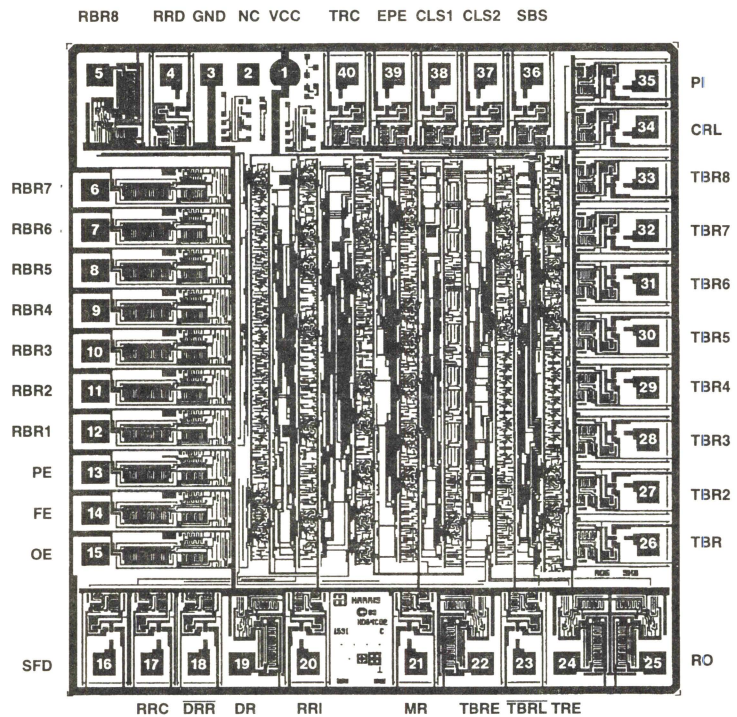
METALLIZATION:
Type: Si-Al
Thickness: 10kÅ - 12kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 7kÅ - 9kÅ

WORST CASE CURRENT DENSITY:
1.42×10^5 A/cm^2

Metallization Mask Layout

HD-6402/883



HARRIS SEMICONDUCTOR

HD-6408

CMOS Asynchronous Serial Manchester Adapter (ASMA)

March 1997

Features

- Low Bit Error Rate
- Data Rate 1MBit/s
- Sync Identification and Lock-In
- Clock Recovery
- Manchester II Encoder, Decoder
- Separate Encode and Decode
- Low Operating Power . . . . . 50mW at 5V
- Single Power Supply
- 24 Lead Package

Ordering Information

PACKAGE	TEMP. RANGE	PART NUMBER	PKG. NO.
PDIP	-40°C to +85°C	HD3-6408-9	E24.6
CERDIP	-40°C to +85°C	HD1-6408-9	E24.6

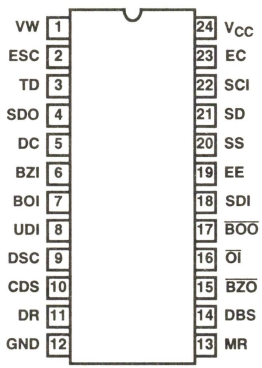
Description

The HD-6408 is a CMOS/LSI Manchester Encoder/Decoder for creating a very high speed asynchronous serial data bus. The Encoder converts serial NRZ data (typically from a shift register) to Manchester II encoded data, adding a sync pulse and parity bit. The Decoder recognizes this sync pulse and identifies it as a Command Sync or a Data Sync. The data is then decoded and shifted out in NRZ code (typically into a shift register). Finally, the parity bit is checked. If there were no Manchester or parity errors the Decoder responds with a valid word signal. The Decoder puts the Manchester code to full use to provide clock recovery and excellent noise immunity at these very high speeds.

The HD-6408 can be used in many commercial applications such as security systems, environmental control systems, serial data links and many others. It utilizes a single 12 x clock and achieves data rates of up to one million bits per second with a very minimum overhead of only 4 bits out of 20, leaving 16 bits for data.

Pinout

HD-6408 (DIP)
TOP VIEW

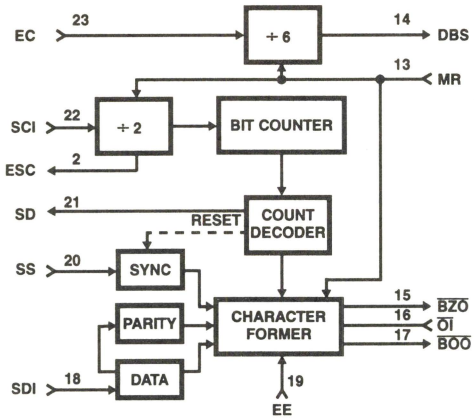


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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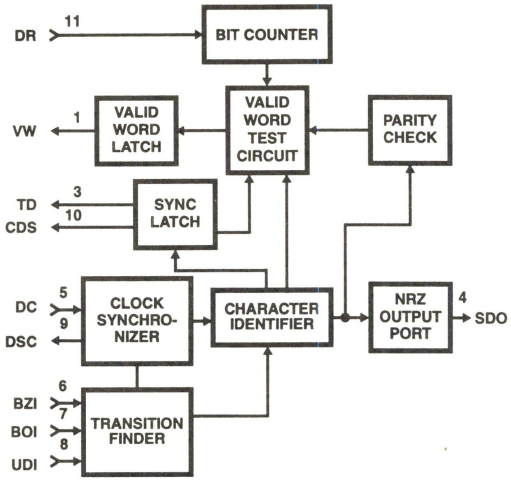
File Number 2952.1

Block Diagrams

ENCODER



DECODER



Pin Description

PIN	TYPE	SYMBOL	SECTION	DESCRIPTION
1	O	VW	Decoder	Output high indicates receipt of a VALID WORD.
2	O	ESC	Encoder	ENCODER SHIFT CLOCK is an output for shifting data into the Encoder. The Encoder samples SDI on the low-to-high transition of ESC.
3	O	TD	Decoder	TAKE DATA output is high during receipt of data after identification of a sync pulse and two valid Manchester data bits.
4	O	SDO	Decoder	SERIAL DATA OUT delivers received data in correct NRZ format.
5	I	DC	Decoder	DECODER CLOCK input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the Decoder. Input a frequency equal to 12X the data rate.
6	I	BZI	Decoder	A high input should be applied to BIPOLAR ZERO IN when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	I	BOI	Decoder	A high input should be applied to BIPOLAR ONE IN when the bus is in its positive state, this pin must be held low when the Unipolar input is used.
8	I	UDI	Decoder	With pin 6 high and pin 7 low, this pin enters UNIPOLAR DATA IN to the transition finder circuit. If not used this input must be held low.
9	O	DSC	Decoder	DECODER SHIFT CLOCK output delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
10	O	CDS	Decoder	COMMAND/DATA SYNC output high occurs during output of decoded data which was preceded by a Command synchronizing character. A low output indicates a Data synchronizing character.
11	I	DR	Decoder	A high input to DECODER RESET during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	I	GND	Both	GROUND supply pin.
13	I	MR	Both	A high on MASTER RESET clears the 2:1 counters in both the encoder and decoder and the ÷ 6 counter.
14	O	DBS	Encoder	DIVIDE BY SIX is an output from 6:1 divider which is driven by the ENCODER CLOCK.
15	O	$\overline{\text{BZO}}$	Encoder	$\overline{\text{BIPOLAR ZERO OUT}}$ is a active low output designed to drive the zero or negative sense of a bipolar line driver.
16	I	$\overline{\text{OI}}$	Encoder	A low on $\overline{\text{OUTPUT INHIBIT}}$ forces pin 15 and 17 high, their inactive states.
17	O	$\overline{\text{BOO}}$	Encoder	$\overline{\text{BIPOLAR ONE OUT}}$ is an active low output designed to drive the one or positive sense of a bipolar line driver.
18	I	SDI	Encoder	SERIAL DATA IN accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	I	EE	Encoder	A high on ENCODER ENABLE initiates the encode cycle. (Subject to the preceding cycle being completed).
20	I	SS	Encoder	SYNC SELECT actuates a Command sync for an input high and data sync for an input low.
21	O	SD	Encoder	SEND DATA is an active high output which enables the external source of serial data.
22	I	SCI	Encoder	SEND CLOCK IN is 2X the Encoder data rate.
23	I	EC	Encoder	ENCODER CLOCK is the input to the 6:1 divider.
24	I	V_{CC}	Both	V_{CC} is the +5V power supply pin. A 0.1μF decoupling capacitor from V_{CC} (pin 24) to GND (pin 12) is recommended.

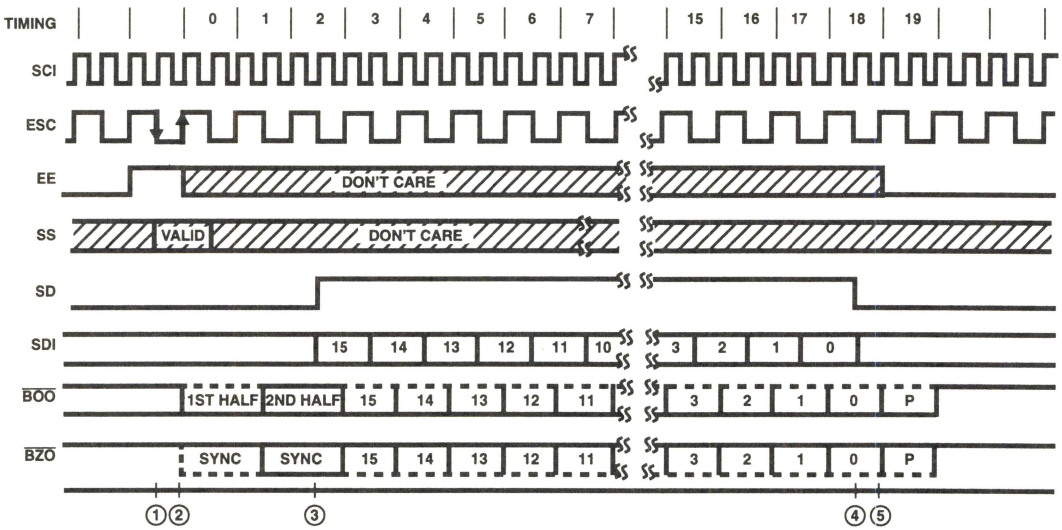
Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SClock input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SClock by dividing the DClock.

The Encoder's cycle begins when EE is high during a falling edge of ESC (1). This cycle lasts for one word length or twenty ESC periods. At the next low-to-high transition of the ESC, a high at SS input actuates a Command sync or a low will produce a Data sync for that word (2). When the Encoder is ready to accept data, the SD output will go high and remain high for sixteen ESC periods (3) - (4).

During these sixteen periods the data should be clocked into the SD Input with every high-to-low transition of the ESC (3) - (4). After the sync and Manchester II encoded data are transmitted through the $\overline{BOO}$ and $\overline{BZO}$ outputs, the Encoder adds on an additional bit which is the (odd) parity for that word (5). If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time (5) as shown to prevent a consecutive word from being encoded. At any time a low on $\overline{OI}$ will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To Abort the Encoder transmission a positive pulse must be applied at MR. Any time after or during this pulse, a low-to-high transition on SCI clears the internal counters and initializes the Encoder for a new word.



Decoder Operation

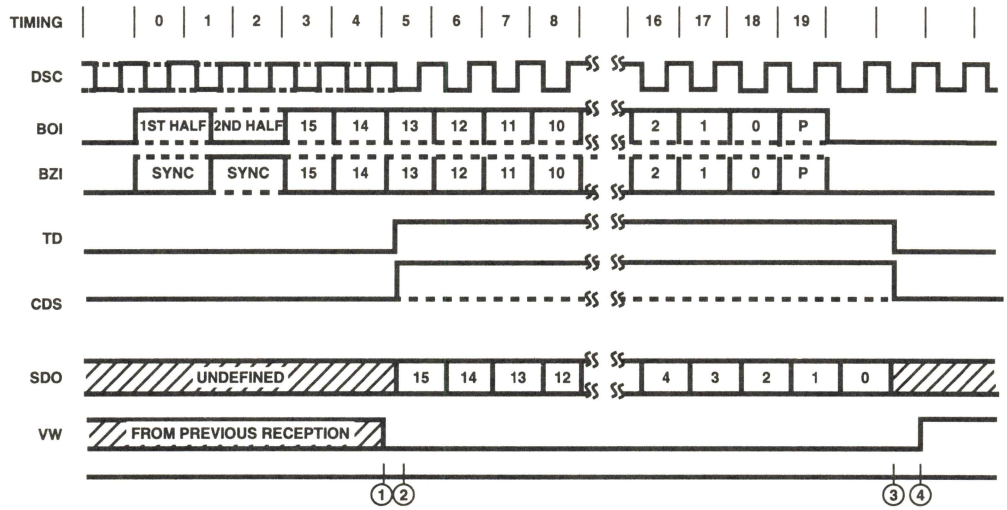
The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DClock input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BOI and BZI inputs will accept data from a differential output comparator. The UDI input can only accept noninverted Manchester II coded data (e.g. from $\overline{BOO}$ of an Encoder through an inverter to UDI).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized (1), the type of sync is indicated by the CDS output. If the sync character was a command, this output will go high (2) and remain high for sixteen DSC periods (3), otherwise it will remain low. The TD output will go high and remain high (2) - (3) while the Decoder is transmitting the decoded data through SDO.

The decoded data available at SDO is in a NRZ format. The DSC is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock (2) - (3). Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all sixteen decoded bits have been transmitted (3) the data is checked for odd parity. A high on VW output (4) indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately 20 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown (1).

At any time in the above sequence a high input on DR during a low-to-high transition of DSC will abort transmission and initialize the Decoder to start looking for a new sync character.



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
Storage Temperature Range . . . . . $-65^{o}C$ to $+150^{o}C$
Junction Temperature . . . . . $+175^{o}C$
Lead Temperature (Soldering 10s) . . . . . $+300^{o}C$
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package	$50^{o}C/W$	$11^{o}C/W$
PDIP Package	$60^{o}C/W$	N/A

Gate Count . . . . . 456 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V

Operating Temperature Range
HD-6408-9 . . . . . $-40^{o}C$ to $+85^{o}C$

DC Electrical Specifications V_{CC} = 5.0V ±10%, T_A = $-40^{o}C$ to $+85^{o}C$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}	-	-	V	
V_{IL}	Logical "0" Input Voltage	-	20% V_{CC}	-	V	
V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5	-	-	V	
V_{ILC}	Logical "0" Input Voltage (Clock)	-	GND +0.5	-	V	
II	Input Leakage	-1.0	-	+1.0	µA	V_{IN} = V_{CC} or GND, DIP Pins 5-8, 11, 13, 16, 18, 19, 20, 22, 23
V_{OH}	Logical "1" Output Voltage	2.4	-	-	V	I_{OH} = -3mA
V_{OL}	Logical "0" Output Voltage	-	-	0.4	V	I_{OL} = 1.8mA
I_{CCSB}	Supply Current Standby	-	0.5	2	mA	V_{IN} = V_{CC} = 5.5V Outputs Open
I_{CCOP}	Supply Current Operating (Note 1)	-	8.0	10.0	mA	V_{CC} = 5.5V, f = 15MHz

NOTE:

1. Guaranteed but not 100% tested.

AC Electrical Specifications V_{CC} = 5.0V ±10%, T_A = $-40^{o}C$ to $+85^{o}C$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
ENCODER TIMING						
(1) F_{EC}	Encoder Clock Frequency	0	-	12	MHz	C_L = 50pF
(2) F_{ESC}	Send Clock Frequency	0	-	2.0	MHz	C_L = 50pF
(3) T_{ECR}	Encoder Clock Rise Time	-	-	8	ns	C_L = 50pF
(4) T_{ECF}	Encoder Clock Fall Time	-	-	8	ns	C_L = 50pF
(5) F_{ED}	Data Rate	0	-	1.0	MHz	C_L = 50pF
(6) T_{MR}	Master Reset Pulse Width	150	-	-	ns	C_L = 50pF
(7) T_{E1}	Shift Clock Delay	-	-	125	ns	C_L = 50pF
(8) T_{E2}	Serial Data Setup	75	-	-	ns	C_L = 50pF
(9) T_{E3}	Serial Data Hold	75	-	-	ns	C_L = 50pF
(10) T_{E4}	Enable Setup	90	-	-	ns	C_L = 50pF
(11) T_{E5}	Enable Pulse Width	100	-	-	ns	C_L = 50pF

AC Electrical Specifications V_{CC} = 5.0V ±10%, T_A = -40°C to +85°C **(Continued)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
(12) T_{E6}	Sync Setup	55	-	-	ns	C_L = 50pF
(13) T_{E7}	Sync Pulse Width	150	-	-	ns	C_L = 50pF
(14) T_{E8}	Send Data Delay	0	-	50	ns	C_L = 50pF
(15) T_{E9}	Bipolar Output Delay	-	-	130	ns	C_L = 50pF
(16) T_{E10}	Enable Hold	10	-	-	ns	C_L = 50pF
(17) T_{E11}	Sync Hold	95	-	-	ns	C_L = 50pF
DECODER TIMING						
(18) F_{DC}	Decoder Clock Frequency	0	-	12	MHz	C_L = 50pF
(19) T_{DCR}	Decoder Clock Rise Time	-	-	8	ns	C_L = 50pF
(20) T_{DCF}	Decoder Clock Fall Time	-	-	8	ns	C_L = 50pF
(21) F_{DD}	Data Rate	0	-	1.0	MHz	C_L = 50pF
(22) T_{DR}	Decoder Reset Pulse Width	150	-	-	ns	C_L = 50pF
(23) T_{DRS}	Decoder Reset Setup Time	75	-	-	ns	C_L = 50pF
(24) T_{DRH}	Decoder Reset Hold Time	10	-	-	ns	C_L = 50pF
(25) T_{MR}	Master Reset Pulse Width	150	-	-	ns	C_L = 50pF
(26) T_{D1}	Bipolar Data Pulse Width	T_{DC} +10	-	-	ns	Note 1, C_L = 50pF
(27) T_{D2}	Sync Transition Span	-	$18T_{DC}$	-	ns	Note 1, C_L = 50pF
(28) T_{D3}	One Zero Overlap	-	-	T_{DC} -10	ns	Note 1, C_L = 50pF
(29) T_{D4}	Short Data Transition Span	-	$6T_{DC}$	-	ns	Note 1, C_L = 50pF
(30) T_{D5}	Long Data Transition Span	-	$12T_{DC}$	-	ns	Note 1, C_L = 50pF
(31) T_{D6}	Sync Delay (ON)	-20	-	110	ns	C_L = 50pF
(32) T_{D7}	Take Data Delay (ON)	0	-	110	ns	C_L = 50pF
(33) T_{D8}	Serial Data Out Delay	-	-	80	ns	C_L = 50pF
(34) T_{D9}	Sync Delay (OFF)	0	-	110	ns	C_L = 50pF
(35) T_{D10}	Take Data Delay (OFF)	0	-	110	ns	C_L = 50pF
(36) T_{D11}	Valid Word Delay	0	-	110	ns	C_L = 50pF

NOTE:

1. T_{DC} = Decoder Clock Period = $^1/F_{DC}$. (These parameters are guaranteed but not 100% tested).

Capacitance T_A = +25°C

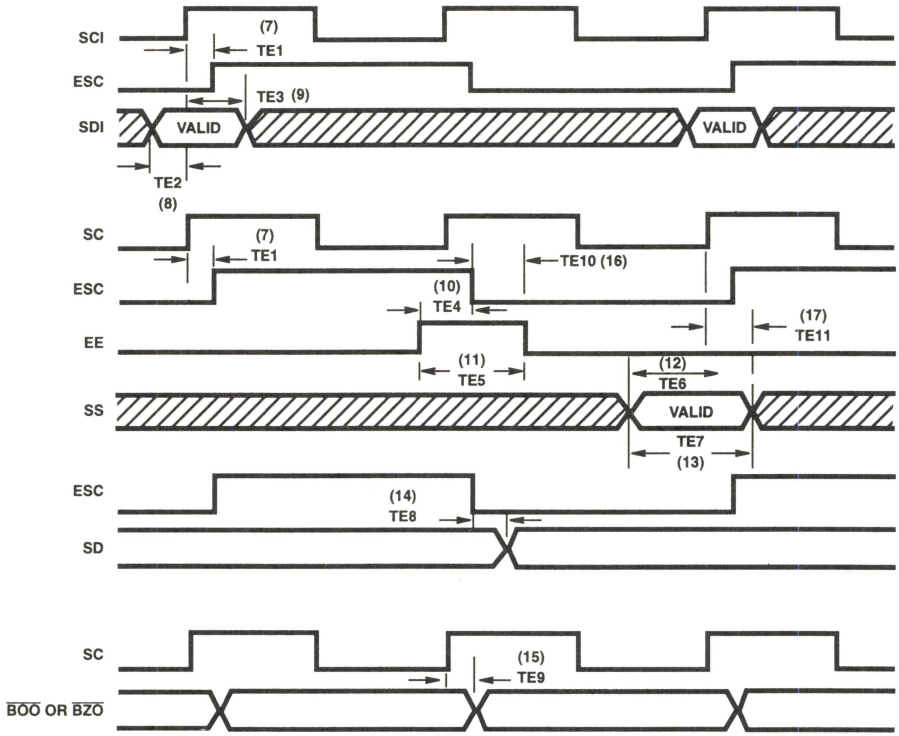
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	-	15	-	pF	FREQ = 1MHz, all measurements are referenced to device GND
C_O	Output Capacitance	-	15	-	pF	

AC Testing Input, Output Waveform



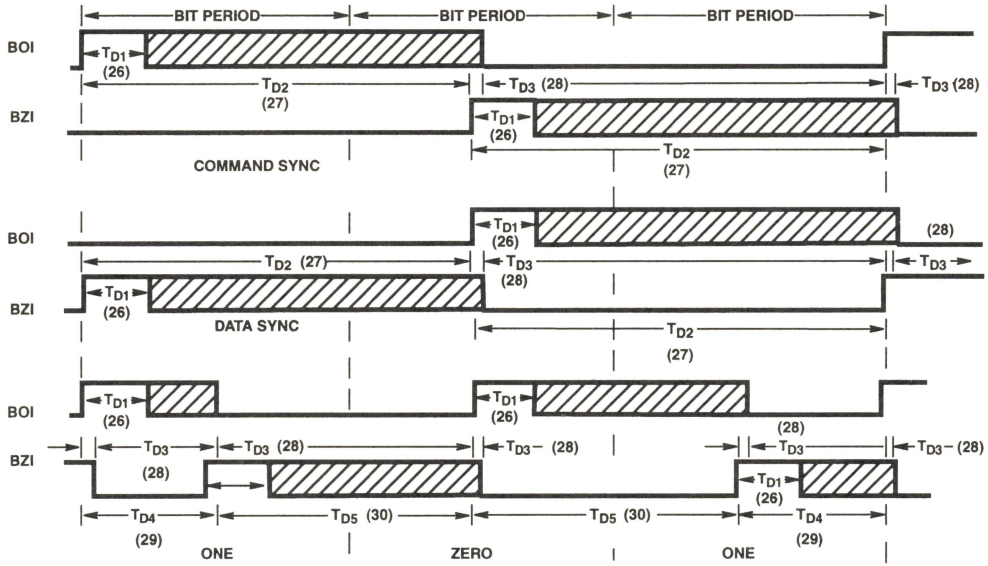
NOTE: AC Testing: All input signals must switch between V_{IL} and V_{IH}. Input rise and fall times are driven at 1ns per volt.

Encoder Timing

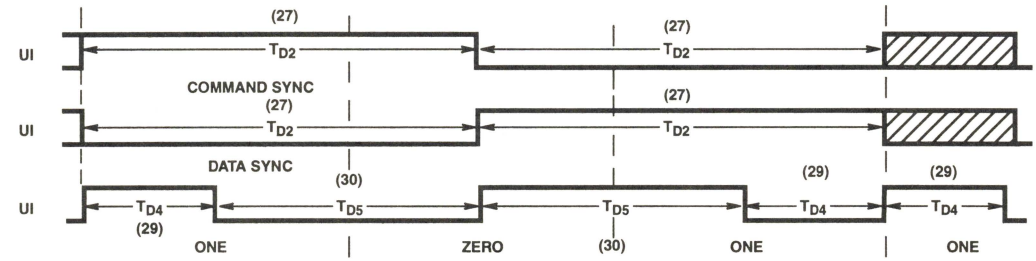


Decoder Timing

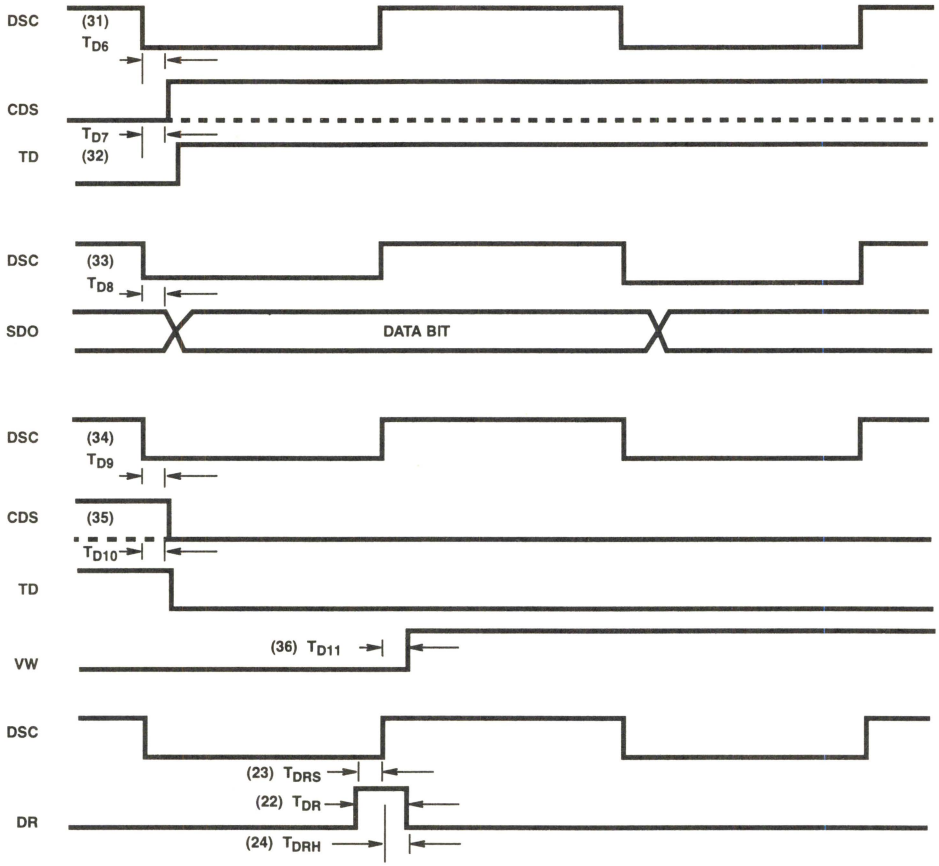
NOTE: UI = 0, FOR NEXT DIAGRAMS



NOTE: BOI = 0, BZI = 1 FOR NEXT DIAGRAMS



Decoder Timing (Continued)



March 1997

CMOS Manchester Encoder-Decoder

Features

- Converter or Repeater Mode
- Independent Manchester Encoder and Decoder Operation
- Static to One Megabit/sec Data Rate Guaranteed
- Low Bit Error Rate
- Digital PLL Clock Recovery
- On Chip Oscillator
- Low Operating Power: 50mW Typical at +5V
- Available in 20 Lead Dual-In-Line and 20 Pad LCC Package

Ordering Information

PACKAGE	TEMPERATURE RANGE	1 MEGABIT/SEC	PKG. NO.
PDIP	-40°C to +85°C	HD3-6409-9	E20.3
SOIC	-40°C to +85°C	HD9P6409-9	M20.3
CERDIP	-40°C to +85°C	HD1-6409-9	F20.3
DESC	-55°C to 125°C	5962-9088801MRA	F20.3
CLCC	-40°C to +85°C	HD4-6409-9	J20.A
DESC	-55°C to 125°C	5962-9088801M2A	J20.A

Description

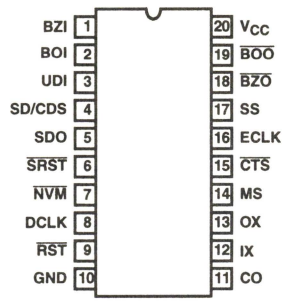
The HD-6409 Manchester Encoder-Decoder (MED) is a high speed, low power device manufactured using self-aligned silicon gate technology. The device is intended for use in serial data communication, and can be operated in either of two modes. In the converter mode, the MED converts Non return-to-Zero code (NRZ) into Manchester code and decodes Manchester code into Nonreturn-to-Zero code. For serial data communication, Manchester code does not have some of the deficiencies inherent in Nonreturn-to-Zero code. For instance, use of the MED on a serial line eliminates DC components, provides clock recovery, and gives a relatively high degree of noise immunity. Because the MED converts the most commonly used code (NRZ) to Manchester code, the advantages of using Manchester code are easily realized in a serial data link.

In the Repeater mode, the MED accepts Manchester code input and reconstructs it with a recovered clock. This minimizes the effects of noise on a serial data link. A digital phase lock loop generates the recovered clock. A maximum data rate of 1MHz requires only 50mW of power.

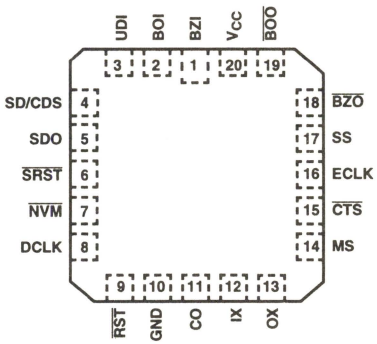
Manchester code is used in magnetic tape recording and in fiber optic communication, and generally is used where data accuracy is imperative. Because it frames blocks of data, the HD-6409 easily interfaces to protocol controllers.

Pinouts

HD-6409 (CERDIP, PDIP, SOIC)
TOP VIEW

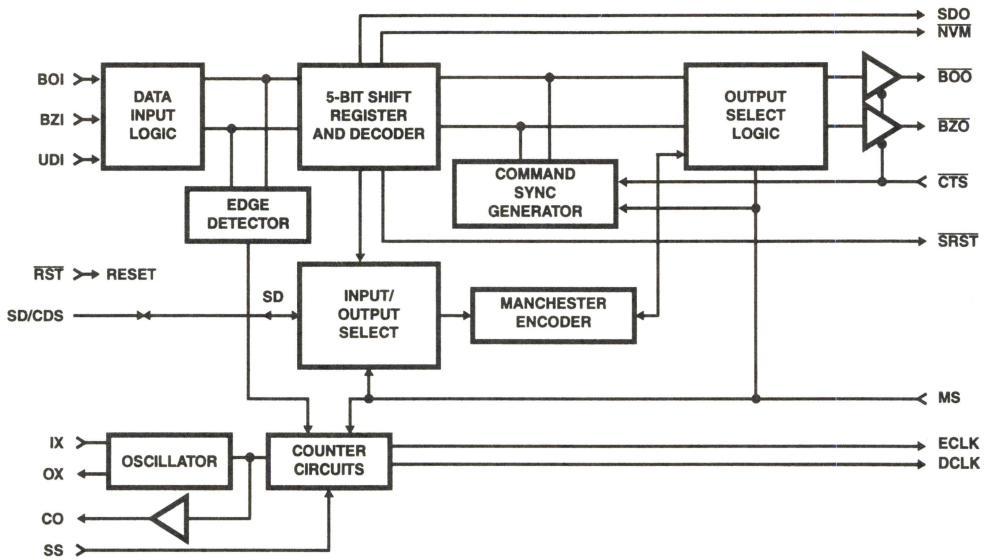


HD-6409 (CLCC)
TOP VIEW

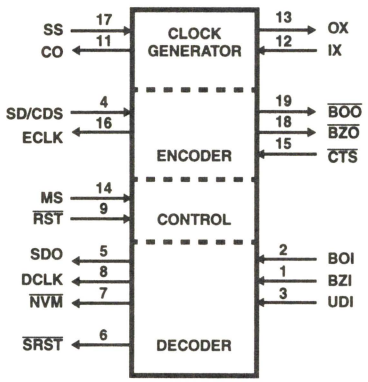


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Block Diagram



Logic Symbol



Pin Description

PIN NUMBER	TYPE	SYMBOL	NAME	DESCRIPTION
1	I	BZI	Bipolar Zero Input	Used in conjunction with pin 2, Bipolar One Input (BOI), to input Manchester II encoded data to the decoder, BZI and BOI are logical complements. When using pin 3, Unipolar Data Input (UDI) for data input, BZI must be held high.
2	I	BOI	Bipolar One Input	Used in conjunction with pin 1, Bipolar Zero Input (BZI), to input Manchester II encoded data to the decoder, BOI and BZI are logical complements. When using pin 3, Unipolar Data Input (UDI) for data input, BOI must be held low.
3	I	UDI	Unipolar Data Input	An alternate to bipolar input (BZI, BOI), Unipolar Data Input (UDI) is used to input Manchester II encoded data to the decoder. When using pin 1 (BZI) and pin 2 (BOI) for data input, UDI must be held low.
4	I/O	SD/CDS	Serial Data/Command Data Sync	In the converter mode, SD/CDS is an input used to receive serial NRZ data. NRZ data is accepted synchronously on the falling edge of encoder clock output (ECLK). In the repeater mode, SD/CDS is an output indicating the status of last valid sync pattern received. A high indicates a command sync and a low indicates a data sync pattern.
5	O	SDO	Serial Data Out	The decoded serial NRZ data is transmitted out synchronously with the decoder clock (DCLK). SDO is forced low when $\overline{RST}$ is low.
6	O	$\overline{SRST}$	Serial Reset	In the converter mode, $\overline{SRST}$ follows $\overline{RST}$. In the repeater mode, when $\overline{RST}$ goes low, $\overline{SRST}$ goes low and remains low after $\overline{RST}$ goes high. $\overline{SRST}$ goes high only when $\overline{RST}$ is high, the reset bit is zero, and a valid synchronization sequence is received.
7	O	$\overline{NVM}$	Nonvalid Manchester	A low on $\overline{NVM}$ indicates that the decoder has received invalid Manchester data and present data on Serial Data Out (SDO) is invalid. A high indicates that the sync pulse and data were valid and SDO is valid. $\overline{NVM}$ is set low by a low on $\overline{RST}$, and remains low after $\overline{RST}$ goes high until valid sync pulse followed by two valid Manchester bits is received.
8	O	DCLK	Decoder Clock	The decoder clock is a 1X clock recovered from BZI and BOI, or UDI to synchronously output received NRZ data (SDO).
9	I	$\overline{RST}$	Reset	In the converter mode, a low on $\overline{RST}$ forces SDO, DCLK, $\overline{NVM}$, and $\overline{SRST}$ low. A high on $\overline{RST}$ enables SDO and DCLK, and forces $\overline{SRST}$ high. $\overline{NVM}$ remains low after $\overline{RST}$ goes high until a valid sync pulse followed by two Manchester bits is received, after which it goes high. In the repeater mode, $\overline{RST}$ has the same effect on SDO, DCLK and $\overline{NVM}$ as in the converter mode. When $\overline{RST}$ goes low, $\overline{SRST}$ goes low and remains low after $\overline{RST}$ goes high. $\overline{SRST}$ goes high only when $\overline{RST}$ is high, the reset bit is zero and a valid synchronization sequence is received.
10	I	GND	Ground	Ground
11	O	C_O	Clock Output	Buffered output of clock input I_X. May be used as clock signal for other peripherals.
12	I	I_X	Clock Input	I_X is the input for an external clock or, if the internal oscillator is used, I_X and O_X are used for the connection of the crystal.
13	O	O_X	Clock Drive	If the internal oscillator is used, O_X and I_X are used for the connection of the crystal.
14	I	MS	Mode Select	MS must be held low for operation in the converter mode, and high for operation in the repeater mode.
15	I	$\overline{CTS}$	Clear to Send	In the converter mode, a high disables the encoder, forcing outputs $\overline{BOO}$, $\overline{BZO}$ high and ECLK low. A high to low transition of $\overline{CTS}$ initiates transmission of a Command sync pulse. A low on $\overline{CTS}$ enables $\overline{BOO}$, $\overline{BZO}$, and ECLK. In the repeater mode, the function of $\overline{CTS}$ is identical to that of the converter mode with the exception that a transition of $\overline{CTS}$ does not initiate a synchronization sequence.
16	O	ECLK	Encoder Clock	In the converter mode, ECLK is a 1X clock output used to receive serial NRZ data to SD/CDS. In the repeater mode, ECLK is a 2X clock which is recovered from BZI and BOI data by the digital phase locked loop.

Pin Description

PIN NUMBER	TYPE	SYMBOL	NAME	DESCRIPTION
17	I	SS	Speed Select	A logic high on SS sets the data rate at 1/32 times the clock frequency while a low sets the data rate at 1/16 times the clock frequency.
18	O	$\overline{BZO}$	$\overline{Bipolar\ Zero\ Output}$	$\overline{BZO}$ and its logical complement $\overline{BOO}$ are the Manchester data outputs of the encoder. The inactive state for these outputs is in the high state.
19	O	$\overline{BOO}$	$\overline{Bipolar\ One\ Out}$	See pin 18.
20	I	V_{CC}	V_{CC}	V_{CC} is the +5V power supply pin. A 0.1µF decoupling capacitor from V_{CC} (pin-20) to GND (pin-10) is recommended.

NOTE: (I) Input (O) Output

Encoder Operation

The encoder uses free running clocks at 1X and 2X the data rate derived from the system clock I_X for internal timing. $\overline{CTS}$ is used to control the encoder outputs, ECLK, $\overline{BOO}$ and $\overline{BZO}$. A free running 1X ECLK is transmitted out of the encoder to drive the external circuits which supply the NRZ data to the MED at pin SD/CDS.

A low on $\overline{CTS}$ enables encoder outputs ECLK, $\overline{BOO}$ and $\overline{BZO}$, while a high on $\overline{CTS}$ forces $\overline{BZO}$, $\overline{BOO}$ high and holds ECLK low. When $\overline{CTS}$ goes from high to low (1), a synchronization sequence is transmitted out on $\overline{BOO}$ and $\overline{BZO}$. A synchronization sequence consists of eight Manchester "0" bits followed by a command sync pulse. (2) A command sync pulse is a 3-bit wide pulse with the first 1 1/2 bits high followed by 1 1/2 bits low. (3) Serial NRZ data is clocked into the encoder at SD/CDS on the high to low transition of ECLK during the command sync pulse. The NRZ data received is encoded into Manchester II data and transmitted out on $\overline{BOO}$ and $\overline{BZO}$ following the command sync pulse. (4) Following the synchronization sequence, input data is encoded and transmitted out continuously without parity check or word framing. The length of the data block encoded is defined by $\overline{CTS}$. Manchester data out is inverted.

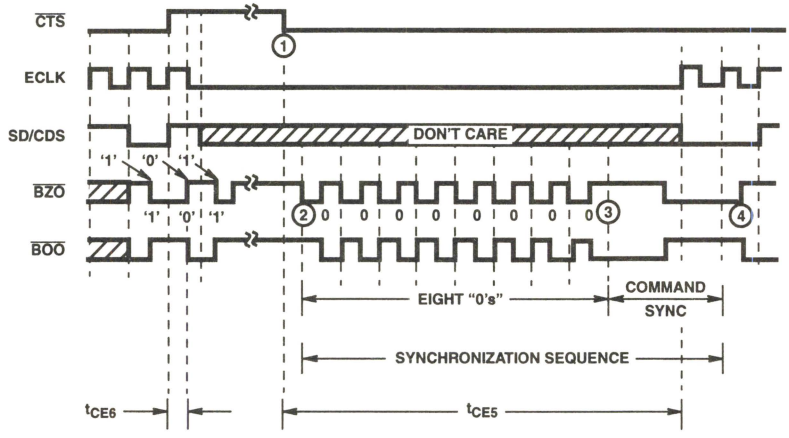


FIGURE 1. ENCODER OPERATION

Decoder Operation

The decoder requires a single clock with a frequency 16X or 32X the desired data rate. The rate is selected on the speed select with SS low producing a 16X clock and high a 32X clock. For long data links the 32X mode should be used as this permits a wider timing jitter margin. The internal operation of the decoder utilizes a free running clock synchronized with incoming data for its clocking.

The Manchester II encoded data can be presented to the decoder in either of two ways. The Bipolar One and Bipolar Zero inputs will accept data from differential inputs such as a comparator sensed transformer coupled bus. The Unipolar Data input can only accept noninverted Manchester II encoded data i.e. $\overline{Bipolar\ One\ Out}$ through an inverter to Unipolar Data Input. The decoder continuously monitors this data input for valid sync pattern. Note that while the MED encoder section can generate only a command sync pattern, the decoder can recognize either a command or data sync pattern. A data sync is a logically inverted command sync.

There is a three bit delay between UDI, BOI, or BZI input and the decoded NRZ data transmitted out of SDO.

Control of the decoder outputs is provided by the $\overline{RST}$ pin. When $\overline{RST}$ is low, SDO, DCLK and $\overline{NVM}$ are forced low. When $\overline{RST}$ is high, SDO is transmitted out synchronously with the recovered clock DCLK. The $\overline{NVM}$ output remains low after a low to high transition on $\overline{RST}$ until a valid sync pattern is received.

The decoded data at SDO is in NRZ format. DCLK is provided so that the decoded bits can be shifted into an external register on every high to low transition of this clock. Three bit periods after an invalid Manchester bit is received on UDI, or BOI, $\overline{NVM}$ goes low synchronously with the questionable data output on SDO. FURTHER, THE DECODER DOES NOT REESTABLISH PROPER DATA DECODING UNTIL ANOTHER SYNC PATTERN IS RECOGNIZED.

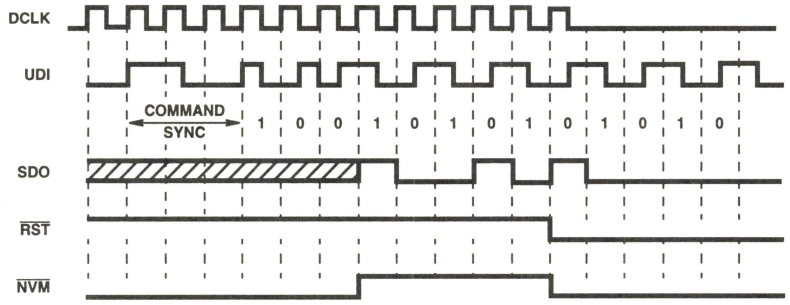


FIGURE 2. DECODER OPERATION

Repeater Operation

Manchester II data can be presented to the repeater in either of two ways. The inputs Bipolar One In and Bipolar Zero In will accept data from differential inputs such as a comparator or sensed transformer coupled bus. The input Unipolar Data In accepts only noninverted Manchester II coded data. The decoder requires a single clock with a frequency 16X or 32X the desired data rate. This clock is selected to 16X with Speed Select low and 32X with Speed Select high. For long data links the 32X mode should be used as this permits a wider timing jitter margin.

The inputs UDI, or BOI, BZI are delayed approximately 1/2 bit period and repeated as outputs $\overline{BOO}$ and $\overline{BZO}$. The 2X ECLK is transmitted out of the repeater synchronously with $\overline{BOO}$ and $\overline{BZO}$.

A low on $\overline{CTS}$ enables ECLK, $\overline{BOO}$, and $\overline{BZO}$. In contrast to the converter mode, a transition on CTS does not initiate a synchronization sequence of eight 0's and a command sync. The repeater mode does recognize a command or data sync pulse. SD/CDS is an output which reflects the state of the most recent sync pulse received, with high indicating a command sync and low indicating a data sync.

When $\overline{RST}$ is low, the outputs SDO, DCLK, and $\overline{NVM}$ are low, and $\overline{SRST}$ is set low. $\overline{SRST}$ remains low after $\overline{RST}$ goes high and is not reset until a sync pulse and two valid manchester bits are received with the reset bit low. The reset bit is the first data bit after the sync pulse. With RST high, NRZ Data is transmitted out of Serial Data Out synchronously with the 1X DCLK.

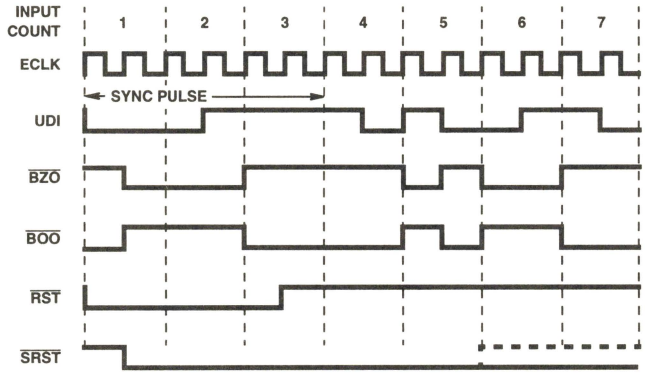


FIGURE 3. REPEATER OPERATION

Manchester Code

Nonreturn-to-Zero (NRZ) code represents the binary values logic-O and logic-1 with a static level maintained throughout the data cell. In contrast, Manchester code represents data with a level transition in the middle of the data cell. Manchester has bandwidth, error detection, and synchronization advantages over NRZ code.

The Manchester II code Bipolar One and Bipolar Zero shown below are logical complements. The direction of the transition indicates the binary value of data. A logic-0 in Bipolar One is defined as a Low to high transition in the middle of the data cell, and a logic-1 as a high to low mid bit transition, Manchester II is also known as Biphase-L code.

The bandwidth of NRZ is from DC to the clock frequency fc/2, while that of Manchester is from fc/2 to fc. Thus, Manchester can be AC or transformer coupled, which has considerable advantages over DC coupling. Also, the ratio of maximum to minimum frequency of Manchester extends one octave, while the ratio for NRZ is the range of 5-10 octaves. It is much easier to design a narrow band than a wideband amp.

Secondly, the mid bit transition in each data cell provides the code with an effective error detection scheme. If noise produces a logic inversion in the data cell such that there is no transition, an error indiction is given, and synchronization must be re-established. This places relatively stringent requirements on the incoming data.

The synchronization advantages of using the HD-6409 and Manchester code are several fold. One is that Manchester is a self clocking code. The clock in serial data communication defines the position of each data cell. Non self clocking codes, as NRZ, often require an extra clock wire or clock track (in magnetic recording). Further, there can be a phase variation between the clock and data track. Crosstalk between the two may be a problem. In Manchester, the serial data stream contains both the clock and the data, with the position of the mid bit transition representing the clock, and the direction of the transition representing data. There is no phase variation between the clock and the data.

A second synchronization advantage is a result of the number of transitions in the data. The decoder resynchronizes on each transition, or at least once every data cell. In contrast, receivers using NRZ, which does not necessarily have transitions, must resynchronize on frame bit transitions, which occur far less often, usually on a character basis. This more frequent resynchronization eliminates the cumulative effect of errors over successive data cells. A final synchronization advantage concerns the HD-6409's sync pulse used to initiate synchronization. This three bit wide pattern is sufficiently distinct from Manchester data that a false start by the receiver is unlikely.

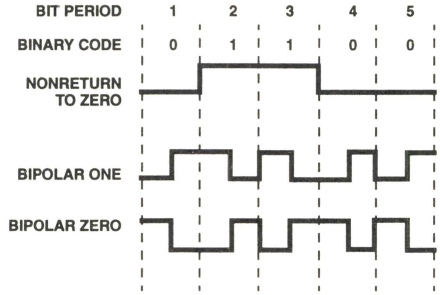


FIGURE 4. MANCHESTER CODE

Crystal Oscillator Mode

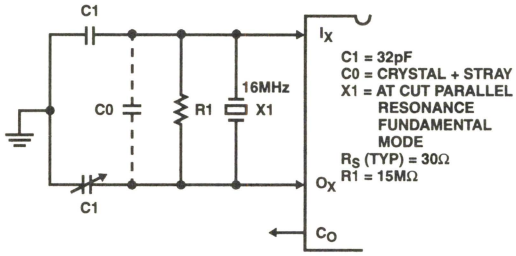


FIGURE 5. CRYSTAL OSCILLATOR MODE

LC Oscillator Mode

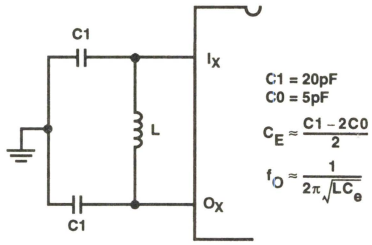


FIGURE 6. LC OSCILLATOR MODE

Using the 6409 as a Manchester Encoded UART

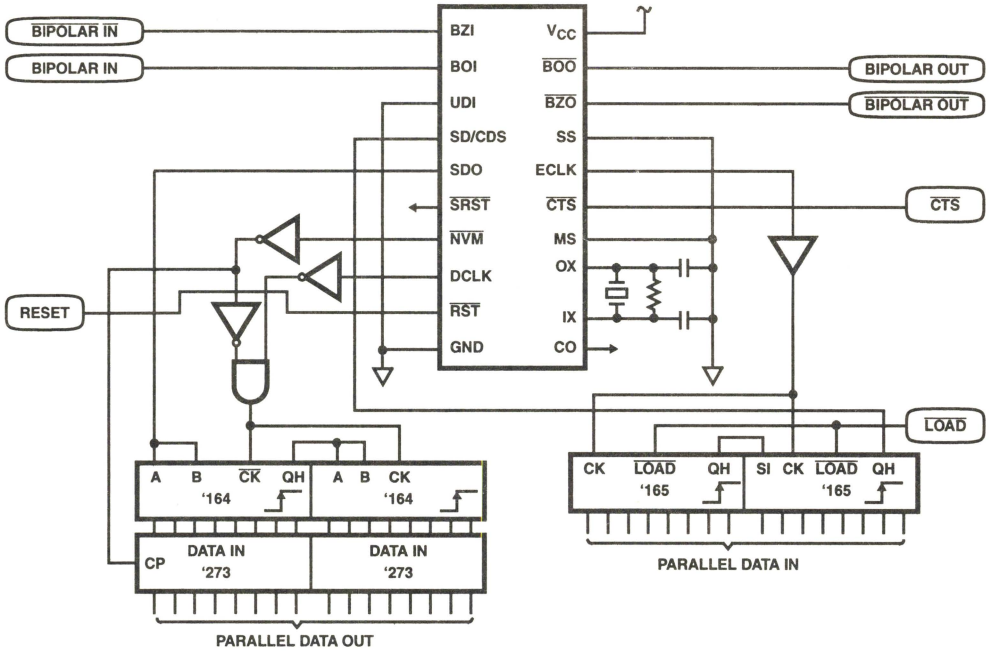


FIGURE 7. MANCHESTER ENCODER UART

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP	83°C/W	23°C/W
CLCC Package	95°C/W	26°C/W
PDIP Package	75°C/W	N/A
SOIC Package	100°C/W	N/A

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package . . . . . +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(Lead Tips Only for Surface Mount Packages)

Die Characteristics

Gate Count . . . . . 250 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range . . . . . -40°C to +85°C
Operating Voltage Range . . . . . +4.5V to +5.5V
Input Rise and Fall Times . . . . . 50ns Max
Sync. Transition Span (t2) . . . . . 1.5 DBP Typical, (Notes 1, 2)
Short Data Transition Span (t4) . . . . . 0.5DBP Typical, (Notes 1, 2)
Long Data Transition Span (t5) . . . . . 1.0DBP Typical, (Notes 1, 2)
Zero Crossing Tolerance (tCD5) . . . . . (Note 3)

NOTES:

1. DBP-Data Bit Period, Clock Rate = 16X, one DBP = 16 Clock Cycles; Clock Rate = 32X, one DBP = 32 Clock Cycles.
2. The input conditions specified are nominal values, the actual input waveforms transition spans may vary by ±2 I_X clock cycles (16X mode) or ±6 I_X clock cycles (32X mode).
3. The maximum zero crossing tolerance is ±2 I_X clock cycles (16X mode) or ±6 I_X clock cycles (32 mode) from the nominal.

DC Electrical Specifications V_{CC} = 5.0V ± 10%, T_A = -40°C to +85° (HD-6409-9)

SYMBOL	PARAMETER	MIN	MAX	UNITS	(NOTE 1) TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}	-	V	V_{CC} = 4.5V
V_{IL}	Logical "0" Input Voltage	-	20% V_{CC}	V	V_{CC} = 4.5V
V_{IHR}	Logic "1" Input Voltage ($\overline{Reset}$)	V_{CC} -0.5	-	V	V_{CC} = 5.5V
V_{ILR}	Logic "0" Input Voltage ($\overline{Reset}$)	-	GND +0.5	V	V_{CC} = 4.5V
V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5	-	V	V_{CC} = 5.5V
V_{ILC}	Logical "0" Input Voltage (Clock)	-	GND +0.5	V	V_{CC} = 4.5V
I_I	Input Leakage Current (Except I_X)	-1.0	+1.0	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V
I_I	Input Leakage Current (I_X)	-20	+20	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V
I_O	I/O Leakage Current	-10	+10	µA	V_{OUT} = V_{CC} or GND, V_{CC} = 5.5V
V_{OH}	Output HIGH Voltage (All Except O_X)	V_{CC} -0.4	-	V	I_{OH} = -2.0mA, V_{CC} = 4.5V (Note 2)
V_{OL}	Output LOW Voltage (All Except O_X)	-	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.5V (Note 2)
I_{CCSB}	Standby Power Supply Current	-	100	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs Open
I_{CCOP}	Operating Power Supply Current	-	18.0	mA	f = 16.0MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.5V, C_L = 50pF
F_T	Functional Test	-	-	-	(Note 1)

NOTES:

1. Tested as follows: f = 16MHz, V_{IH} = 70% V_{CC}, V_{IL} = 20% V_{CC}, $V_{OH} \geq V_{CC}/2$, and $V_{OL} \leq V_{CC}/2$, V_{CC} = 4.5V and 5.5V.
2. Interchanging of force and sense conditions is permitted

Capacitance T_A = +25°C, Frequency = 1MHz

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	10	pF	All measurements are referenced to device GND
C_{OUT}	Output Capacitance	12	pF	

AC Electrical Specifications V_{CC} = 5.0V ±10%, T_A = -40°C to +85°C (HD-6409-9)

SYMBOL	PARAMETER	MIN	MAX	UNITS	(NOTE 1) TEST CONDITIONS
f_C	Clock Frequency	-	16	MHz	-
t_C	Clock Period	$1/f_C$	-	sec	-
t_1	Bipolar Pulse Width	t_C+10	-	ns	-
t_3	One-Zero Overlap	-	t_C-10	ns	-
t_{CH}	Clock High Time	20	-	ns	f = 16.0MHz
t_{CL}	Clock Low Time	20	-	ns	f = 16.0MHz
t_{CE1}	Serial Data Setup Time	120	-	ns	-
t_{CE2}	Serial Data Hold Time	0	-	ns	-
t_{CD2}	DCLK to SDO, $\overline{NVM}$	-	40	ns	-
t_{R2}	ECLK to $\overline{BZO}$	-	40	ns	-
t_r	Output Rise Time (All except Clock)	-	50	ns	From 1.0V to 3.5V, C_L = 50pF, Note 2
t_f	Output Fall Time (All except Clock)	-	50	ns	From 3.5V to 1.0V, C_L = 50pF, Note 2
t_r	Clock Output Rise Time	-	11	ns	From 1.0V to 3.5V, C_L = 20pF, Note 2
t_f	Clock Output Fall Time	-	11	ns	From 3.5V to 1.0V, C_L = 20pF, Note 2
t_{CE3}	ECLK to $\overline{BZO}$, $\overline{BOO}$	0.5	1.0	DBP	Notes 2, 3
t_{CE4}	$\overline{CTS}$ Low to $\overline{BZO}$, $\overline{BOO}$ Enabled	0.5	1.5	DBP	Notes 2, 3
t_{CE5}	$\overline{CTS}$ Low to ECLK Enabled	10.5	11.5	DBP	Notes 2, 3
t_{CE6}	$\overline{CTS}$ High to ECLK Disabled	-	1.0	DBP	Notes 2, 3
t_{CE7}	$\overline{CTS}$ High to $\overline{BZO}$, $\overline{BOO}$ Disabled	1.5	2.5	DBP	Notes 2, 3
t_{CD1}	UDI to SDO, $\overline{NVM}$	2.5	3.0	DBP	Notes 2, 3
t_{CD3}	$\overline{RST}$ Low to CDLK, SDO, $\overline{NVM}$ Low	0.5	1.5	DBP	Notes 2, 3
t_{CD4}	$\overline{RST}$ High to DCLK, Enabled	0.5	1.5	DBP	Notes 2, 3
t_{R1}	UDI to $\overline{BZO}$, $\overline{BOO}$	0.5	1.0	DBP	Notes 2, 3
t_{R3}	UDI to SDO, $\overline{NVM}$	2.5	3.0	DBP	Notes 2, 3

NOTES:

1. AC testing as follows: f = 4.0MHz, V_{IH} = 70% V_{CC}, V_{IL} = 20% V_{CC}, Speed Select = 16X, $V_{OH} \geq V_{CC}/2$, $V_{OL} \leq V_{CC}/2$, V_{CC} = 4.5V and 5.5V. Input rise and fall times driven at 1ns/V, Output load = 50pF.
2. Guaranteed via characteristics at initial device design and after major process and/or design changes, not tested.
3. DBP-Data Bit Period, Clock Rate = 16X, one DBP = 16 Clock Cycles; Clock Rate = 32X, one DBP = 32 Clock Cycles.

Timing Waveforms

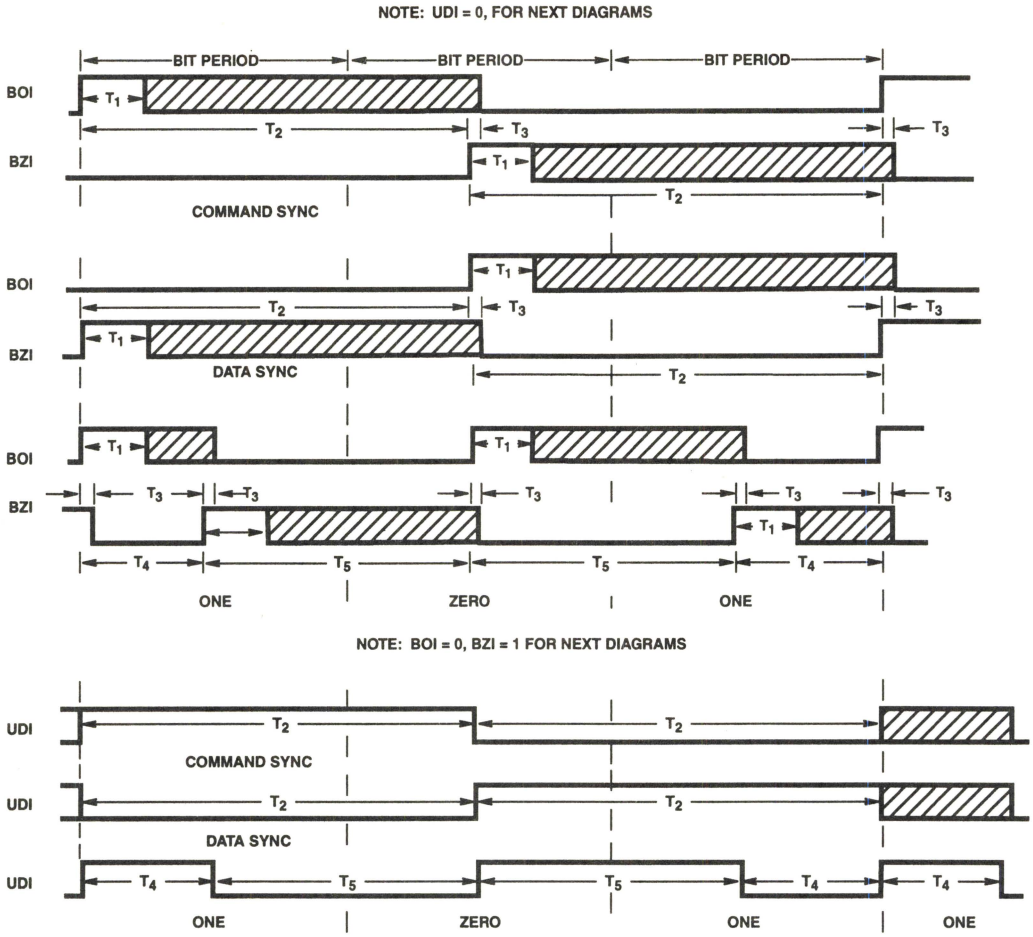


FIGURE 8.

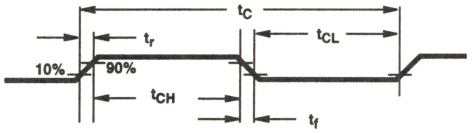


FIGURE 9. CLOCK TIMING

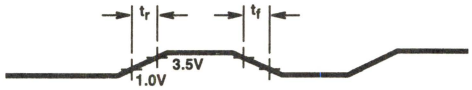


FIGURE 10. OUTPUT WAVEFORM

Timing Waveforms (Continued)

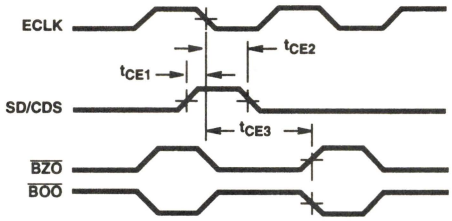


FIGURE 11. ENCODER TIMING

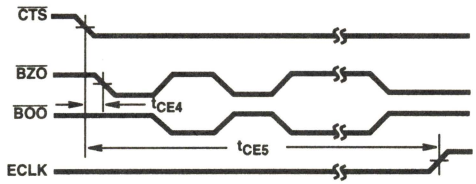


FIGURE 12. ENCODER TIMING

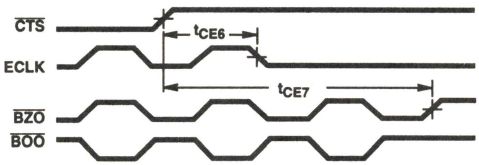
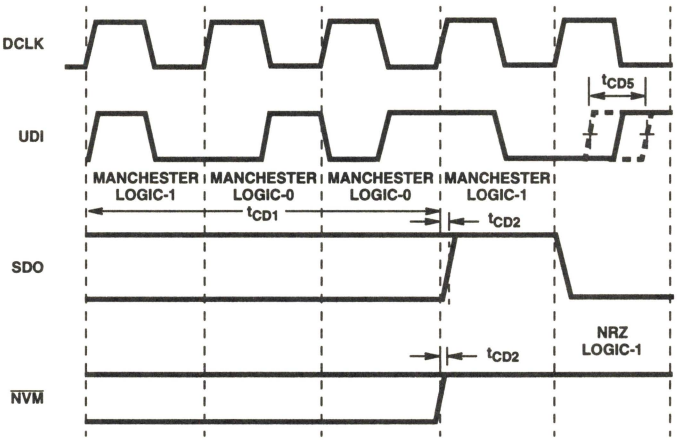


FIGURE 13. ENCODER TIMING



NOTE: Manchester Data-In is not synchronous with Decoder Clock.
Decoder Clock is synchronous with decoded NRZ out of SDO.

FIGURE 14. DECODER TIMING

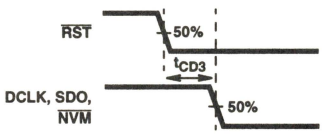


FIGURE 15. DECODER TIMING

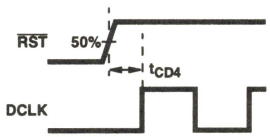


FIGURE 16. DECODER TIMING

Timing Waveforms (Continued)

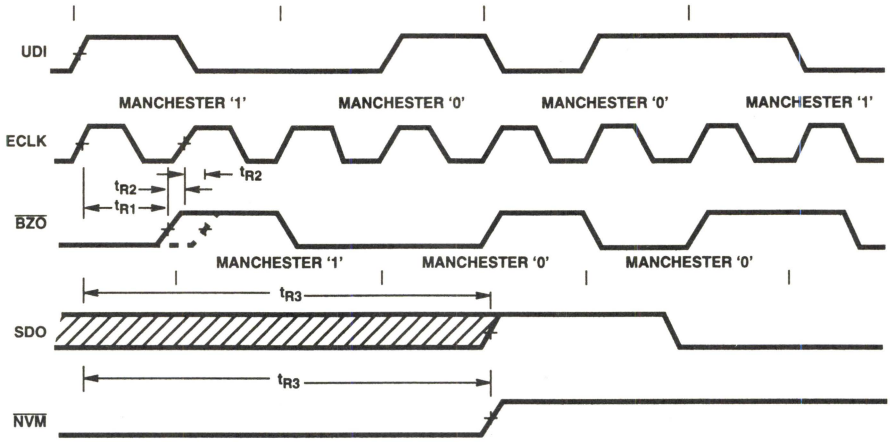
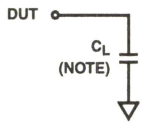


FIGURE 17. REPEATER TIMING

Test Load Circuit



NOTE: INCLUDES STRAY AND JIG CAPACITANCE

FIGURE 18. TEST LOAD CIRCUIT

HARRIS SEMICONDUCTOR

HD-6409/883

March 1997

CMOS Manchester Encoder-Decoder

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Converter or Repeater Mode**
- **Independent Manchester Encoder and Decoder Operation**
- **Static to One Megabit/Sec Data Rate Guaranteed**
- **Low Bit Error Rate**
- **Digital PLL Clock Recovery**
- **On Chip Oscillator**
- **Low Operating Power: 50mW Typical at +5V**
- **Available in 20 Lead Dual-In-Line and 20 Pad LCC Package**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PKG. NO.
HD1-6409/883	-55°C to +125°C	CERDIP	F20.3
HD4-6409/883	-55°C to +125°C	CLCC	J20.A

Description

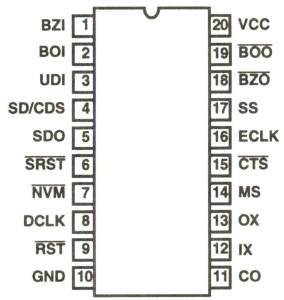
The HD-6409/883 Manchester Encoder-Decoder (MED) is a high speed, low power device manufactured using self-aligned silicon gate technology. The device is intended for use in serial data communication, and can be operated in either of two modes. In the converter mode, the MED converts Nonreturn-to-Zero code (NRZ) into Manchester code and decodes Manchester code into Nonreturn-to-Zero code. For serial data communication, Manchester code does not have some of the deficiencies inherent in Nonreturn-to-Zero code. For instance, use of the MED on a serial line eliminates DC components, provides clock recovery, and gives a relatively high degree of noise immunity. Because the MED converts the most commonly used code (NRZ) to Manchester code, the advantages of using Manchester code are easily realized in a serial data link.

In the Repeater mode, the MED accepts Manchester code input and reconstructs it with a recovered clock. This minimizes the effects of noise on a serial data link. A digital phase lock loop generates the recovered clock. A maximum data rate of 1MHz requires only 50mW of power.

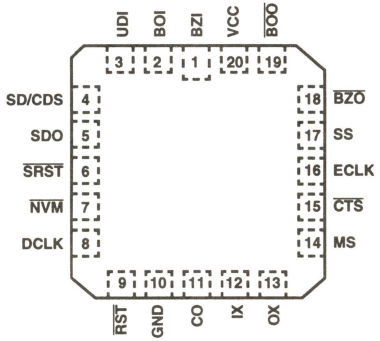
Manchester code is used in magnetic tape recording and in fiber optic communication, and generally is used where data accuracy is imperative. Because it frames blocks of data, the HD-6409/883 easily interfaces to protocol controllers.

Pinouts

HD1-6409/883 (CERDIP)
TOP VIEW



HD4-6409/883 (CLCC)
TOP VIEW



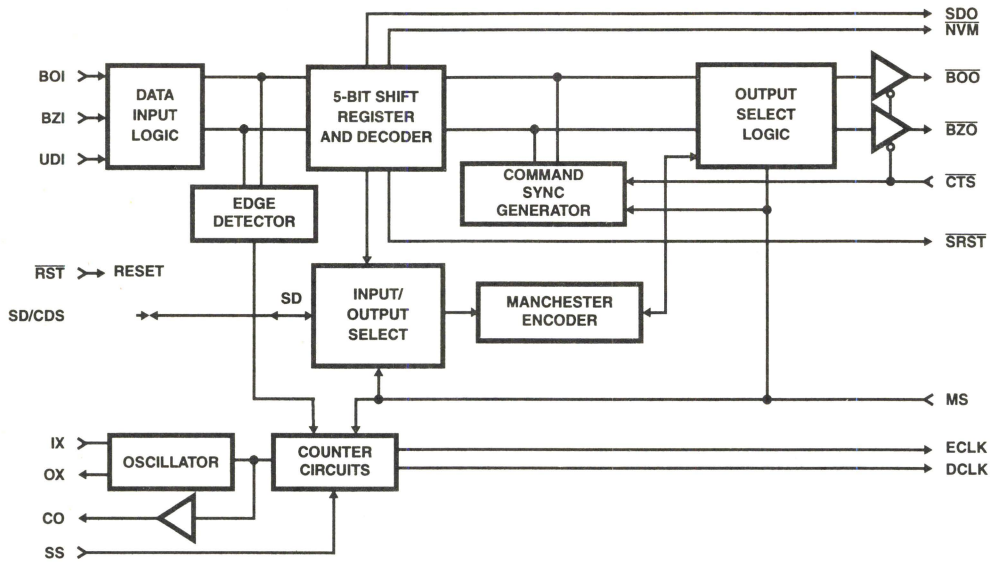
5 CMOS DATA COMMUNICATIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

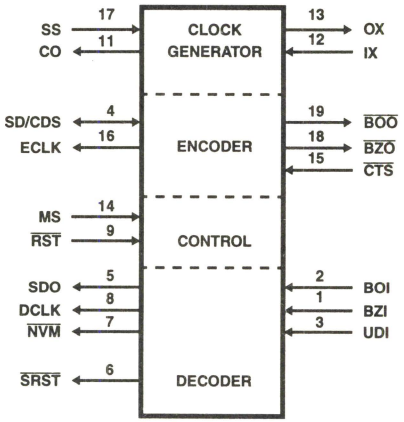
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File Number **2959.1**

Block Diagram



Logic Symbol



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage Applied. . . . . GND -0.5V to VCC +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Voltage Range . . . . . +4.5V to +5.5V
Input Rise and Fall Times . . . . . 50ns Max
Sync. Transition Span (t2) . . . . . 1.5 DBP Typical, (Notes 1, 2)
Short Data Transition Span (t4) . . . . . 0.5 DBP Typical, (Notes 1, 2)
Long Data Transition Span (t5) . . . . . 1.0 DBP Typical, (Notes 1, 2)
Zero Crossing Tolerance (tCD5) . . . . . (Note 3)

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	83	23
CLCC Package	95	26

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 250 Gates

NOTES:

1. DBP - Data Bit Period. Clock Rate = 16X, one DBP = 16 Clock Cycles; Clock Rate = 32X; one DBP = 32 Clock Cycles.
2. The input conditions specified are nominal values, the actual input waveforms transition spans may vary by ±2 IX clock cycles (16X mode) or ±6 IX clock cycles (32X mode).
3. The maximum zero crossing tolerance is ±2 IX clock cycles (16X mode) or ±6 IX clock cycles (32X mode) from the nominal.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

TABLE 1. HD-6409/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logic "1" Input Voltage	VIH	VCC = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	70% VCC	-	V
Logic "0" Input voltage	VIL	VCC = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	20% VCC	V
Logic "1" Input Voltage ($\overline{RST}$)	VIHR	VCC = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	VCC -0.5	-	V
Logic "0" Input Voltage ($\overline{RST}$)	VILR	VCC = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	GND +0.5	V
Logic "1" Input Voltage (IX)	VIHC	VCC = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	VCC -0.5	-	V
Logic "0" Input Voltage (IX)	VILC	VCC = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	GND +0.5	V
Input Leakage Current (Except IX)	II	VIN = VCC or GND VCC = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	+1.0	µA
Input Leakage Current (IX)	II	VIN = VCC or GND VCC = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-20	+20	µA
I/O Leakage Current	IO	VOUT = VCC or GND VCC = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	+10	µA
Output HIGH Voltage (All except OX)	VOH	IOH = -2.0mA VCC = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	VCC -0.4	-	V
Output LOW Voltage (All except OX)	VOL	IOL = +2.0mA VCC = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V

TABLE 1. HD-6409/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Standby Power Supply Current	ICCSB	VIN = VCC or GND, VCC = 5.5V, Outputs Open	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	100	µA
Operating Power Supply Current	ICCOP	f = 16.0MHz, VIN = VCC or GND VCC = 5.5V, CL = 50pF	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	18.0	mA
Functional Test	FT	(Note 2)	7, 8	$-55^oC \le T_A \le +125^oC$	-	-	-

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Tested as follows: f = 16MHz, VIH = 70% VCC, VIL = 20% VCC, VOH ≥ VCC/2, and VOL ≤ VCC/2, VCC = 4.5V and 5.5V.

TABLE 2. HD-6409/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Clock Frequency	fC		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	16	MHz
Clock Period	tC		9, 10, 11	$-55^oC \le T_A \le +125^oC$	1/fC	-	sec
Bipolar Pulse Width	t1		9, 10, 11	$-55^oC \le T_A \le +125^oC$	tC +10	-	ns
One-Zero Overlap	t3		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	tC - 10	ns
Clock High Time	tCH	f =16.0MHz	9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	ns
Clock Low Time	tCL	f =16.0MHz	9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	ns
Serial Data Setup Time	tCE1		9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	ns
Serial Data Hold Time	tCE2		9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	ns
DCLK to SDO, $\overline{NVM}$	tCD2		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	40	ns
ECLK to $\overline{BZO}$	tR2		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	40	ns

NOTES:

1. AC Testing as follows: f = 4.0MHz, VIH = 70% VCC, VIL = 20% VCC, Speed Select = 16X; VOH ≥ VCC/2, VOL ≤ VCC/2; VCC = 4.5V and 5.5V; Input rise and fall times driven at 1 ns/V, Output load = 50pF.

TABLE 3. HD-6409/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CIN	VCC = Open, f =1MHz All Measurements are referenced to device GND	1, 2	$T_A = +25^oC$	-	10	pF
I/O Capacitance	CI/O		1, 2	$T_A = +25^oC$	-	12	pF
Output Rise Time (All except CO)	tr	From 1.0 to 3.5V CL = 50pF	1, 2	$-55^oC \le T_A \le +125^oC$	-	50	ns

TABLE 3. HD-6409/883 ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Fall Time (All except CO)	tf	From 3.5 to 1.0V CL = 50pF	1, 2	$-55^oC \le T_A \le +125^oC$	-	50	ns
CO Rise Time	tr	From 1.0 to 3.5V CL = 20pF	1, 2	$-55^oC \le T_A \le +125^oC$	-	11	ns
CO Fall Time	tf	From 3.5 to 1.0V CL = 20pF	1, 2	$-55^oC \le T_A \le +125^oC$	-	11	ns
ECLK to $\overline{BZO}$, $\overline{BOO}$	tCE3		1, 3	$-55^oC \le T_A \le +125^oC$	0.5	1.0	DBP
$\overline{CTS}$ Low to $\overline{BZO}$ $\overline{BOO}$ Enabled	tCE4		1, 3	$-55^oC \le T_A \le +125^oC$	0.5	1.5	DBP
$\overline{CTS}$ Low to ECLK Enabled	tCE5		1, 3	$-55^oC \le T_A \le +125^oC$	10.5	11.5	DBP
$\overline{CTS}$ High to ECLK Disabled	tCE6		1, 3	$-55^oC \le T_A \le +125^oC$	-	1.0	DBP
$\overline{CTS}$ High to $\overline{BZO}$ $\overline{BOO}$ Disabled	tCE7		1, 3	$-55^oC \le T_A \le +125^oC$	1.5	2.5	DBP
UDI to SDO, $\overline{NVM}$	tCD1		1, 3	$-55^oC \le T_A \le +125^oC$	2.5	3.0	DBP
$\overline{RST}$ Low to DCLK, SDO, $\overline{NVM}$ Low	tCD3		1.3	$-55^oC \le T_A \le +125^oC$	0.5	1.5	DBP
$\overline{RST}$ High to DCLK, Enabled	tCD4		1, 3	$-55^oC \le T_A \le +125^oC$	0.5	1.5	DBP
UDI to $\overline{BZO}$, $\overline{BOO}$	tR1		1, 3	$-55^oC \le T_A \le +125^oC$	0.5	1.0	DBP
UDI to SDO, $\overline{NVM}$	tR3		1, 3	$-55^oC \le T_A \le +125^oC$	2.5	3.0	DBP

NOTES:

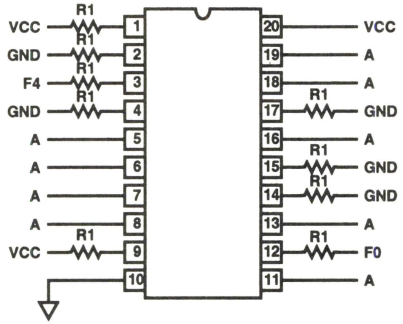
1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested.
2. Guaranteed via characterization at initial device design and after major process and/or design changes.
3. DBP-Data Bit Period, Clock Rate = 16X, one DBP = 16 Clock Cycles; Clock Rate = 32X, one DBP = 32 Clock Cycles.

TABLE 4. APPLICABLE SUBGROUPS

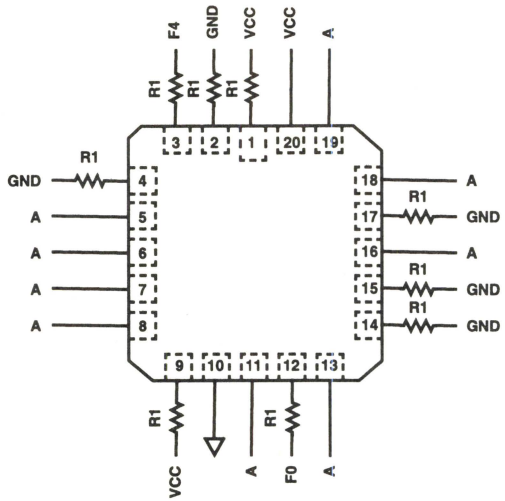
CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

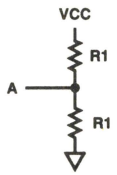
Burn-In Circuits

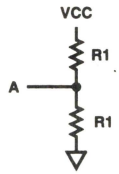
HD-6409/883 CERDIP



HD-6409/883 CLCC







NOTES:

1. VCC = 5.5V ±0.5V
2. VIH = 4.5V ±10%
3. VIL = -0.2V to 0.4V
4. R1 = 47kΩ ±5%
5. F0 = 100kHz ±10%
6. F4 = F0/16

Die Characteristics

DIE DIMENSIONS:
88 x 78 x 19 ±1mils

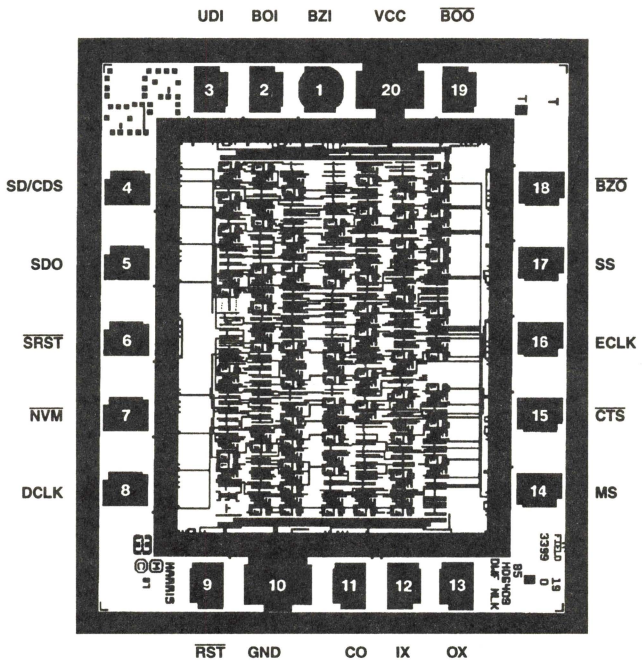
METALLIZATION:
Type: Silicon - Aluminum
Thickness: Metal 1: 8kÅ ±1kÅ
Metal 2: 16kÅ ±1kÅ

GLASSIVATION:
Type: Si3N4 • SiOX
Thickness: 10kÅ ±2kÅ

WORST CASE CURRENT DENSITY:
0.8×10^5 A/cm^2

Metallization Mask Layout

HD-6409/883



HARRIS SEMICONDUCTOR

HD-15530

March 1997

CMOS Manchester Encoder-Decoder

Features

- Support of MIL-STD-1553
- Data Rate . . . . . 1.25 MBit/s
- Sync Identification and Lock-In
- Clock Recovery
- Manchester II Encode, Decode
- Separate Encode and Decode
- Low Operating Power . . . . . 50mW at 5V

Ordering Information

PACKAGE	TEMP. RANGE	1.25 MEGABIT/s	PKG. NO.
CERDIP	-40°C to +85°C	HD1-15530-9	F24.6
	-55°C to +125°C	HD1-15530-8	
SMD#		7802901JA	
CLCC	-40°C to +85°C	HD4-15530-9	J28.A
	-55°C to +125°C	HD4-15530-8	
SMD#		78029013A	
PDIP	-40°C to +85°C	HD3-15530-9	E24.6

Description

The Harris HD-15530 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset functions.

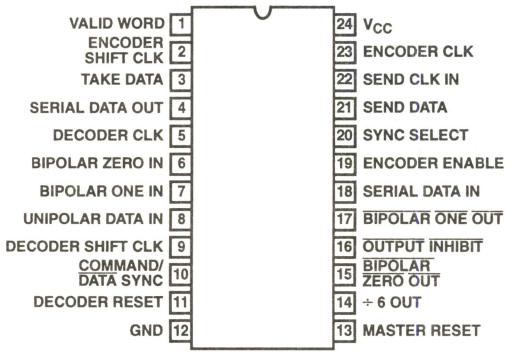
This circuit meets many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5V supply.

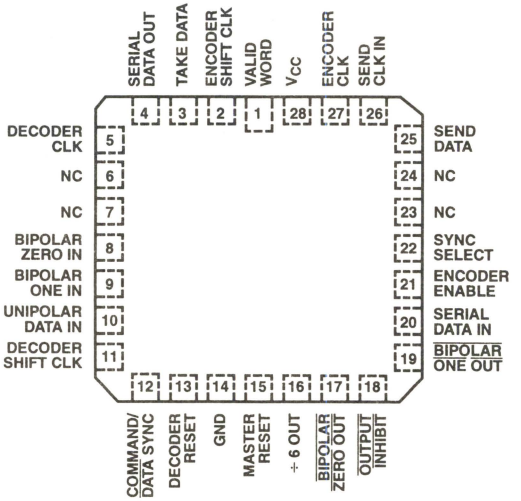
The HD-15530 can also be used in many party line digital data communications applications, such as an environmental control system driven from a single twisted pair cable of fiber optic cable throughout the building.

Pinouts

HD-15530 (CERDIP, PDIP)
TOP VIEW



HD-15530 (CLCC)
TOP VIEW

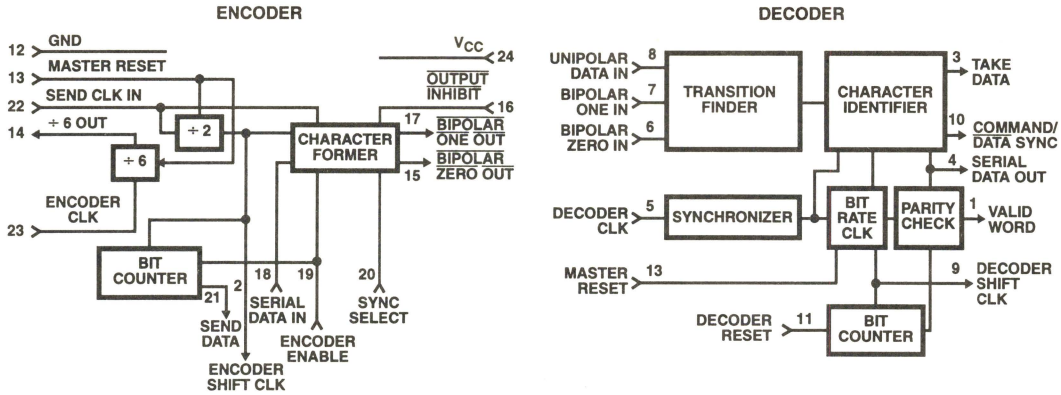


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2960.1**

Block Diagrams



Pin Description

PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
1	O	VALID WORD	Decoder	Output high indicates receipt of a valid word, (valid parity and no Manchester errors).
2	O	ENCODER SHIFT CLOCK	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI on the low-to-high transition of Encoder Shift Clock.
3	O	TAKE DATA	Decoder	Output is high during receipt of data after identification of a sync pulse and two valid Manchester data bits.
4	O	SERIAL DATA OUT	Decoder	Delivers received data in correct NRZ format.
5	I	DECODER CLOCK	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder, input a frequency equal to 12X the data rate.
6	I	BIPOLAR ZERO IN	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	I	BIPOLAR ONE IN	Decoder	A high input should be applied when the bus is in its positive state. This pin must be held low when the Unipolar input is used.
8	I	UNLPOLAR DATA IN	Decoder	With pin 6 high and pin 7 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
9	O	DECODER SHIFT CLOCK	Decoder	Output which delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
10	O	COMMAND SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character.
11	I	DECODER RESET	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	I	GROUND	Both	Ground Supply pin.
13	I	MASTER RESET	Both	A high on this pin clears 2:1 counters in both Encoder and Decoder, and resets the ÷ 6 circuit.
14	O	÷ 6 OUT	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK.
15	O	$\overline{\text{BIPOLAR ZERO OUT}}$	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver.
16	I	$\overline{\text{OUTPUT INHIBIT}}$	Encoder	A low on this pin forces pin 15 and 17 high, the inactive states.
17	O	$\overline{\text{BIPOLAR ONE OUT}}$	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver.

Pin Description (Continued)

PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
18	I	SERIAL DATA IN	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	I	ENCODER ENABLE	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete.)
20	I	SYNC SELECT	Encoder	Actuates a Command sync for an input high and Data sync for an input low.
21	O	SEND DATA	Encoder	An active high output which enables the external source of serial data.
22	I	SEND CLOCK IN	Encoder	Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.
23	I	ENCODER CLOCK	Encoder	Input to the 6:1 divider, a frequency equal to the data rate X12 is usually input here.
24	I	V_{CC}	Both	V_{CC} is the +5V power supply pin. A 0.1µF decoupling capacitor from V_{CC} (pin 24) to GROUND (pin 12) is recommended.

I = Input O = Output

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a command sync or a low will produce a data sync for the word ②. When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods ③. During these sixteen periods the data should be clocked into the SERIAL DATA input with every high-to-low transition of the ENCODER SHIFT CLOCK so it can be sampled on the low-to-high transition ③ - ④. After the sync and Manchester II coded data are transmitted through the BIPOLAR ONE and BIPOLAR ZERO outputs, the Encoder adds on an additional bit which is the parity for that word ⑤. If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time ⑤ as shown to prevent a consecutive word from being encoded. At any time a low on OUTPUT INHIBIT input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.

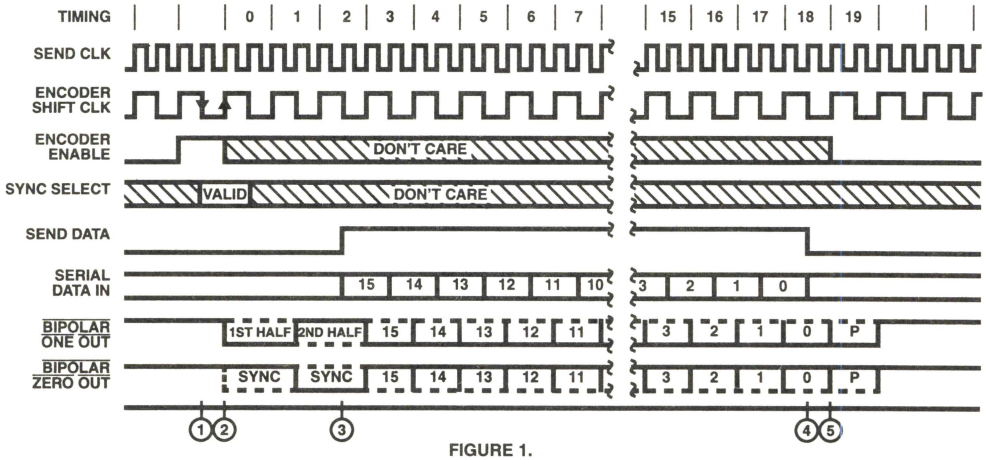


FIGURE 1.

Decoder Operation

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from $\overline{\text{BIPOLAR ONE OUT}}$ of an Encoder through an inverter to Unipolar Data Input).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high ② and remain high for sixteen DECODER SHIFT CLOCK periods ③, otherwise it will remain low. The TAKE DATA output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock ② - ③. Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately 20 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown ①.

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

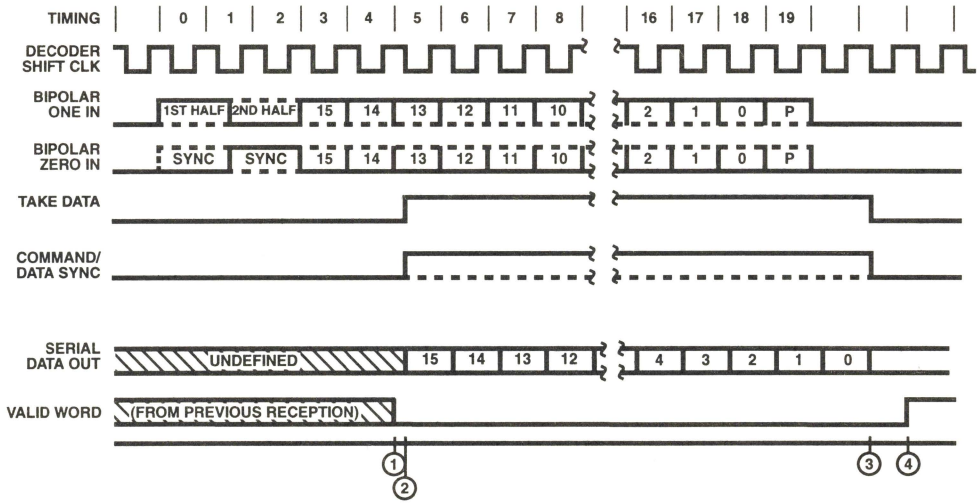


FIGURE 2.

How to Make Our MTU Look Like a Manchester Encoded UART

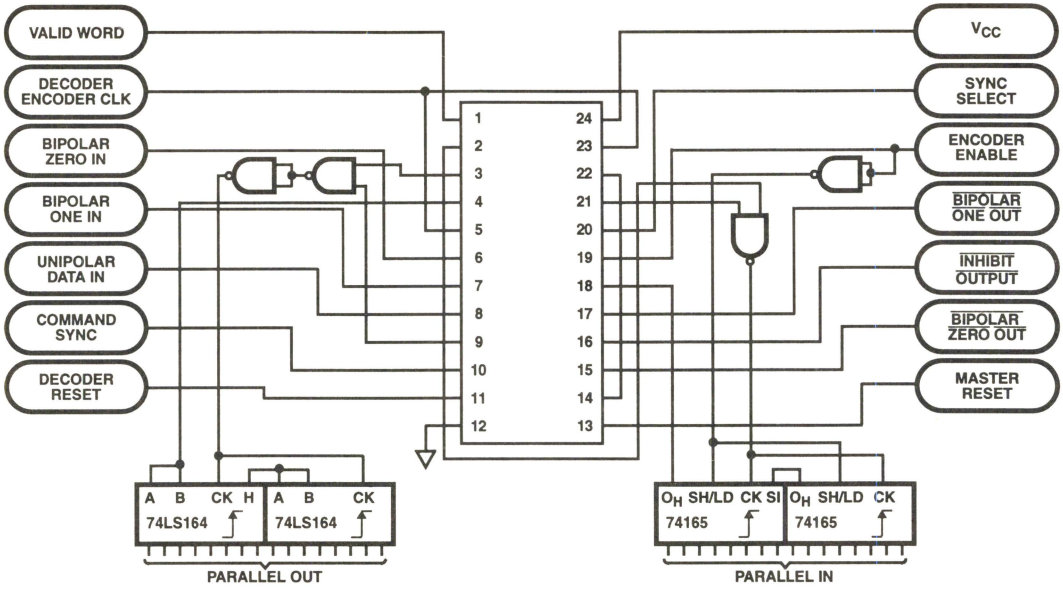


FIGURE 3.

Typical Timing Diagrams for a Manchester Encoded UART

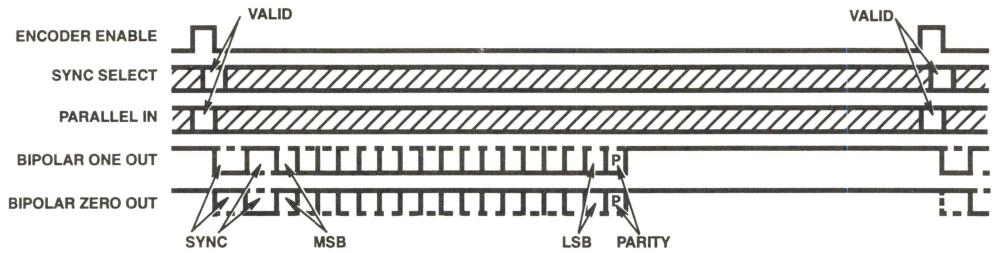


FIGURE 4. ENCODER TIMING

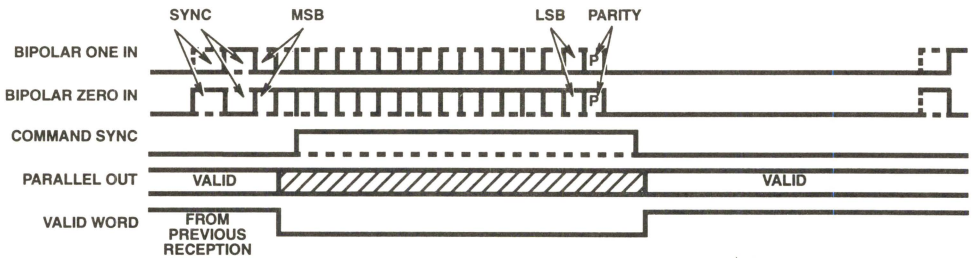


FIGURE 5. DECODER TIMING

MIL-STD- 1553

The 1553 standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HD-15530 supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words. Terminals respond with Status Words. Each word is preceded by a synchronizing pulse, and followed by parity bit, occupying a total of 20µs. The word formats are shown in Figure 4. The special abbreviations are as follows:

P Parity, which is defined to be odd, taken across all 17 bits.

R/T Receive on logical zero, transmit on ONE.

ME Message Error if logical 1.

TF Terminal Flat, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553, and do not completely describe its bus requirements, timing or protocols.

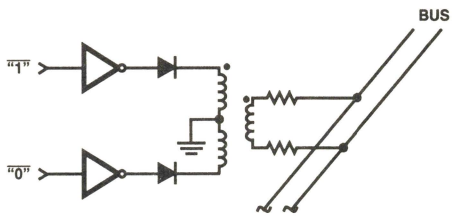


FIGURE 6. SIMPLIFIED MIL-STD-1553 DRIVER

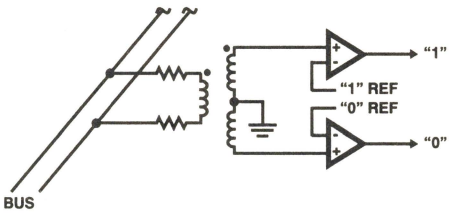


FIGURE 7. SIMPLIFIED MIL-STD-1553 RECEIVER

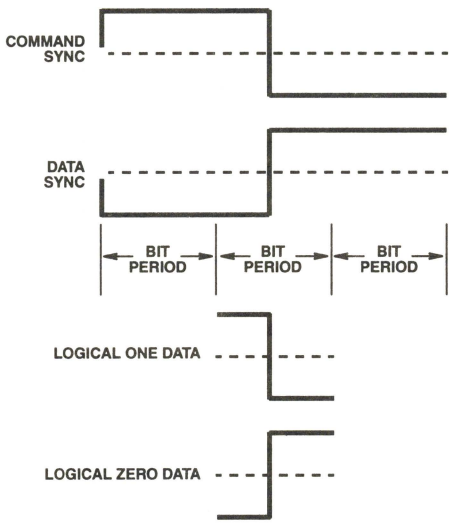


FIGURE 8. MIL-STD-1553 CHARACTER FORMATS

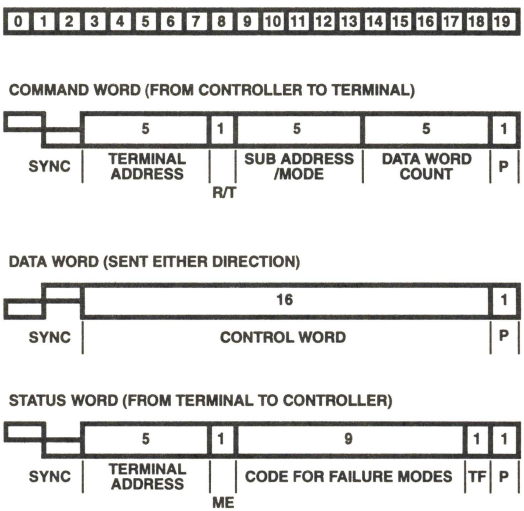


FIGURE 9. MIL-STD-1553 WORD FORMATS

NOTE: This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HD-15530.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND-0.3V to V_{CC} +0.3V
ESD Classification . . . . . Class 1

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Temperature Range (T_A)
HD-15530-9 . . . . . -40°C to +85°C
HD-15530-8 . . . . . -55°C to +125°C
Encoder/Decoder Clock Rise Time . . . . . 8ns Max
Encoder/Decoder Clock Fall Time . . . . . 8ns Max
Sync Transition Span (TD2) . . . . . 18 TDC Typ (Note 1)
Short Data Transition Span (TD4) . . . . . 6 TDC Typ (Note 1)
Long Data Transition Span (TD5) . . . . . 12 TDC Typ (Note 1)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	55	12
CLCC Package	65	14
Plastic DIP Package	60	N/A

Maximum Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 456 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5V ±10%, T_A = -40°C to +85°C (HD-15530-9)
T_A = -55°C to +125°C (HD-15530-8)

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	TEST CONDITIONS	UNITS
Input LOW Voltage	V_{IL}	-	0.2 V_{CC}	V_{CC} = 4.5V and 5.5V	V
Input HIGH Voltage	V_{IH}	0.7 V_{CC}	-	V_{CC} = 4.5V and 5.5V	V
Input LOW Clock Voltage	V_{ILC}	-	GND +0.5	V_{CC} = 4.5V and 5.5V	V
Input HIGH Clock Voltage	V_{IHC}	V_{CC} -0.5	-	V_{CC} = 4.5V and 5.5V	V
Output LOW Voltage	V_{OL}	-	0.4	I_{OL} = 1.8mA (Note 2), V_{CC} = 4.5V	V
Output HIGH Voltage	V_{OH}	2.4	-	I_{OH} = -3mA (Note 2), V_{CC} = 4.5V	V
Input Leakage Current	I_I	-1.0	+1.0	V_I = GND or V_{CC}, V_{CC} = 5.5V	µA
Standby Supply Current	I_{CCSB}	-	2	V_{IN} = V_{CC} = 5.5V Output Open	mA
Operating Power Supply Current	I_{CCOP}	-	10	V_{CC} = 5.5V, V_{IN} = V_{CC}, f =15MHz, Outputs Open	mA
Function Test	F_T	-	-	(Note 3)	-

NOTES:

1. TDC = Decoder clock period = 1/FDC
2. Interchanging of force and sense conditions is permitted.
3. Tested as follows: = f = 15MHz, V_{IH} = 70% V_{CC}, V_{IL} = 20% V_{CC}, C_L = 50pF, $V_{OH} \geq$ 1.5V and $V_{OL} \leq$ 1.5V.

Capacitance

T_A = +25°C; Frequency = 1MHz

SYMBOL	PARAMETER	TYPICAL	UNITS	CONDITIONS
C_{IN}	Input Capacitance	15	pF	All measurements are referenced to device GND
C_O	Output Capacitance	15	pF	

AC Electrical Specifications V_{CC} = 5V ±10%, T_A = -40°C to +85°C (HD-15530-9)
T_A = -55°C to +125°C (HD-15530-8)

PARAMETER	SYMBOL	(NOTE 2) TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
ENCODER TIMING					
Encoder Clock Frequency	FEC	V_{CC} = 4.5V and 5.5V, C_L = 50pF	-	15	MHz
Send Clock Frequency	FESC	V_{CC} = 4.5V and 5.5V, C_L = 50pF	-	2.5	MHz
Encoder Data Rate	FED	V_{CC} = 4.5V and 5.5V, C_L = 50pF	-	1.25	MHz
Master Reset Pulse Width	TMR	V_{CC} = 4.5V and 5.5V, C_L = 50pF	150	-	ns
Shift Clock Delay	TE1	V_{CC} = 4.5V and 5.5V, C_L = 50pF	-	125	ns
Serial Data Setup	TE2	V_{CC} = 4.5V and 5.5V, C_L = 50pF	75	-	ns
Serial Data Hold	TE3	V_{CC} = 4.5V and 5.5V, C_L = 50pF	75	-	ns
Enable Setup	TE4	V_{CC} = 4.5V and 5.5V, C_L = 50pF	90	-	ns
Enable Pulse Width	TE5	V_{CC} = 4.5V and 5.5V, C_L = 50pF	100	-	ns
Sync Setup	TE6	V_{CC} = 4.5V and 5.5V, C_L = 50pF	55	-	ns
Sync Pulse Width	TE7	V_{CC} = 4.5V and 5.5V, C_L = 50pF	150	-	ns
Send Data Delay	TE8	V_{CC} = 4.5V and 5.5V, C_L = 50pF	0	50	ns
Bipolar Output Delay	TE9	V_{CC} = 4.5V and 5.5V, C_L = 50pF	-	130	ns
Enable Hold	TE10	V_{CC} = 4.5V and 5.5V, C_L = 50pF	10	-	ns
Sync Hold	TE11	V_{CC} = 4.5V and 5.5V, C_L = 50pF	95	-	ns
DECODER TIMING					
Decoder Clock Frequency	FDC	V_{CC} = 4.5V and 5.5V, C_L = 50pF	-	15	MHz
Decoder Data Rate	FDD	V_{CC} = 4.5V and 5.5V, C_L = 50pF	-	1.25	MHz
Decoder Reset Pulse Width	TDR	V_{CC} = 4.5V and 5.5V, C_L = 50pF	150	-	ns
Decoder Reset Setup Time	TDRS	V_{CC} = 4.5V and 5.5V, C_L = 50pF	75	-	ns
Decoder Reset Hold Time	TDRH	V_{CC} = 4.5V and 5.5V, C_L = 50pF	10	-	ns
Master Reset Pulse	TMR	V_{CC} = 4.5V and 5.5V, C_L = 50pF	150	-	ns
Bipolar Data Pulse Width	TD1	V_{CC} = 4.5V and 5.5V, C_L = 50pF	TDC + 10 (Note 1)	-	ns
One Zero Overlap	TD3	V_{CC} = 4.5V and 5.5V, C_L = 50pF	-	TDC - 10 (Note 1)	ns
Sync Delay (ON)	TD6	V_{CC} = 4.5V and 5.5V, C_L = 50pF	-20	110	ns
Take Data Delay (ON)	TD7	V_{CC} = 4.5V and 5.5V, C_L = 50pF	0	110	ns
Serial Data Out Delay	TD8	V_{CC} = 4.5V and 5.5V, C_L = 50pF	-	80	ns
Sync Delay (OFF)	TD9	V_{CC} = 4.5V and 5.5V, C_L = 50pF	0	110	ns
Take Data Delay (OFF)	TD10	V_{CC} = 4.5V and 5.5V, C_L = 50pF	0	110	ns
Valid Word Delay	TD11	V_{CC} = 4.5V and 5.5V, C_L = 50pF	0	110	ns

NOTES:

1. TDC = Decoder clock period = 1/FDC
2. AC Testing as follows: Input levels: V_{IH} = 70% V_{CC}, V_{IL} = 20% V_{CC}; Input rise/fall times driven at 1ns/V; Timing Reference levels: 1.5V; Output load: C_L = 50pF.

Timing Waveforms

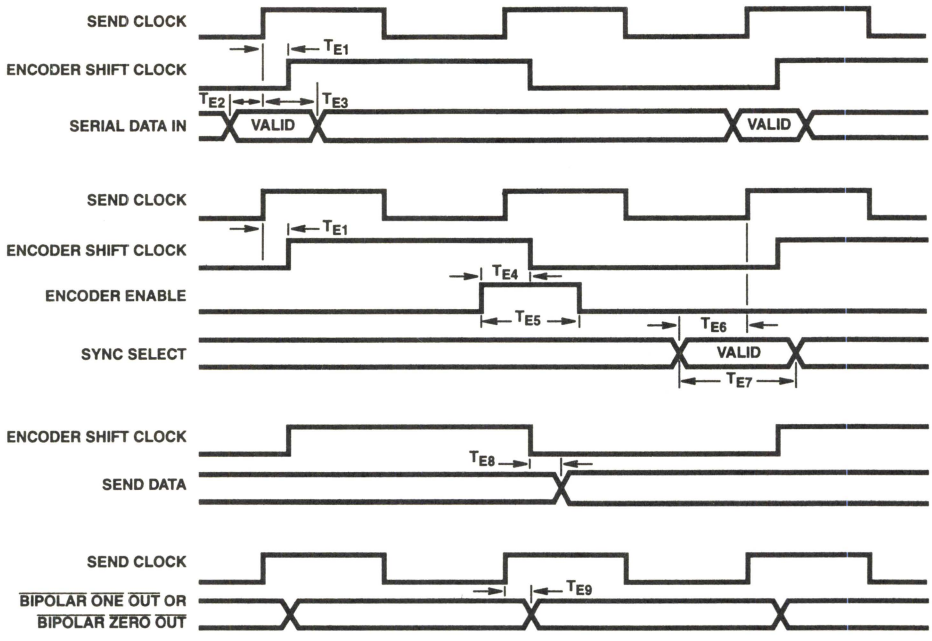


FIGURE 10. ENCODER TIMING

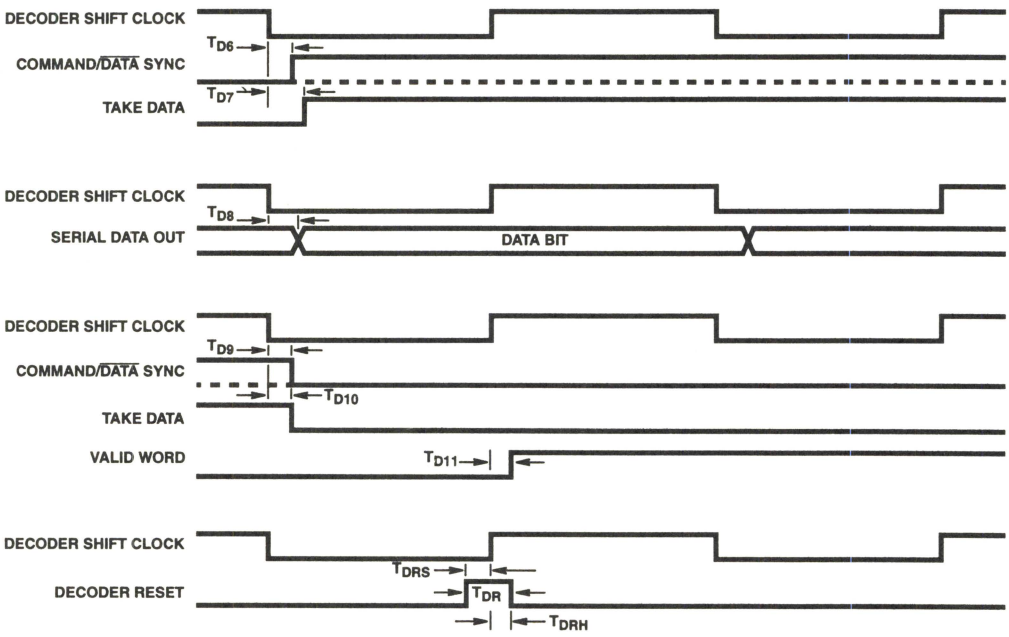


FIGURE 11. DECODER TIMING

Timing Waveforms (Continued)

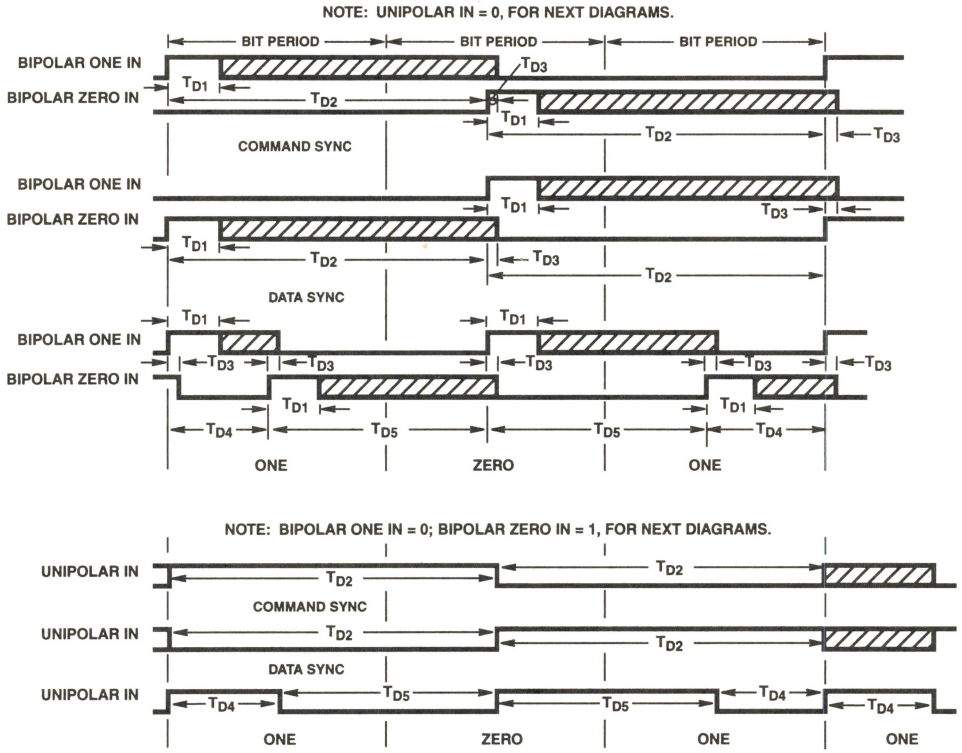
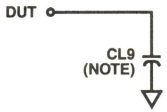


FIGURE 12. DECODER TIMING

Test Load Circuit



NOTE: Includes stray and jig capacitance.

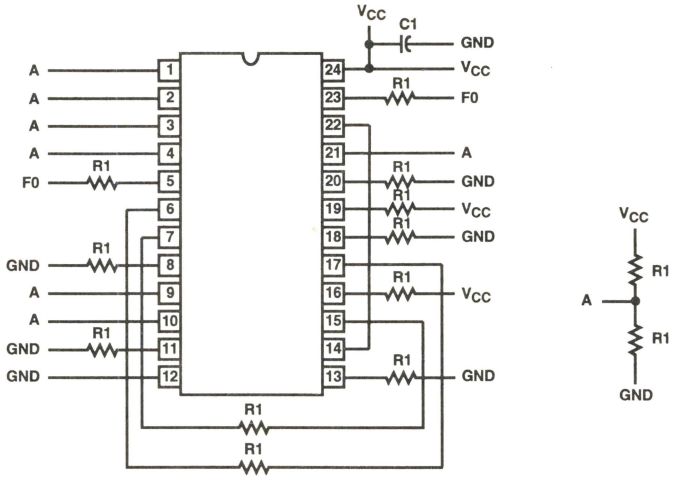
AC Testing Input, Output Waveform



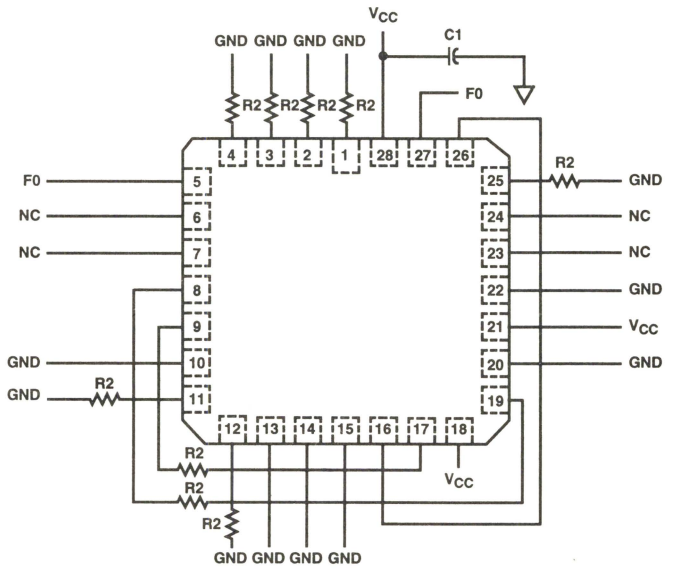
AC Testing: All input signals must switch between V_{IL} and V_{IH}. Input rise and fall times are driven at 1ns per volt.

Burn-In Circuits

HD1-15530 CERDIP



HD4-15530 CLCC



NOTES:

1. V_{CC} = 5.5V ± 0.5V
2. V_{IH} = 4.5V ± 10%
3. V_{IL} = -0.2V +0.4V
4. R1 = 47KΩ ± 5%
5. R2 = 1.8KΩ ± 5%
6. F0 = 100KHz ± 10%
7. C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
155 x 195 x 19mils

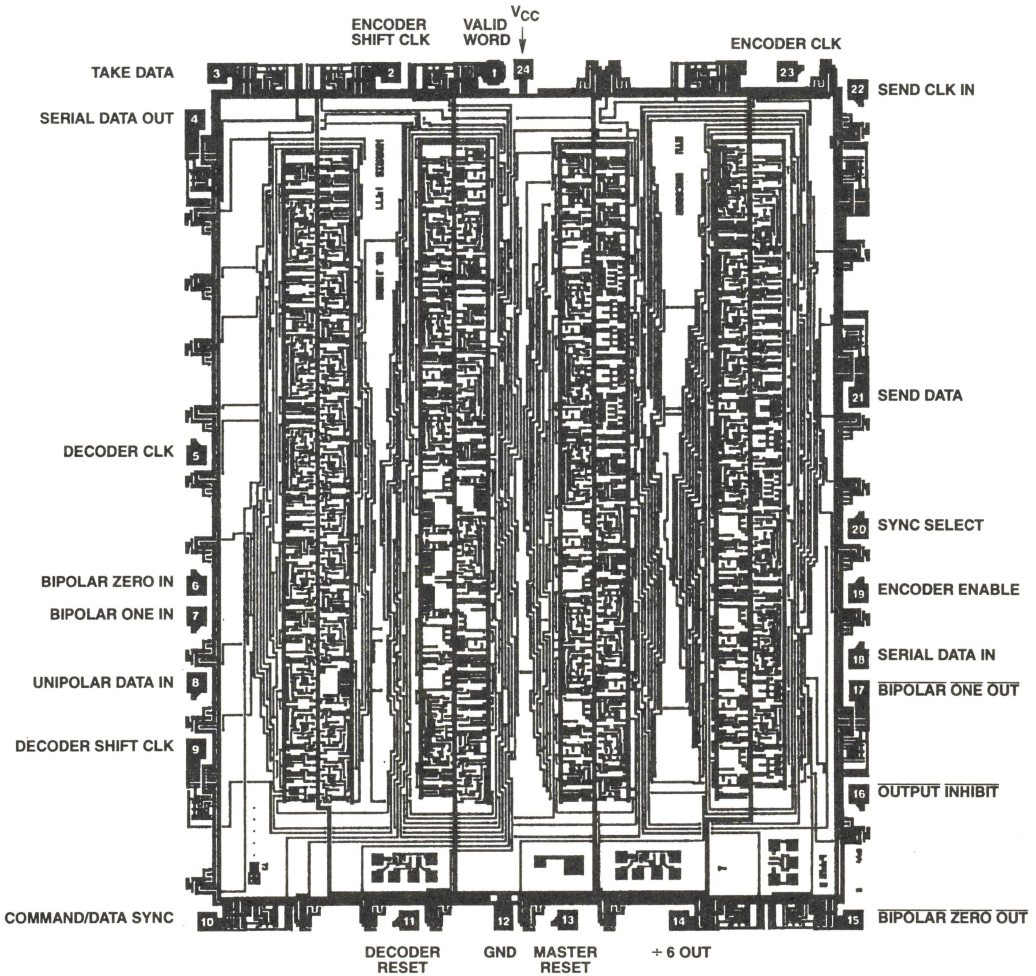
METALLIZATION:
Type: Si-Al
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kA ±1kÅ

WORST CASE CURRENT DENSITY:
1.8×10^5 A/cm^2

Metallization Mask Layout

HD-15530



HARRIS SEMICONDUCTOR

HD-15531

March 1997

CMOS Manchester Encoder-Decoder

Features

- Support of MIL-STD-1553
- Data Rate (15531B) ..... 2.5 Megabit/Sec
- Data Rate (15531)..... 1.25 Megabit/Sec
- Variable Frame Length to 32 Bits
- Sync Identification and Lock-In
- Separate Manchester II Encode, Decode
- Low Operating Power .....50mW at 5V

Ordering Information

PACKAGE	TEMP. RANGE	1.25MBIT /SEC	2.5MBIT /SEC	PKG. NO.
PDIP	-40°C to +85°C	-	HD3-15531B-9	E40.6
CERDIP	-40°C to +85°C	HD1-15531-9	HD1-15531B-9	F40.6
	-55°C to +125°C	HD1-15531-8	HD1-15531B-8	F40.6
DESC (CERDIP)	-55°C to +125°C	5962-9054901MQA	HD1-15531	F40.6
	-55°C to +125°C	5962-9054902MQA	HD1-15531B	F40.6

Description

The Harris HD-15531 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate independently of each other, except for the master reset and word length functions. This circuit provides many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

The HD-15531 also surpasses the requirements of MIL-STD-1553 by allowing the word length to be programmable (from 2 to 28 data bits). A frame consists of three bits for sync followed by the data word (2 to 28 data bits) followed by one bit of parity, thus, the frame length will vary from 6 to 32 bit periods. This chip also allows selection of either even or odd parity for the Encoder and Decoder separately.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. For high speed applications the 15531B will support a 2.5 Megabit/sec data rate.

The HD-15531 can also be used in many party line digital data communications applications, such as a local area network or an environmental control system driven from a single twisted pair of fiber optic cable throughout a building.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

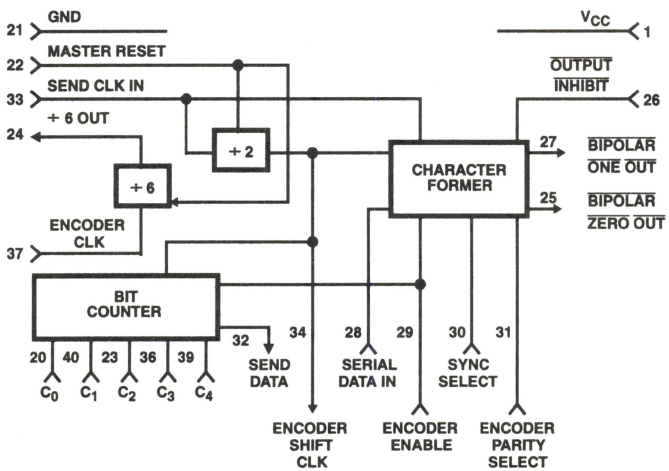
Pinout

HD-15531 (CERDIP, PDIP)
TOP VIEW

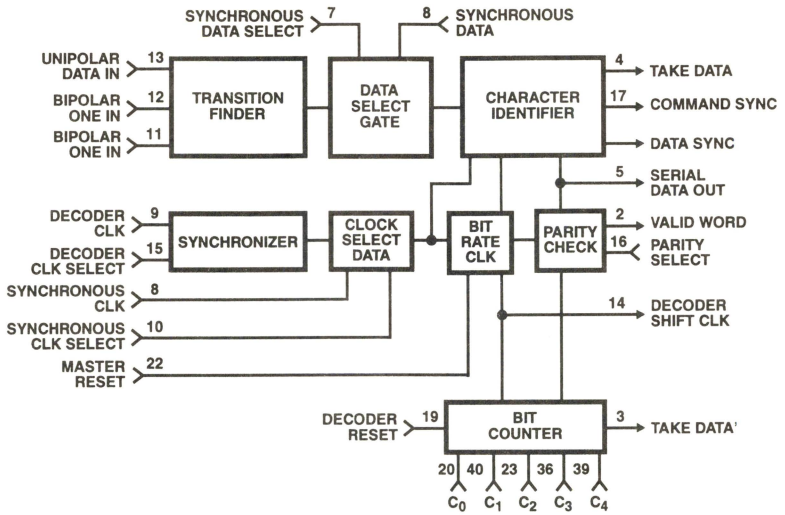


Block Diagrams

ENDODER



DECODER



Pin Description

PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
1		V_{CC}	Both	Positive supply pin. A 0.1µF decoupling capacitor from V_{CC} (pin 1) to GROUND (pin 21) is recommended.
2	O	VALID WORD	Decoder	Output high indicates receipt of a valid word, (valid parity and no Manchester errors).
3	O	TAKE DATA'	Decoder	A continuous, free running signal provided for host timing or data handling. When data is present on the bus, this signal will be synchronized to the incoming data and will be identical to TAKE DATA.
4	O	TAKE DATA	Decoder	Output is high during receipt of data after identification of a valid sync pulse and two valid Manchester bits.
5	O	SERIAL DATA OUT	Decoder	Delivers received data in correct NRZ format.
6	I	SYNCHRONOUS DATA	Decoder	Input presents Manchester data directly to character identification logic. SYNCHRONOUS DATA SELECT must be held high to use this input. If not used, this pin must be held high.
7	I	SYNCHRONOUS DATA SELECT	Decoder	In high state allows the synchronous data to enter the character identification logic. Tie this input low for asynchronous data.
8	I	SYNCHRONOUS CLOCK	Decoder	Input provides externally synchronized clock to the decoder, for use when receiving synchronous data. This input must be tied high when not in use.
9	I	DECODER CLOCK	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder. Input a frequency equal to 12X the data rate.
10	I	SYNCHRONOUS CLOCK SELCT	Decoder	In high state directs the SYNCHRONOUS CLOCK to control the decoder character identification logic. A low state selects the DECODER CLOCK.
11	I	BIPOLAR ZERO IN	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the unipolar input is used.
12	I	BIPOLAR ONE IN	Decoder	A high input should be applied when the bus is in its positive state. This pin must he held low when the unipolar input is used.
13	I	UNIPOLAR DATA IN	Decoder	With pin 11 high and pin 12 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.

Pin Description (Continued)

PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
14	O	DECODER SHIFT CLOCK	Decoder	Output which delivers a frequency (DECODER CLOCK + 1 2), synchronous by the recovered serial data stream.
15	I	TRANSITION SELECT	Decoder	A high input to this pin causes the transition finder to synchronize on every transition of input data. A low input causes the transition finder to synchronize only on mid-bit transitions.
16		NC	Blank	Not connected.
17	O	COMMAND SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character.
18	I	DECODER PARITY SELECT	Decoder	An input for parity sense, calling for even parity with input high and odd parity with input low.
19	I	DECODER RESET	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
20	I	COUNT C0	Both	One of five binary inputs which establish the total bit count to be encoded or decoded.
21		GROUND	Both	Supply pin.
22	I	MASTER RESET	Both	A high on this pin clears 2:1 counters in both encoder and decoder, and resets the ÷ 6 circuit.
23	I	COUNT C2	Both	See pin 20.
24	O	÷ 6 OUT	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK.
25	O	$\overline{\text{BIPOLAR ZERO OUT}}$	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver.
26	I	$\overline{\text{OUTPUT INHIBIT}}$	Encoder	A low on this pin forces pin 25 and 27 high, the inactive states.
27	O	$\overline{\text{BIPOLAR ONE OUT}}$	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver.
28	I	SERIAL DATA IN	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
29	I	ENCODER ENABLE	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceding cycle being complete).
30	I	SYNC SELECT	Encoder	Actuates a Command sync for an input high and Data sync for an input low.
31	I	ENCODER PARITY SELECT	Encoder	Sets transmit parity odd for a high input, even for a low input.
32	O	SEND DATA	Encoder	Is an active high output which enables the external source of serial data.
33	I	SEND CLOCK IN	Encoder	Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.
34	O	ENCODER SHIFT CLOCK	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI pin-28 on the low-to-high transition of ESC.
35		NC	Blank	Not connected.
36	I	COUNT C3	Both	See pin 20.
37	I	ENCODER CLOCK	Encoder	Input to the 6:1 divider, a frequency equal to 12 times the data rate is usually input here.
38	O	DATA SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a data synchronizing character.
39	I	COUNT C4	Both	See pin 20.
40	I	COUNT C1	Both	See pill 20.

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK. The frame length is set by programming the COUNT inputs. Parity is selected by programming ENCODER PARITY SELECT high for odd parity or low for even parity.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or K + 4 ENCODER SHIFT CLOCK periods, where K is the number of bits to be sent. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a Command sync or a low will produce a Data sync for the word ②. When the Encoder is ready to accept data, the SEND DATA output will go high for K ENCODER SHIFT CLOCK periods ④. During these K periods the data should be clocked into the SERIAL DATA input with every high-to-low transition of the ENCODER SHIFT CLOCK ③ - ④ so it can be sampled on the low-to-high transition. After the sync and Manchester II encoded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit with the parity for that word ⑤. If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time ⑤ (as shown) to prevent a consecutive word from being encoded. At any time a low on $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission, a positive pulse must be applied at MASTER RESET. Any time after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.

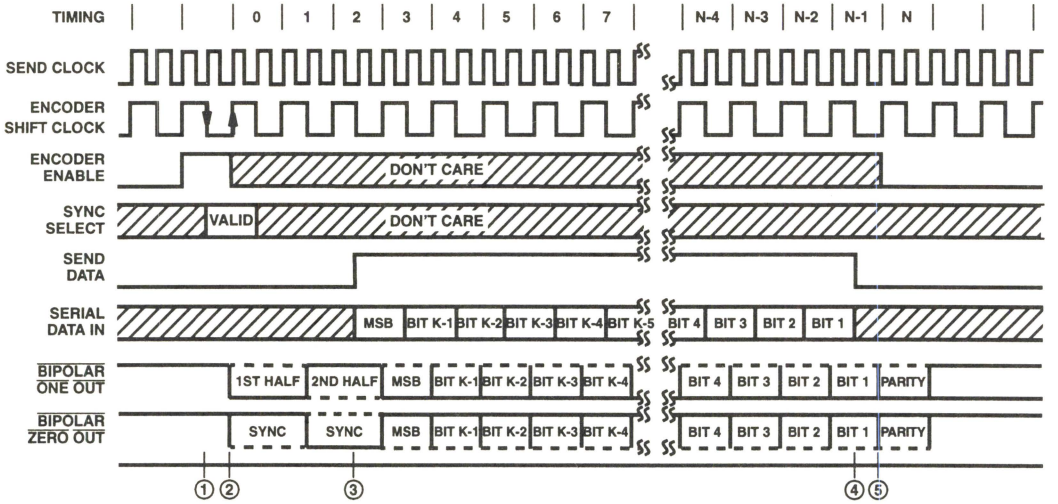


FIGURE 1. ENCODER

Decoder Operation

To operate the Decoder asynchronously requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. To operate the Decoder synchronously requires a SYNCHRONOUS CLOCK at a frequency 2 times the data rate which is synchronized with the data at every high-to-low transition applied to the SYNCHRONOUS CLK input. The Manchester II coded data can be presented to the Decoder asynchronously in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept noninverted Manchester II coded data. (e.g., from $\overline{\text{BIPOLAR ONE}}$ $\overline{\text{OUT}}$ on an Encoder through an inverter to Unipolar Data Input).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated by a high level at either COMMAND SYNC or DATA SYNC output. If the sync character was a command sync the COMMAND SYNC output will go high ② and remain high for K SHIFT CLOCK periods ③, where K is the number of bits to be received. If the sync character was a data sync, the DATA SYNC output will go high. The TAKE DATA output will go high and remain high ② - ③ while the Decoder is transmit-

ting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock (2) - (3). Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all K decoded bits have been transmitted (3) the data is checked for parity. A high input on DECODER PARITY SELECT will set the Decoder to check for even parity or a low input will set the Decoder to check for odd parity. A high on VALID WORD output (4) indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately K + 4 DECODER SHIFT CLOCK periods after it goes high, if not reset low sooner by a valid sync and two valid Manchester bits as shown (1).

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

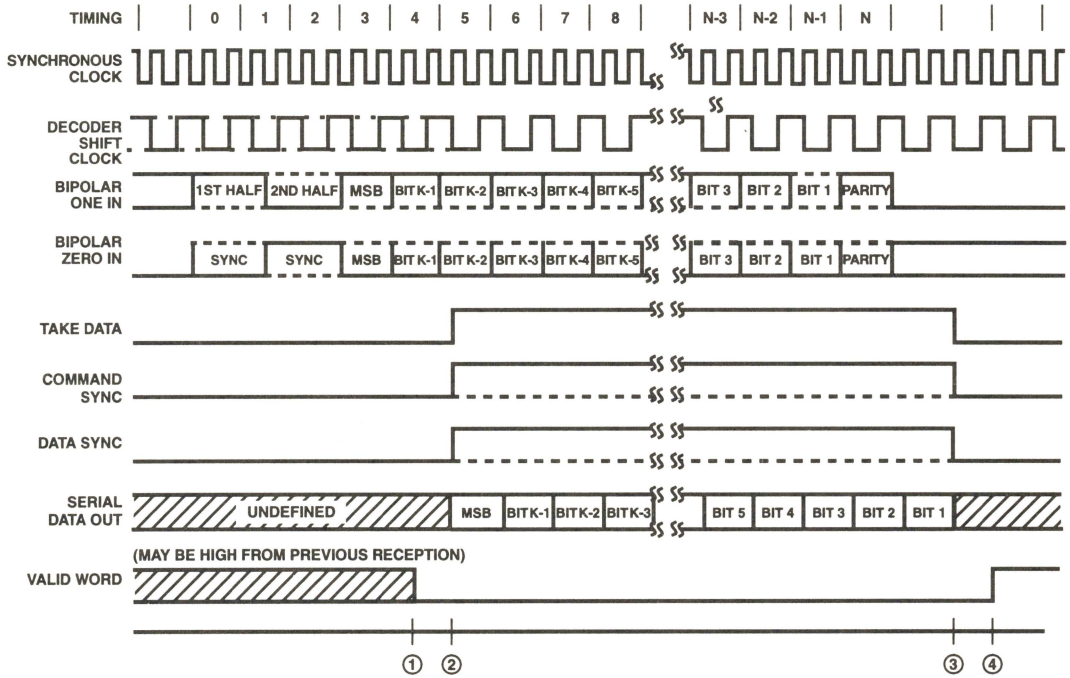


FIGURE 2. DECODER

Frame Counter

DATA BITS	FRAME LENGTH (BIT PERIODS)	PIN WORD				
		C_4	C_3	C_2	C_1	C_0
2	6	L	L	H	L	H
3	7	L	L	H	H	L
4	8	L	L	H	H	H
5	9	L	H	L	L	L
6	10	L	H	L	L	H
7	11	L	H	L	H	L
8	12	L	H	L	H	H
9	13	L	H	H	L	L
10	14	L	H	H	L	H
11	15	L	H	H	H	L
12	16	L	H	H	H	H
13	17	H	L	L	L	L
14	18	H	L	L	L	H
15	19	H	L	L	H	L
16	20	H	L	L	H	H
17	21	H	L	H	L	L
18	22	H	L	H	L	H
19	23	H	L	H	H	L
20	24	H	L	H	H	H
21	25	H	H	L	L	L
22	26	H	H	L	L	H
23	27	H	H	L	H	L
24	28	H	H	L	H	H
25	29	H	H	H	L	L
26	30	H	H	H	L	H
27	31	H	H	H	H	L
28	32	H	H	H	H	H

NOTE:

1. The above table demonstrates all possible combinations of frame lengths ranging from 6 to 32 bits. The pin word described here is common to both the Encoder and Decoder.

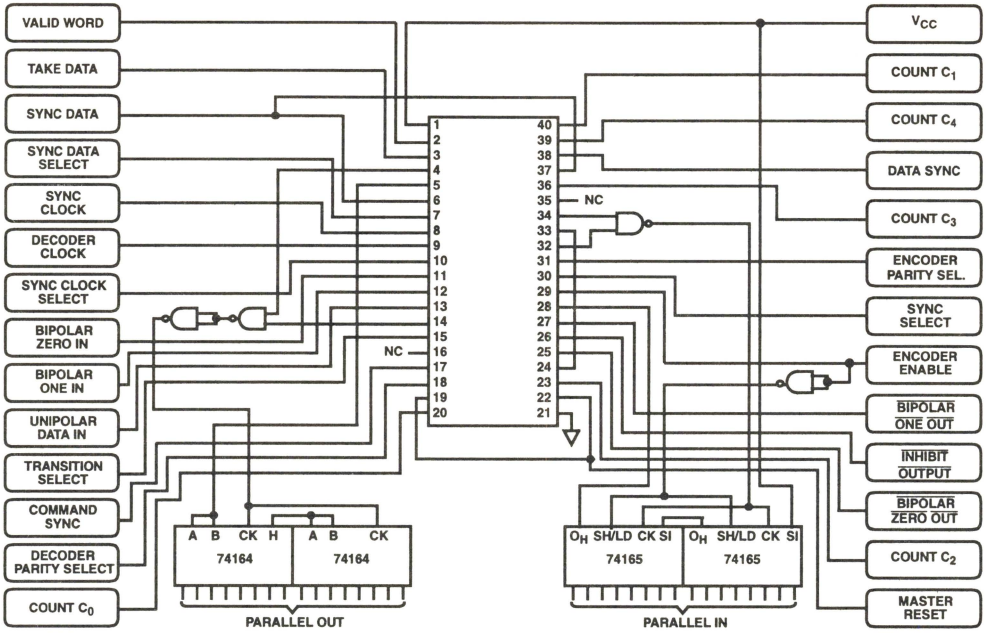


FIGURE 3. HOW TO MAKE OUR MTU LOOK LIKE A MANCHESTER ENCODED UART

Typical Timing Diagrams for a Manchester Encoded UART

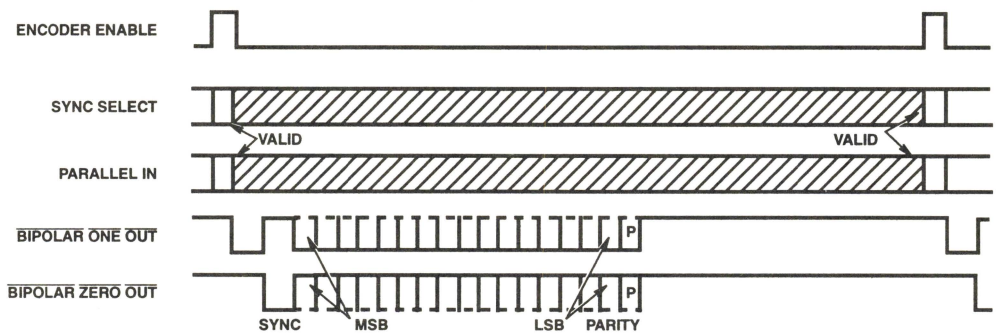


FIGURE 4. ENCODER TIMING

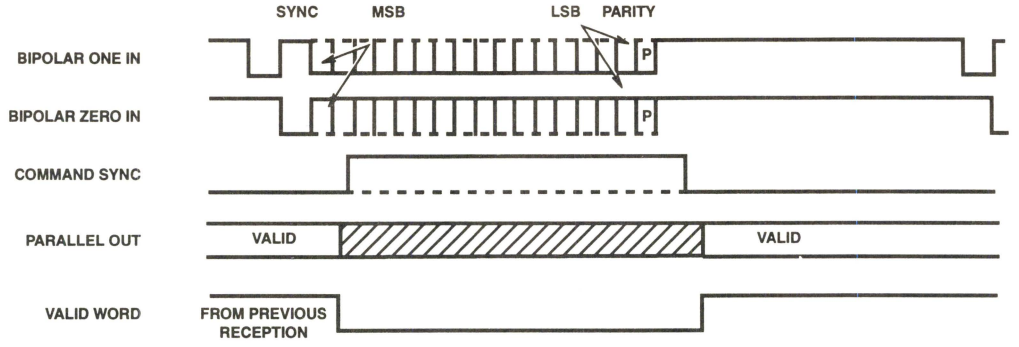


FIGURE 5. DECODER TIMING

MIL-STD-1553

The 1553 Standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HD-15531 supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command-Words, and Data. Terminals respond with Status Words, and Data. Each word is preceded by a synchronizing pulse, and followed by parity bit, occupying a total of 20μs. The word formats are shown in Figure 4. The special abbreviations are as follows:

P	Parity, which is defined to be odd, taken across all 17 bits.
R/T	Receive on logical zero, transmit on ONE.
ME	Message Error if logical 1.
TF	Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553, and do not completely describe its bus requirements, timing or protocols.

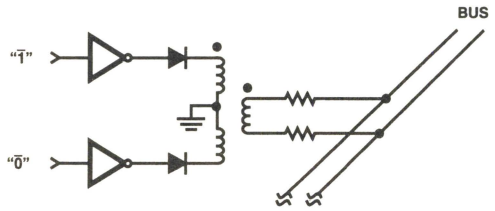


FIGURE 6. SIMPLIFIED MIL-STD-1553 DRIVER

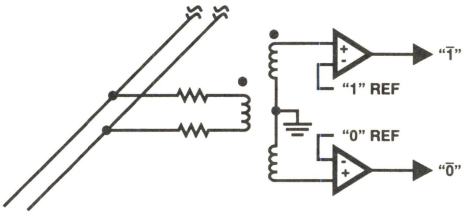


FIGURE 7. SIMPLIFIED MIL-STD-1553 RECEIVER

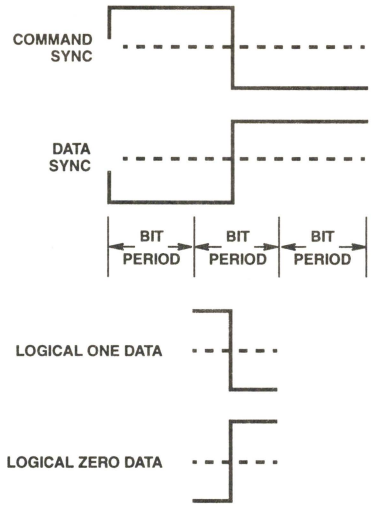


FIGURE 8. MIL-STD-1553 CHARACTER FORMATS

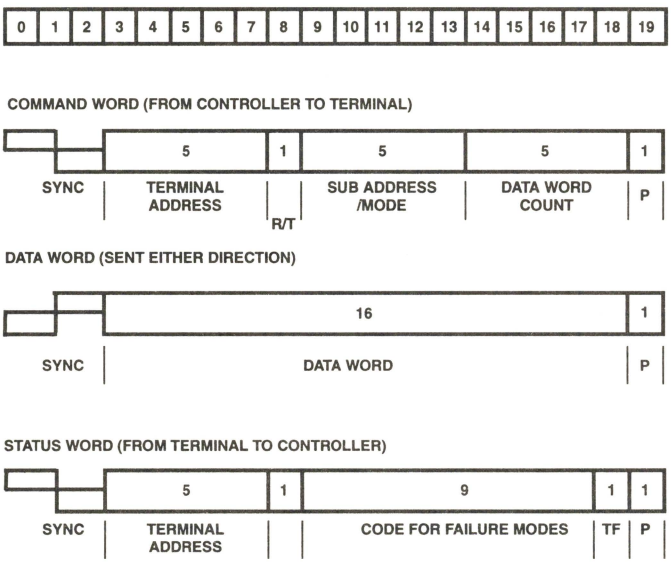


FIGURE 9. MIL-STD-1553 WORD FORMATS

NOTE:

1. This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HD-15531.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A)
HD-15531-9 . . . . . -40°C to +85°C
HD-15531-8 . . . . . -55°C to +125°C
Encoder/Decoder Clock Rise Time (TECR, TDCR) . . . . . 8ns Max
Encoder/Decoder Clock Fall Time (TECF, TDCF) . . . . . 8ns Max

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package	35°C/W	9°C/W
PDIP Package	50°C/W	N/A

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package . . . . . +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 250 Gates
Sync. Transition Span (TD2) . . . . . 18 TDC Typical, (Note 1)
Short Data Transition Span (TD4) . . . . . 6 TDC Typical, (Note 1)
Long Data Transition Span (TD5) . . . . . 12 TDC Typical, (Note 1)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5.0V ±10%, T_A = -40°C to +85°C (HD-15531-9)
T_A = -55°C to +125°C (HD-15531-8)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Input LOW Voltage	V_{IL}	V_{CC} = 4.5V and 5.5V	-	0.2 V_{CC}	V
Input HIGH Voltage	V_{IH}	V_{CC} = 4.5V and 5.5V	0.7 V_{CC}	-	V
Input LOW Clock Voltage	V_{ILC}	V_{CC} = 4.5V and 5.5V	-	GND +0.5	V
Input HIGH Clock Voltage	V_{IHC}	V_{CC} = 4.5V and 5.5V	V_{CC} -0.5	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +1.8mA, V_{CC} = 4.5V (Note 2)	-	0.4	V
Output HIGH Voltage	V_{OH}	I_{OH} = -3.0mA, V_{CC} = 4.5V (Note 2)	2.4	-	V
Input Leakage Current	I_I	V_I = V_{CC} or GND, V_{CC} = 5.5V	-1.0	+1.0	µA
Standby Supply Current	I_{CCSB}	V_{IN} = V_{CC} = 5.5V, Outputs Open	-	2	mA
Operating Power Supply Current	ICCOP	V_{IN} = V_{CC} = 5.5V, f = 15MHz, Outputs Open	-	10	mA
Functional Test	F_T	(Note 3)	-	-	-

NOTES:

1. TDC = Decoder clock period = 1/FDC.
2. Interchanging of force and sense conditions is permitted.
3. Tested as follows: f = 15MHz, V_{IH} = 70% V_{CC}, V_{IL} = 20% V_{CC}, C_L = 50pF, $V_{OH} \geq V_{CC}/2$ and $V_{OL} \leq V_{CC}/2$.

Capacitance

T_A = +25°C, Frequency = 1MHz

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	25	pF	All measurements are referenced to device GND
C_{OUT}	Output Capacitance	25	pF	

AC Electrical Specifications V_{CC} = 5V ±10%, T_A = -40°C to +85°C (HD-15530-9)
T_A = -55°C to +125°C (HD-15530-8)

SYMBOL	PARAMETER	HD-15531		HD-15531B		UNITS	TEST CONDITIONS (NOTE 2)
		MIN	MAX	MIN	MAX		
ENCODER TIMING							
FEC	Encoder Clock Frequency	-	15	-	30	MHz	V_{CC} = 4.5V and 5.5V, C_L = 50pF
FESC	Send Clock Frequency	-	2.5	-	5.0	MHz	V_{CC} = 4.5V and 5.5V, C_L = 50pF
FED	Encoder Data Rate	-	1.25	-	2.5	MHz	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TMR	Master Reset Pulse Width	150	-	150	-	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TE1	Shift Clock Delay	-	125	-	80	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TE2	Serial Data Setup	75	-	50	-	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TE3	Serial Data Hold	75	-	50	-	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TE4	Enable Setup	90	-	90	-	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TE5	Enable Pulse Width	100	-	100	-	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TE6	Sync Setup	55	-	55	-	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TE7	Sync Pulse Width	150	-	150	-	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TE8	Send Data Delay	0	50	0	50	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TE9	Bipolar Output Delay	-	130	-	130	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TE10	Enable Hold	10	-	10	-	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TE11	Sync Hold	95	-	95	-	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
DECODER TIMING							
FDC	Decoder Clock Frequency	-	15	-	30	MHz	V_{CC} = 4.5V and 5.5V, C_L = 50pF
FDS	Decoder Sync Clock	-	2.5	-	5.0	MHz	V_{CC} = 4.5V and 5.5V, C_L = 50pF
FDD	Decoder Data Rate	-	1.25	-	2.5	MHz	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TDR	Decoder Reset Pulse Width	150	-	150	-	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TDRS	Decoder Reset Setup Time	75	-	75	-	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TDRH	Decoder Reset Hold Time	10	-	10	-	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TMR	Master Reset Pulse	150	-	150	-	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TD1	Bipolar Data Pulse Width	TDC + 10 (Note 1)	-	TDC + 10 (Note 1)	-	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TD3	One Zero Overlap	-	TDC - 10 (Note 1)	-	TDC - 10 (Note 1)	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TD6	Sync Delay (ON)	-20	110	-20	110	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TD7	Take Data Delay (ON)	0	110	0	110	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TD8	Serial Data Out Delay	-	80	-	80	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TD9	Sync Delay (OFF)	0	110	0	110	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TD10	Take Data Delay (OFF)	0	110	0	110	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TD11	Valid Word Delay	0	110	0	110	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TD12	Sync Clock to Shift Clock Delay	-	75	-	75	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF
TD13	Sync Data Setup	75	-	75	-	ns	V_{CC} = 4.5V and 5.5V, C_L = 50pF

NOTES:

1. TDC = Decoder clock period = 1/FDC.
2. AC Testing as follows: Input levels: V_{IH} = 70% V_{CC}, V_{IL} = 20% V_{CC}; Input rise/fall times driven at 1ns/V; Timing Reference levels: $V_{CC}/2$; Output load: C_L = 50pF.

Timing Waveforms

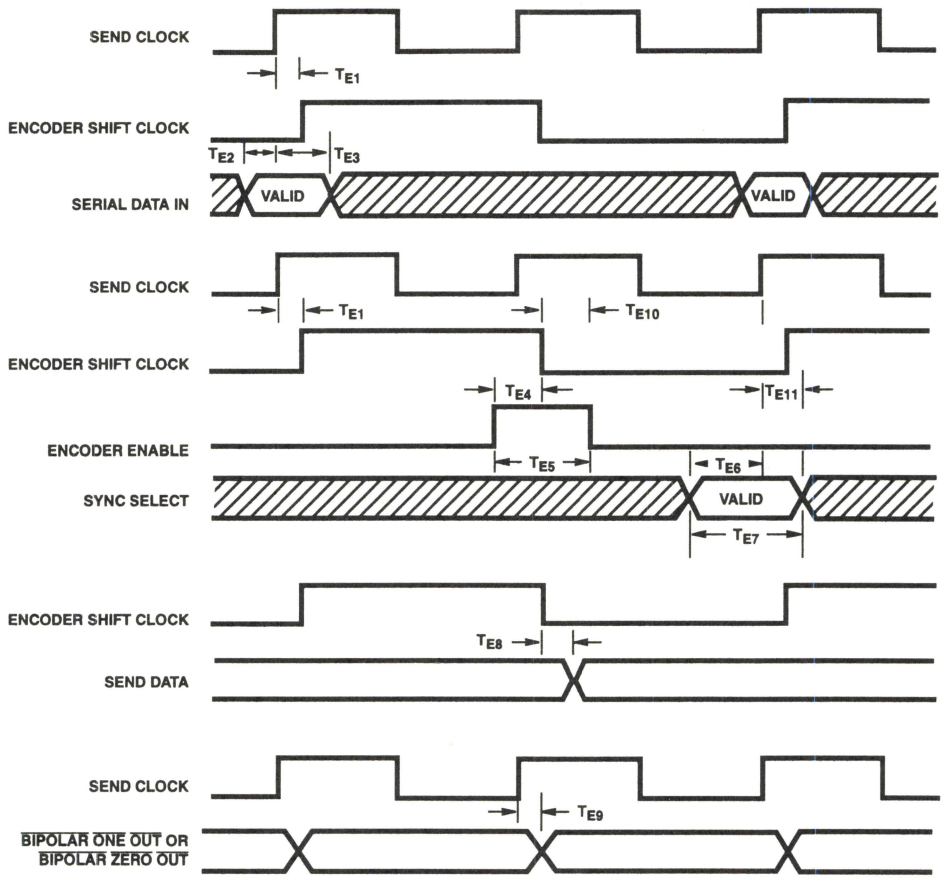
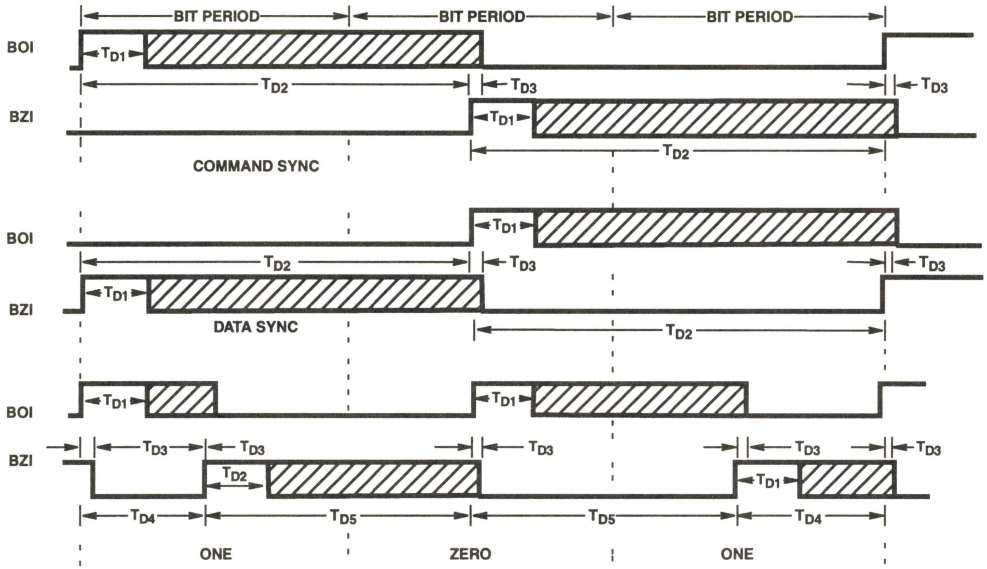


FIGURE 10. ENCODER TIMING

Timing Waveforms (Continued)

NOTE: UNIPOLAR IN = 0, FOR NEXT DIAGRAMS.



NOTE: BIPOLAR ONE IN = 0, BIPOLAR ZERO IN = 1, FOR NEXT DIAGRAMS.

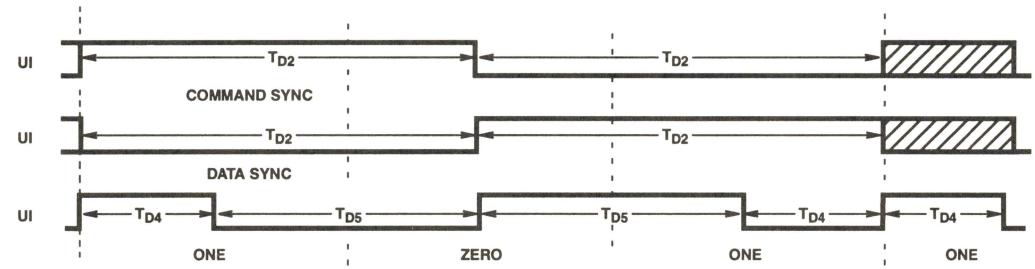


FIGURE 11. DECODER TIMING

Timing Waveforms (Continued)

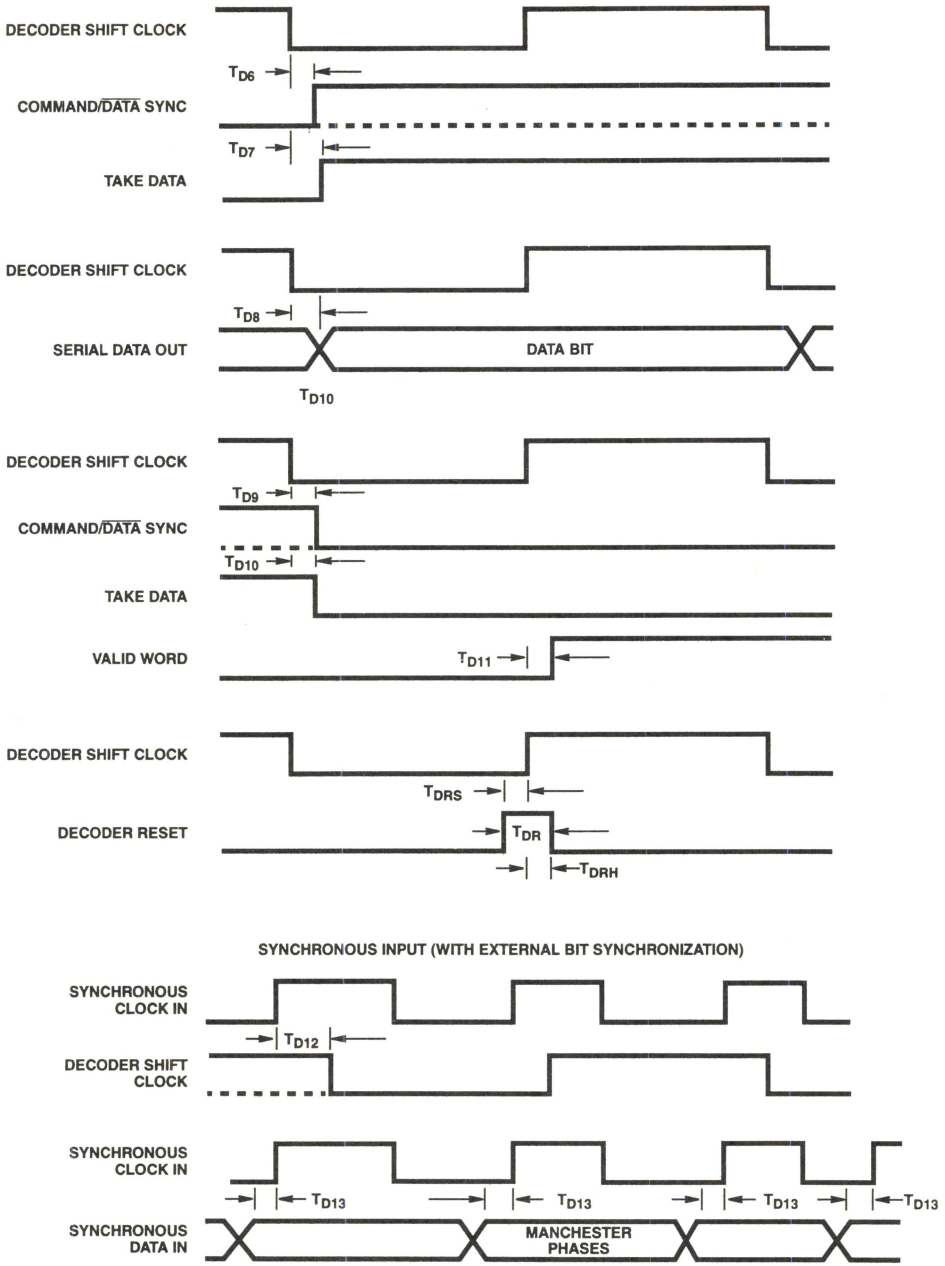


FIGURE 12. DECODER TIMINGS

Test Load Circuit

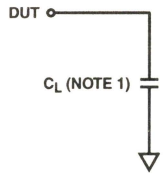


FIGURE 13.

NOTE:

1. Includes stray and jig capacitance.

AC Testing Input, Output Waveform

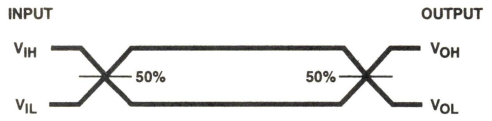


FIGURE 14.

NOTE:

1. AC Testing: All input signals must switch between V_{IL} and V_{IH}, input rise and fall times are driven at 1ns per volt.

HARRIS SEMICONDUCTOR

HD-15531/883

March 1997

CMOS Manchester Encoder-Decoder

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Support of MIL-STD-1553**
- **Data Rate (15531B) ..... 2.5 Megabit/Sec**
- **Data Rate (15531)..... 1.25 Megabit/Sec**
- **Variable Frame Length to 32-Bits**
- **Sync Identification and Lock-In**
- **Separate Manchester II Encode, Decode**
- **Low Operating Power .....50mW at 5V**

Description

The Harris HD-15531/883 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate independently of each other, except for the master reset and word length functions. This circuit provides many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

The HD-15531/883 also surpasses the requirements of MIL-STD-1553 by allowing the word length to be programmable (from 2 to 28 data bits). A frame consists of three bits for sync followed by the data word (2 to 28 data bits) followed by one bit of parity, thus, the frame length will vary from 6 to 32 bit periods. This chip also allows selection of either even or odd parity for the Encoder and Decoder separately.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. For high speed applications the 15531B will support a 2.5 Megabit/sec data rate.

The HD-15531/883 can also be used in many party line digital data communications applications, such as a local area network or an environmental control system driven from a single twisted pair or fiber optic cable throughout a building.

Ordering Information

PACKAGE	TEMPERATURE RANGE	1.25MBIT/SEC	2.5MBIT/SEC	PKG. NO.
CERDIP	-55°C to +125°C	HD1-15531/883	HD1-15531B/883	F40.6

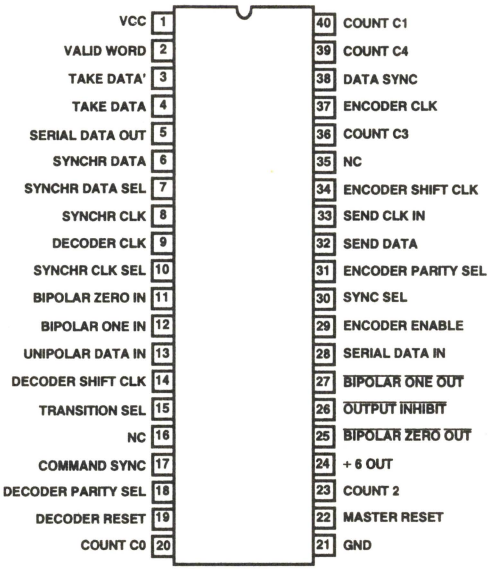
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2962.1**

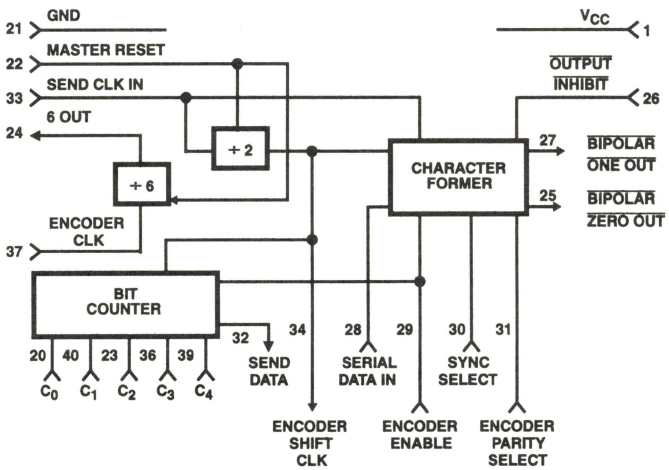
Pinout

HD-15531/883 (CERDIP)
TOP VIEW



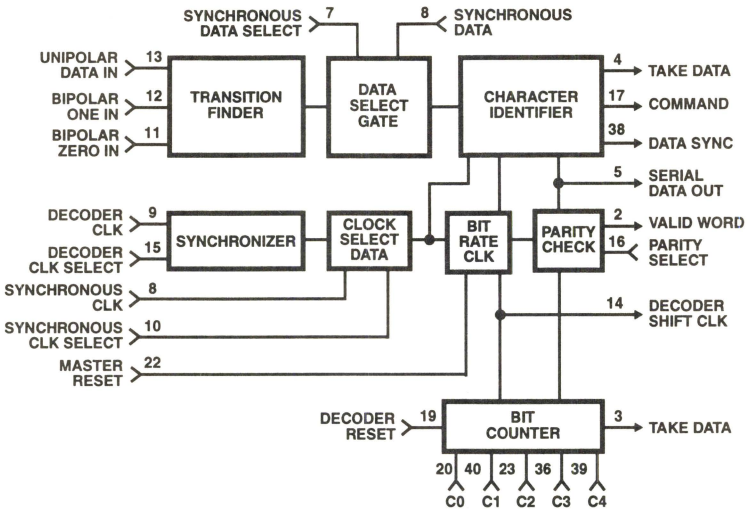
Block Diagrams

ENCODER



Block Diagrams (Continued)

DECODER



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to VCC +0.5V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	35°C/W	9°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 250 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Encoder/Decoder Clock Rise Time (TECR, TDCR) . . . . . 8ns Max
Encoder/Decoder Clock Fall Time (TECF, TDCF) . . . . . 8ns Max
Sync. Transition Span (TD2) . . . . . 18 TDC Typical, (Note 1)
Short Data Transition Span (TD4) . . . . . 6 TDC Typical, (Note 1)
Long Data Transition Span (TD5) . . . . . 12 TDC Typical, (Note 1)

TABLE 1. HD-15531/883, HD-15531B/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input LOW Voltage	VIL	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.2 VCC	V
Input HIGH Voltage	VIH	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	0.7 VCC	-	V
Input LOW Clock Voltage	VILC	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	GND +0.5	V
Input HIGH Clock Voltage	VIHC	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	VCC -0.5	-	V
Output LOW Voltage	VOL	IOL = +1.8mA, VCC = 4.5V (Note 2)	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Output HIGH Voltage	VOH	IOH = -3.0mA, VCC = 4.5V (Note 2)	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
Input Leakage Current	II	VI = VCC or GND, VCC = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Standby Supply Current	ICCSB	VIN = VCC = 5.5V, Outputs Open	1, 2, 3	$-55°C \le T_A \le +125°C$	-	2	mA
Functional Test	FT	(Note 3)	7, 8	$-55°C \le T_A \le +125°C$	-	-	-

NOTES:

1. TDC = Decoder clock period = 1/FDC.
2. Interchanging of force and sense conditions is permitted.
3. Tested as follows: f = 15MHz, VIH = 70% VCC, VIL = 20% VCC, CL = 50pF, VOH ≥ VCC/2 and VOL ≤ VCC/2.

TABLE 2. HD-15531/883, HD-15531B/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	(NOTE 2) CONDI-TIONS	GROUP A SUB-GROUPS	TEMPERATURE	HD-15531/883 MIN	HD-15531/883 MAX	HD-15531B/883 MIN	HD-15531B/883 MAX	UNITS
ENCODER TIMING									
Encoder Clock Frequency	FEC	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	15	-	30	MHz
Send Clock Frequency	FESC	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	2.5	-	5.0	MHz

TABLE 2. HD-15531/883, HD-15531B/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

PARAMETER	SYMBOL	(NOTE 2) CONDI-TIONS	GROUP A SUB-GROUPS	TEMPERATURE	HD-15531/883		HD-15531B/883		UNITS
					MIN	MAX	MIN	MAX	
Encoder Data Rate	FED	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	1.25	-	2.5	MHz
Master Reset Pulse Width	TMR	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	150	-	ns
Shift Clock Delay	TE1	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	125	-	80	ns
Serial Data Setup	TE2	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	75	-	50	-	ns
Serial Data Hold	TE3	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	75	-	50	-	ns
Enable Setup	TE4	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	90	-	90	-	ns
Enable Pulse Width	TE5	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	100	-	ns
Sync Setup	TE6	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	55	-	55	-	ns
Sync Pulse Width	TE7	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	150	-	ns
Send Data Delay	TE8	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	50	0	50	ns
Bipolar Output Delay	TE9	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	130	-	130	ns
Enable Hold	TE10	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	10	-	ns
Sync Hold	TE11	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	95	-	95	-	ns
DECODER TIMING									
Decoder Clock Frequency	FDC	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	15	-	30	MHz
Decoder Sync Clock	FDS	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	2.5	-	5.0	MHz
Decoder Data Rate	FDD	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	1.25	-	2.5	MHz
Decoder Re-set Pulse Width	TDR	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	150	-	ns
Decoder Re-set Setup Time	TDRS	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	75	-	75	-	ns
Decoder Re-set Hold Time	TDRH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	10	-	ns
Master Reset Pulse	TMR	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	150	-	ns
Bipolar Data Pulse Width	TD1	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	TDC +10 (Note 1)	-	TDC +10 (Note 1)	-	ns
One Zero Overlap	TD3	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	TDC-10 (Note 1)	-	TDC-10 (Note 1)	ns
Sync Delay (ON)	TD6	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-20	110	-20	110	ns

TABLE 2. HD-15531/883, HD-15531B/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

PARAMETER	SYMBOL	(NOTE 2) CONDI-TIONS	GROUP A SUB-GROUPS	TEMPERATURE	HD-15531/883		HD-15531B/883		UNITS
					MIN	MAX	MIN	MAX	
Take Data Delay (ON)	TD7	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	110	0	110	ns
Serial Data Out Delay	TD8	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	80	-	80	ns
Sync Delay (OFF)	TD9	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	110	0	110	ns
Take Data Delay (OFF)	TD10	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	110	0	110	ns
Valid Word Delay	TD11	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	110	0	110	ns
Sync Clock to Shift Clock Delay	TD12	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	75	-	75	ns
Sync Data Setup	TD13	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	75	-	75	-	ns

NOTES:

1. TDC = Decoder Clock Period = 1/FDC.
2. AC Testing as follows: VIH = 70% VCC, VIL = 20% VCC; Input rise/fall times driven at 1ns/V; Timing reference levels: VCC/2; Output load: CL = 50pF.

TABLE 3. HD-15531/883, HD-15531B/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CI	VCC = OPEN, f = 1MHz, All measurements referenced to device GND	1	$T_A = +25^oC$	-	25	pF
Input/Output Capacitance	CIO	VCC = OPEN, f = 1MHz, All measurements referenced to device GND	1	$T_A = +25^oC$	-	25	pF
Operating Power Supply Current	ICCOP	VCC = 5.5V, f = 1MHz	1, 2	$-55^oC \le T_A \le +125^oC$	-	10	mA

NOTES:

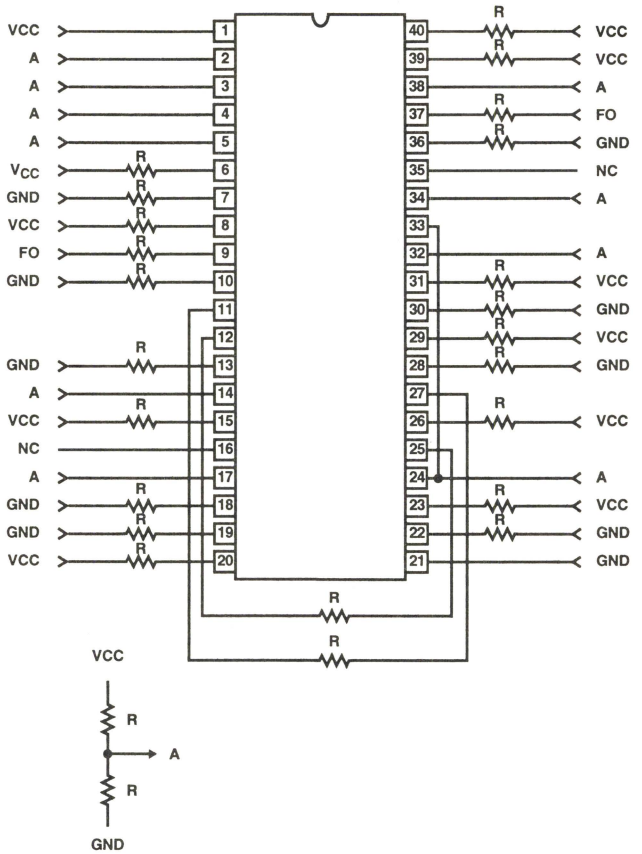
1. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
2. Guaranteed but not 100% tested.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Burn-In Circuit

HD1-15531/883 CERDIP



NOTES:

1. VCC = 5.5V ±0.5V.
2. VIH = 4.5V ±10%.
3. VIL = -0.2V to +0.4V.
4. R = 47kΩ ±5%.
5. F0 = 100kHz ±10%.

Die Characteristics

DIE DIMENSIONS:
155 x 195 x 19 ±1mils

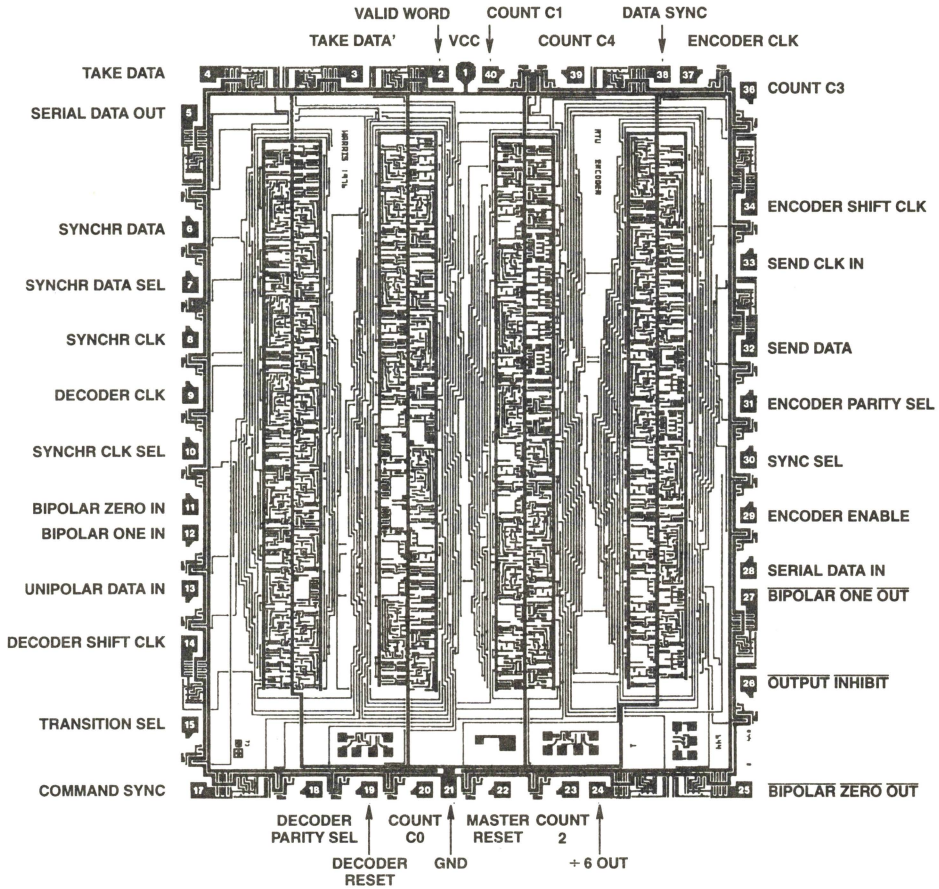
METALLIZATION:
Type: Si-Al
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
2.0×10^5 A/cm^2

Metallization Mask Layout

HD-15531/883



HARRIS SEMICONDUCTOR

HS-3182

March 1997

ARINC 429 Bus Interface Line Driver Circuit

Features

- TTL and CMOS Compatible Inputs
- Adjustable Rise and Fall Times via Two External Capacitors
- Programmable Output Differential Voltage via V_{REF} Input
- Operates at Data Rates Up to 100 Kilobits/Sec
- Output Short Circuit Proof and Contains Over-Voltage Protection
- Outputs are Inhibited (0 Volts) If DATA (A) and DATA (B) Inputs are Both in the "Logic One" State
- DATA (A) and DATA (B) Signals are "AND'd" with Clock and Sync Signals
- Full Military Temperature Range

Ordering Information

PACKAGE	TEMPERATURE RANGE	PART NUMBER	PKG. NO
SBDIP	-40°C to +85°C	HS1-3182-9+	D16.3
	-55°C to +125°C	HS1-3182-8	D16.3
SMD#	-55°C to +125°C	5962-8687901EA	D16.3
CLCC	-55°C to +125°C	HS4-3182-8	J28.A
SMD#	-55°C to +125°C	5962-86879013A	J28.A

Description

The HS-3182 is a monolithic dielectrically isolated bipolar differential line driver designed to meet the specifications of ARINC 429. This Device is intended to be used with a companion chip, HS-3282 CMOS ARINC Bus Interface Circuit, which provides the data formatting and processor interface function.

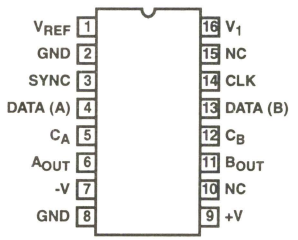
All logic inputs are TTL and CMOS compatible. In addition to the DATA (A) and DATA (B) inputs, there are also inputs for CLOCK and SYNC signals which are AND'd with the DATA inputs. This feature enhances system performance and allows the HS-3182 to be used with devices other than the HS-3182.

Three power supplies are necessary to operate the HS-3182: +V = +15V ± 10%, -V = -15V ± 10%, and V_1 = 5V ± 5%. V_{REF} is used to program the differential output voltage swing such that V_{OUT} (DIFF) = ± $2V_{REF}$. Typically, V_{REF} = V_1 = 5V ± 5%, but a separate power supply may be used for V_{REF} which should not exceed 6V.

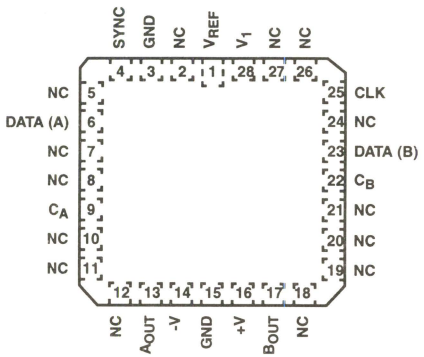
The driver output impedance is 75Ω ± 20% at 25°C. Driver output rise and fall times are independently programmed through the use of two external capacitors connected to the C_A and C_B inputs. Typical capacitor values are C_A = C_B = 75pF for high-speed operation (100KBPS), and C_A = C_B = 300pF for low-speed operation (12 to 14.5KBPS). The outputs are protected against over-voltage and short circuit as shown in the Block Diagram. The HS-3182 is designed to operate with a case temperature range of -55°C to +125°C, or 0°C to +70°C.

Pinouts

HS-3182 (SBDIP)
TOP VIEW



HS-3182 (CLCC)
TOP VIEW



TRUTH TABLE

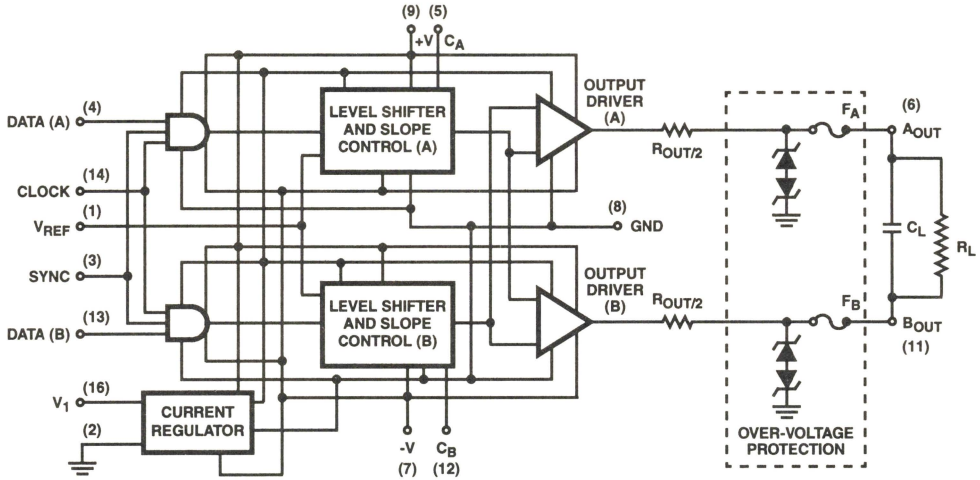
SYNC	CLK	DATA (A)	DATA (B)	A_{OUT}	B_{OUT}	COMMENTS
X	L	X	X	0V	0V	Null
L	X	X	X	0V	0V	Null
H	H	L	L	0V	0V	Null
H	H	L	H	$-V_{REF}$	$+V_{REF}$	Low
H	H	H	L	$+V_{REF}$	$-V_{REF}$	High
H	H	H	H	0V	0V	Null

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

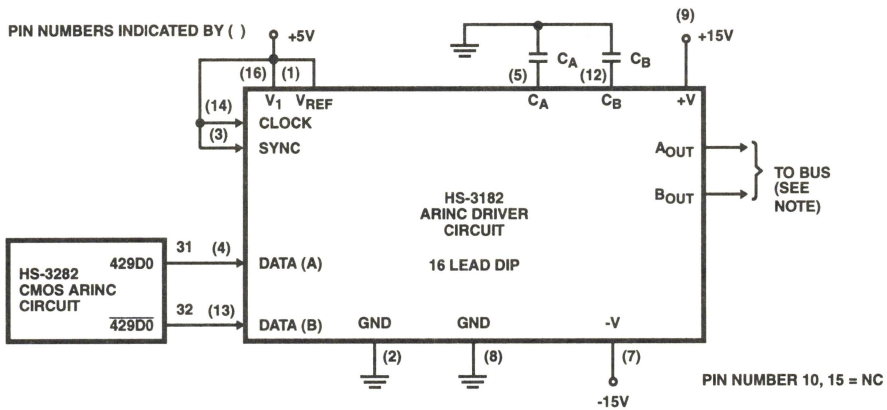
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File Number **2963.1**

Block Diagram



Typical Application



NOTE: The rise and fall time of the outputs are set to ARINC specified values by C_A and C_B. Typical $C_A = C_B = 75pF$ for high speed and 300pF for low speed operation. The output HI and low levels are set to ARINC specifications by V_{REF}.

Absolute Maximum Ratings

Voltage Between +V and -V Terminals 40V
V_1 . . . . . 7V
V_{REF} 6V
Logic Input Voltage . . . . . GND -0.3V to V_1 +0.3V
ESD Classification . . . . . Class 1
Output Short Circuit Duration . . . . . See Note 1
Output Over-Voltage Protection . . . . . See Note 2

Recommended Operating Conditions

Operating Voltage
+V . . . . . +15V ± 10%
-V . . . . . -15V ± 10%
V_1 . . . . . 5V ± 5%
V_{REF} (For ARINC 429) . . . . . 5V ± 5%
Operating Temperature Range
HS-3182-5 . . . . . 0°C to +70°C
HS-3182-8 . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
SBDIP Package	75°C/W	18°C/W
CLCC Package	60°C/W	14°C/W

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Transistor Count 133

NOTES:

1. Heat sink may be required for 100K bits/s at +125°C and output short circuit at +125°C.
2. The fuses used for output over-voltage protection may be blown by a fault at each output of greater than ± 6.5V relative to GND.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Performance Specifications

DC PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	MIN	MAX	UNITS
Supply Current +V (Operating)	I_{CCOP} (+V)	No Load (0-100K bits/s)	-	16	mA
Supply Current -V (Operating)	I_{CCOP} (-V)	No Load (0-100K bits/s)	-16	-	mA
Supply Current V_1 (Operating)	I_{CCOP} (V_1)	No Load (0-100K bits/s)	-	975	µA
Supply Current V_{REF} (Operating)	I_{CCOP} (V_{REF})	No Load (0-100K bits/s)	-1.0	-	mA
Logic "1" Input Voltage	V_{IH}		2.0	-	V
Logic "0" Input Voltage	V_{IL}		-	0.5	V
Output Voltage High (Output to GND)	V_{OH}	No Load (0-100K bits/s)	V_{REF} (-250mV)	V_{REF} (+250mV)	
Output Voltage Low (Output to GND)	V_{OL}	No Load (0-100K bits/s)	$-V_{REF}$ (-250mV)	$-V_{REF}$ (+250mV)	
Output Voltage Null	V_{NULL}	No Load (0-100K bits/s)	-250	+250	mV
Input Current (Input Low)	I_{IL}		-20	-	µA
Input Current (Input High)	I_{IH}		-	10	µA
Output Short Circuit Current (Output High)	I_{OHSC}	Short to GND	-	-80	mA
Output Short Circuit Current (Output Low)	I_{OLSC}	Short to GND	80	-	mA
Output Impedance	Z_O	T_A = +25°C	60	90	Ω

NOTE:

1. +V = +15V ± 10%, -V = -15V ± 10%, V_1 = V_{REF} = 5V ± 5%, unless otherwise specified T_A = 0°C to +70°C for HS-3182-5 and T_A = -55°C to +125°C for HS-3182-8.

AC Electrical Performance Specifications

AC PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	MIN	MAX	UNITS
Rise Time (A_{OUT}, B_{OUT})	t_R	$C_A = C_B = 75pF$, Note 2	1	2	µS
		(at $T_A = -55^oC$ Only)	0.9	2.4	µS
		$C_A = C_B = 300pF$, Note 2	3	9	µS
Fall Time (A_{OUT}, B_{OUT})	t_F	$C_A = C_B = 75pF$, Note 3	1	2	µS
		(at $T_A = -55^oC$ Only)	0.9	2.4	µS
		$C_A = C_B = 300pF$, Note 3	3	9	µS
Propagation Delay Input to Output	t_{PLH}	$C_A = C_B = 75pF$, No Load	-	3.3	µS
Propagation Delay Input to Output	t_{PHL}	$C_A = C_B = 75pF$, No Load	-	3.3	µS

NOTES:

1. $+V = +15V$, $-V = -15V$, $V_1 = V_{REF} = 5V$, unless otherwise specified $T_A = 0^oC$ to $+70^oC$ for HS-3182-5 and $T_A = -55^oC$ to $+125^oC$ for HS-3182-8.
2. t_R measured 50% to 90% times 2, no load.
3. t_F measured 50% to 10% times 2, no load.

Electrical Performance Specifications

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	MIN	MAX	UNITS
Input Capacitance	C_{IN}	$T_A = +25^oC$	-	15	pF
Supply Current +V (Short Circuit)	I_{SC} (+V)	Short to GND, $T_A = +25^oC$	-	150	mA
Supply Current -V (Short Circuit)	I_{SC} (-V)	Short to GND, $T_A = +25^oC$	-150	-	mA

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes affecting these parameters.

Power Specifications

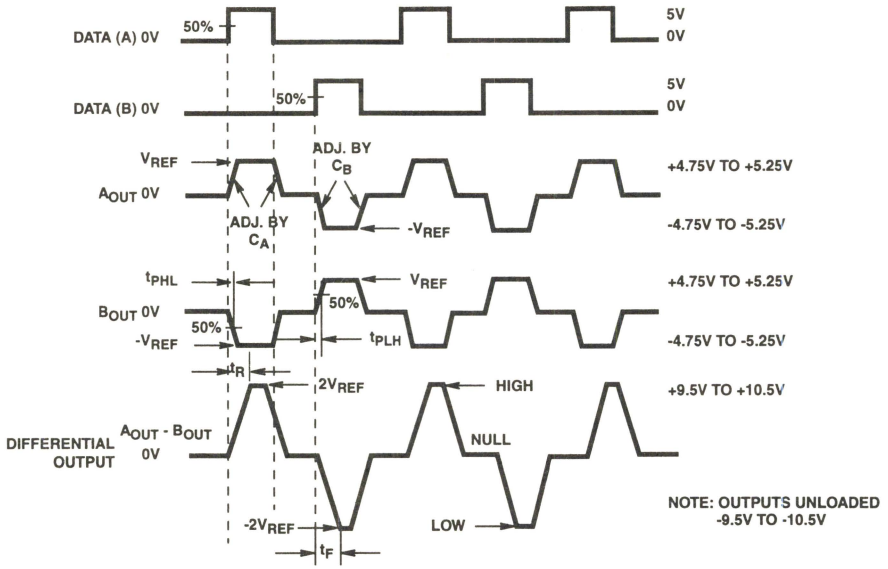
Nominal Power at $+25^oC$, $+V = +15V$, $-V = -15V$, $V1 = V_{REF} = 5V$, Notes 1, 3

DATA RATE (K BITS/s)	LOAD	+V	V-	V_1	CHIP POWER	POWER DISSIPATION IN LOAD
0-100	No Load	11mA	-10mA	600µA	325mW	0
12.5-14	Full Load, Note 2	24mW	-24mW	600µA	660mW	60mW
100	Full Load, Note 2	46mW	-46mW	600µA	1 Watt	325mW

NOTES:

1. Heat sink may be required for 100K bits/s at $+125^oC$ and output short circuit at $+125^oC$.
   Thermal characteristics: $T_{(CASE)} = T_{(Junction)} - \theta_{(Junction - Case)} P_{(Dissipation)}$.
   Where: $T_{(Junction\ Max)} = +175^oC$
   $\theta_{(Junction - Case)} = 10.9^oC/W$ ($6.1^oC/W$ for LCC)
   $\theta_{(Junction - Ambient)} = 73.5^oC/W$ ($54.0^oC/W$ for LCC)
2. Full Load for ARINC 429: $R_L = 400\Omega$ and $C_L = 30{,}000pF$ in parallel between A_{OUT} and B_{OUT} (see block diagram).
3. Output Over-Voltage Protection: The fuses used for output over-voltage protection may be blown by a fault at each output of greater than ±6.5V relative to GND.

Driver Waveforms



NOTES: t_R measured 50% to 90% times 2

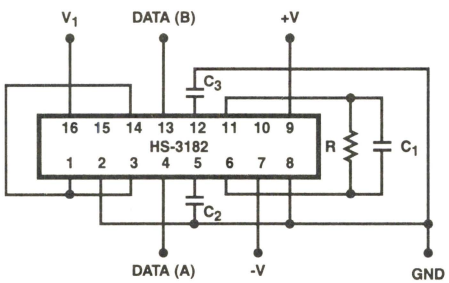
t_F measured 50% to 10% times 2

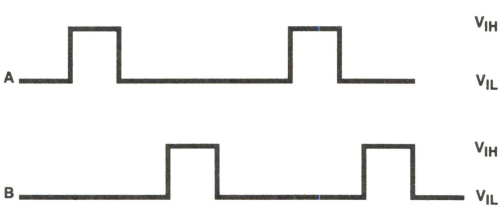
V_{IH} = 5V V_{OL} = -4.75V to -5.25V

V_{IL} = 0V V_{OH} = 4.75V to 5.25V

When the Data (A) input is in the Logic One state and the Data (B) input is in the Logic Zero state, A_{OUT} is equal to V_{REF} and B_{OUT} is equal to $-V_{REF}$. This constitutes the Output High state. Data (A) and Data (B) both in the Logic Zero state causes both A_{OUT} and B_{OUT} to be equal to 0V which designates the output Null state. Data (A) in the Logic Zero state and Data (B) in the Logic One state causes A_{OUT} to be equal to $-V_{REF}$ and B_{OUT} to be equal to V_{REF} which is the Output Low state.

Burn-In Schematic





NOTES: R = 400Ω ± 5%

C_1 = 0.03µF ± 20%

$C_2 = C_3$ = 500pF, NPO

+V = +15.5V ± 0.5V

-V = -15.5V ± 0.5V

V_1 = +5.5V ± 0.5V

A 0.0µF decoupling capacitor is required on each of the three supply lines (+V, -V and V_1) at every 3rd Burn-In socket.

Ambient Temp. Max. = +125°C.

Package = 16 Lead Side Brazed DIP.

Pulse Conditions = A & B = 6.25kHz ± 10%. B is delayed one-half cycle and in sync with A.

V_{IH} = 2.0V Min.

V_{IL} = 0.5V Max.

HARRIS SEMICONDUCTOR

HS-3282

REFERENCE AN400

March 1997

CMOS ARINC Bus Interface Circuit

Features

- ARINC Specification 429 Compatible
- Data Rates of 100 Kilobits or 12.5 Kilobits
- Separate Receiver and Transmitter Section
- Dual and Independent Receivers, Connecting Directly to ARINC Bus
- Serial to Parallel Receiver Data Conversion
- Parallel to Serial Transmitter Data Conversion
- Word Lengths of 25 or 32 Bits
- Parity Status of Received Data
- Generate Parity of Transmitter Data
- Automatic Word Gap Timer
- Single 5V Supply
- Low Power Dissipation
- Full Military Temperature Range

Ordering Information

PACKAGE	TEMP. RANGE	PART NUMBER	PKG. NO.
CERDIP	-55°C to +125°C	HS1-3282-8	F40.6
SMD#		5962-8688001QA	F40.6
CLCC	-40°C to +85°C	HS4-3282-9+	J44.A
	-55°C to +125°C	HS4-3282-8	J44.A
SMD#		5962-8688001XA	J44.A

Description

The HS-3282 is a high performance CMOS bus interface circuit that is intended to meet the requirements of ARINC Specification 429, and similar encoded, time multiplexed serial data protocols. This device is intended to be used with the HS-3182, a monolithic DI bipolar differential line driver designed to meet the specifications of ARINC 429. The ARINC 429 bus interface circuit consists of two (2) receivers and a transmitter operating independently as shown in Figure 1. The two receivers operate at a frequency that is ten (10) times the receiver data rate, which can be the same or different from the transmitter data rate. Although the two receivers operate at the same frequency, they are functionally independent and each receives serial data asynchronously. The transmitter section of the ARINC bus interface circuit consists mainly of a First-In First-Out (FIFO) memory and timing circuit. The FIFO memory is used to hold up to eight (8) ARINC data words for transmission serially. The timing circuit is used to correctly separate each ARINC word as required by ARINC Specification 429. Even though ARINC Specification 429 specifies a 32-bit word, including parity, the HS-3282 can be programmed to also operate with a word length of 25 bits. The incoming receiver data word parity is checked, and a parity status is stored in the receiver latch and output on Pin BD08 during the 1st word. [A logic "0" indicates that an odd number of logic "1" s were received and stored; a logic "1" indicates that an even number of logic "1"s were received and stored]. In the transmitter the parity generator will generate either odd or even parity depending upon the status of PARCK control signal. A logic "0" on BD12 will cause odd parity to be used in the output data stream.

Versatility is provided in both the transmitter and receiver by the external clock input which allows the bus interface circuit to operate at data rates from 0 to 100 kilobits. The external clock must be ten (10) times the data rate to insure no data ambiguity.

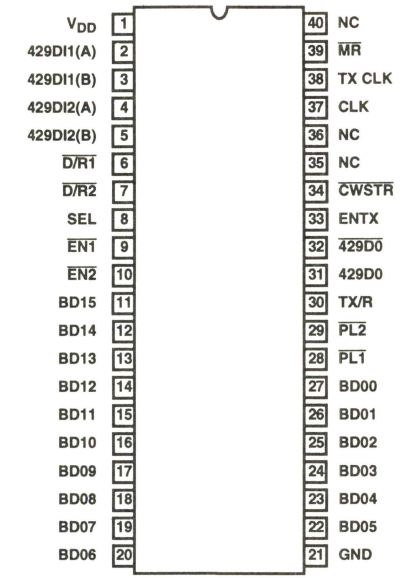
The ARINC bus interface circuit is fully guaranteed to support the data rates of ARINC specification 429 over both the voltage (±5%) and full military temperature range. It interfaces with UL, CMOS or NMOS support circuitry, and uses the standard 5-volt V_{CC} supply.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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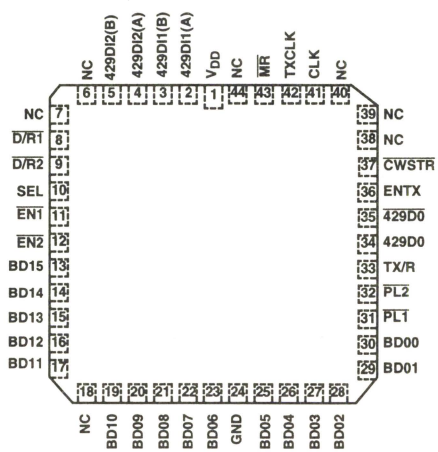
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Pinouts

HS-3282 (CERDIP)
TOP VIEW



HS-3282 (CLCC)
TOP VIEW



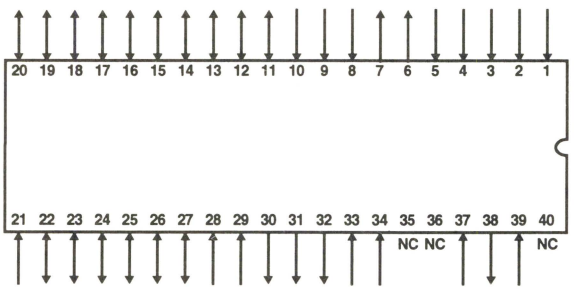
Pin Description

PIN	SYMBOL	SECTION	DESCRIPTION
1	V_{CC}	Recs/Trans	Supply pin 5 volts ±5%.
2	429 DI1 (A)	Receiver	ARINC 429 data input to Receiver 1.
3	429 DI1 (B)	Receiver	ARINC 429 data input to Receiver 1.
4	429 DI2 (A)	Receiver	ARINC 429 data input to Receiver 2.
5	429 DI2 (B)	Receiver	ARINC 429 data input to Receiver 2.
6	$\overline{D/R1}$	Receiver	Device ready flag output from Receiver 1 indicating a valid data word is ready to be fetched.
7	$\overline{D/R2}$	Receiver	Device ready flag output from Receiver 2 indicating a valid data word is ready to be fetched.
8	SEL	Receiver	Bus Data Selector - Input signal to select one of two 16-bit words from either Receiver 1 or 2.
9	$\overline{EN1}$	Receiver	Input signal to enable data from Receiver 1 onto the data bus.
10	$\overline{EN2}$	Receiver	Input signal to enable data from Receiver 2 onto the data bus.
11	BD15	Recs/Trans	Bi-directional data bus for fetching data from either of the Receivers, or for loading data into the Transmitter memory or control word register. See Control Word Table for description of Control Word bits.
12	BD14	Recs/Trans	See Pin 11.
13	BD13	Recs/Trans	See Pin 11.
14	BD12	Recs/Trans	See Pin 11.
15	BD11	Recs/Trans	See Pin 11.
16	BD10	Recs/Trans	See Pin 11.
17	BD09	Recs/Trans	See Pin 11.
18	BD08	Recs/Trans	See Pin 11.
19	BD07	Recs/Trans	See Pin 11.
20	BD06	Recs/Trans	See Pin 11.
21	GND	Recs/Trans	Circuit Ground.
22	BD05	Recs/Trans	See Pin 11.
23	BD04	Recs/Trans	See Pin 11. Control Word function not applicable.
24	BD03	Recs/Trans	See Pin 11. Control Word function not applicable.
25	BD02	Recs/Trans	See Pin 11. Control Word function not applicable.
26	BD01	Recs/Trans	See Pin 11. Control Word function not applicable.
27	BD00	Recs/Trans	See Pin 11. Control Word function not applicable.
28	$\overline{PL1}$	Transmitter	Parallel load input signal loading the first 16-bit word into the Transmitter memory.
29	$\overline{PL2}$	Transmitter	Parallel load input signal loading the first 16-bit word into the Transmitter memory and initiates data transfer into the memory stack.
30	TX/R	Transmitter	Transmitter flag output to indicate the memory is empty.

Pin Description (Continued)

PIN	SYMBOL	SECTION	DESCRIPTION
31	429D0	Transmitter	Data output from Transmitter
32	$\overline{429D0}$	Transmitter	Data output from Transmitter.
33	ENTX	Transmitter	Transmitter Enable input signal to initiate data transmission from FIFO memory.
34	$\overline{CWSTR}$	Recs/Trans	Control word input strobe signal to latch the control word from the databus into the control word register.
35	-	-	No connection. Must be left open.
36	-	-	No connection. Must be left open or tied low but never tied high.
37	CLK	Recs/Trans	External clock input. May be either ten (10) or eighty (80) times the data rate. If using both ARINC data rates it must be ten (10) times the highest data rate, (typically 1MHz).
38	TXCLK	Transmitter	Transmitter Clock output. Delivers a clock frequency equal to the transmitter data rate.
39	$\overline{MR}$	Recs/Trans	Master Reset. Active low pulse used to reset FIFO, bit counters, gap timer, word count signal, TX/R and various other flags and controls. Master reset does not reset the control word register. Usually only used on Power-Up or System Reset.
40	-	-	No Connection.

Pinout



Operational Description

The HS-3282 is designed to support ARINC Specification 429 and other serial data protocols that use a similar format by collecting the receiving, transmitting, synchronizing, timing and parity functions on a single, low power LSI circuit. It goes beyond the ARINC requirements by providing for either odd or even parity, and giving the user a choice of either 25 or 32-bit word lengths. The receiver and transmitter sections operate independently of each other. The serial-to-parallel conversion required of the receiver and the parallel-to-serial conversion requirements of the transmitter have been incorporated into the bus interface circuit.

Provisions have been made through the external clock input to provide data rate flexibility. This requires an external clock that is 10 times the data rate.

To obtain the flexibility discussed above, a number of external control signals are required, To reduce the pin count requirements, an internal control word register is used. The control word is latched from the data bus into the register by the Control Word Strobe ($\overline{\text{CWSTR}}$) signal going to a logic "1". Eleven (11) control functions are used, and along with the Bus Data (BD) line are listed below:

Control Word

PIN NAME	SYMBOL	FUNCTION
BD05	SLFTST	Connects the self test signal from the transmitter directly to the receiver shift registers, bypassing the input receivers. Receiver 1 receives Data True and Receiver 2 receives Data Not. Note that the transmitter output remains active. (Logic "0" on SLFTST Enables Self Test).
BD06	SDENB1	Signal to Activate the Source/Destination (S/D) Decoder for Receiver 1. (Logic "1" activates S/D Decoder).
BD07	X1	If SDENB1 = "1" then this bit is compared with ARINC Data Bit #9. If Y1 also matches (see Y1), the word will be accepted by the Receiver 1. If SDENB1 = "0" this bit becomes a don't care.
BD08	Y1	If SDENBI = "1" then this bit is compared with ARINC Data Bit #10. If X1 also matches (see X1), the word will be accepted by the Receiver 1. If SDENB1 = "0" this bit becomes a don't care.
BD09	SDENB2	Signal to activate the Source/Destination (S/D) Decoder for Receiver 2. (Logic "1" activates S/D Decoder).
BD10	X2	If SDENB2 = "1" then this bit is compared with ARINC Data Bit #9. If Y2 also matches (see Y2), the word will be accepted by the Receiver 2. If SDENB2 = "0" this bit becomes a don't care.
BD11	Y2	If SDENB2 = "1" then this bit is compared with ARINC Data Bit #10. If X2 also matches (see X2), the word will be accepted by the Receiver 2. If SDENB2 = "0" this bit becomes a don't care.
BD12	PARCK	Signal used to invert the transmitter parity bit for test of parity circuits. Logic "0" selects normal odd parity. Logic "I" selects even parity.
BD13	TXSEL	Selects high or low Transmitter data rate. If TXSEL = "0" then transmitter data rate is equal to the clock rate divided by ten (10). If TXSEL = "1" then transmitter data rate is equal to the clock rate divided by eighty (80).
BD14	RCVSEL	Selects high or low Receiver data rate. If RCVSEL = "0" then the received data rate should be equal to the clock rate divided by ten (10), if RCVSEL = "1 "then the received data rate should be equal to the clock rate divided by eighty (80).
BD15	WLSEL	Selects word length. If WLSEL = "0" a 32-bit word format will be selected. If WLSEL = "1" a 25-Bit word format will be selected.

ARINC 429 DATA FORMAT as input to the Receiver and output from the Transmitter is as follows:

TABLE 1. ARINC 429 32-BIT DATA FORMAT

ARINC BIT #	FUNCTION
1 - 8	Label
9 - 10	SDI or Data
11	LSB
12 - 27	Data
28	MSB
29	Sign
30, 31	SSM
32	Parity Status

This format is shuffled when seen on the sixteen bidirectional input/outputs. The format shown below is used from the receivers and input to the transmitter:

TABLE 2A. WORD 1 FORMAT

BI-DIRECTIONAL BIT #	FUNCTION	ARINC BIT #
15, 14	Data	13, 12
13	LSB	11
12, 11	SDI or Data	10, 9
10, 9	SSM Status	31, 30
8	Parity Status	32
7 - 00	Label	1 - 8

TABLE 2B. WORD 2 FORMAT

BI-DIRECTIONAL BIT#	FUNCTION	ARINC BIT#
15	Sign	29
14	MSB	28
13 - 00	Data	27 - 14

Receiver Parity Status:

0 = Odd Parity

1 = Even Parity

If the receiver input data word string is broken before the entire data word is received, the receiver will reset and ignore the partially received data word.

If the transmitter is used to transmit consecutive data words, each word will be separated by a four (4) bit "null" state (both positive and negative outputs will maintain a zero (0) volt level.)

TABLE 3. ARINC 25-BIT DATA FORMAT

ARINC BIT #	FUNCTION
1 - 8	Label
9	LSB
11 - 23	Data
24	MSB
25	Parity Status

TABLE 4A. WORD 1 FORMAT

BI-DIRECTIONAL BIT#	FUNCTION	ARINC BIT#
15 - 9	Don't Care	XXX
8	Parity Status	25
7 - 0	Label	1 - 8

TABLE 4B. WORD 2 FORMAT

BI-DIRECTIONAL BIT#	FUNCTION	ARINC BIT#
15	MSB	24
14 - 1	Data	23 -10
0	LSB	9

Receiver Parity Status:

0 = Odd Parity

1 = Even Parity

No Source/Destination (S/D) in 25-Bit format.

Receiver Operation

Since the two receivers are functionally identical, only one will be discussed in detail, and the block diagram will be used for reference in this discussion. The receiver consists of the following circuits:

- The **Line Receiver** functions as a voltage level translator. It transforms the 10 volt differential line voltage, ARINC 429 format, into 5 volt internal logic level.
- The output of the Line Receiver is one of two inputs to the **Self-Test Data Selector (SEL)**. The other input to the Data Selector is the Self-Test Signal from the Transmitter section.
- The incoming data, either Self-Test or ARINC 429, is double sampled by the **Word Gap Timer** to generate a Data Clock. The Receiver sample frequency (RCVCLK), 1MHz, or 125kHz, is generated by the Receiver/Transmitter Timing Circuit. This sampling frequency is ten times the Data Rate to ensure no data ambiguity.
- The derived data clock then shifts the data down a 32-Bit long **Data Shift Register** (Data S/RI). The Data Word Length is selectable for either 25 Bits or 32 Bits long by the Control Signal (WLSEL). As soon as the data word is completely received, an internal signal (WDCNT1) is generated by the Word Gap Timer Circuit.
- The Source/Destination (S/D) Decoder compares the user set code (X and Y) with Bits 9 and 10 of the Data Word. If the two codes are matched, a positive signal is generated to enable the WDCNT1 signal to latch in the received data. Otherwise, the data word is ignored and no latching action takes place. The S/D Decoder can be Enabled and Disabled by the control signal S/D ENB. If the data word is latched, an indicator flag ($\overline{D/R1}$) is set. This indicates a valid data word is ready to be fetched by the user.
- After the receiver data has been shifted down the shift register, it is placed in a holding register. The device ready flag will then be set indicating that data is ready to be fetched. If the data is ignored and left in the holding register, it will be written over when the next data word is received.
- The received data in the 32-bit holding register is placed on the bus in the form of two (2)16-bit words regardless of whether the format is for 32 or 25-bit data words. Either word can be accessed first or repeatedly until the next received data word falls into the holding register.
- The parity of the incoming word is checked and the status (i.e., logic "0" for odd parity and logic "1" for even parity) stored in the receiver latch and output on BD08 during the Word No. 1.
- Assuming the user desires to access the data, he first sets the Data Select Line (SEL) to a Logic "0" level and pulses the Enable ($\overline{EN1}$) line. This action causes the Data Selector (SELI) to select the first-data word, which contains the label field and Enable it onto the Data Bus. To obtain the second data word, the user sets the SEL line to a Logic "1" level and pulse the Enable ($\overline{EN1}$) line again. The Enable pulse duration is matched to the user circuit requirement needed to read the Data Word from the Data Bus. The second Enable pulse is also used to reset the Device Ready ($\overline{D/R1}$) flip-flop. This completes a receiving cycle.

Transmitter Operation

The Transmitter section consists of an 8-word deep by 31-Bit long FIFO Memory, Parity Generator, Transmitter Word Gap Timing Circuit and Driver Circuit.

- The FIFO Memory is organized in such a way that data loaded in the input register is automatically transferred to the output register for Serial Data Transmission. This eliminates a large amount of data managing time since the data need not be clocked from the input register to the output register. The FIFO input register is made up of two sets of 16 D-type flip-flops, which are clocked by the two parallel load signals ($\overline{PL1}$ and $\overline{PL2}$). $\overline{PL1}$ must always precede $\overline{PL2}$. Multiple $\overline{PL1}$'s may occur and data will be written over. As soon as $\overline{PL2}$ is received, data is transferred to the FIFO. The data from the Data Bus is clocked into the D-type flip-flop on the positive going edge of the PL signals. If the FIFO memory is initially empty, or the stack is not full, the data will be automatically transferred down the Memory Stack and into the output register or to the last empty FIFO storage register. If the Transmitter Enable signal (ENTX) is not active, a Logic "0", the data remains at the output register. The FIFO Memory has storage locations to hold eight 31-bit words. If the memory is full and the new data is again strobed with $\overline{PL}$, the old data at the input register is written over by the new data. Data will remain in the Memory until ENTX goes to a Logic "1". This activates the FIFO Clock and data is shifted out serially to the Transmitter Driver. Data may be loaded into the FIFO only while ENTX is inactive (low). It is not possible to write data into the FIFO while transmitting. WARNING: If $\overline{PL1}$ or $\overline{PL2}$ is applied while ENTX is high, i.e., while transmitting, the FIFO may be disrupted such that it would require a $\overline{MR}$ (Master Reset) signal to recover.
- The Output Register of the FIFO is designed such that it can shift out a word of 24 Bits long or 31 Bits long. This word length is again controlled by the WLSEL bit. The TX word Gap Timer Circuit also automatically inserts a gap equivalent to 4-Bit Times between each word. This gives a minimum requirement of 29-Bit time or 36-Bit time for each word transmission. Assuming the signal, ENTX, remains at a Logic "1", a transfer to stack signal is generated to transfer the data down the Memory Stack one position. This action is continued until the last word is shifted out of the FIFO memory. At this time a Transmitter Ready (TX/R) flag is generated to signal the user that the Transmitter is ready to receive eight more data words. During transmission, if ENTX is taken low then high again, transmission will cease leaving a portion of the word untransmitted, and the data integrity of the FIFO will be destroyed.
- A Bit Counter is used to detect the last Bit shifted out of the FIFO memory and appends the Parity Bit generated by the Parity Generator. The Parity Generator has a control signal, Parity Check (PARCK), which establishes whether odd or even parity is used in the output data word. PARCK set to a logic "0" will result in odd parity and when set to a logic "1" will result in even parity.

Sample Interface Technique

From Figure 1, one can see that the Data Bus is time shared between the Receiver and Transmitter. Therefore, bus controlling must be synchronously shared between the Receiver and the Transmitter.

Figure 2 shows the typical interface timing control of the ARINC Chip for Receiving function and for Transmitting function. Timing sequence for loading the Transmitter FIFO Memory is shown in Timing Interval A. A transmitter Ready (TX/R) Flag signals the user that the Transmitter Memory is empty. The user then Enables the Transmitter Data, a 16-Bit word, on the Data Bus and strobes the Transmitter with a Parallel Load ($\overline{PL1}$) Signal. The second part of the 32-Bit word is similarly loaded into the Transmitter with $\overline{PL2}$, which also initiates data transfer to stack. This is continuous until the Memory is full, which is eight 31-Bit words. The user must keep track of the number of words loaded into the Memory to ensure no data is written over by other data. During the time the user is loading the Transmitter, he does not have to service the Receiver, even if the Receiver flags the user with the signal $\overline{D/R1}$ that a valid received word is ready to be fetched. This is shown by the Timing interval B. If the user decides to obtain the received data before the Transmitter is completely loaded, he sets the two parallel load signals ($\overline{PL1}$ and $\overline{PL2}$) at a Logic "1" state, and strobes $\overline{EN1}$ while the signal SEL is at a Logic "0" state. After the negative edge of $\overline{EN1}$, the first 16-Bit segment of the received word becomes valid on the Data Bus. At the positive edge of $\overline{EN1}$, the user should toggle the signal SEL to ready the Receiver for the second 16-Bit word. Strobing the Receiver with $\overline{EN1}$, the second time, enables the second 16-Bit word and resets the Receiver Ready Flag $\overline{D/R1}$. The user should now reset the signal SEL to a Logic "0" state to ready the Receiver for another Read Cycle. During the time period that the user is fetching the received words, he can load the transmitter. This is done by interlacing the $\overline{PL}$ signals with the $\overline{EN}$ signals as shown in the Timing Interval B. Servicing the Receiver 2 is similar and is illustrated by Timing interval C. Timing interval D shows the rest of the Transmitter loading sequence and the beginning of the transmission by switching the signal TX Enable to a Logic "1" state. Timing interval E is the time it takes to transmit all data from the FIFO Memory, either 288 Bit times or 232 Bit times.

Repeater Operation

This mode of operation allows a data word that has been received to be placed directly in the FIFO for transmission. A timing diagram is shown in Figure 7. A 32-bit word is used in this example. The data word is shifted into the shift register and the $\overline{D/R}$ flag goes low. A logic "0" is placed on the SEL line and $\overline{EN1}$ is strobed. This is the same as the normal receiver operation and places half the data word (16 bits) on the data bus. By strobing $\overline{PL1}$ at the same time as $\overline{EN1}$, these 16 bits will be taken off the bus and placed in the FIFO. SEL is brought back high and $\overline{EN1}$ is strobed again for the second 16 bits of the data word. Again by strobing $\overline{PL2}$ at the same time the second 16 bits will be placed in the FIFO. The parity bit will have been stripped away leaving the 31-bit data word in the FIFO ready for transmission as shown in Figure 6.

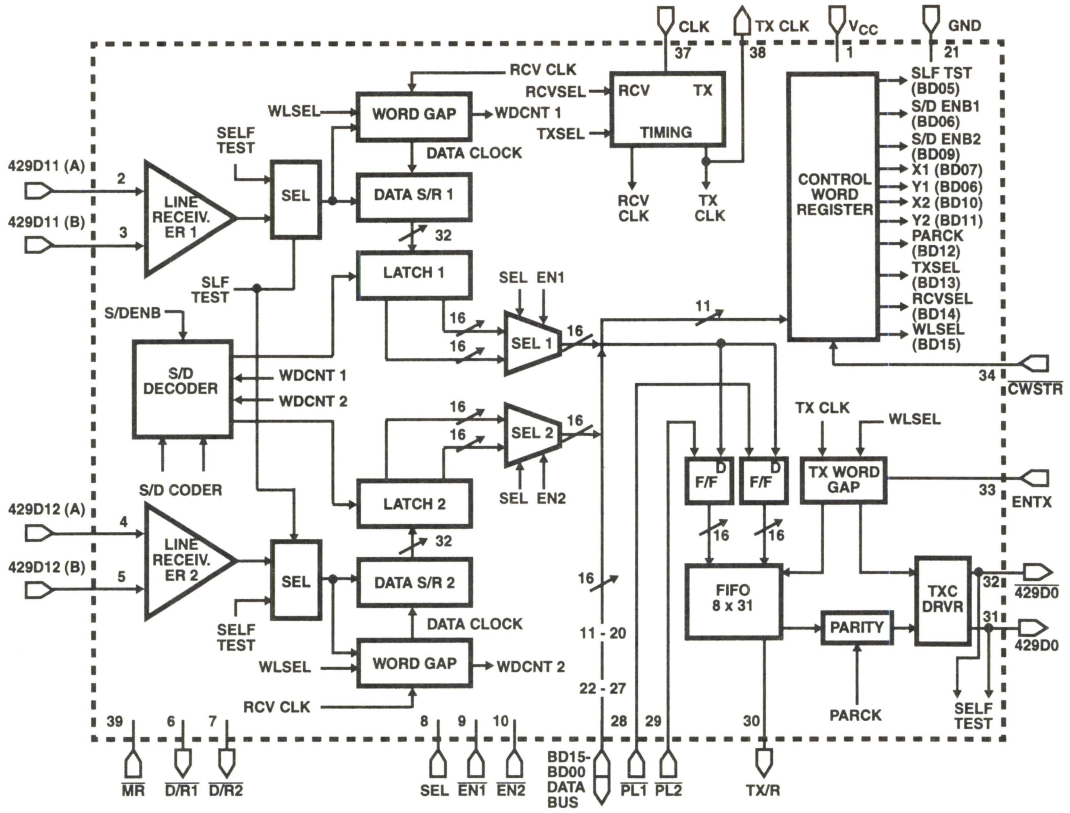


FIGURE 1. SINGLE CHIP ARINC 429 INTERFACE FUNCTIONAL BLOCK DIAGRAM

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage Applied
(Except Pins 2 - 5) . . . . . GND -0.3V to V_{DD} +0.3V
Input Voltage Applied (Pins 2 - 5) . . . . . -29V to +29V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.75V to +5.25V
Operating Temperature Range
HS-3282-5. . . . . 0^oC to $+70^oC$
HS-3282-8. . . . . -55^oC to $+125^oC$

Thermal Information

Thermal Resistance	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CDIP Package	35	8
CLCC Package	55	12

Maximum Junction Temperature . . . . . $+175^oC$
Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 2632 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Performance Specifications

V_{DD} = 5V ±5%, T_A = 0^oC to $+70^oC$ (HS-3282-5),
T_A = -55^oC to $+125^oC$ (HS-3282-8)

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
ARINC INPUTS Pins 2-3,4-5					
Logic "1" Input Voltage	V_{IH}	V_{DD} = 5.25V	6.7	13.0	V
Logic "0" Input Voltage	V_{IL}	V_{DD} = 5.25V	-13.0	-6.7	V
Null Input Voltage	V_{NUL}	V_{DD} = 4.75V, 5.25V	-2.5	+2.5	V
Common Mode Voltage	V_{CH}	V_{DD} = 4.75V, 5.25V	-5.0	+5.0	V
Input Leakage	I_{IH}	V_{DD} = 5.25V, V_{IN} = ±6.5V	-	200	µA
Input Leakage	I_{IL}	V_{DD} = 5.25V, V_{IN} = 0.0V	-450	-	µA
Differential Input Impedance	RI	V_{DD} = 5.25V, V_{IN} = +5V, -5V	12	-	kΩ
Input Impedance to V_{DD}	RH	V_{DD} = 5.25V, V_{IN} = 0V	12	-	kΩ
Input Impedance to GND	RG	V_{DD} = Open, V_{IN} = 5.0V	12	-	kΩ
BIDIRECTIONAL INPUTS Pins 11-20, 22-27					
Logic "1" Input Voltage	V_{IH}	V_{DD} = 5.25V	2.1	-	V
Logic "0" Input Voltage	V_{IL}	V_{DD} = 4.75V	-	0.7	V
Input Leakage	I_{IH}	V_{DD} = 5.25V,V_{IN} = 5.25V	-	1.5	µA
Input Leakage	I_{IL}	V_{DD} = 5.25V, V_{IN} = 0.0V	-1.5	-	µA
ALL OTHER INPUTS Pins 8-10, 28, 29, 33, 34, 37, 39					
Logic "1" Input Voltage	V_{IH}	V_{DD} = 5.25V	3.5	-	V
Logic "0" Input Voltage	V_{IL}	V_{DD} = 4.75V	-	0.7	V
Input Leakage	I_{IH}	V_{DD} = 5.25V, V_{IN} = 5.25V	-	10	µA
Input Leakage	I_{IL}	V_{DD} = 5.25V, V_{IN} = 0.0V	-75	-	µA
OUTPUTS Pins 6, 7, 11-20, 22-27, 30-32, 38, Supply Pin 1					
Logic "1" Output Voltage	V_{OH}	V_{DD} = 4.75V, I_{OH} = -1.5mA	2.7	-	V
Logic "0" Output Voltage	V_{OL}	V_{DD} = 4.75V I_{OL}= 1.8mA	-	0.4	V
Standby Supply Current	I_{CC1}	V_{DD} = 5.25V, V_{IN} = 0V Except 9,10, 29 = 5.25V	-	20	mA
Operating Supply Current	I_{CC2}	V_{DD} = 5.25V, V_{IN} = 5.25V Except 8, 33 = 0.0V, CLK = 1MHz	-	20	mA

AC Electrical Performance Specifications V_{DD} = 5V ±5%, T_A = 0°C to +70°C (HS-3282-5), T_A = -55°C to +125°C (HS-3282-8)

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Clock Frequency	FC	V_{DD} = 4.75V, 5.25V	-	1	MHz
Data Rate 1/	FD	V_{DD} = 4.75V, 5.25V	-	100	kHz
Data Rate 2/	FD	V_{DD} = 4.75V, 5.25V	-	12.5	kHz
Master Reset Pulse Width	TMR	V_{DD} = 4.75V, 5.25V	200	-	ns
RECEIVER TIMING					
Receiver Ready Time From 32nd Bit 1/	TD/R2	V_{DD} = 4.75V, 5.25V	-	16	µs
Receiver Ready Time From 32nd Bit 2/	TD/R2	V_{DD} = 4.75V, 5.25V	-	128	µs
Device Ready to Enable Time	TD/REN	V_{DD} = 4.75V, 5.25V	0	-	ns
Data Enable Pulse Width	TEN	V_{DD} = 4.75V, 5.25V	200	-	ns
Data Enable to Data Enable Time	TENEN	V_{DD} = 4.75V, 5.25V	50	-	ns
Data Enable to Device Ready Reset Time	TEND/R	V_{DD} = 4.75V, 5.25V	-	200	ns
Output Data Valid to Enable Time	TENDATA	V_{DD} = 4.75V, 5.25V	-	200	ns
Data Enable to Data Select Time	TENSEL	V_{DD} = 4.75V, 5.25V	20	-	ns
Data Select to Data Enable Time	TSELEN	V_{DD} = 4.75V, 5.25V	20	-	ns
Output Data Disable Time	TDATAEN	V_{DD} = 4.75V, 5.25V	-	80	ns
CONTROL WORD TIMING					
Control Word Strobe Pulse Width	TCWSTR	V_{DD} = 4.75V, 5.25V	130	-	ns
Control Word Setup Time	TCWSET	V_{DD} = 4.75V, 5.25V	130	-	ns
Control Word Hold Time	TCWHLD	V_{DD} = 4.75V, 5.25V	0	-	ns
TRANSMITTER FIFO Write Timing					
Parallel Load Pulse Width	TPL	V_{DD} = 4.75V, 5.25V	200	-	ns
Parallel Load to Parallel Load 2 Delay	TPL12	V_{DD} = 4.75V, 5.25V	0	-	ns
Transmitter Ready Delay Time	TTX/R	V_{DD} = 4.75V, 5.25V	-	840	ns
Data Word Setup Time	TDWSET	V_{DD} = 4.75V, 5.25V	110	-	ns
Data Word Hold Time	TDWHLD	V_{DD} = 4.75V, 5.25V	0	-	ns
TRANSMITTER Output Timing					
Enable Transmit to Output Data Valid Time 1/	TENDAT	V_{DD} = 4.75V, 5.25V	-	25	µs
Enable Transmit to Output Data Valid Time 2/	TENDAT	V_{DD} = 4.75V, 5.25V	-	200	µs
Output Data Bit Time 1/	TBIT	V_{DD} = 4.75V, 5.25V	4.95	5.05	µs
Output Data Bit Time 2/	TBIT	V_{DD} = 4.75V, 5.25V	39.6	40.4	µs
Output Data Null Time 1/	TNULL	V_{DD} = 4.75V, 5.25V	4.95	5.05	µs
Output Data Null Time 2/	TNULL	V_{DD} = 4.75V, 5.25V	39.6	40.4	µs

AC Electrical Performance Specifications V_{DD} = 5V ±5%, T_A = 0°C to +70°C (HS-3282-5), T_A = -55°C to +125°C (HS-3282-8) **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Data Word Gap Time 1/	TGAP	V_{DD} = 4.75V, 5.25V	39.6	40.4	µs
Data Word Gap Time 2/	TGAP	V_{DD} = 4.75V, 5.25V	316.8	323.2	µs
Data Transmission Word to TX/R Set Time	TDTX/R	V_{DD} = 4.75V, 5.25V	-	400	ns
Enable Transmit Turnoff Time	TENTX/R	V_{DD} = 4.75V, 5.25V	0	-	ns
REPEATER OPERATION TIMING					
Data Enable to Parallel Load Delay Time	TENPL	V_{DD} = 4.75V, 5.25V	0	-	ns
Data Enable Hold for Parallel Load Time	TPLEN	V_{DD} = 4.75V, 5.25V	0	-	ns
Enable Transmit Delay Time	TTX/REN	V_{DD} = 4.75V, 5.25V	0	-	ns

NOTES:

1. 100kHz Data Rate.
2. 12.5kHz Data Rate.

Electrical Performance Specifications V_{DD} = 5V ±5%, T_A = 0°C to +70°C (HS-3282-5), T_A = -55°C to +125°C (HS-3282-8)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Differential Input Capacitance	CD	V_{DD} = Open, f = 1MHz, Note 2, 3	-	20	pF
Input Capacitance to V_{DD}	CH	V_{DD} = GND, f = 1MHz, Note 2, 3	-	20	pF
Input Capacitance to GND	CG	V_{DD} = Open, f = 1MHz, Note 2, 3	-	20	pF
Input Capacitance	CI	V_{DD} = Open, f = 1MHz, Note 2, 4	-	15	pF
Output Capacitance	CO	V_{DD} = Open, f = 1MHz, Note 2, 5	-	15	pF
Clock Rise Time	TLHC	CLK = 1MHz, From 0.7V to 3.5V	-	10	ns
Clock Fall Time	THLC	CLK = 1MHz, From 3.5V to 0.7V	-	10	ns
Input Rise Time	TLHI	From 0.7V to 3.5V, Note 6	-	15	ns
Input Fall Time	THLI	From 3.5V to 0.7V, Note 6	-	15	ns

NOTES:

1. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes affecting these parameters.
2. All measurements are referenced to device GND.
3. Pins 2-3, 4-5.
4. Pins 8-10, 28, 29, 33, 34, 37, 39.
5. Pins 6, 7, 11-20, 22-27, 30-32, 38.
6. Pins 8-20, 22-29, 33, 34.

Timing Waveforms

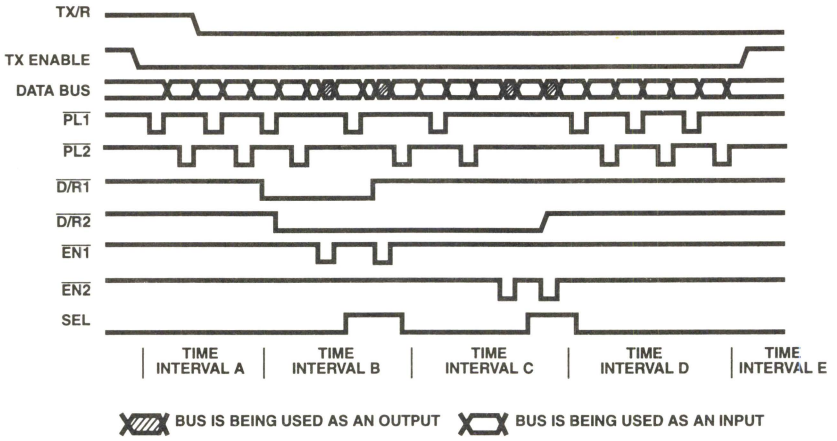


FIGURE 2. TYPICAL INTERFACE TIMING SEQUENCE

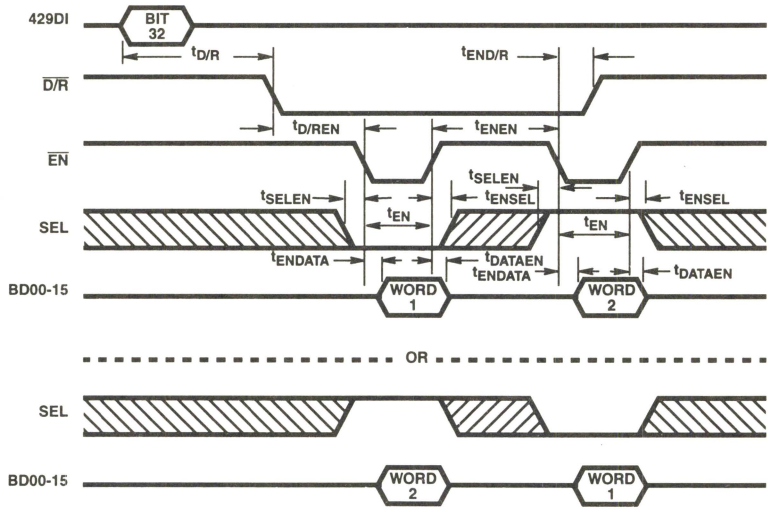


FIGURE 3. RECEIVER TIMING

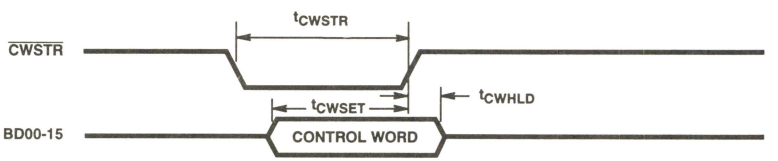


FIGURE 4. CONTROL WORD TIMING

Timing Waveforms (Continued)

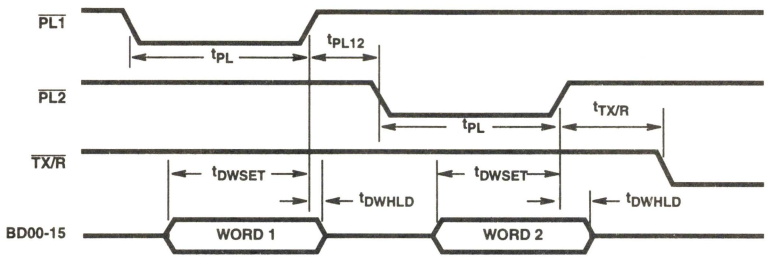


FIGURE 5. TRANSMITTER FIFO WRITE TIMING

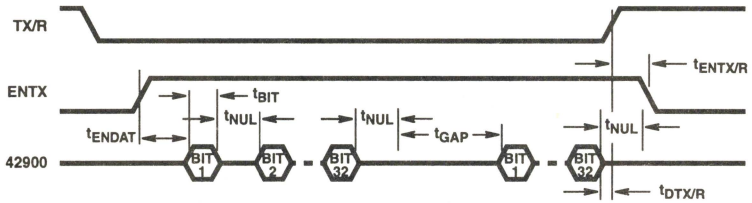


FIGURE 6. TRANSMITTER OUTPUT TIMING

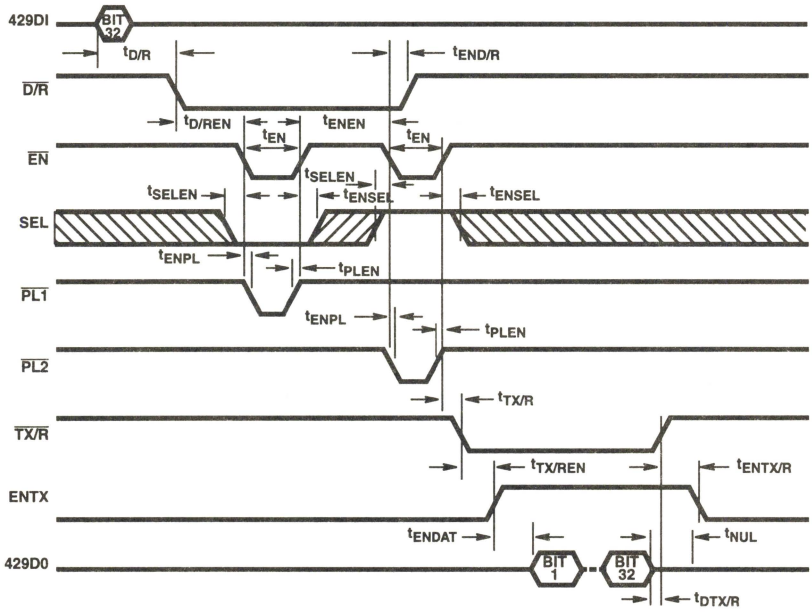
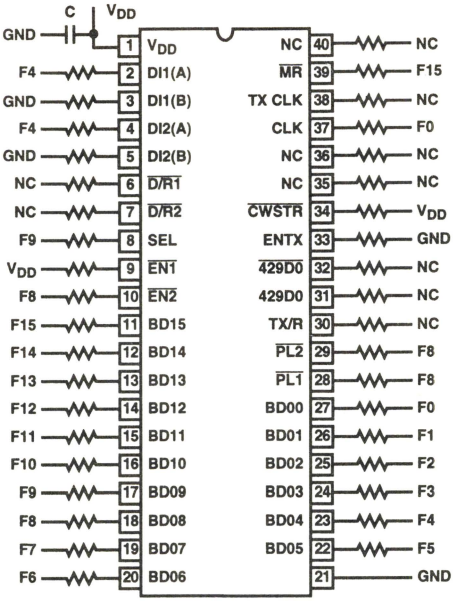


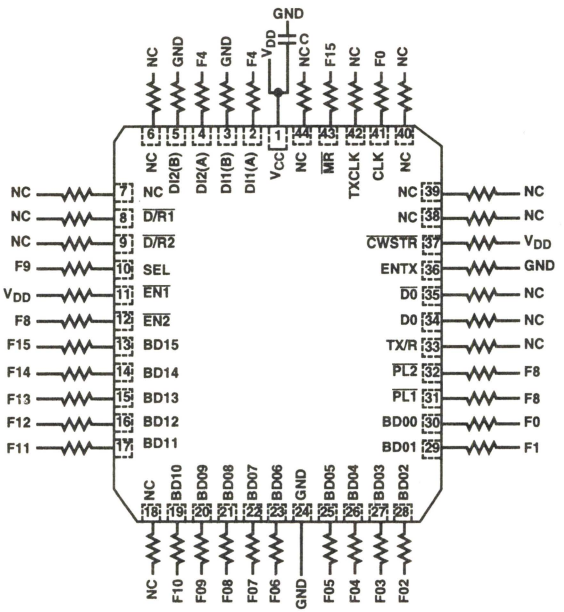
FIGURE 7. REPEATER OPERATION TIMING

Burn-In Circuits

HS-3282 CERDIP



HS-3282 CLCC


GND
VDD
C
NC
GND
F4
GND
F4
NC
F15
NC
F0
NC
1 VCC
2 DI1(A)
3 DI1(B)
4 DI2(A)
5 DI2(B)
6 NC
7 NC
8 D/R1
9 D/R2
10 SEL
11 EN1
12 EN2
13 BD15
14 BD14
15 BD13
16 BD12
17 BD11
18 NC
19 BD10
20 BD09
21 BD08
22 BD07
23 BD06
24 GND
25 BD05
26 BD04
27 BD03
28 BD02
41 CLK
42 TXCLK
43 MR
44 NC
39 NC
38 NC
37 CWSTR
36 ENTX
35 D0
34 D0
33 TX/R
32 PL2
31 PL1
30 BD00
29 BD01
F9
F10
F11
F12
F13
F14
F15
F8
F7
F6
F5
F4
F3
F2
F1
F0
F8
F8
VDD
GND
NC
NC
NC

Die Characteristics

DIE DIMENSIONS:
246 x 224 x 19 mils)
(6250 x 5700 x 483µm)

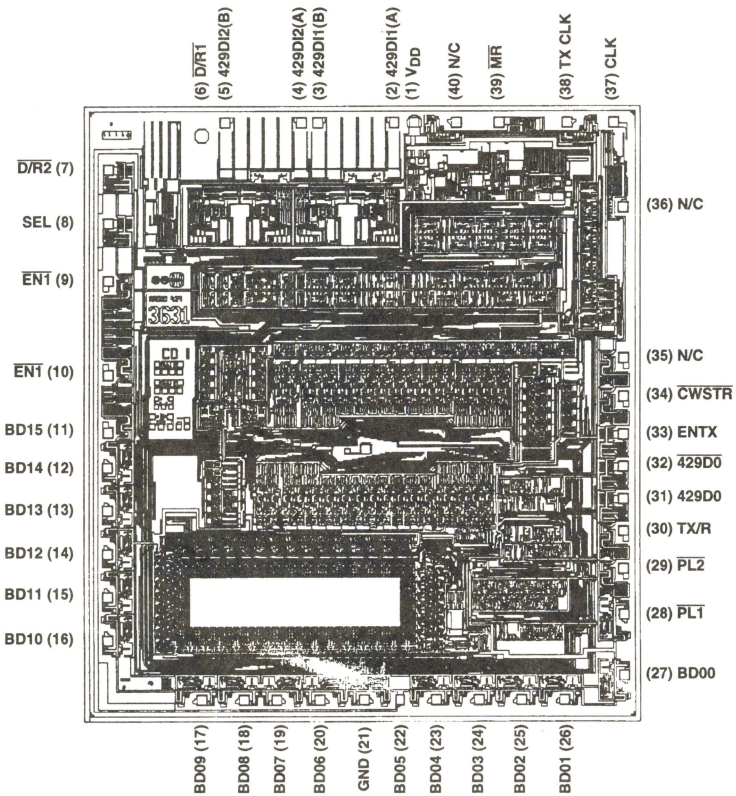
METALLIZATION:
Type: Si-Al
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kA ±1kÅ

WORST CASE CURRENT DENSITY:
2×10^5 A/cm^2

Metallization Mask Layout

HS-3282



HARRIS SEMICONDUCTOR

ICL232

March 1997

+5V Powered Dual RS-232 Transmitter/Receiver

Features

- Meets All RS-232C and V.28Specifications
- Requires Only Single +5V Power Supply
- Onboard Voltage Doubler/Inverter
- Low Power Consumption
- 2 Drivers
  - ±9V Output Swing for +5V Input
  - 300Ω Power-off Source Impedance
  - Output Current Limiting
  - TTL/CMOS Compatible
  - 30V/μs Maximum Slew Rate
- 2 Receivers
  - ±30V Input Voltage Range
  - 3kΩ to 7kΩ Input Impedance
  - 0.5V Hysteresis to Improve Noise Rejection
- All Critical Parameters are Guaranteed Over the Entire Commercial, Industrial and Military Temperature Ranges

Applications

- Any System Requiring RS-232 Communications Port
  - Computer - Portable and Mainframe
  - Peripheral - Printers and Terminals
  - Portable Instrumentation
  - Modems
- Dataloggers

Description

The ICL232 is a dual RS-232 transmitter/receiver interface circuit that meets all EIA RS-232C and V.28 specifications. It requires a single +5V power supply, and features two onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply.

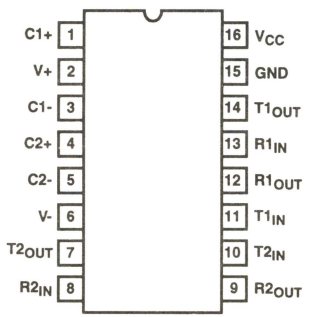
The drivers feature true TTL/CMOS input compatibility, slew-rate-limited output, and 300Ω power-off source impedance. The receivers can handle up to +30V, and have a 3kΩ to 7kΩ input impedance. The receivers also have hysteresis to improve noise rejection.

Ordering Information

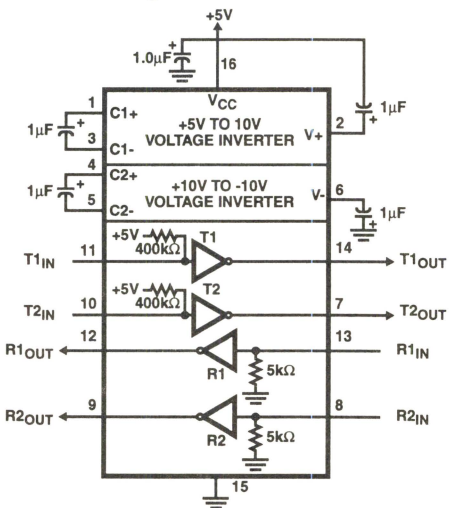
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICL232CPE	0 to 70	16 Ld PDIP	E16.3
ICL232CJE	0 to 70	16 Ld CerDIP	F16.3
ICL232CBE	0 to 70	16 Ld SOIC (W)	M16.3
ICL232IPE	-40 to 85	16 Ld PDIP	E16.3
ICL232IJE	-40 to 85	16 Ld CerDIP	F16.3
ICL232IBE	-40 to 85	16 Ld SOIC (W)	M16.3
ICL232MJE	-55 to 125	16 Ld CerDIP	F16.3

Pinout

ICL232 (PDIP, CERDIP, SOIC)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Copyright © Harris Corporation 1997

File Number **3020.4**

Absolute Maximum Ratings

V_{CC} to Ground . . . . . (GND -0.3V) < V_{CC} < 6V
V+ to Ground . . . . . (V_{CC} -0.3V) < V+ < 12V
V- to Ground . . . . . -12V < V- < (GND +0.3V)
Input Voltages
$T1_{IN}$, $T2_{IN}$ . . . . . (V- -0.3V) < V_{IN} < (V+ +0.3V)
$R1_{IN}$, $R2_{IN}$ . . . . . ±30V
Output Voltages
$T1_{OUT}$, $T2_{OUT}$ . . . . . (V- -0.3V) < V_{TXOUT} < (V+ +0.3V)
$R1_{OUT}$, $R2_{OUT}$ . . . . . (GND -0.3V) < V_{RXOUT} < (V_{CC} +0.3V)
Short Circuit Duration
$T1_{OUT}$, $T2_{OUT}$ . . . . . Continuous
$R1_{OUT}$, $R2_{OUT}$ . . . . . Continuous
Storage Temperature Range . . . . . -65°C to 150°C
Lead Temperature (Soldering 10s) . . . . . 300°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CerDIP Package	80	18
PDIP Package	100	N/A
SOIC Package	100	N/A

Maximum Junction Temperature
Plastic Package . . . . . 150°C
Ceramic Package . . . . . 175°C
Operating Temperature Range
ICL232C . . . . . 0°C to 70°C
ICL232I . . . . . -40°C to 85°C
ICL232M . . . . . -55°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Test Conditions: V_{CC} = +5V ±10%, T_A = Operating Temperature Range. Test Circuit as in Figure 8 Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Transmitter Output Voltage Swing, T_{OUT}	$T1_{OUT}$ and $T2_{OUT}$ loaded with 3kΩ to Ground	±5	±9	±10	V
Power Supply Current, I_{CC}	Outputs Unloaded, T_A = 25°C	-	5	10	mA
T_{IN}, Input Logic Low, V_{IL}		-	-	0.8	V
T_{IN}, Input Logic High, V_{IH}		2.0	-	-	V
Logic Pullup Current, I_P	$T1_{IN}$, $T2_{IN}$ = 0V	-	15	200	µA
RS-232 Input Voltage Range, V_{IN}		-30	-	+30	V
Receiver Input Impedance, R_{IN}	V_{IN} = ±3V	3.0	5.0	7.0	kΩ
Receiver Input Low Threshold, V_{IN} (H-L)	V_{CC} = 5V, T_A = 25°C	0.8	1.2	-	V
Receiver Input High Threshold, V_{IN} (L-H)	V_{CC} = 5V, T_A = 25°C	-	1.7	2.4	V
Receiver Input Hysteresis, V_{HYST}		0.2	0.5	1.0	V
TTL/CMOS Receiver Output Voltage Low, V_{OL}	I_{OUT} = 3.2mA	-	0.1	0.4	V
TTL/CMOS Receiver Output Voltage High, V_{OH}	I_{OUT} = -1.0mA	3.5	4.6	-	V
Propagation Delay, t_{PD}	RS-232 to TTL	-	0.5	-	µs
Instantaneous Slew Rate, SR	C_L = 10pF, R_L = 3kΩ, T_A = 25°C (Notes 1, 2)	-	-	30	V/µs
Transition Region Slew Rate, SR_T	R_L = 3kΩ, C_L = 2500pF Measured from +3V to -3V or -3V to +3V	-	3	-	V/µs
Output Resistance, R_{OUT}	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V	300	-	-	Ω
RS-232 Output Short Circuit Current, I_{SC}	$T1_{OUT}$ or $T2_{OUT}$ shorted to GND	-	±10	-	mA

NOTES:

1. Guaranteed by design.
2. See Figure 4 for definition.

Test Circuits

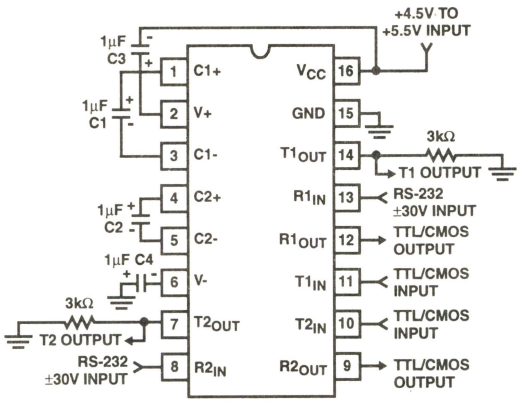


FIGURE 1. GENERAL TEST CIRCUIT

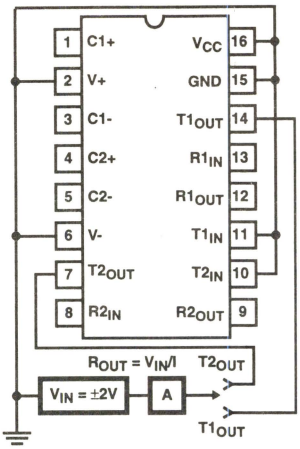


FIGURE 2. POWER-OFF SOURCE RESISTANCE CONFIGURATION

Typical Performance Curves

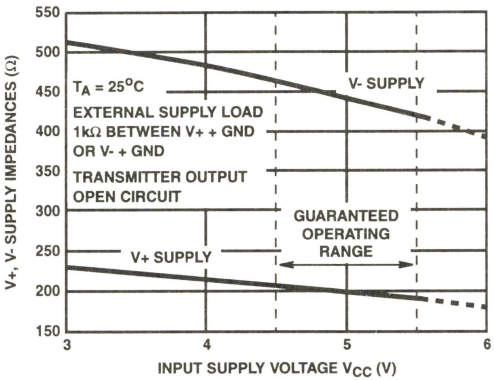


FIGURE 3. V+, V- OUTPUT IMPEDANCES vs V_{CC}

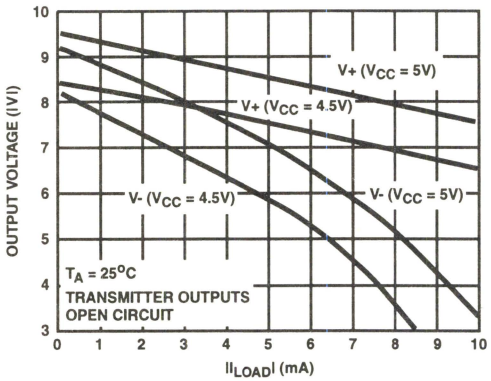


FIGURE 4. V+, V- OUTPUT VOLTAGES vs LOAD CURRENT

Pin Descriptions

PDIP, CERDIP	SOIC	PIN NAME	DESCRIPTION
1	1	C1+	External capacitor "+" for internal voltage doubler.
2	2	V+	Internally generated +10V (typical) supply.
3	3	C1-	External capacitor "-" for internal voltage doubler.
4	4	C2+	External capacitor "+" internal voltage inverter.
5	5	C2-	External capacitor "-" internal voltage inverter.
6	6	V-	Internally generated -10V (typical) supply.
7	7	$T2_{OUT}$	RS-232 Transmitter 2 output ±10V (Typical).
8	8	$R2_{IN}$	RS-232 Receiver 2 input, with internal 5K pulldown resistor to GND.
9	9	R2out	Receiver 2 TTL/CMOS output.
10	10	$T2_{IN}$	Transmitter 2 TTL/CMOS input, with internal 400K pullup resistor to V_{CC}.
11	11	$T1_{IN}$	Transmitter 1 TTL/CMOS input, with internal 400K pullup resistor to V_{CC}.

Pin Descriptions (Continued)

PDIP, CERDIP	SOIC	PIN NAME	DESCRIPTION
12	12	$R1_{OUT}$	Receiver 1 TTL/CMOS output.
13	13	$R1_{IN}$	RS-232 Receiver 1 input, with internal 5K pulldown resistor to GND.
14	14	$T1_{OUT}$	RS-232 Transmitter 1 output ±10V (Typical).
15	15	GND	Supply Ground.
16	16	V_{CC}	Positive Power Supply +5V ±10%

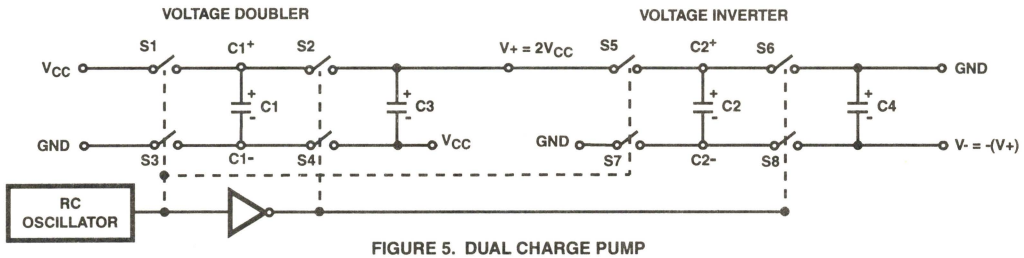


FIGURE 5. DUAL CHARGE PUMP

Detailed Description

The ICL232 is a dual RS-232 transmitter/receiver powered by a single +5V power supply which meets all EIA RS232C specifications and features low power consumption. The functional diagram illustrates the major elements of the ICL232. The circuit is divided into three sections: a voltage doubler/inverter, dual transmitters, and dual receiversVoltage Converter.

An equivalent circuit of the dual charge pump is illustrated in Figure 5.

The voltage quadrupler contains two charge pumps which use two phases of an internally generated clock to generate +10V and -10V. The nominal clock frequency is 16kHz. During phase one of the clock, capacitor C1 is charged to V_{CC}. During phase two, the voltage on C1 is added to V_{CC}, producing a signal across C2 equal to twice V_{CC}. At the same time, C3 is also charged to $2V_{CC}$, and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The voltage converter accepts input voltages up to 5.5V. The output impedance of the doubler (V+) is approximately 200Ω, and the output impedance of the inverter (V-) is approximately 450Ω. Typical graphs are presented which show the voltage converters output vs input voltage and output voltages vs load characteristics. The test circuit (Figure 3) uses 1µF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, and increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V+ and V- supplies.

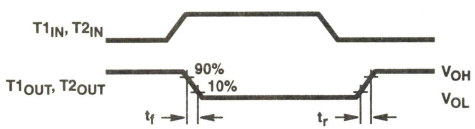


FIGURE 6. SLEW RATE DEFINITION

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC}, or 1.3V for V_{CC} = 5V. A logic 1 at the input results in a voltage of between -5V and V- at the output, and a logic 0 results in a voltage between +5V and (V+ - 0.6V). Each transmitter input has an internal 400kΩ pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specification of ±5V minimum with the worst case conditions of: both transmitters driving 3kΩ minimum load impedance, V_{CC} = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/µs. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300Ω with ±2V applied to the outputs and V_{CC} = 0V.

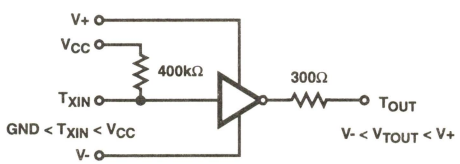


FIGURE 7. TRANSMITTER

Receivers

The receiver inputs accept up to ±30V while presenting the required 3kΩ to 7kΩ input impedance even it the power is off (V_{CC} = 0V). The receivers have a typical input threshold of 1.3V which is within the ±3V limits, known as the transition region, of the RS-232 specification. The receiver output is 0V to V_{CC}. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis to improve noise rejection.

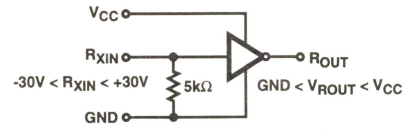
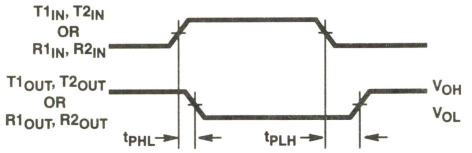


FIGURE 8. RECEIVER



$$\text{Average Propagation Delay} = \frac{t_{PHL} + t_{PLH}}{2}$$

FIGURE 9. PROPAGATION DELAY DEFINITION

Applications

The ICL232 may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where ±12V power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 10. Fixed output signals such as DTR (data terminal ready) and DSRS (data signaling rate select) is generated by driving them through a 5kΩ resistor connected to V+.

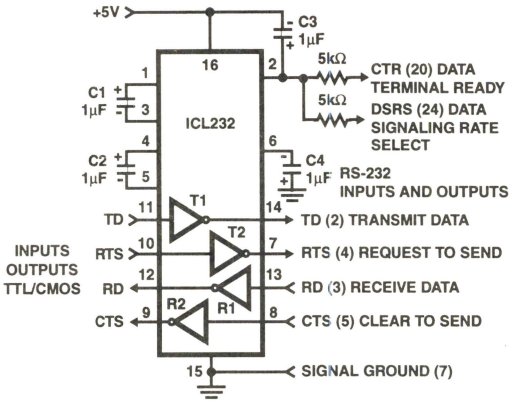


FIGURE 10. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

In applications requiring four RS-232 inputs and outputs (Figure 11), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

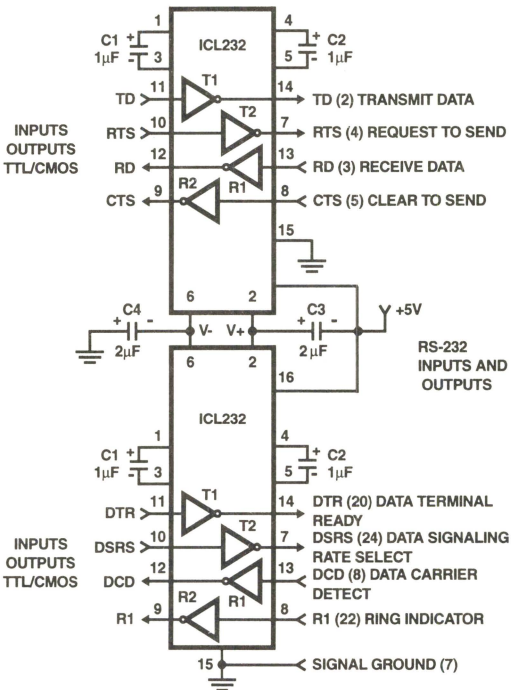


FIGURE 11. COMBINING TWO ICL232s FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS

HARRIS SEMICONDUCTOR HIN200 thru HIN213

+5V Powered RS-232 Transmitters/Receivers with 0.1Microfarad External Capacitors

March 1997

Features

- Meets All RS-232E and V.28 Specifications
- Requires Only 0.1μF or Greater External Capacitors
- 120kbit/s Data Rate
- Two Receivers Active in Shutdown Mode (HIN213)
- Requires Only Single +5V Power Supply
  - (+5V and +12V - HIN201 and HIN209)
- Onboard Voltage Doubler/Inverter
- Low Power Consumption (Typ) 5mA
- Low Power Shutdown Function (Typ) 1μA
- Three-State TTL/CMOS Receiver Outputs
- Multiple Drivers
  - ±10V Output Swing for +5V Input
  - 300Ω Power-Off Source Impedance
  - Output Current Limiting
  - TTL/CMOS Compatible
  - 30V/μs Maximum Slew Rate
- Multiple Receivers
  - ±30V Input Voltage Range
  - 3kΩ to 7kΩ Input Impedance
  - 0.5V Hysteresis to Improve Noise Rejection

Description

The HIN200-HIN213 family of RS-232 transmitters/receivers interface circuits meet all EIA RS-232E and V.28 specifications, and are particularly suited for those applications where ±12V is not available. They require a single +5V power supply (except HIN201 and HIN209) and feature onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply. The family of devices offers a wide variety of RS-232 transmitter/receiver combinations to accommodate various applications (see Selection Table).

The HIN200, HIN206, HIN211 and HIN213 feature a low power shutdown mode to conserve energy in battery powered applications. In addition, the HIN213 provides two active receivers in shutdown mode allowing for easy "wakeup" capability.

The drivers feature true TTL/CMOS input compatibility, slew rate-limited output, and 300Ω power-off source impedance. The receivers can handle up to ±30V input, and have a 3kΩ to 7kΩ input impedance. The receivers also feature hysteresis to greatly improve noise rejection.

Applications

- Any System Requiring RS-232 Communications Port
  - Computer - Portable, Mainframe, Laptop
  - Peripheral - Printers and Terminals
  - Portable Instrumentation
  - Modems

Selection Table

PART NUMBER	POWER SUPPLY VOLTAGE	NUMBER OF RS-232 DRIVERS	NUMBER OF RS-232 RECEIVERS	NUMBER OF 0.1μF EXTERNAL COMPONENTS	LOW POWER SHUTDOWN/TTL THREE-STATE	NUMBER OF RECEIVERS ACTIVE IN SHUTDOWN
HIN200	+5V	5	0	4 Capacitors	Yes/No	0
HIN201	+5V and +9V to 13.2V	2	2	2 Capacitors	No/No	0
HIN202	+5V	2	2	4 Capacitors	No/No	0
HIN204	+5V	4	0	4 Capacitors	No/No	0
HIN206	+5V	4	3	4 Capacitors	Yes/Yes	0
HIN207	+5V	5	3	4 Capacitors	No/No	0
HIN208	5V	4	4	4 Capacitors	No/No	0
HIN209	+5V and +9V to 13.2V	3	5	2 Capacitors	No/Yes	0
HIN211	+5V	4	5	4 Capacitors	Yes/Yes	0
HIN213	+5V	4	5	4 Capacitors	Yes/Yes	2

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Ordering Information

PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIN200CB	0 to 70	20 Ld SOIC (W)	M20.3
HIN200IB	-40 to 85	20 Ld SOIC (W)	M20.3
HIN201CB	0 to 70	16 Ld SOIC (W)	M16.3
HIN201IB	-40 to 85	16 Ld SOIC (W)	M16.3
HIN202CP	0 to 70	16 Ld PDIP	E16.3
HIN202CB	0 to 70	16 Ld SOIC (W)	M16.3
HIN202IP	-40 to 85	16 Ld PDIP	E16.3
HIN202CA	0 to 70	16 Ld SSOP	M16.209
HIN202IA	-40 to 85	16 Ld SSOP	M16.209
HIN202IB	-40 to 85	16 Ld SOIC (W)	M16.3
HIN202CBN	0 to 70	16 Ld SOIC (N)	M16.15
HIN202IBN	-40 to 85	16 Ld SOIC (N)	M16.15
HIN204CB	0 to 70	16 Ld SOIC (W)	M16.3
HIN204IB	-40 to 85	16 Ld SOIC (W)	M16.3
HIN206CP	0 to 70	24 Ld PDIP (N)	E24.3
HIN206CB	0 to 70	24 Ld SOIC (W)	M24.3
HIN206CA	0 to 70	24 Ld SSOP	M24.209
HIN206IP	-40 to 85	24 Ld PDIP (N)	E24.3
HIN206IB	-40 to 85	24 Ld SOIC (W)	M24.3
HIN206IA	-40 to 85	24 Ld SSOP	M24.209
HIN207CP	0 to 70	24 Ld PDIP (N)	E24.3
HIN207CB	0 to 70	24 Ld SOIC (W)	M24.3

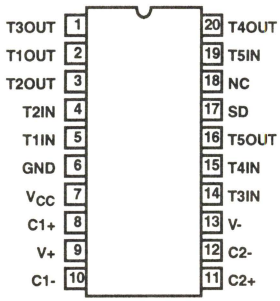
PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIN207CA	0 to 70	24 Ld SSOP	M24.209
HIN207IP	-40 to 85	24 Ld PDIP (N)	E24.3
HIN207IB	-40 to 85	24 Ld SOIC (W)	M24.3
HIN207IA	-40 to 85	24 Ld SSOP	M24.209
HIN208CP	0 to 70	24 Ld PDIP (N)	E24.3
HIN208CB	0 to 70	24 Ld SOIC (W)	M24.3
HIN208CA	0 to 70	24 Ld SSOP	M24.209
HIN208IP	-40 to 85	24 Ld PDIP (N)	E24.3
HIN208IB	-40 to 85	24 Ld SOIC (W)	M24.3
HIN208IA	-40 to 85	24 Ld SSOP	M24.209
HIN209CP	0 to 70	24 Ld PDIP (N)	E24.3
HIN209CB	0 to 70	24 Ld SOIC (W)	M24.3
HIN209IP	-40 to 85	24 Ld PDIP (N)	E24.3
HIN209IB	-40 to 85	24 Ld SOIC (W)	M24.3
HIN211CB	0 to 70	28 Ld SOIC (W)	M28.3
HIN211CA	0 to 70	28 Ld SSOP	M28.209
HIN211IB	-40 to 85	28 Ld SOIC (W)	M28.3
HIN211IA	-40 to 85	28 Ld SSOP	M28.209
HIN213CB	0 to 70	28 Ld SOIC (W)	M28.3
HIN213CA	0 to 70	28 Ld SSOP	M28.209
HIN213IB	-40 to 85	28 Ld SOIC (W)	M28.3
HIN213IA	-40 to 85	28 Ld SSOP	M28.209

Pin Descriptions

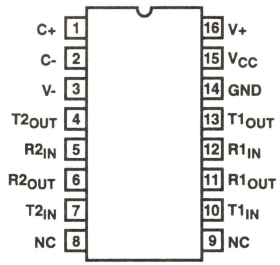
PIN	FUNCTION
V_{CC}	Power Supply Input 5V ±10%.
V+	Internally generated positive supply (+10V nominal), HIN201 and HIN209 requires +9V to +13.2V.
V-	Internally generated negative supply (-10V nominal).
GND	Ground lead. Connect to 0V.
C1+	External capacitor (+ terminal) is connected to this lead.
C1-	External capacitor (- terminal) is connected to this lead.
C2+	External capacitor (+ terminal) is connected to this lead.
C2-	External capacitor (- terminal) is connected to this lead.
T_{IN}	Transmitter Inputs. These leads accept TTL/CMOS levels. An internal 400kΩ pull-up resistor to V_{CC} is connected to each lead.
T_{OUT}	Transmitter Outputs. These are RS-232 levels (nominally ±10V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 input levels. An internal 5kΩ pull-down resistor to GND is connected to each input.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{EN}$, EN	Enable input. This is an active low input which enables the receiver outputs. With $\overline{EN}$ = 5V, (HIN213 EN = 0V), the outputs are placed in a high impedance state.
SD, $\overline{SD}$	Shutdown Input. With SD = 5V (HIN213 $\overline{SD}$ = 0V), the charge pump is disabled, the receiver outputs are in a high impedance state (except R4 and R5 of HIN213) and the transmitters are shut off.
NC	No Connect. No connections are made to these leads.

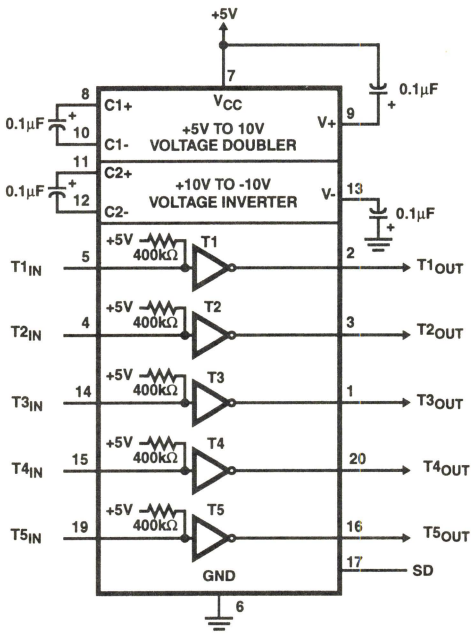
Pinouts

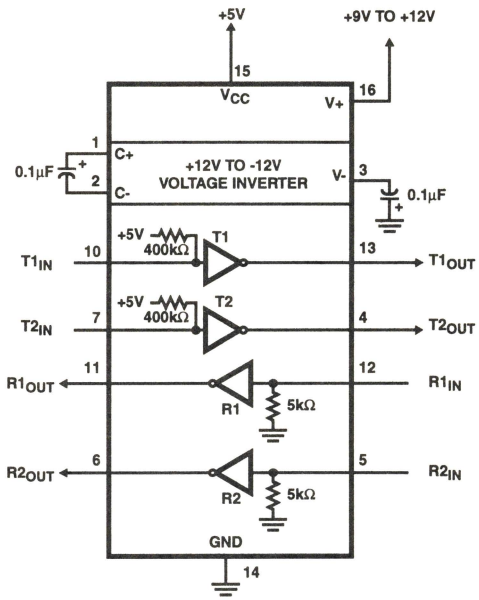
HIN200 (SOIC)
TOP VIEW



HIN201 (SOIC)
TOP VIEW

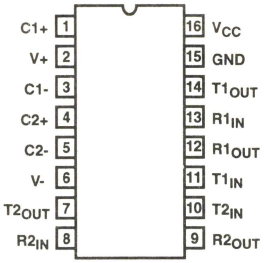




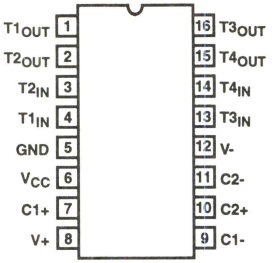


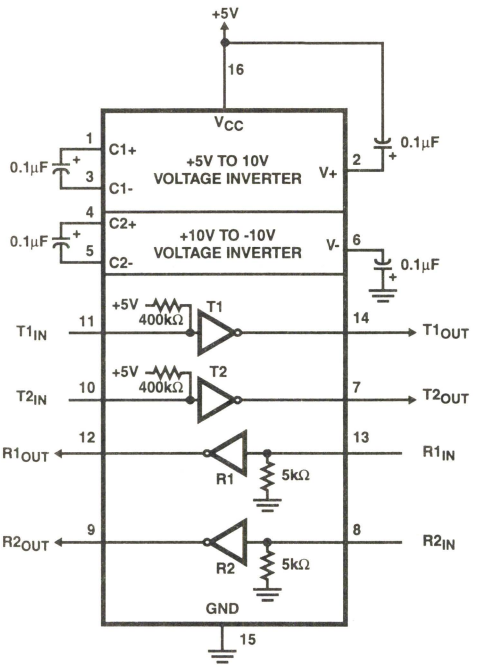
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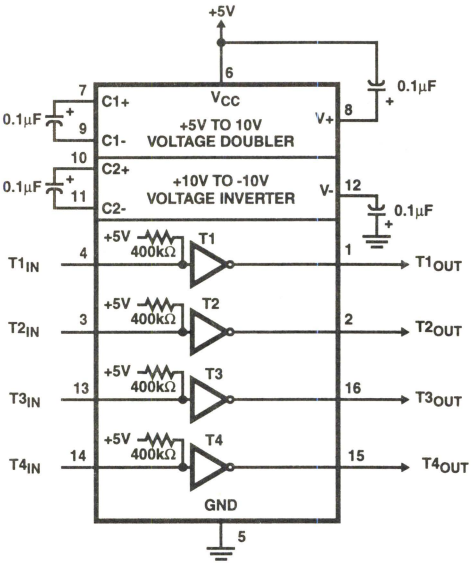
HIN202 (PDIP, SOIC, SSOP)
TOP VIEW



HIN204 (SOIC)
TOP VIEW

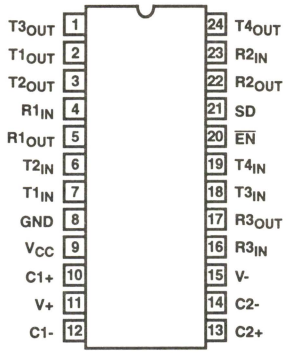




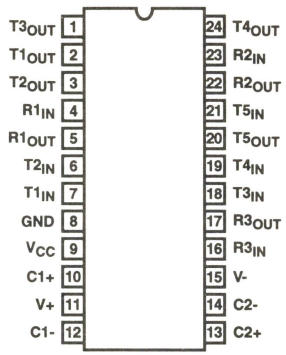


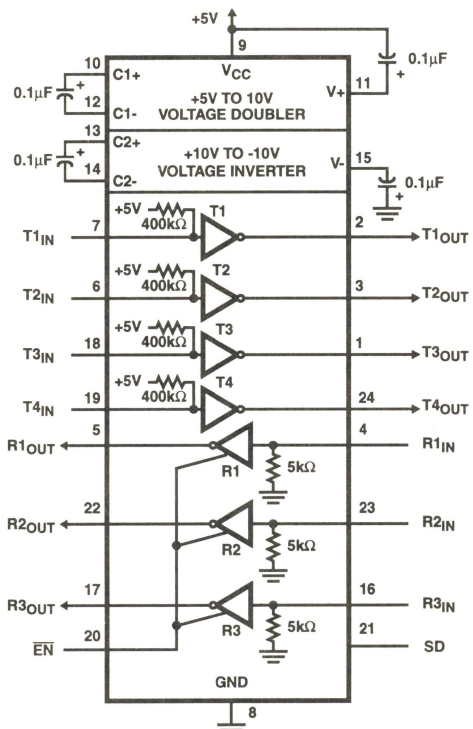
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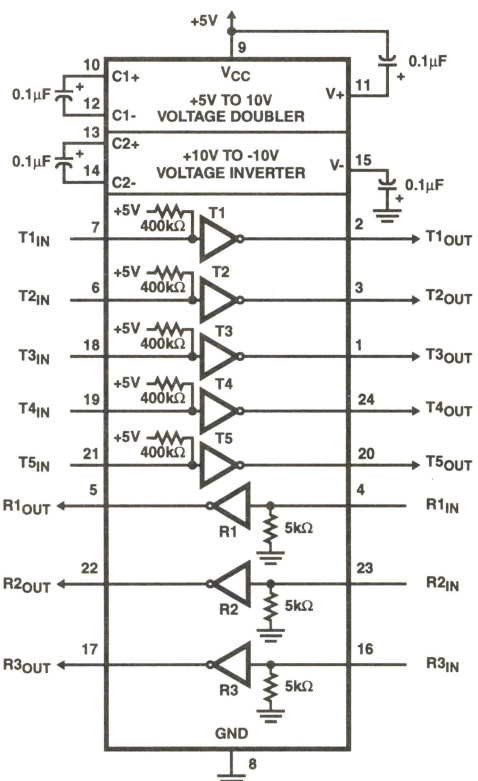
HIN206 (PDIP, SOIC, SSOP)
TOP VIEW



HIN207 (PDIP, SOIC, SSOP)
TOP VIEW

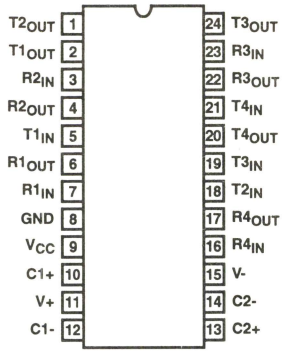




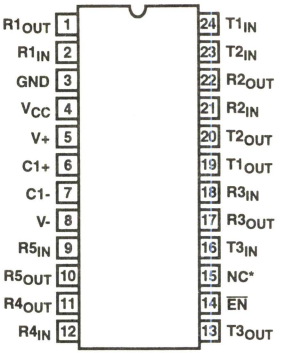


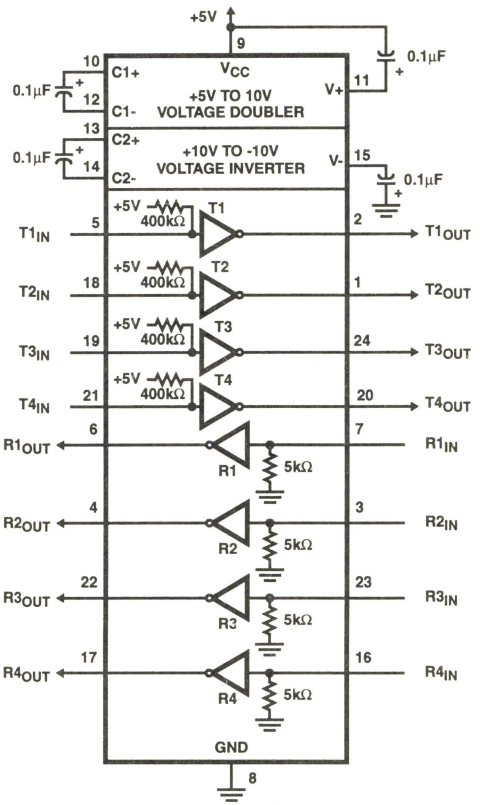
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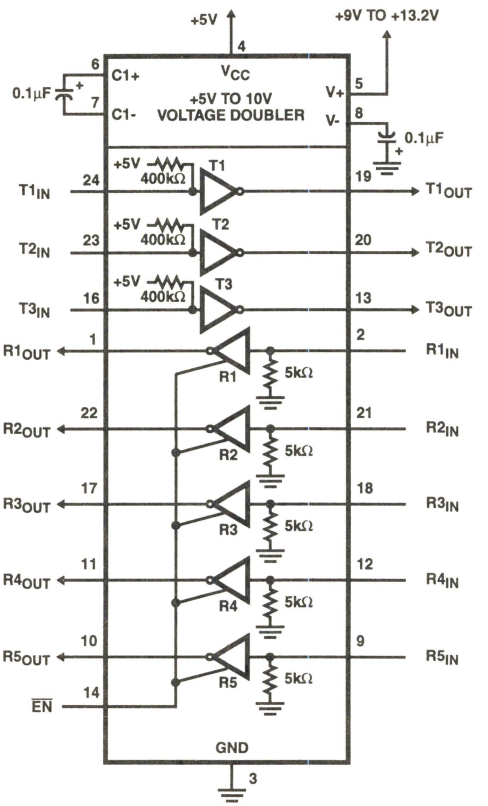
HIN208 (PDIP, SOIC, SSOP)
TOP VIEW



HIN209 (PDIP, SOIC, SSOP)
TOP VIEW

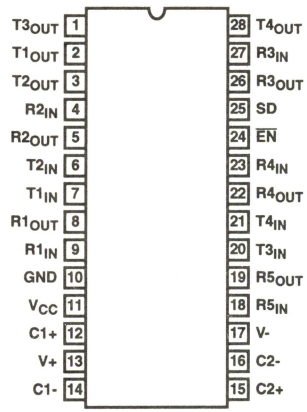




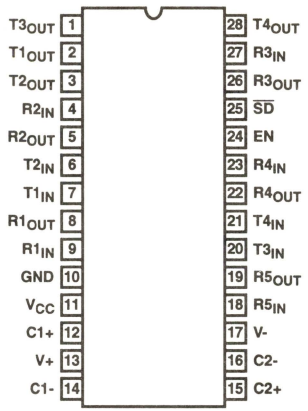


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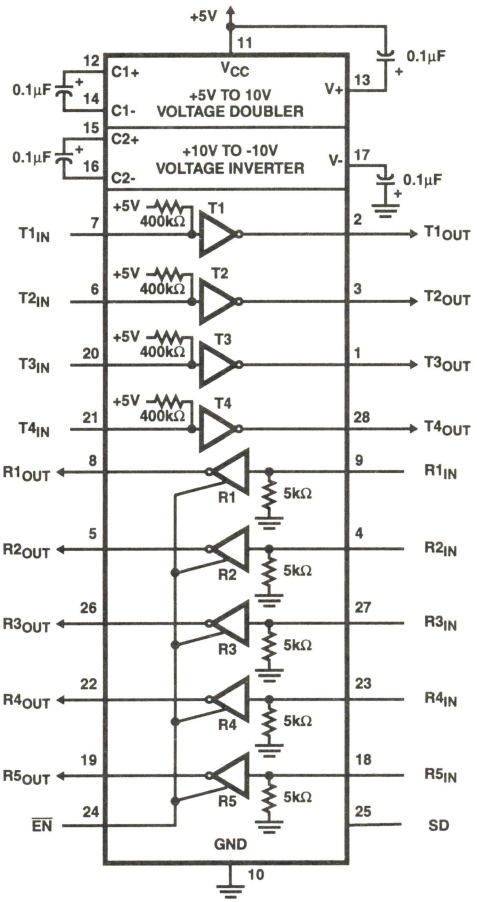
HIN211 (SOIC, SSOP)
TOP VIEW

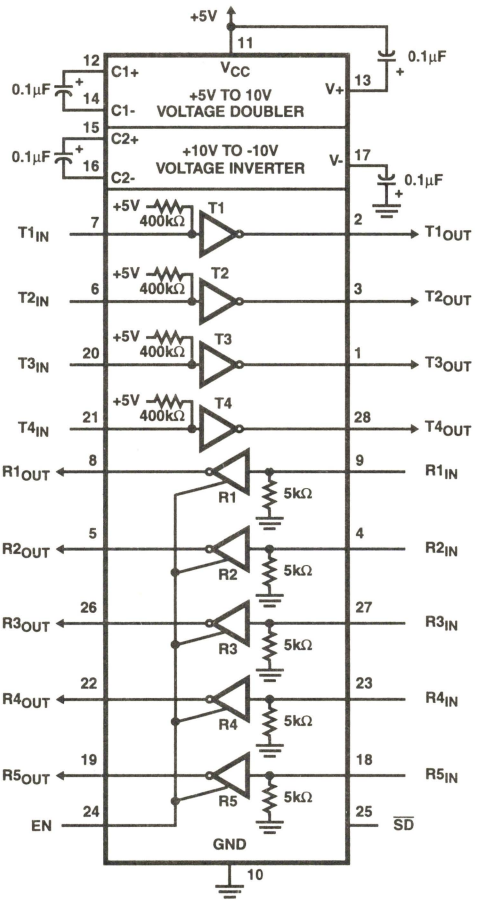


HIN213 (SOIC, SSOP)
TOP VIEW



NOTE: R4 AND R5 ACTIVE IN SHUTDOWN





Absolute Maximum Ratings

V_{CC} to Ground . . . . . (GND -0.3V) <V_{CC} < 6V
V+ to Ground . . . . . (V_{CC} -0.3V) <V+ < 12V
V- to Ground . . . . . -12V < V- < (GND +0.3V)
Input Voltages
  T_{IN} . . . . . (V_{CC} -0.3V) < V_{IN} < (V+ +0.3V)
  R_{IN} . . . . . ±30V
Output Voltages
  T_{OUT} . . . . . (V_{CC} -0.3V) < V_{TXOUT} < (V+ +0.3V)
  R_{OUT} . . . . . (GND -0.3V) < V_{RXOUT} < (V+ +0.3V)
Short Circuit Duration
  T_{OUT} . . . . . Continuous
  R_{OUT} . . . . . Continuous
Lead Temperature (Soldering 10s) . . . . . 300°C
  (SOIC and SSOP - Lead Tips Only)
ESD Classification . . . . . Class 1

Continuous Power Dissipation (T_A = 70°C) (Typical)
  16 Lead Plastic SSOP
  (Derate 6.45mW/°C above 70°C) 516mW
  16 Lead Plastic DIP
  (Derate 11.1mW/°C above 70°C) 888mW
  24 Lead Plastic DIP (N)
  (Derate 13.3mW/°C above 70°C) 1067mW
  16 Lead Plastic SOIC (W)
  (Derate 10mW/°C above 70°C) 800mW
  16 Lead Plastic SOIC (N)
  (Derate 9mW/°C above 70°C) 695mW
  20 Lead Plastic SOIC (W)
  (Derate 10mW/°C above 70°C) 800mW
  24 Lead Plastic SOIC (W)
  (Derate 12.5mW/°C above 70°C) 1000mW
  28 Lead Plastic SOIC (W)
  (Derate 13.3mW/°C above 70°C) 1067mW
  24 Lead Plastic SSOP
  (Derate 7.4mW/°C above 70°C) 592mW
  28 Lead Plastic SSOP
  (Derate 10mW/°C above 70°C) 800mW
Storage Temperature Range . . . . . -40°C to 85°C
Maximum Die Junction Temperature
  Plastic Package . . . . . 150°C
Operating Temperature Range
  HIN-XXXCX . . . . . 0°C to 70°C
  HIN-XXXIX . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Test Conditions: V_{CC} = +5V ±10%, (V_{CC} = +5V ±5% HIN200 and HIN207; V+ = 9V to 13.2V, HIN201 and HIN209), C1-C4 = 0.1µF; T_A = Operating Temperature Range

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing, T_{OUT}	Transmitter Outputs, 3kΩ to Ground		±5	±9	±10	V
Power Supply Current, I_{CC}	No Load, T_A = 25°C	HIN202	-	8	15	mA
		HIN200, HIN204-208, HIN211-213	-	11	20	mA
		HIN201, HIN209	-	0.4	1	mA
V+ Power Supply Current, I_{CC}	No Load, T_A = 25°C	HIN201	-	5.0	10	mA
		HIN209	-	7.0	15	mA
Shutdown Supply Current, I_{CC}(SD)	T_A = 25°C	HIN200, HIN206, HIN211	-	1	10	µA
		HIN213	-	15	50	µA
Input Logic Low, T_{IN}, $\overline{EN}$, V_{IL}	T_{IN}, $\overline{EN}$, SD, EN, $\overline{SD}$		-	-	0.8	V
Input Logic High, V_{IH}	T_{IN}		2.0	-	-	V
	$\overline{EN}$, SD, EN, $\overline{SD}$		2.4	-	-	V
Logic Pullup Current, I_P	T_{IN} = 0V		-	15	200	µA
RS-232 Input Voltage Range, V_{IN}			-30	-	+30	V
Receiver Input Impedance, R_{IN}	T_A = 25°C, V_{IN} = ±3V		3.0	5.0	7.0	kΩ

Electrical Specifications Test Conditions: V_{CC} = +5V ±10%, (V_{CC} = +5V ±5% HIN200 and HIN207; V+ = 9V to 13.2V, HIN201 and HIN209), C1-C4 = 0.1µF; T_A = Operating Temperature Range **(Continued)**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Receiver Input Low Threshold, V_{IN} (H-L)	V_{CC} = 5V, T_A = 25°C	Active Mode	0.8	1.2	-	V
		Shutdown Mode HIN213 R4 and R5	0.6	1.5	-	V
Receiver Input High Threshold, V_{IN} (L-H)	V_{CC} = 5V, T_A = 25°C	Active Mode	-	1.7	2.4	V
		Shutdown Mode HIN213 R4 and R5	-	1.5	2.4	V
Receiver Input Hysteresis, V_{HYST}	V_{CC} = 5V No Hysteresis in Shutdown Mode		0.2	0.5	1.0	V
TTL/CMOS Receiver Output Voltage Low, V_{OL}	I_{OUT} = 1.6mA (I_{OUT} = 3.2mA)		-	0.1	0.4	V
TTL/CMOS Receiver Output Voltage High, V_{OH}	I_{OUT} = -1mA		3.5	4.6	-	V
Output Enable Time, t_{EN}	HIN206, HIN209, HIN211, HIN213		-	600	-	ns
Output Disable Time, t_{DIS}	HIN206, HIN209, HIN211, HIN213		-	200	-	ns
Propagation Delay, t_{PD}	HIN213 $\overline{SD}$ = 0V, R4, R5		-	4.0	40	µs
	HIN213 $\overline{SD}$ = V_{CC}		-	0.5	10	µs
	HIN200 - HIN211		-	0.5	10	µs
Transition Region Slew Rate, SR_T	R_L = 3kΩ, C_L = 2500pF Measured from +3V to -3V or -3V to +3V (Note 1)	HIN200, HIN204 to HIN211, HIN213	3	-	30	V/µs
		HIN201, HIN202	-	4.0	30	V/µs
Output Resistance, R_{OUT}	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300	-	-	Ω
RS-232 Output Short Circuit Current, I_{SC}	T_{OUT} shorted to GND		-	±10	-	mA
TTL/CMOS Receiver Output Leakage	EN = V_{CC}, EN = 0, 0V < R_{OUT} < V_{CC}		-	0.5	±10	µA

NOTE:

1. Guaranteed by design.

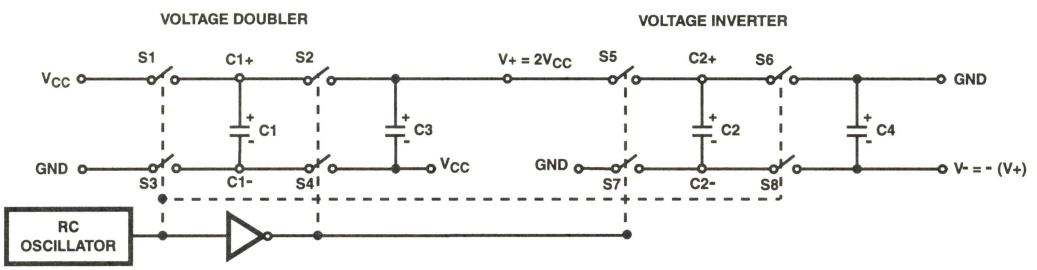


FIGURE 1. CHARGE PUMP

Detailed Description

The HIN200 thru HIN213 family of RS-232 transmitters/receivers are powered by a single +5V power supply (except HIN201 and HIN209), feature low power consumption, and meet all EIA RS232C and V.28 specifications. The circuit is divided into three sections: the charge pump, transmitter, and receiver.

Charge Pump

An equivalent circuit of the charge pump is illustrated in Figure 1. The charge pump contains two sections: the voltage doubler and the voltage inverter. Each section is driven by a two phase, internally generated clock to generate +10V and -10V. The nominal clock frequency is 125kHz. During phase one of the clock, capacitor C1 is charged to V_{CC}. During phase two, the voltage on C1 is added to V_{CC}, producing a signal across C3 equal to twice V_{CC}. During phase two, C2 is also charged to $2V_{CC}$, and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The charge pump accepts input voltages up to 5.5V. The output impedance of the voltage doubler section (V+) is approximately 200Ω, and the output impedance of the voltage inverter section (V-) is approximately 450Ω. A typical application uses 0.1µF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V+ and V- supplies.

During shutdown mode (HIN200, HIN206 and HIN211, SD = V_{CC}, HIN213, $\overline{SD}$ = 0V) the charge pump is turned off, V+ is pulled down to V_{CC}, V- is pulled up to GND, and the supply current is reduced to less than 10µA. The transmitter outputs are disabled and the receiver outputs (except for HIN213, R4 and R5) are placed in the high impedance state.

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC}, or 1.3V for V_{CC} = 5V. A logic 1 at the input results in a voltage of between -5V and V- at the output, and a logic 0 results in a voltage between +5V and (V+ -0.6V). Each transmitter input has an internal 400kΩ pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specifications of ±5V minimum with the worst case conditions of: all transmitters driving 3kΩ minimum load impedance, V_{CC} = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/µs. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300Ω with ±2V applied to the outputs and V_{CC} = 0V.

Receivers

The receiver inputs accept up to ±30V while presenting the required 3kΩ to 7kΩ input impedance even if the power is off (V_{CC} = 0V). The receivers have a typical input threshold of 1.3V which is within the ±3V limits, known as the transition region, of the RS-232 specifications. The receiver output is 0V to V_{CC}. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis (except during shutdown) to improve noise rejection. The receiver Enable line ($\overline{EN}$, on HIN206, HIN209, and HIN211, EN on HIN213) when unasserted, disables the receiver outputs, placing them in the high impedance mode. The receiver outputs are also placed in the high impedance state when in shutdown mode (except HIN213 R4 and R5).

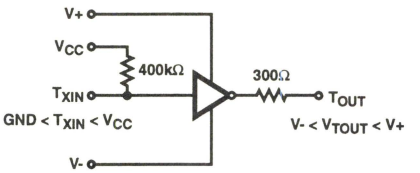


FIGURE 2. TRANSMITTER

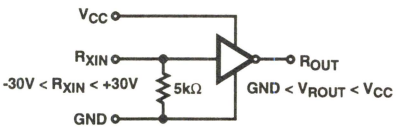
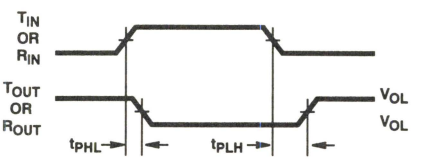


FIGURE 3. RECEIVER



$$\text{AVERAGE PROPAGATION DELAY} = \frac{t_{PHL} + t_{PLH}}{2}$$

FIGURE 4. PROPAGATION DELAY DEFINITION

HIN213 Operation in Shutdown

The HIN213 features two receivers, R4 and R5, which remain active in shutdown mode. During normal operation the receivers propagation delay is typically 0.5µs. This propagation delay increases to 4µs (typical) during shutdown. When entering shut down mode, receivers R4 and R5 are not valid for 80µs after $\overline{SD}$ = V_{IL}. When exiting shutdown mode, all receiver outputs will be invalid until the charge pump circuitry reaches normal operating voltage. This is typically less than 2ms when using 0.1µF capacitors.

Typical Performance Curves

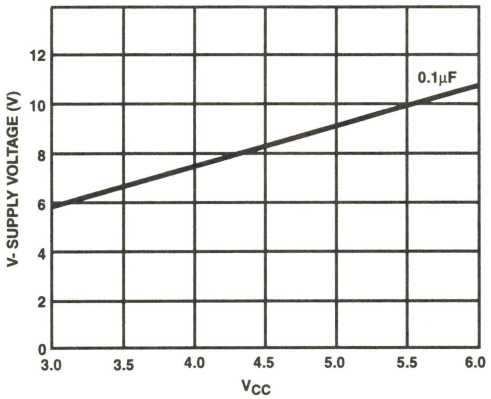


FIGURE 5. V- SUPPLY VOLTAGE vs V_{CC}

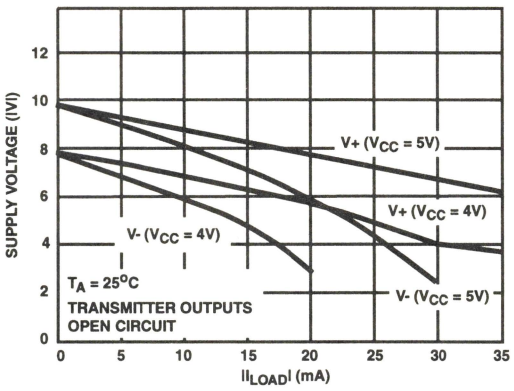


FIGURE 6. V+, V- OUTPUT VOLTAGE vs LOAD

Test Circuits (HIN-202)

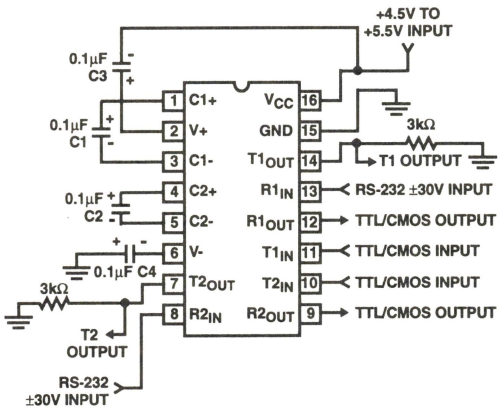


FIGURE 7. GENERAL TEST CIRCUIT

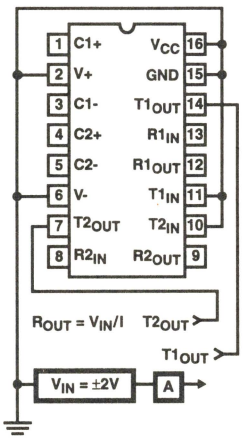


FIGURE 8. POWER-OFF SOURCE RESISTANCE CONFIGURATION

Application Information

The HINXXX may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where ±12V power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 9. Fixed output signals such as DTR (data terminal ready) and DSRS (data signaling rate select) is generated by driving them through a 5kΩ resistor connected to V+.

In applications requiring four RS-232 inputs and outputs (Figure 10), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

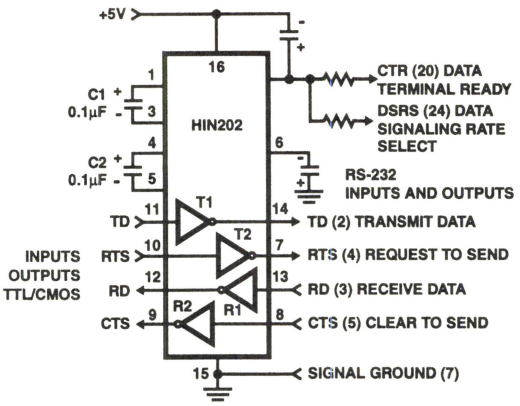


FIGURE 9. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

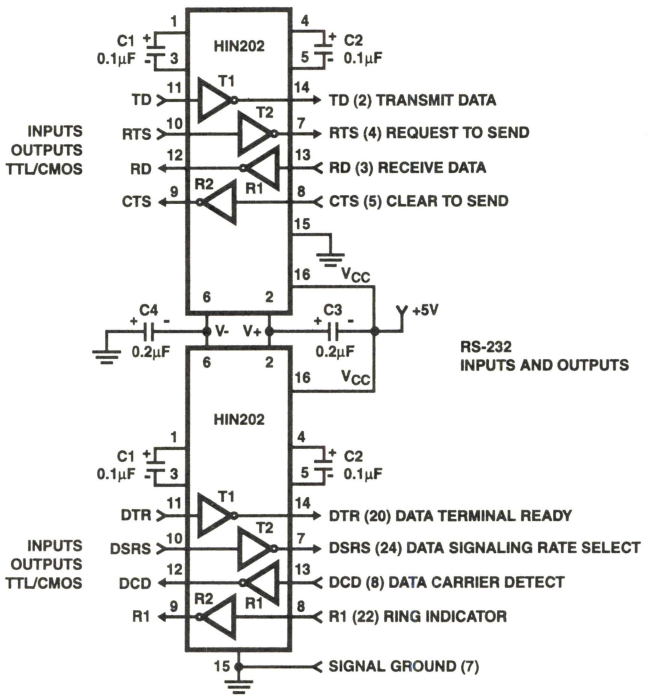


FIGURE 10. COMBINING TWO HIN202s FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS

Die Characteristics

DIE DIMENSIONS:

160 mils x 140 mils

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

SUBSTRATE POTENTIAL

V+

PASSIVATION:

Type: Nitride over Silox
Nitride Thickness: 8kÅ
Silox Thickness: 7kÅ

TRANSISTOR COUNT:

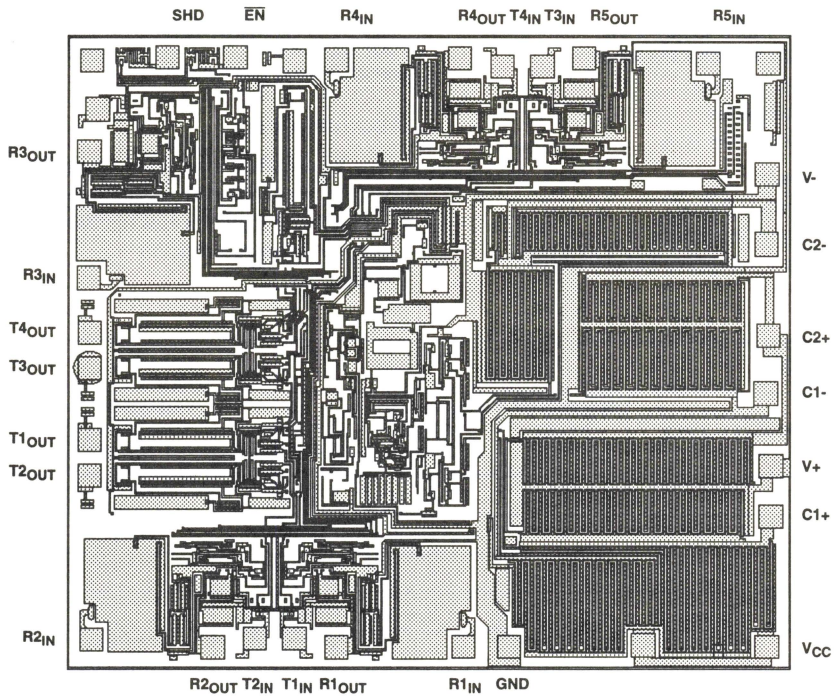
238

PROCESS:

CMOS Metal Gate

Metallization Mask Layout

HIN211



HARRIS SEMICONDUCTOR

HIN230 thru HIN241

March 1997

+5V Powered RS-232 Transmitters/Receivers

Features

- Meets All RS-232C and V.28 Specifications
- Requires Only Single +5V Power Supply
  - (+5V and +12V - HIN231 and HIN239)
- Onboard Voltage Doubler/Inverter
- Low Power Consumption
- Low Power Shutdown Function
- Three-State TTL/CMOS Receiver Outputs
- Multiple Drivers
  - ±10V Output Swing for +5V Input
  - 300Ω Power-Off Source Impedance
  - Output Current Limiting
  - TTL/CMOS Compatible
  - 30V/μs Maximum Slew Rate
- Multiple Receivers
  - ±30V Input Voltage Range
  - 3kΩ to 7kΩ Input Impedance
  - 0.5V Hysteresis to Improve Noise Rejection

Description

The HIN230-HIN241 family of RS-232 transmitters/receivers interface circuits meet all EIA RS-232C and V.28 specifications, and are particularly suited for those applications where ±12V is not available. They require a single +5V power supply (except HIN231 and HIN239) and features onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply. The family of devices offer a wide variety of RS-232 transmitter/receiver combinations to accommodate various applications (see Selection Table).

The drivers feature true TTL/CMOS input compatibility, slew-rate-limited output, and 300Ω power-off source impedance. The receivers can handle up to ±30V, and have a 3kΩ to 7kΩ input impedance. The receivers also feature hysteresis to greatly improve noise rejection.

Applications

- Any System Requiring RS-232 Communications Port
  - Computer - Portable, Mainframe, Laptop
  - Peripheral - Printers and Terminals
  - Portable Instrumentation
  - Modems

Selection Table

PART NUMBER	POWER SUPPLY VOLTAGE	NUMBER OF RS-232 DRIVERS	NUMBER OF RS-232 RECEIVERS	EXTERNAL COMPONENTS	LOW POWER SHUTDOWN/TTL THREE-STATE	NUMBER OF LEADS
HIN230	+5V	5	0	4 Capacitors	YES/NO	20
HIN231	+5V and +7.5V to 13.2V	2	2	2 Capacitors	NO/NO	16
HIN232	+5V	2	2	4 Capacitors	NO/NO	16
HIN234	+5V	4	0	4 Capacitors	NO/NO	16
HIN236	+5V	4	3	4 Capacitors	YES/YES	24
HIN237	+5V	5	3	4 Capacitors	NO/NO	24
HIN238	5V	4	4	4 Capacitors	NO/NO	24
HIN239	+5V and +7.5V to 13.2V	3	5	2 Capacitors	NO/YES	24
HIN240	+5V	5	5	4 Capacitors	YES/YES	44
HIN241	+5V	4	5	4 Capacitors	YES/YES	28

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3138.3**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIN230CB	0 to 70	20 Ld SOIC (W)	M20.3
HIN230IB	-40 to 85	20 Ld SOIC (W)	M20.3
HIN230BY		Die	
HIN231CB	0 to 70	16 Ld SOIC (W)	M16.3
HIN231IB	-40 to 85	16 Ld SOIC (W)	M16.3
HIN231BY		Die	
HIN232CP	0 to 70	16 Ld PDIP	E16.3
HIN232CB	0 to 70	16 Ld SOIC (W)	M16.3
HIN232IP	-40 to 85	16 Ld PDIP	E16.3
HIN232IJ	-40 to 85	16 Ld CERDIP	F16.3
HIN232IB	-40 to 85	16 Ld SOIC (W)	M16.3
HIN232MJ	-55 to 125	16 Ld CERDIP	F16.3
HIN232BY		Die	
HIN234CB	0 to 70	16 Ld SOIC (W)	M16.3
HIN234IB	-40 to 85	16 Ld SOIC (W)	M16.3
HIN234BY		Die	
HIN236CP	0 to 70	24 Ld PDIP (N)	E24.3
HIN236CB	0 to 70	24 Ld SOIC (W)	M24.3
HIN236IP	-40 to 85	24 Ld PDIP (N)	E24.3
HIN236IB	-40 to 85	24 Ld SOIC (W)	M24.3
HIN236BY		Die	

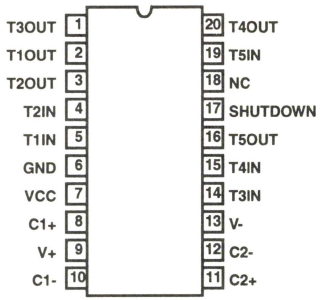
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIN237CP	0 to 70	24 Ld PDIP (N)	E24.3
HIN237CB	0 to 70	24 Ld SOIC (W)	M24.3
HIN237IP	-40 to 85	24 Ld PDIP (N)	E24.3
HIN237IB	-40 to 85	24 Ld SOIC (W)	M24.3
HIN237BY		Die	
HIN238CP	0 to 70	24 Ld PDIP (N)	E24.3
HIN238CB	0 to 70	24 Ld SOIC (W)	M24.3
HIN238IP	-40 to 85	24 Ld PDIP (N)	E24.3
HIN238IB	-40 to 85	24 Ld SOIC (W)	M24.3
HIN238BY		Die	
HIN239CB	0 to 70	24 Ld SOIC (W)	M24.3
HIN239IB	-40 to 85	24 Ld SOIC (W)	M24.3
HIN239BY		Die	
HIN240CN	0 to 70	44 Ld MQFP	Q44.10X10
HIN240IN	-40 to 85	44 Ld MQFP	Q44.10X10
HIN240BY		Die	
HIN241CB	0 to 70	28 Ld SOIC (W)	M28.3
HIN241IB	-40 to 85	28 Ld SOIC (W)	M28.3
HIN241CA	0 to 70	28 Ld SSOP (W)	M28.209
HIN241IA	-40 to 85	28 Ld SSOP (W)	M28.209
HIN241BY		Die	

Pin Descriptions

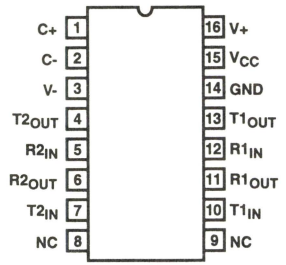
PIN	FUNCTION
V_{CC}	Power Supply Input 5V ±10%.
V+	Internally generated positive supply (+10V nominal), HIN231 and HIN239 requires +7.5V to +13.2V.
V-	Internally generated negative supply (-10V nominal).
GND	Ground lead. Connect to 0V.
C1+	External capacitor (+ terminal) is connected to this lead.
C1-	External capacitor (- terminal) is connected to this lead.
C2+	External capacitor (+ terminal) is connected to this lead.
C2-	External capacitor (- terminal) is connected to this lead.
T_{IN}	Transmitter Inputs. These leads accept TTL/CMOS levels. An internal 400kΩ pull-up resistor to V_{CC} is connected to each lead.
T_{OUT}	Transmitter Outputs. These are RS-232 levels (nominally ±10V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 input levels. An internal 5kΩ pull-down resistor to GND is connected to each input.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{EN}$	Enable input. This is an active low input which enables the receiver outputs. With $\overline{EN}$ = 5V, the outputs are placed in a high impedance state.
SD	Shutdown Input. With SD = 5V, the charge pump is disabled, the receiver outputs are in a high impedance state and the transmitters are shut off.
NC	No Connect. No connections are made to these leads.

Pinouts

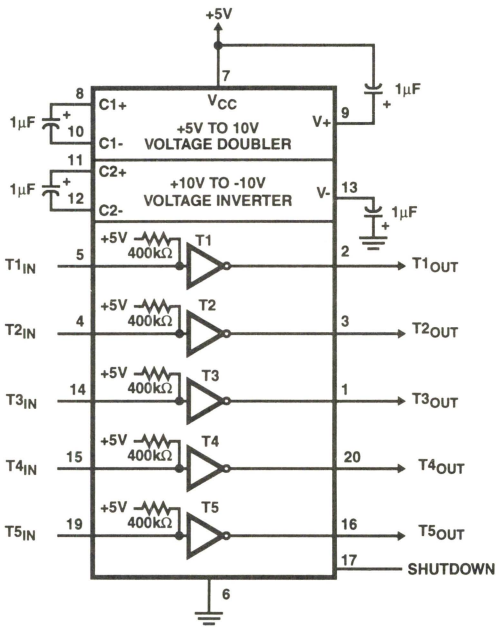
HIN230 (SOIC)
TOP VIEW



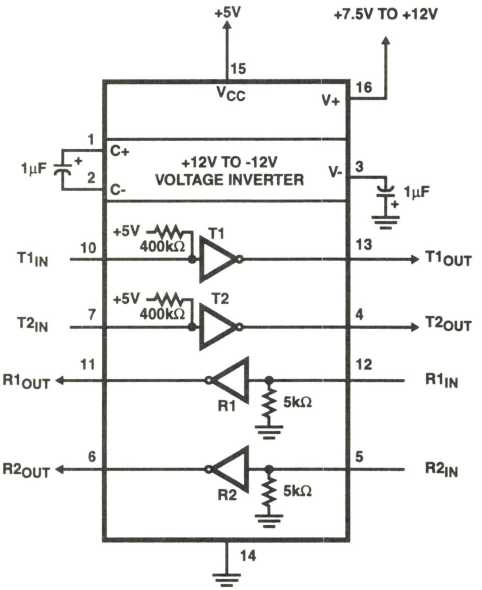
HIN231 (SOIC)
TOP VIEW



HIN230 (SOIC)

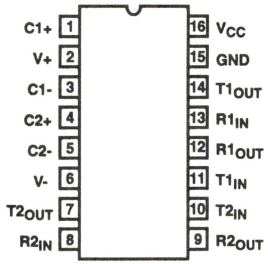


HIN231 (SOIC)

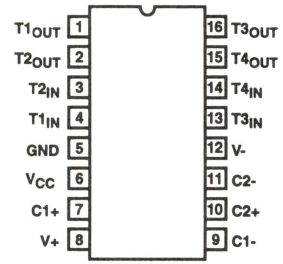


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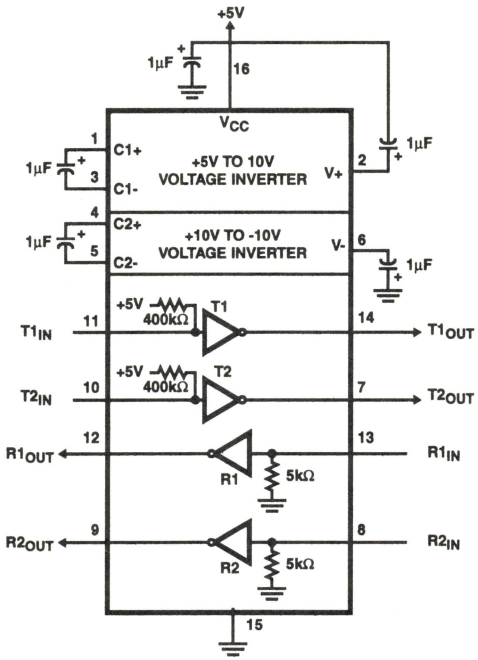
HIN232 (PDIP, CERDIP, SOIC)
TOP VIEW



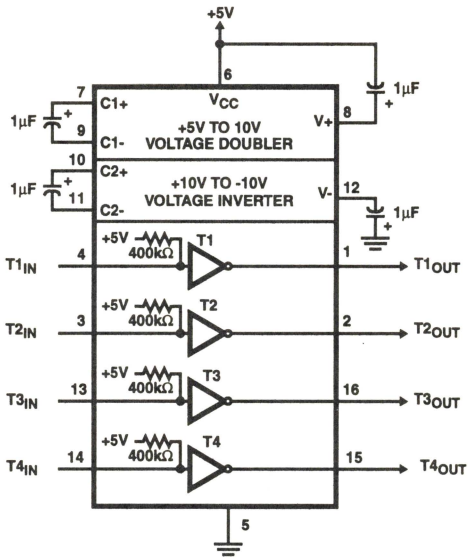
HIN234 (SOIC)
TOP VIEW



HIN232 (PDIP, CERDIP, SOIC)

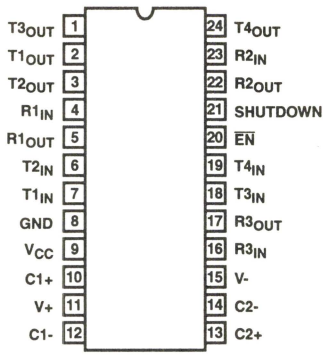


HIN234 (SOIC)

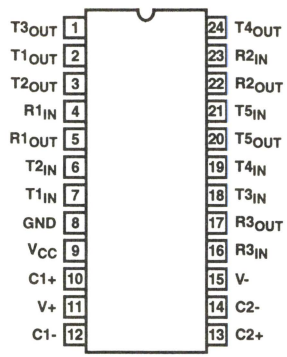


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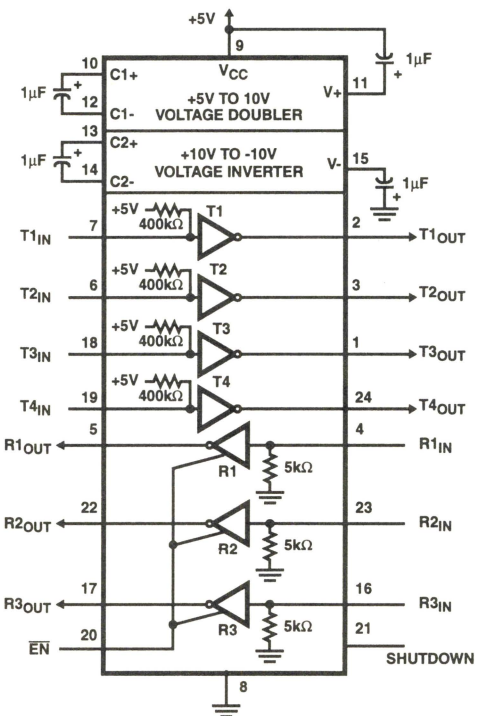
HIN236 (PDIP, SOIC)
TOP VIEW



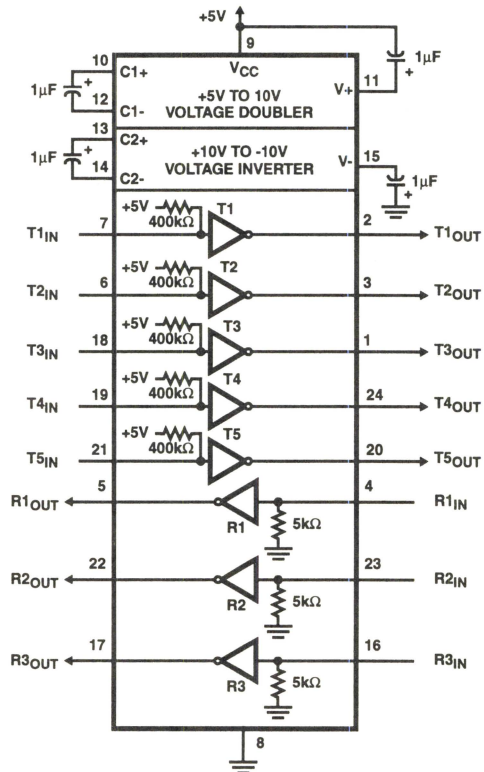
HIN237 (PDIP, SOIC)
TOP VIEW



HIN236 (PDIP, SOIC)

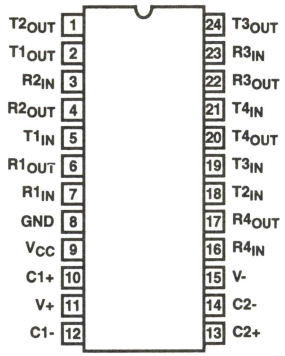


HIN237 (PDIP, SOIC)

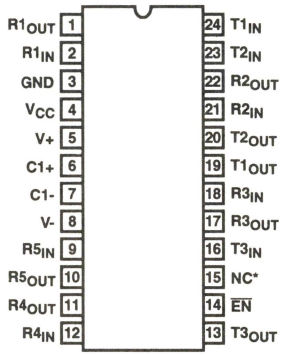


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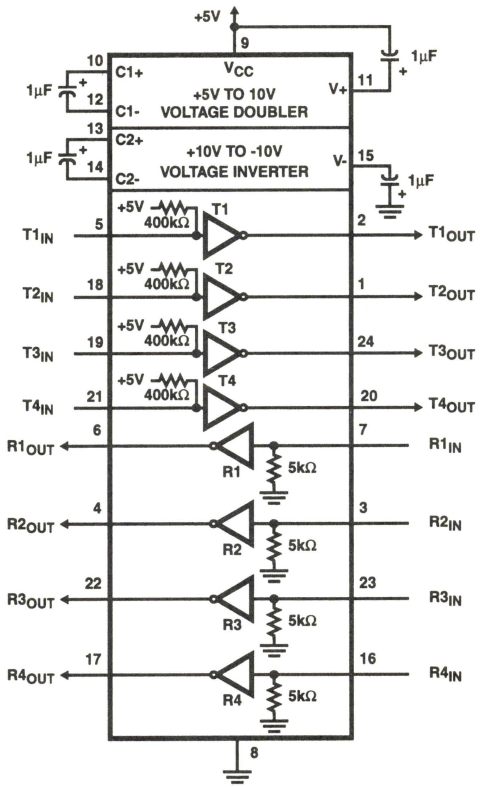
HIN238 (PDIP, SOIC)
TOP VIEW



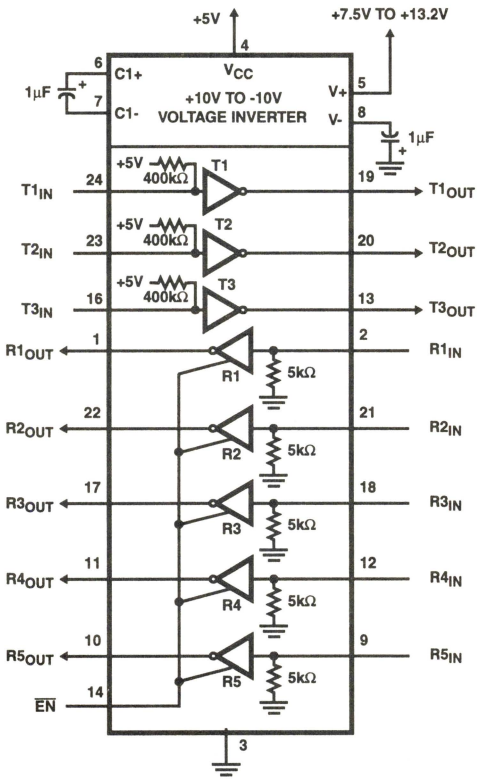
HIN239 (SOIC)
TOP VIEW



HIN238 (PDIP, SOIC)

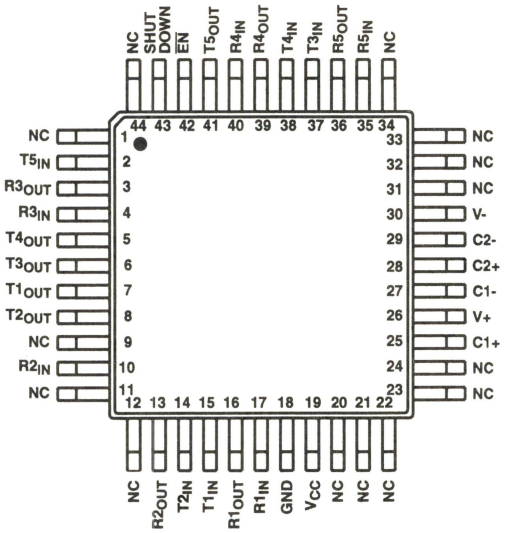


HIN239 (SOIC)



Pinouts (Continued)

HIN240 (MQFP)

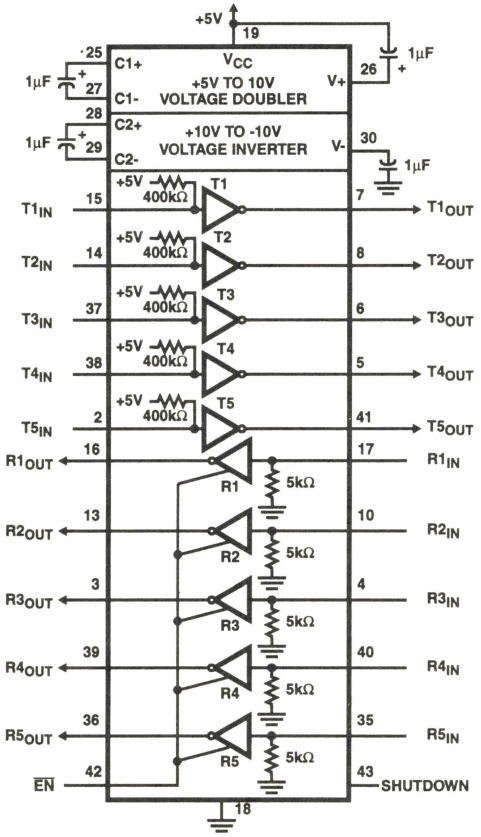


HIN241 (SOIC, SSOP)

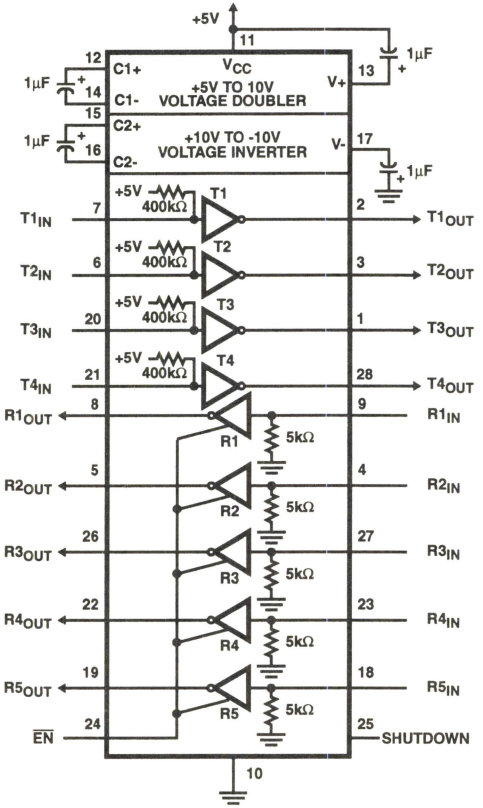
TOP VIEW



HIN240 (MQFP)



HIN241 (SOIC, SSOP)



Absolute Maximum Ratings

V_{CC} to Ground . . . . . (GND -0.3V) < V_{CC} < 6V
V+ to Ground . . . . . (V_{CC} -0.3V) < V+ < 12V
V- to Ground . . . . . -12V < V- < (GND +0.3V)
Input Voltages
  T_{IN} . . . . . (V_{CC} -0.3V) < V_{IN} < (V+ +0.3V)
  R_{IN} . . . . . ±30V
Output Voltages
  T_{OUT} . . . . . (V_{CC} -0.3V) < V_{TXOUT} < (V+ +0.3V)
  R_{OUT} . . . . . (GND -0.3V) < V_{RXOUT} < (V+ +0.3V)
Short Circuit Duration
  T_{OUT} . . . . . Continuous
  R_{OUT} . . . . . Continuous
Lead Temperature (Soldering 10s) . . . . . 300°C
  (SOIC, SSOP, MQFP - Lead Tips Only)

Thermal Information

Continuous Total Power Dissipation (T_A = 25°C)

Package	θ_{JA} (°C/W)	θ_{JC}(°C/W)
16 Ld PDIP Package	90	N/A
24 Ld PDIP Package	75	N/A
16 Ld SOIC (W) Package	100	N/A
24 Ld SOIC Package	80	N/A
28 Ld SOIC Package	75	N/A
28 Ld SSOP Package	100	N/A
44 Ld MQFP Package	80	N/A
16 Ld CERDIP Package	80	18

Storage Temperature Range . . . . . -65°C to 150°C
Maximum Die Junction Temperature
  Plastic Package . . . . . 150°C
  Ceramic Package . . . . . 175°C
Operating Temperature Range
  HIN-XXXCX . . . . . 0°C to 70°C
  HIN-XXXIX . . . . . -40°C to 85°C
  HIN-XXXMX . . . . . -55°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Test Conditions: V_{CC} = +5V ±10%, T_A = Operating Temperature Range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Swing, T_{OUT}	Transmitter Outputs, 3kΩ to Ground	±5	±9	±10	V
Power Supply Current, I_{CC}	No Load, T_A = 25°C, HIN232-233	-	5	10	mA
	HIN230, HIN234-238, HIN240-241	-	7	15	mA
	HIN231, HIN239	-	0.4	1	mA
V+ Power Supply Current, I_{CC}	HIN231	-	1.8	5	mA
	HIN239	-	5.0	15	mA
Shutdown Supply Current, I_{CC}(SD)		-	1	10	µA
Input Logic Low, T_{IN}, $\overline{EN}$, V_{IL}	T_{IN}, $\overline{EN}$, Shutdown	-	-	0.8	V
Input Logic High, V_{IH}	T_{IN}	2.0	-	-	V
	$\overline{EN}$, Shutdown	2.4	-	-	V
Logic Pullup Current, I_P	T_{IN} = 0V	-	15	200	µA
RS-232 Input Voltage Range, V_{IN}		-30	-	+30	V
Receiver Input Impedance, R_{IN}	V_{IN} = ±3V	3.0	5.0	7.0	kΩ
Receiver Input Low Threshold, V_{IN} (H-L)	V_{CC} = 5V, T_A = 25°C	0.8	1.2	-	V
Receiver Input High Threshold, V_{IN} (L-H)	V_{CC} = 5V, T_A = 25°C	-	1.7	2.4	V
Receiver Input Hysteresis, V_{HYST}		0.2	0.5	1.0	V
TTL/CMOS Receiver Output Voltage Low, V_{OL}	I_{OUT} = 1.6mA (HIN231-HIN232 I_{OUT} = 3.2mA)	-	0.1	0.4	V
TTL/CMOS Receiver Output Voltage High, V_{OH}	I_{OUT} = -1.0mA	3.5	4.6	-	V
Output Enable Time, t_{EN}	HIN236, 239, 240, 241	-	400	-	ns
Output Disable Time, t_{DIS}	HIN236, 239, 240, 241	-	250	-	ns
Propagation Delay, t_{PD}	RS-232 to TTL	-	0.5	-	µs
Instantaneous Slew Rate, SR	C_L = 10pF, R_L = 3kΩ, T_A = 25°C (Note 1)	-	-	30	V/µs
Transition Region Slew Rate, SR_T	R_L = 3kΩ, C_L = 2500pF Measured from +3V to -3V or -3V to +3V	-	3	-	V/µs
Output Resistance, R_{OUT}	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V	300	-	-	Ω
RS-232 Output Short Circuit Current, I_{SC}	T_{OUT} shorted to GND	-	±10	-	mA

NOTE: 1. Guaranteed by design.

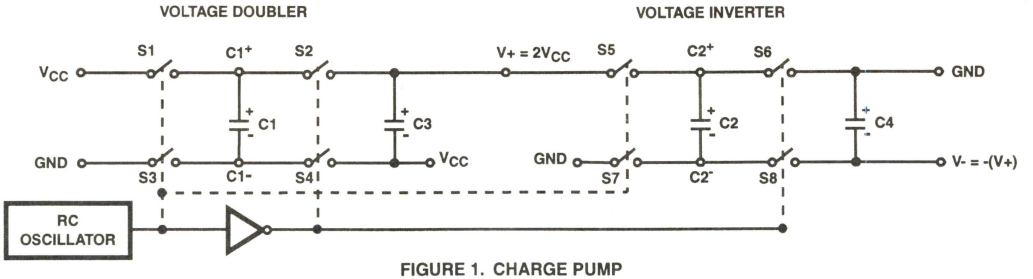


FIGURE 1. CHARGE PUMP

Detailed Description

The HIN230 thru HIN241 family of RS-232 transmitters/receivers are powered by a single +5V power supply (except HIN-231 and HIN239), feature low power consumption, and meet all EIA RS-232C and V.28 specifications. The circuit is divided into three sections: the charge pump, transmitter, and receiver.

Charge Pump

An equivalent circuit of the charge pump is illustrated in Figure 1. The charge pump contains two sections: the voltage doubler and the voltage inverter. Each section is driven by a two phase, internally generated clock to generate +10V and -10V. The nominal clock frequency is 16kHz. During phase one of the clock, capacitor C1 is charged to V_{CC}. During phase two, the voltage on C1 is added to V_{CC}, producing a signal across C3 equal to twice V_{CC}. During phase one, C2 is also charged to $2V_{CC}$, and then during phase two, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The charge pump accepts input voltages up to 5.5V. The output impedance of the voltage doubler section (V+) is approximately 200Ω, and the output impedance of the voltage inverter section (V-) is approximately 450Ω. A typical application uses 1µF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V+ and V- supplies.

During shutdown mode (HIN230, 236, 240 and 241), SHUTDOWN control line set to logic "1", the charge pump is turned off, V+ is pulled down to V_{CC}, V- is pulled up to GND, and the supply current is reduced to less than 10µA. The transmitter outputs are disabled and the receiver outputs are placed in the high impedance state.

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC}, or 1.3V for V_{CC} = 5V. A logic 1 at the input results in a voltage of between -5V and V- at the output, and a logic 0 results in a voltage between +5V and (V+ -0.6V). Each transmitter input has an internal 400kΩ pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specifications of ±5V minimum with the worst case conditions of: all transmitters driving 3kΩ minimum load impedance, V_{CC} = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/µs. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300Ω with ±2V applied to the outputs and V_{CC} = 0V.

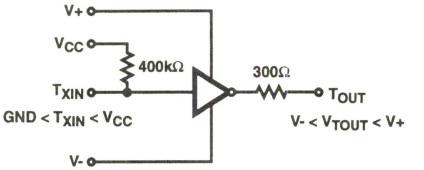


FIGURE 2. TRANSMITTER

Receivers

The receiver inputs accept up to ±30V while presenting the required 3kΩ to 7kΩ input impedance even it the power is off (V_{CC} = 0V). The receivers have a typical input threshold of 1.3V which is within the ±3V limits, known as the transition region, of the RS-232 specifications. The receiver output is 0V to V_{CC}. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis to improve noise rejection. The receiver Enable line $\overline{EN}$, when set to logic "1", (HIN236, 239, 240, and 241) disables the receiver outputs, placing them in the high impedance mode. The receiver outputs are also placed in the high impedance state when in shutdown mode.

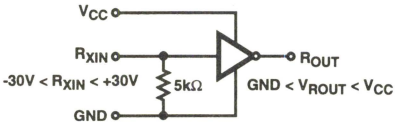
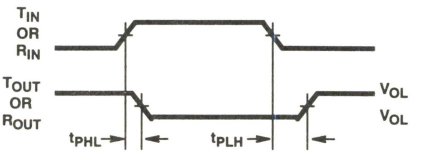


FIGURE 3. RECEIVER



$$\text{Average Propagation Delay} = \frac{t_{PHL} + t_{PLH}}{2}$$

FIGURE 4. PROPAGATION DELAY DEFINITION

Typical Performance Curves

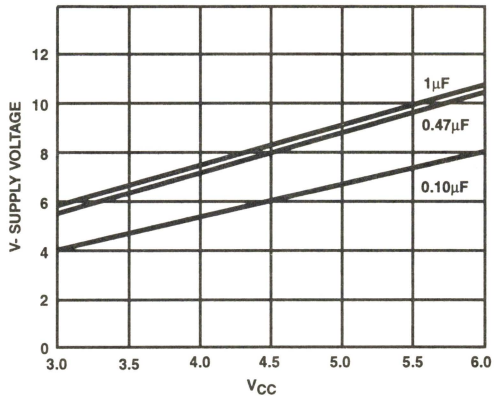


FIGURE 5. V- SUPPLY VOLTAGE vs V_{CC}, VARYING CAPACITORS

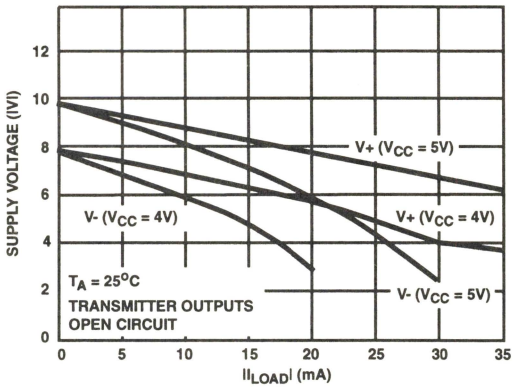


FIGURE 6. V+, V- OUTPUT VOLTAGE vs LOAD

Test Circuits (HIN-232)

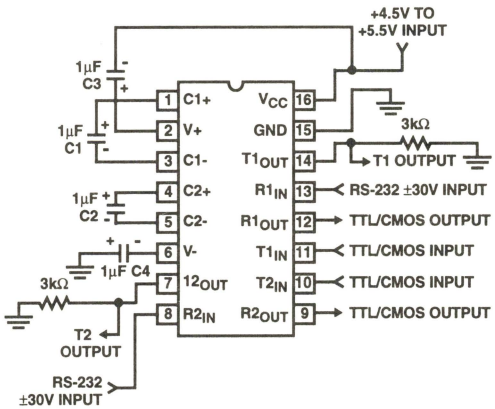


FIGURE 7. GENERAL TEST CIRCUIT

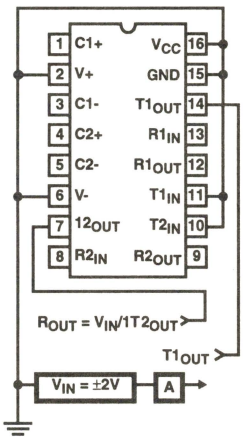


FIGURE 8. POWER-OFF SOURCE RESISTANCE CONFIGURATION

Applications

The HINXXX may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where ±12V power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 9. Fixed output signals such as DTR (data terminal ready) and DSRS (data signaling rate select) is generated by driving them through a 5kΩ resistor connected to V+.

In applications requiring four RS-232 inputs and outputs (Figure 10), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

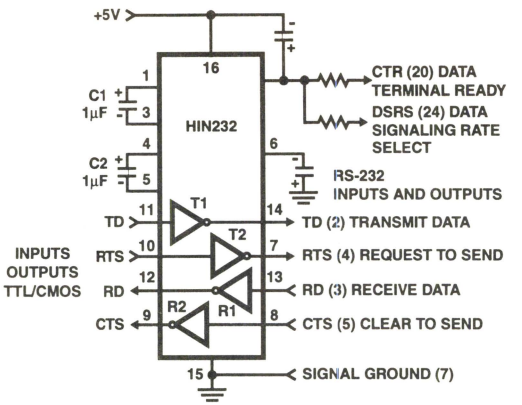


FIGURE 9. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

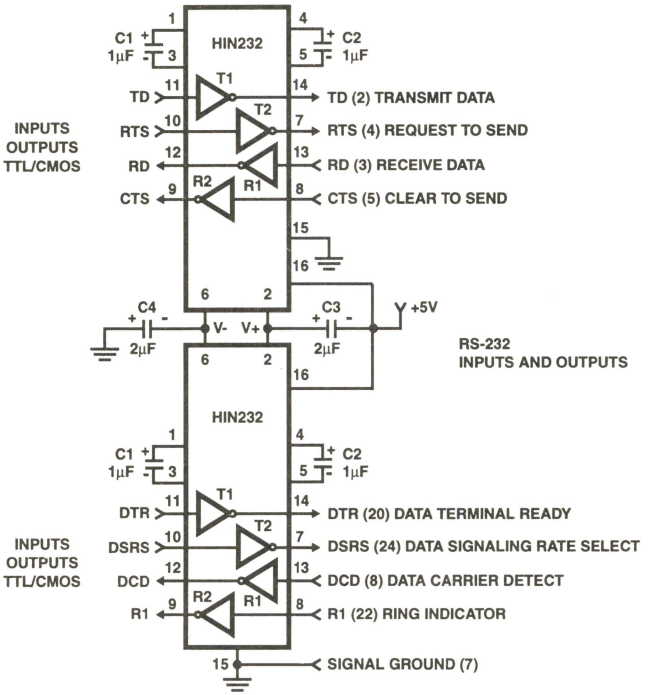


FIGURE 10. COMBINING TWO HIN232s FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS

Die Characteristics

DIE DIMENSIONS:

160 mils x 140 mils

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

SUBSTRATE POTENTIAL

V+

PASSIVATION:

Type: Nitride over Silox
Nitride Thickness: 8kÅ
Silox Thickness: 7kÅ

TRANSISTOR COUNT:

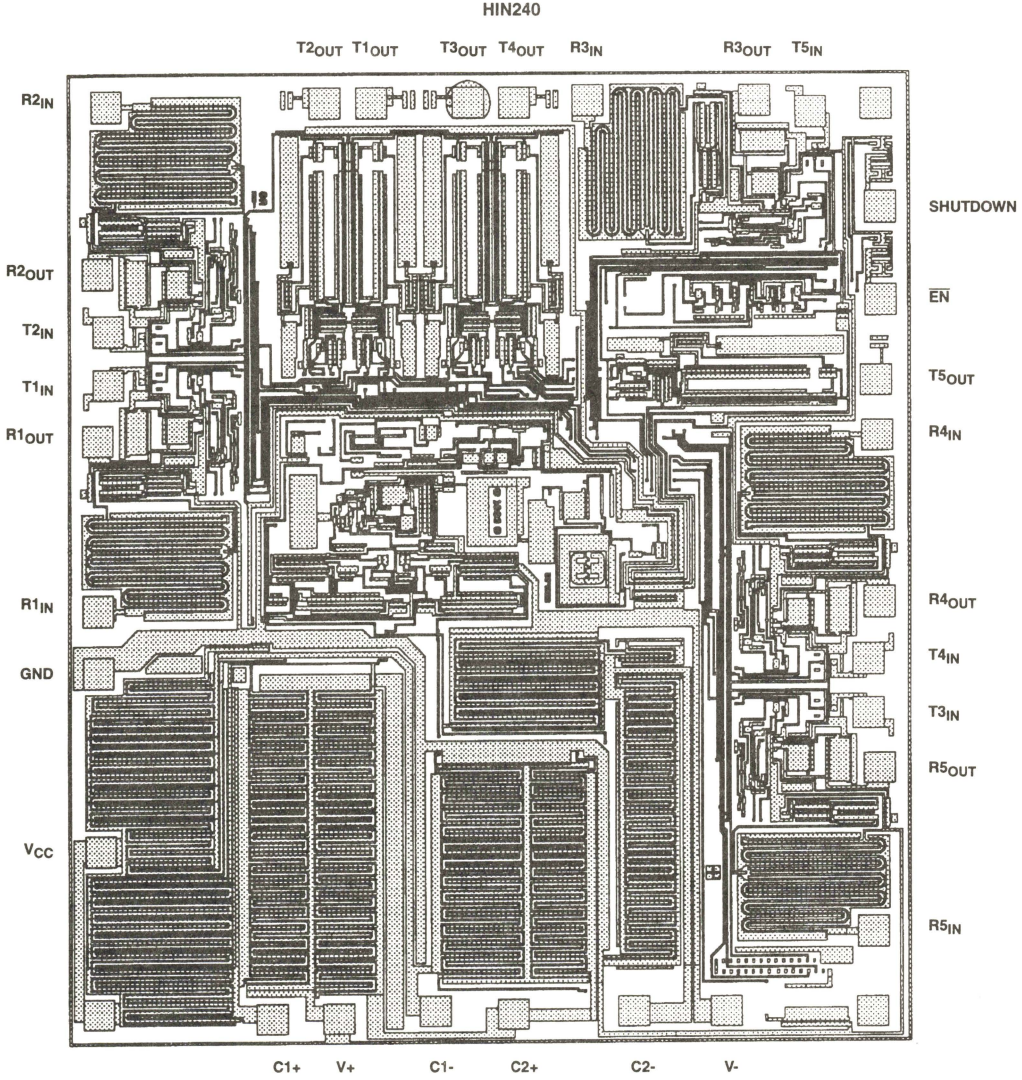
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PROCESS:

CMOS Metal Gate

Metallization Mask Layout

HIN240



MICROPROCESSOR PRODUCTS 6

CMOS MEMORY

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CMOS Memory (Continued)

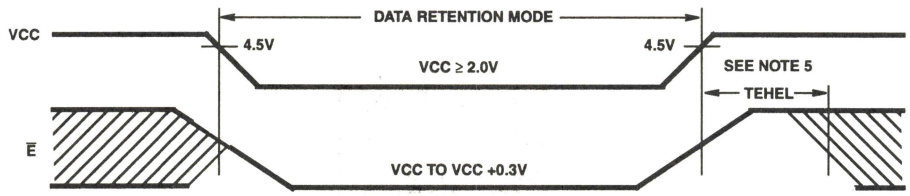
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HM-XXXX Series Low Voltage Data Retention

HARRIS HM-XXXX Series CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC to VCC +0.3V
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC +0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL (for synchronous RAMs) and >5ns (for asynchronous RAMs) after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



Industry CMOS RAM Cross Reference

HARRIS CMOS RAMs

DESCRIPTION	HARRIS	AMD	EDI	FUJI-TSU	HIT-ACHI	IDT	MITSU-BISHI	MOT-OROLA	NAT-IONAL	NEC	OKI	HARRIS/ RCA	SMOS	TOSH-IBA	NMOS, OTHER
1K CMOS RAMs															
1k x 1, 16 Pin Synchronous	HM-6508	-	-	8401	-	-	-	6508	6508 74C929	443	-	6508 1821	-	5508	2125, 4015
1K x 1, 18 Pin Synchronous	HM-6518	-	-	-	-	-	-	6518	6518 74C930	-	-	-	-	-	-
256 x 4, 22 Pin Synchronous	HM-6551	-	-	-	-	-	-	-	6551 74C920	-	-	1822 5101	-	5101	2101
256 x 4, 18 Pin Synchronous	HM-6561	-	-	-	-	-	-	-	-	-	-	-	-	-	2111
4K CMOS RAMs															
4K x 1, 18 Pin Synchronous	HM-6504	92L44	-	8404	4315 6147	-	-	6504	6504	-	5104	-	6504	5504	2141, 2147, 315D, 4104, 4404
1K x 4, 18 Pin Synchronous	HM-6514	91L14 91L24	-	8414	4334 6148	-	58981	6514	6514	444	5114 5115	5114	6514	5514	2114, 2148, 2149, 4045, 314A
16K CMOS RAMs															
2K x 8, 24 Pin Synchronous	HM-6516	-	-	-	-	-	-	-	6516	-	-	-	-	-	-
2K x 8, 24 Pin Asynchronous	HM-65162	-	-	8416	6116	6116	5117	65116	6116	446	5128	6116	2016	5517	4802, 2116, 2016, 4016
16K x 1, 20 Pin Asynchronous	HM-65262	-	-	8167	6167	6167	-	-	-	-	-	-	2267 2367	-	2167, 8167,1400
64K CMOS RAMs															
8K x 8, 28 Pin Asynchronous	HM-65642 HM-8808A† HM-8808†	99C88	8808A 8808	8464	6264	7164 7M864 8M864	5164	6164	6164	4464	-	6264	2064 2264	5564 5565	
128K CMOS RAM MODULE															
16K x 8, 28 Pin Asynchronous	HM-8816H	-	8816H												
256K CMOS RAM MODULE															
32K x 8/16K x 16 48 Pin Module Asynchronous	HM-92560 HM-92570	-	-	-	-	-	-	-	-	-	-	-	-	-	-
32K x 8 28 Pin Module Asynchronous	HM-8832	-	8832	-	-	-	-	-	-	-	-	-	-	-	-
1M CMOS MODULE															
128 x 8/64K x 16	HM-91M2	-	-	-	-	-	-	-	-	-	-	-	-	-	-

† CMOS RAM Module

HARRIS SEMICONDUCTOR

CDP1821C/3

High-Reliability CMOS 1024-Word x 1-Bit Static RAM

March 1997

Features

- Static CMOS Silicon-On-Sapphire Circuitry CD4000-Series Compatible
- Compatible with CDP1800-Series Microprocessors at Maximum Speed
- Fast Access Time. . . . . 100ns Typ. at V_{DD} = 5V
- Single Voltage Supply
- No Precharge or External Clocks Required
- Low Quiescent and Operating Power
- Separate Data Inputs and Outputs
- High Noise Immunity . . . . . 30% of V_{DD}
- Memory Retention for Standby Battery Voltage Down to 2V at +25°C
- Latch-Up-Free Transient-Radiation Tolerance

Ordering Information

PACKAGE	TEMP. RANGE	PART NUMBER	PKG. NO.
SBDIP	-55°C to +125°C	CDP1821CD3	D16.3

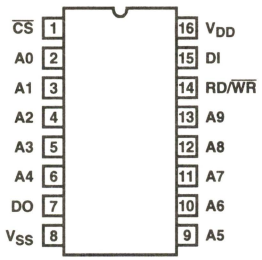
Description

The CDP1821C/3 is a 1024-word x 1-bit CMOS silicon-on-sapphire (SOS), fully static, random-access memory designed for use in CDP1800 microprocessor systems. This device has a recommended operating voltage range of 4V to 6.5V.

The output state of the CDP1821C/3 is a function of the input address and chip-select states only. Valid data will appear at the output in one access time following the latest address change to a selected chip. After valid data appears, the address may be changed immediately. It is not necessary to clock the chip-select input or any other input terminal for fully static operation; therefore the chip-select input may be used as an additional address input. When the device is in an unselected state ($\overline{CS}$ = 1), the internal write circuitry and output sense amplifier are disabled. This feature allows the three-state data outputs from many arrays to be OR-tied to a common bus for easy memory expansion.

Pinout

CDP1821C/3
(SBDIP)
TOP VIEW

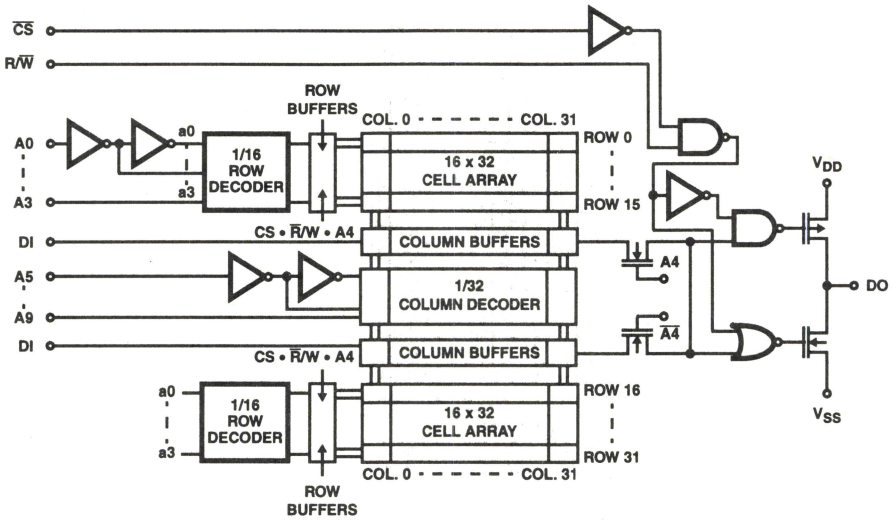


6 CMOS MEMORY

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **2983.1**

Functional Block Diagram



OPERATIONAL MODES

MODE	INPUTS		OUTPUT
	READ/WRITE R/$\overline{W}$	CHIP-SELECT $\overline{CS}$	DATA OUTPUT DO
Standby	X	1	High Impedance
Write	0	0	High Impedance
Read	1	0	Contents of Addressed Call

X = Don't Care Logic 1 = High Logic 0 = Low

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal) ..... -0.5V to +7V
Input Voltage Range, All Inputs ..... -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input ..... ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	75	20

Maximum Operating Temperature Range (T_A) ....-55°C to +125°C
Maximum Storage Temperature Range (T_{STG}) ...-65°C to +150°C
Maximum Lead Temperature (During Soldering) .....+265°C
Maximum Junction Temperature .....+150°C

Recommended Operating Conditions

T_A = Full Package-Temperature Range. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	CDP1821CD/3		UNITS
	MIN	MAX	
DC Operating Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V

Static Electrical Specifications

V_{DD} = 5V ±5%

PARAMETER	SYMBOL	CONDITIONS	-55°C, +25°C		+125°C		UNITS
			MIN	MAX	MIN	MAX	
Quiescent Device Current (Note 1)	I_{DD}	V_{IN} = 0V or V_{DD}	-	260	-	1000	µA
Output Low Drive (Sink) Current (Note 1)	I_{OL}	V_{OUT} = 0.4V	2.7	-	1.6	-	mA
Output High Drive (Source) Current (Note 1)	I_{OH}	V_{OUT} = V_{DD} -0.4V	-1.3	-	-0.8	-	mA
Output Voltage Low-Level	V_{OL}	-	-	0.1	-	0.5	V
Output Voltage High-Level	V_{OH}	-	V_{DD}-0.1	-	V_{DD}-0.5	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{DD}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	0.7 V_{DD}	-	V
Input Current (Note 1)	I_{IN}	V_{IN} = 0V or V_{DD}	-	2.6	-	10	µA
Three-State Output Leakage Current (Note 1)	I_{OUT}	V_{IN} = 0V or V_{DD}	-	2.6	-	10	µA
Operating Current (Note 2)	I_{DD1}	-	-	5	-	10	mA
Input Capacitance	C_{IN}	-	-	7.5	-	7.5	pF
Output Capacitance	C_{OUT}	-	-	15	-	15	pF

NOTES:

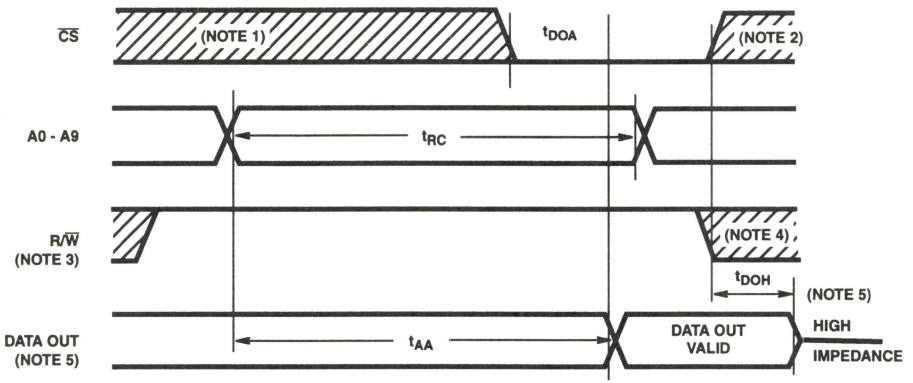
1. Limits designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing
2. Measured with 1µs read-cycle time and outputs floating.

Read Cycle Dynamic Electrical Specifications t_R, t_F = 10ns, C_L = 50pF

PARAMETER	SYMBOL	V_{DD} (V)	-55°C, +25°C		+125°C		UNITS
			MIN	MAX	MIN	MAX	
Data Access Time (Note 1)	t_{DA}	5	-	190	-	255	ns
Read Cycle Time	t_{RC}	5	190	-	255	-	ns
Output Enable Time	t_{EN}	5	65	-	90	-	ns
Output Disable Time	t_{DIS}	5	-	65	-	90	ns

NOTE:

1. 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.



NOTES:

1. Chip-Select ($\overline{CS}$) permitted to change from high to low level or remain low on a selected device.
2. Chip-Select ($\overline{CS}$) permitted to change from low to high level or remain low.
3. Read/Write (R/$\overline{W}$) must be at a high level during all address transitions.
4. Don't care.
5. Data-Out (DO) is a high impedance within t_{DIS} ns after the falling edge of R/$\overline{W}$ or the rising edge of $\overline{CS}$.

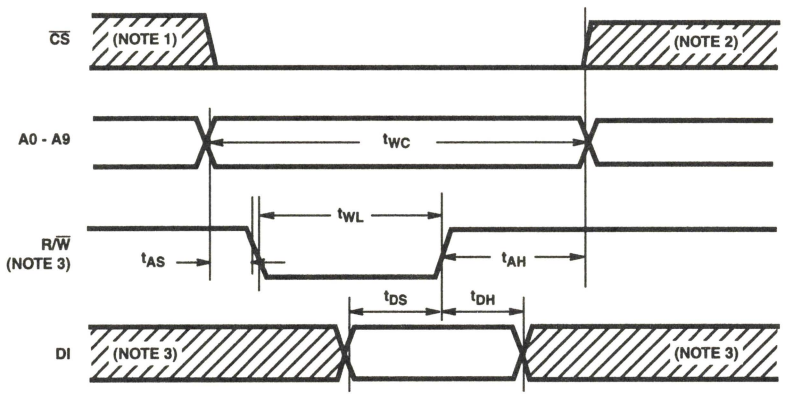
FIGURE 1. READ CYCLE TIMING DIAGRAM

Write Cycle Dynamic Electrical Specifications t_R, t_F = 10ns, C_L = 50pF

PARAMETER	SYMBOL	V_{DD} (V)	-55°C, +25°C		+125°C		UNITS
			MIN	MAX	MIN	MAX	
Write Cycle Time	t_{WC}	5	300	-	420	-	ns
Address Setup Time (Note 1)	t_{AS}	5	60	-	84	-	ns
Address Hold Time (Note1)	t_{AH}	5	130	-	180	-	ns
Input Data Setup Time (Note 1)	t_{DS}	5	90	-	125	-	ns
Input Data Hold Time (Note 1)	t_{DH}	5	60	-	84	-	ns
Read/$\overline{\text{Write}}$ Pulse Width Low (Note 1)	t_{WL}	5	110	-	155	-	ns

NOTE:

1. 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.



NOTES:

1. Chip-Select ($\overline{CS}$) permitted to change from high to low level or remain low on a selected device.
2. Chip-Select ($\overline{CS}$) permitted to change from low to high level or remain low.
3. Don't care.

FIGURE 2. WRITE CYCLE TIMING DIAGRAM

Data Retention Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		-55°C, +25°C		+125°C		UNITS
		V_{DR} (V)	V_{DD} (V)	MIN	MAX	MIN	MAX	
Minimum Data Retention Voltage (Note 1)	V_{DD}	-	-	-	2	-	2.5	V
Data Retention Quiescent Current (Note 1)	I_{DD}	2	-	-	50	-	200	µA
Chip Deselect to Data Retention Time	t_{CDR}	-	5	450	-	650	-	ns
Recovery to Normal Operation Time	t_{RC}	-	5	450	-	650	-	ns

NOTE:

1. 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing

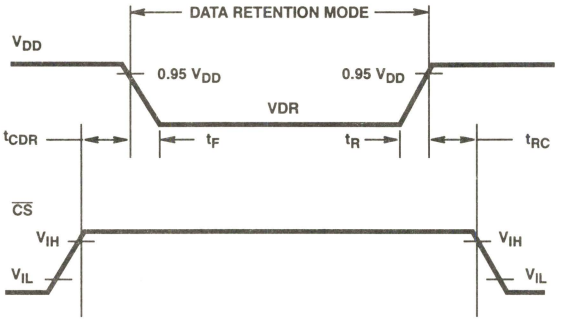
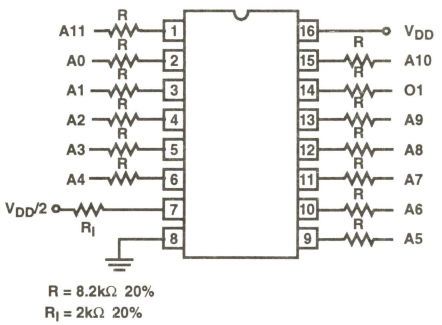
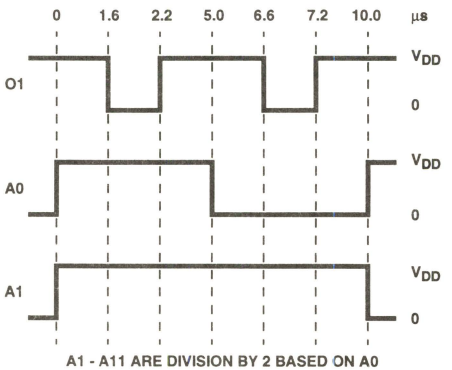


FIGURE 3. LOW V_{DD} DATA RETENTION WAVEFORMS AND TIMING DIAGRAM

Burn-In Circuit



R = 8.2kΩ 20%
R_I = 2kΩ 20%



A1 - A11 ARE DIVISION BY 2 BASED ON A0

PACKAGE	V_{DD}	TEMPERATURE	DURATION
D	7V	+125°C	160 Hrs.

FIGURE 4. DYNAMIC/OPERATING BURN-IN CIRCUIT AND TIMING DIAGRAM

HARRIS SEMICONDUCTOR

CDP1822, CDP1822C

256-Word x 4-Bit LSI Static RAM

March 1997

Features

- Low Operating Current
  - V_{DD} = 5V, Cycle Time 1μs 8mA
- Industry Standard Pinout
- Two Chip-Select Inputs-Simple Memory Expansion
- Memory Retention for Standby Battery Voltage of 2V Minimum
- Output-Disable for Common I/O Systems
- Three-State Data Output for Bus-Oriented Systems
- Separate Data Inputs and Outputs

Ordering Information

5V	10V	PACKAGE	TEMP. RANGE	PKG. NO.
CDP1822CE	CDP1822E	PDIP	-40°C to +85°C	E22.4
CDP1822CEX	CDP1822EX	Burn-In		E22.4
CDP1822CD	CDP1822D	SBDIP	-40°C to +85°C	D22.4A
CDP1822CDX	-	Burn-In		D22.4A

Description

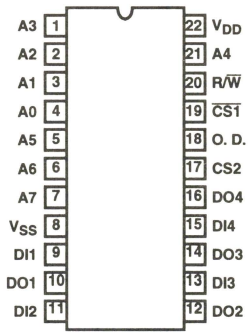
The CDP1822 and CDP1822C are 256-word by 4-bit static random-access memories designed for use in memory systems where high speed, low operating current, and simplicity in use are desirable. The CDP1822 features high speed and a wide operating voltage range. Both types have separate data inputs and outputs and utilize single power supplies of 4V to 6.5V for the CDP1822C and 4V to 10.5V for the CDP1822.

Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems. The Output Disable input allows these RAMs to be used in common data Input/Output systems by forcing the output into a high-impedance state during a write operation independent of the Chip-Select input condition. The output assumes a high-impedance state when the Output Disable is at high level or when the chip is deselected by $\overline{CS1}$ and/or CS2.

The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5V operation, excellent system noise margin is preserved by using an external pull-up resistor at each input.

Pinout

CDP1822, CDP1822C
(PDIP, SBDIP)
TOP VIEW



OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	$\overline{CHIP\ SELECT\ 1}$ ($\overline{CS_1}$)	CHIP SELECT 2 (CS_2)	OUTPUT DISABLE (OD)	$\overline{READ/WRITE}$ (R/$\overline{W}$)	
Read	0	1	0	1	Read
Write	0	1	0	0	Data In
Write	0	1	1	0	High Impedance
Standby	1	X	X	X	High Impedance
Standby	X	0	X	X	High Impedance
Output Disable	X	X	1	X	High Impedance

NOTE:
Logic 1 = High, Logic 0 = Low, X = Don't Care.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 1074.2

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1822 ..... -0.5V to +11V
CDP1822C ..... -0.5V to +7V
Input Voltage Range, All Inputs ..... -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input ..... ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	75	N/A
SBDIP Package	80	21

Maximum Operating Temperature Range (T_A)
Package Type D ..... -55°C to +125°C
Package Type E ..... -40°C to +85°C
Maximum Junction Temperature
Ceramic Package ..... 175°C
Plastic Package ..... 150°C
Storage Temperature Range (T_{STG}) ..... -65°C to +150°C
T_A = -40°C to +60°C (Package Type E) 500mW
T_A = +60°C to +85°C (Package Type E) ..... Derate Linearly at 12mW/°C to 200mW
Lead Temperature (During Soldering) ..... 300°C

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	SYMBOL	LIMITS				UNITS
		CDP1822		CDP1822C		
		MIN	MAX	MIN	MAX	
DC Operating Voltage Range		4	10.5	4	6.5	V
Input Voltage Range		V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Static Electrical Specifications

At T_A = -40°C to +85°C, Except as Noted

PARAMETER	SYMBOL	CONDITIONS			LIMITS						UNITS
					CDP1822			CDP1822C			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	-	500	-	-	500	µA
		-	0, 10	10	-	-	1000	-	-	-	µA
Output Low (Sink) Current	I_{OL}	0.4	0, 5	5	2	4	-	2	4	-	mA
		0.5	0, 10	10	4.5	9	-	-	-	-	mA
Output High (Source) Current	I_{OH}	4.6	0, 5	5	-1	-2	-	-1	-2	-	mA
		9.5	0, 10	10	-2.2	-4.4	-	-	-	-	mA
Output Voltage Low-Level	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High-Level	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 9.5	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 9.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	-	0, 5	5	-	-	±5	-	-	±5	µA
		-	0, 10	10	-	-	±10	-	-	-	µA

Static Electrical Specifications At T_A = -40°C to +85°C, Except as Noted (Continued)

PARAMETER	SYMBOL	CONDITIONS			LIMITS						UNITS
					CDP1822			CDP1822C			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Operating Current (Note 2)	I_{DD1}	-	0, 5	5	-	4	8	-	4	8	mA
		-	0, 10	10	-	8	16	-	-	-	mA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	-	±5	-	-	±5	µA
		0, 10	0, 10	10	-	-	±10	-	-	-	µA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = +25°C and nominal V_{DD}.
2. Outputs open circuited; Cycle time = 1µs.

Dynamic Electrical Specifications At T_A + -40 to +85°C, V_{DD} ±5%, Input t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

PARAMETER		TEST CONDITIONS	LIMITS						UNITS
			CD1822			CDP1822C			
		V_{DD} (V)	(NOTE 1) MIN	(NOTE 2) TYP	MAX	(NOTE 1) MIN	(NOTE 2) TYP	MAX	
Read Cycle Times (Figure 1)									
Read Cycle	t_{RC}	5	450	-	-	450	-	-	ns
		10	250	-	-	-	-	-	ns
Access from Address	t_{AA}	5	-	250	450	-	250	450	ns
		10	-	150	250	-	-	-	ns
Output Valid from $\overline{\text{Chip-Select}}$ 1	t_{DOA1}	5	-	250	450	-	250	450	ns
		10	-	150	250	-	-	-	ns
Output Valid from Chip-Select 2	t_{DOA2}	5	-	250	450	-	250	450	ns
		10	-	150	250	-	-	-	ns
Output Valid from Output Disable	t_{DOA3}	5	-	-	200	-	-	200	ns
		10	-	-	110	-	-	-	ns
Output Hold from $\overline{\text{Chip-Select}}$ 1	t_{DOH1}	5	20	-	-	20	-	-	ns
		10	20	-	-	-	-	-	ns
Output Hold from Chip-Select 2	t_{DOH2}	5	20	-	-	20	-	-	ns
		10	20	-	-	-	-	-	ns
Output Hold from Output Disable	t_{DOH3}	5	20	-	-	20	-	-	ns
		10	20	-	-	-	-	-	ns

NOTES:

1. Time required by a limit device to allow for indicated function.
2. Typical values are for T_A = 25°C and nominal V_{DD}.

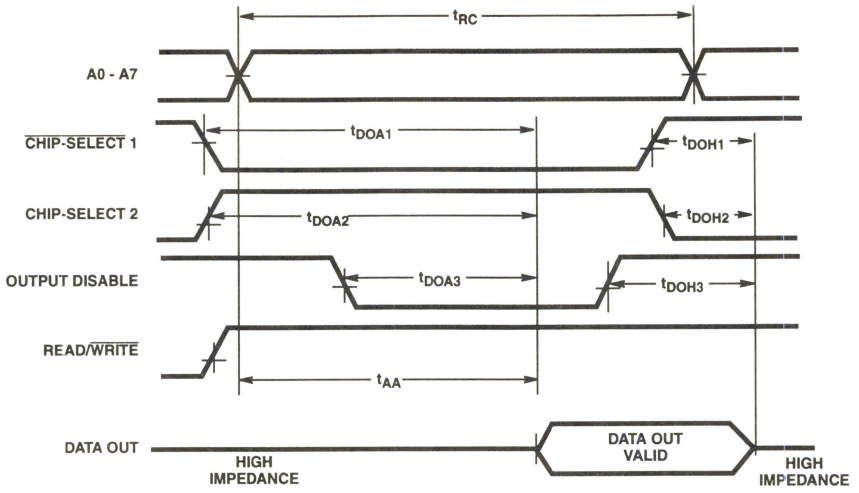


FIGURE 1. READ CYCLE TIMING WAVEFORMS

Dynamic Electrical Specifications At T_A + -40 to +85°C, V_{DD} ±5%, Input t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF.

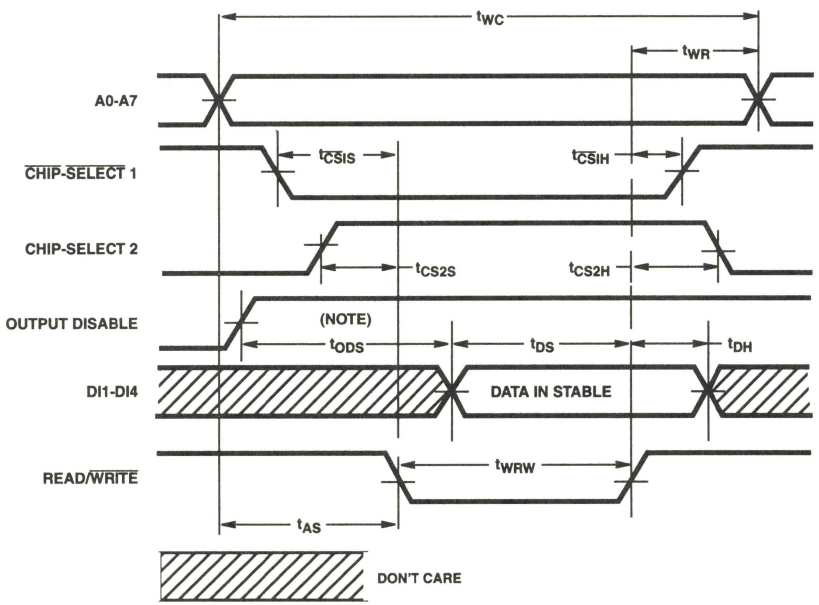
PARAMETER		TEST CONDITIONS	LIMITS						UNITS
			CD1822			CDP1822C			
		V_{DD} (V)	(NOTE 1) MIN	(NOTE 2) TYP	MAX	(NOTE 1) MIN	(NOTE 2) TYP	MAX	
Read Cycle Times (Figure 2)									
Write Cycle	t_{WC}	5	500	-	-	500	-	-	ns
		10	300	-	-	-	-	-	ns
Address Setup	t_{AS}	5	200	-	-	200	-	-	ns
		10	110	-	-	-	-	-	ns
Write Recovery	t_{WR}	5	50	-	-	50	-	-	ns
		10	40	-	-	-	-	-	ns
Write Width	t_{WRW}	5	250	-	-	250	-	-	ns
		10	150	-	-	-	-	-	ns
Input Data Setup Time	t_{DS}	5	250	-	-	250	-	-	ns
		10	150	-	-	-	-	-	ns
Data Hold	t_{DH}	5	50	-	-	50	-	-	ns
		10	40	-	-	-	-	-	ns
$\overline{\text{Chip-Select}}$ 1 Setup	$t_{\overline{CS}1S}$	5	200	-	-	200	-	-	ns
		10	110	-	-	-	-	-	ns
Chip-Select 2 Setup	t_{CS2S}	5	200	-	-	200	-	-	ns
		10	110	-	-	-	-	-	ns

Dynamic Electrical Specifications At T_A + -40 to +85°C, V_{DD} ±5%, Input t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF. **(Continued)**

PARAMETER		TEST CONDITIONS	LIMITS						UNITS
			CD1822			CDP1822C			
		V_{DD} (V)	(NOTE 1) MIN	(NOTE 2) TYP	MAX	(NOTE 1) MIN	(NOTE 2) TYP	MAX	
$\overline{\text{Chip-Select}}$ 1 Hold	$t_{\overline{CS}1H}$	5	0	-	-	0	-	-	ns
		10	0	-	-	0	-	-	ns
Chip-Select 2 Hold	t_{CS2H}	5	0	-	-	0	-	-	ns
		10	0	-	-	0	-	-	ns
Output Disable Set-Up	t_{ODS}	5	200	-	-	200	-	-	ns
		10	110	-	-	-	-	-	ns

NOTES:

1. Time required by a limit device to allow for indicated function.
2. Typical values are for T_A = 25°C and nominal V_{DD}.



NOTE: t_{ODS} is required for common I/O operation only. For separate I/O operations, output disable is don't care.

FIGURE 2. WRITE CYCLE TIME WAVEFORMS

Data Retention Specifications At T_A = -40 to +85°C, see Figure 3.

PARAMETER		TEST CONDITIONS		LIMITS						UNITS
				CDP1822			CDP1822C			
		V_{DR} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Min. Data Retention Voltage	V_{DR}	-	-	-	1.5	2	-	1.5	2	V
Data Retention Quiescent Current	I_{DD}	2	-	-	30	100	-	30	100	µA
Chip Deselect to Data Retention Time	t_{CDR}	-	5	600	-	-	600	-	-	ns
		-	10	300	-	-	-	-	-	ns
Recovery to Normal Operation Time	t_{RC}	-	5	600	-	-	600	-	-	ns
		-	10	300	-	-	-	-	-	ns
V_{DD} to VDR Rise and Fall Time	t_R, t_F	2	5	1	-	-	1	-	-	µA

NOTE: Typical values are for T_A = 25°C and nominal V_{DD}.

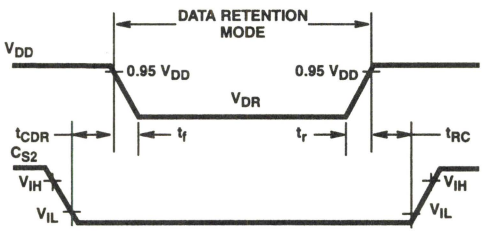


FIGURE 3. LOW V_{DD} DATA RETENTION TIME WAVEFORMS

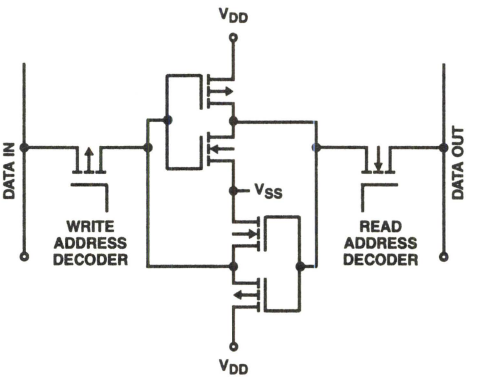


FIGURE 4. MEMORY CELL CONFIGURATION

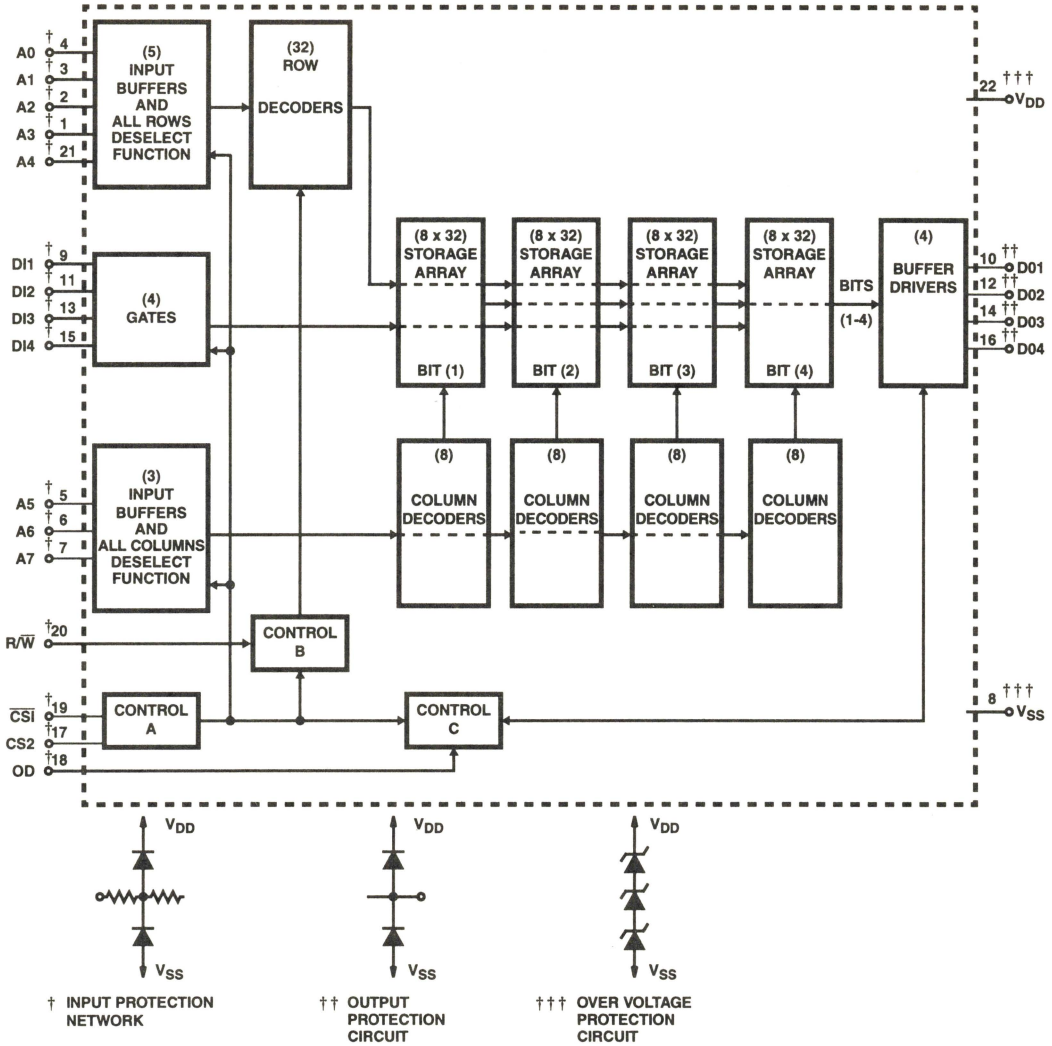


FIGURE 5. FUNCTIONAL BLOCK DIAGRAM FOR CDP1822 AND CDP1822C

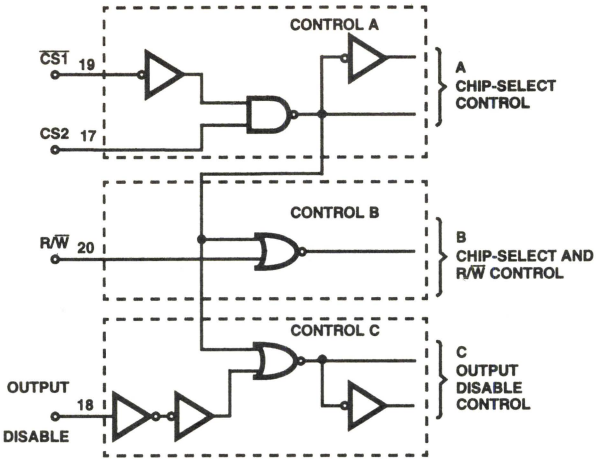


FIGURE 6. LOGIC DIAGRAM OF CONTROLS FOR CDP1822 AND CDP1822C

HARRIS SEMICONDUCTOR

CDP1822C/3

High-Reliability CMOS 256-Word x 4-Bit LSI Static RAM

March 1997

Features

- For Applications in Aerospace, Military, and Critical Industrial Equipment
- Interfaces Directly with CDP1802 Microprocessor
- Very Low Operating Current
  - At V_{DD} = 5V and Cycle Time = 1μs . . . . . 4mA (Typ)
- Static CMOS Silicon-On-Sapphire Circuitry
  - CD4000 Series Compatible
- Industry Standard Pinout
- Two Chip Select Inputs - Simple Memory Expansion
- Memory Retention for Standby. . . . . 2V (Min) Battery Voltage
- Single Power Supply Operation . . . . . 4V to 6.5V
- High Noise Immunity 30% of V_{DD}. . . . . 4V to 6.5V
- Output Disable for Common I/O Systems
- Three-State Data Output for Bus Oriented Systems
- Separate Data Inputs and Outputs
- Latch-Up-Free Transient Radiation Tolerance

Description

The CDP1822C/3 is a 256 word by 4-bit random access memory designed for use in memory systems where high speed, low operating current, and simplicity in use are desirable. The CDP1822 features high speed and excellent noise immunity. It has separate data inputs and outputs and utilizes a single power supply of 4V to 6.5V.

Two Chip Select inputs simplify system expansion. An output Disable control provides Wire-OR-capability and is also useful in common Input/Output systems. The Output Disable input allows this RAM to be used in common data Input/Output systems by forcing the output into a high impedance state during a write operation independent of the Chip Select input condition. The output assumes a high impedance state when the Output Disable is at high level or when the chip is deselected by $\overline{CS1}$ and/or CS2.

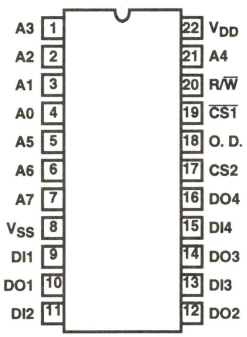
The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5V operation, excellent system noise margin is preserved by using an external pull-up resistor at each input.

Ordering Information

PACKAGE	TEMP. RANGE	PART NUMBER	PKG. NO.
SBDIP	-55°C to +125°C	CDP1822CD3	D22.4A

Pinout

CDP1822C/3 (SBDIP)
TOP VIEW



OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	$\overline{CHIP\ SELECT\ 1}$ ($\overline{CS1}$)	CHIP SELECT 2 (CS2)	OUTPUT DISABLE (OD)	$\overline{READ/WRITE}$ (R/$\overline{W}$)	
Read	0	1	0	1	Read
Write	0	1	0	0	Data In
Write	0	1	1	0	High Impedance
Standby	1	X	X	X	High Impedance
Standby	X	0	X	X	High Impedance
Output Disable	X	X	1	X	High Impedance

Logic 1 = High, Logic 0 = Low, X = Don't Care

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1822C/3 . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	80	21

Maximum Storage Temperature Range (T_{STG}) . . . -65°C to +150°C
Maximum Lead Temperature (During Soldering) . . . . . +265°C
Maximum Junction Temperature . . . . . +150°C

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS		UNITS
	MIN	MAX	
DC Operating Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V

Static Electrical Specifications

PARAMETER	SYMBOL	CONDITIONS			LIMITS				UNITS
					-55°C, +25°C		+125°C		
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	MAX	MIN	MAX	
Quiescent Device Current (Note 1)	I_{DD}	-	0, 5	5	-	390	-	1000	µA
Output Low (Sink) Current (Note 1)	I_{OL}	0.4	0, 5	5	2.6	-	1.6	-	mA
Output High (Source) Current (Note 1)	I_{OH}	4.6	0, 5	5	-	-1.2	-	-0.8	mA
Output Voltage Low-Level	V_{OL}	-	0, 5	5	-	0.1	-	0.5	V
Output Voltage High-Level	V_{OH}	-	0, 5	5	V_{DD} - 0.1	-	V_{DD} - 0.5	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	0.3 V_{DD}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	0.7 V_{DD}	-	0.7 V_{DD}	-	V
Input Leakage Current (Note 1)	I_{IN}	-	0, 5	5	-	±3.2	-	±10	µA
Operating Current (Note 1)	I_{DD1}	-	0, 5	5	-	6.5	-	10	mA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	±3.2	-	± 19	µA
Input Capacitance	C_{IN}	-	-	-	-	7.5	-	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	7.5	-	7.5	pF

NOTE:

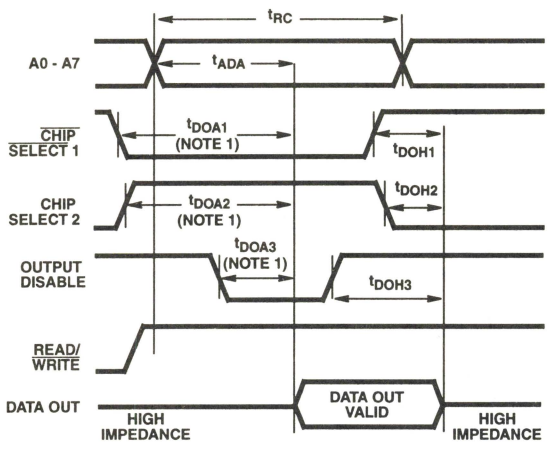
1. Limits designate 100% testing, all other limits are designer's parameters under given test conditions and do not represent 100% testing.

Read Cycle Dynamic Electrical Specifications t_R, t_F = 10ns, C_L = 50pF

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS				UNITS
			+25°C, -55°C		+125°C		
			MIN	MAX	MIN	MAX	
Read Cycle (Note 1)	t_{RC}	5	370	-	500	-	ns
Access from Address (Note 1)	t_{ADA}	5	-	370	-	500	ns
Output Valid from $\overline{\text{Chip Select}}$ 1 (Note 1)	t_{DOA1}	5	-	370	-	500	ns
Output Valid from Chip Select 2 (Note 1)	t_{DOA2}	5	-	370	-	500	ns
Output Active from Output Disable (Note 1)	t_{DOA3}	5	-	170	-	225	ns
Output Hold from $\overline{\text{Chip Select}}$ 1	t_{DOH1}	5	10	-	20	-	ns
Output Hold from Chip Select 2	t_{DOH2}	5	10	-	20	-	ns
Output Hold from Output Disable	t_{DOH3}	5	10	-	20	-	ns

NOTE:

1. Limits designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing



NOTE: Minimum timing for valid data output. Longer times will initiate an earlier but invalid output.

FIGURE 1. READ CYCLE WAVEFORMS AND TIMING DIAGRAM

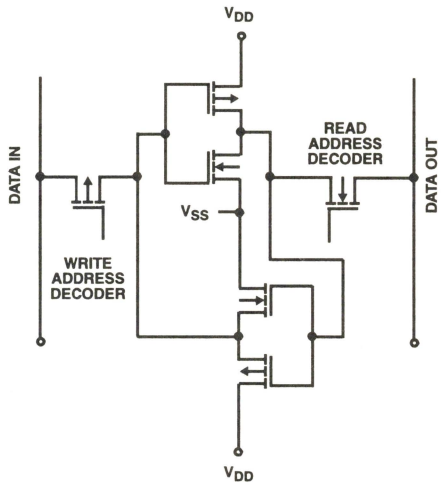


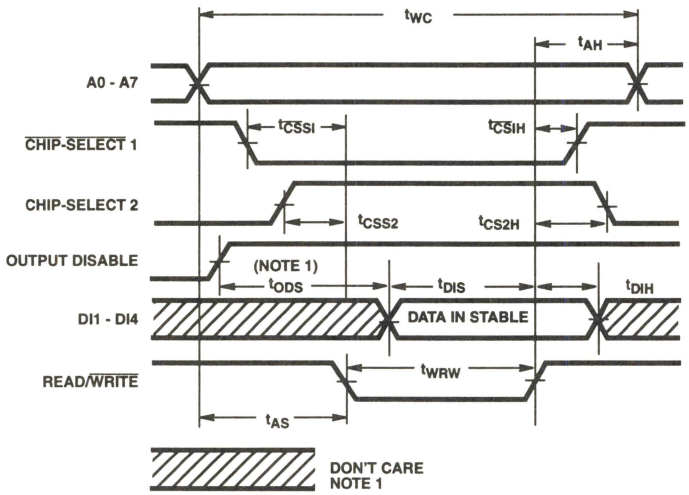
FIGURE 2. MEMORY CELL CONFIGURATION

Write Cycle Dynamic Electrical Specifications t_R, t_F = 10ns, C_L = 50pF

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS				UNITS
			+25°C, -55°C		+125°C		
			MIN	MAX	MIN	MAX	
Write Cycle (Note 1)	t_{WC}	5	400	-	560	-	ns
Address Setup (Note 1)	t_{AS}	5	160	-	225	-	ns
Address Hold (Note 1)	t_{AH}	5	40	-	55	-	ns
Write Pulse Width (Note 1)	t_{WRW}	5	200	-	280	-	ns
Data in Setup (Note 1)	t_{DIS}	5	200	-	280	-	ns
Data in Hold (Note 1)	t_{DIH}	5	40	-	55	-	ns
$\overline{\text{Chip Select}}$ 1 Setup	$t_{\overline{CSS}1}$	5	200	-	280	-	ns
Chip Select 2 Setup	t_{CSS2}	5	200	-	280	-	ns
Output Disable Setup	t_{ODS}	5	140	-	225	-	ns

NOTE:

1. Limits designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing



NOTE:

1. t_{ODS} is required for common I/O operation only; for separate I/O operations, output disable is don't care.

FIGURE 3. WRITE CYCLE TIMING WAVEFORMS

Data Retention Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_{DR} (V)	TEST CONDITIONS V_{DD} (V)	LIMITS +25°C, -55°C MIN	LIMITS +25°C, -55°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
Minimum Data Retention Voltage (Note 1)	V_{DR}	-	-	-	2	-	2.5	V
Data Retention Quiescent Current (Note 1)	I_{DD}	2	-	-	70	-	380	µA
Chip Deselect to Data Retention Time	t_{CDR}	-	5	450	-	650	-	ns
		-	10					
Recovery to Normal Operation Time	t_{RC}	5	5	450	-	650	-	ns

NOTE:

1. Limits designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

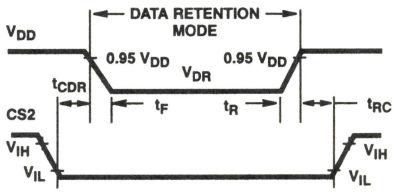
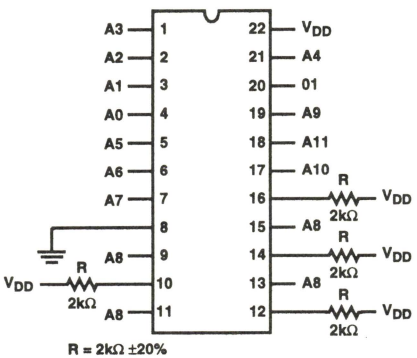


FIGURE 4. LOW V_{DD} DATA RETENTION TIMING WAVEFORMS

PACKAGE	TEMPERATURE	DURATION	V_{DD}
D	125°C	160 Hrs	7V



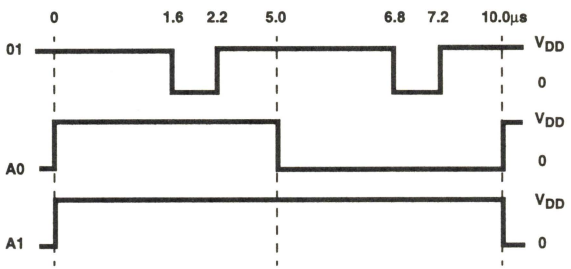


FIGURE 5. DYNAMIC/OPERATING BURN-IN CIRCUIT AND TIMING DIAGRAM

HARRIS SEMICONDUCTOR

CDP1823, CDP1823C

128-Word x 8-Bit LSI Static RAM

March 1997

Features

- **Fast Access Time**
  - V_{DD} = 5V 450ns
  - V_{DD} = 10V 250ns
- **Common Data Inputs and Outputs**
- **Multiple Chip Select Inputs to Simplify Memory System Expansion**

Ordering Information

5V	10V	PACKAGE	TEMP. RANGE	PKG. NO.
CDP1823CE	CDP1823E	PDIP	-40°C to +85°C	E24.6
CDP1823CD	CDP1823D	SBDIP	-40°C to +85°C	D24.6
CDP1823CDX	-	Burn-In		D24.6

Description

The CDP1823 and CDP1823C are 128-word by 8-bit CMOS SOS static random-access memories. These memories are compatible with general-purpose microprocessors. The two memories are functionally identical. They differ in that the CDP1823 has a recommended operating voltage range of 4V to 10.5V, and the CDP1823C has a recommended operating voltage range of 4V to 6.5V.

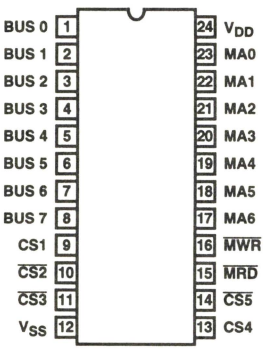
The CDP1823 memory has 8 common data input and data output terminals for direct connection to a bidirectional data bus and is operated from a single voltage supply. Five chip-select inputs are provided to simplify memory-system expansion. In order to enable the CDP1823, the chip-select inputs $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS5}$ require a low input signal, and the chip-select inputs CS1 and CS4 require a high input signal.

The $\overline{MRD}$ signal enables all 8 output drivers when in the low state and should be in a high state during a write cycle.

After valid data appear at the output, the address inputs may be changed immediately. Output data will be valid until either the $\overline{MRD}$ signal goes high, the device is deselected, or t_{AA} (access time) after address changes.

Pinout

CDP1823, CDP1823C
(PDIP, SBDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1198.2**

OPERATIONAL MODES

FUNCTION	$\overline{MRD}$	$\overline{MWR}$	CS1	$\overline{CS2}$	$\overline{CS3}$	CS4	$\overline{CS5}$	BUS TERMINAL STATE
Read	0	X	1	0	0	1	0	Storage State of Addressed Word
Write	1	0	1	0	0	1	0	Input High-Impedance
Stand-By (Active)	1	1	1	0	0	1	0	High Impedance
Not Selected	X	X	0	X	X	X	X	High Impedance
	X	X	X	1	X	X	X	High Impedance
	X	X	X	X	1	X	X	High Impedance
	X	X	X	X	X	0	X	High Impedance
	X	X	X	X	X	X	1	High Impedance

Logic 1 = High, Logic 0 = Low, X = Don't Care

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1823 . . . . . -0.5V to +11V
CDP1823C. . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA
Operating Temperature Range (T_A)
Package Type D . . . . . -55°C to +125°C
Package Type E . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	60	N/A
SBDIP Package	60	17

Maximum Storage Temperature Range (T_{STG}) . . . -65°C to +150°C
Maximum Junction Temperature
Plastic Package . . . . . +150°C
Maximum Lead Temperature (During Soldering) . . . . . 300°C

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS				UNITS
	CDP1823D		CDP1823CD		
	MIN	MAX	MIN	MAX	
Supply Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Static Electrical Specifications

At T_A = -40°C to +85°C, Except as Noted:

PARAMETER	SYMBOL	CONDITIONS			LIMITS						UNITS
					CDP1823			CDP1823C			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	-	500	-	-	500	µA
		-	0, 10	10	-	-	1000	-	-	-	µA
Output Low (Sink) Current	I_{OL}	0.4	0, 5	5	2	4	-	2	4	-	mA
		0.5	0, 10	10	4.5	9	-	-	-	-	mA
Output High (Source) Current	I_{OH}	4.6	0, 5	5	-1	-2	-	-1	-2	-	mA
		9.5	0, 10	10	-2.2	-4.4	-	-	-	-	mA
Output Voltage Low-Level	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High-Level	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 9.5	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 9.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	-	±5	-	-	±5	µA
			0, 10	10	-	-	±10	-	-	-	µA
Operating Current (Note 2)	I_{DD1}	-	0, 5	5	-	4	8	-	4	8	mA
		-	0, 10	10	-	8	16	-	-	-	mA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	-	±5	-	-	±5	µA
		0, 10	0, 10	10	-	-	±10	-	-	-	µA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = +25°C and nominal V_{DD}.
2. Outputs open circuited; Cycle time = 1µs.

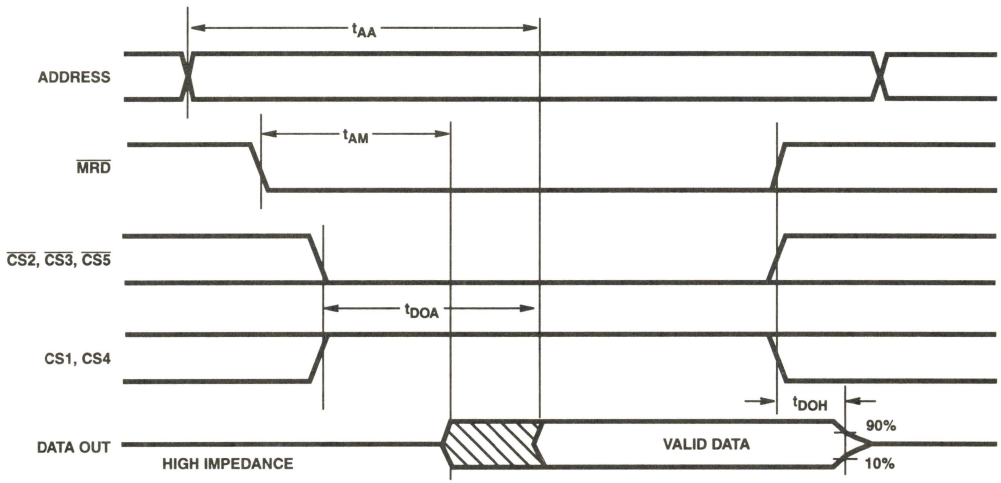
Dynamic Electrical Specifications

At T_A = -40 to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, C_L = 100pF

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS						UNITS
			CDP1823			CDP1823C			
			(NOTE 2) MIN	(NOTE 1) TYP	MAX	(NOTE 2) MIN	(NOTE 1) TYP	MAX	
Read Cycle (See Figure 1)									
Access Time From Address Change	t_{AA}	5	-	275	450	-	275	450	ns
		10	-	150	250	-	-	-	ns
Access Time From Chip Select	t_{DOA}	5	-	150	250	-	150	250	ns
		10	-	100	150	-	-	-	ns
$\overline{MRD}$ to Output Active	t_{AM}	5	-	150	250	-	150	250	ns
		10	-	100	150	-	-	-	ns
Data Hold Time After Read	t_{DOH}	5	25	50	75	25	50	75	ns
		10	15	25	40	-	-	-	ns

NOTES:

1. Typical values are at T_A = 25°C and nominal voltage.
2. Time required by a limit device to allow for the indicated function.



NOTE:

1. $\overline{MWR}$ is high during read operation. Timing measurement reference is 0.5 V_{DD}.

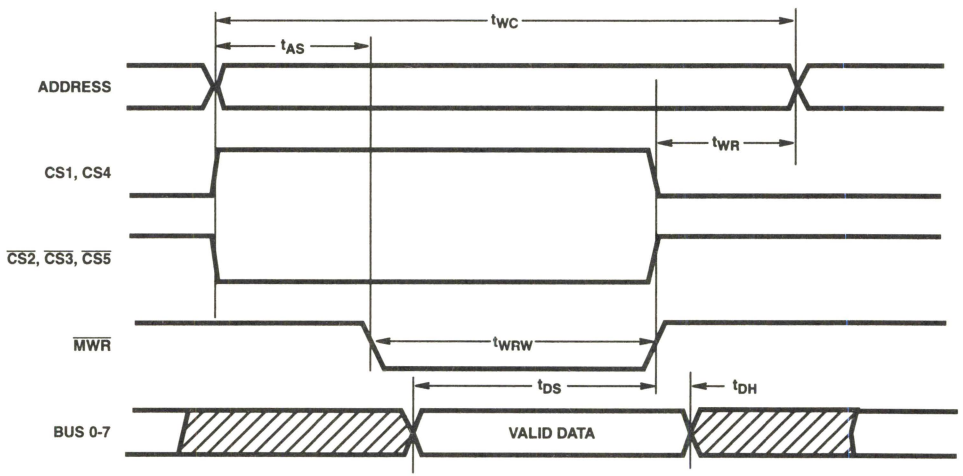
FIGURE 1. READ CYCLE TIMING DIAGRAM

Dynamic Electrical Specifications At T_A = -40 to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, C_L = 100pF

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS						UNITS
			CDP1823			CDP1823C			
			(NOTE 2) MIN	(NOTE 1) TYP	MAX	(NOTE 2) MIN	(NOTE 1) TYP	MAX	
Write Cycle (See Figure 2)									
Write Recovery	t_{WR}	5	75	-	-	75	-	-	ns
		10	50	-	-	-	-	-	ns
Write Cycle	t_{WC}	5	400	-	-	400	-	-	ns
		10	225	-	-	-	-	-	ns
Write Pulse Width	t_{WRW}	5	200	-	-	200	-	-	ns
		10	100	-	-	-	-	-	ns
Address Setup Time	t_{AS}	5	125	-	-	125	-	-	ns
		10	75	-	-	-	-	-	ns
Data Setup Time	t_{DS}	5	100	-	-	100	-	-	ns
		10	75	-	-	-	-	-	ns
Data Hold Time From $\overline{MWR}$	t_{DH}	5	75	-	-	75	-	-	ns
		10	50	-	-	-	-	-	ns

NOTES:

1. Typical values are at T_A = 25°C and nominal voltage.
2. Time required by a limit device to allow for the indicated function.



NOTE:

1. $\overline{MRD}$ must be high during write operation.

FIGURE 2. WRITE CYCLE TIMING DIAGRAM

Data Retention Specifications At T_A = -40 to +85°C, see Figure 3

PARAMETER	TEST CONDITIONS V_{DR} (V)	TEST CONDITIONS V_{DD} (V)	LIMITS CDP1823 MIN	CDP1823 (NOTE 1) TYP	CDP1823 MAX	CDP1823C MIN	CDP1823C (NOTE 1) TYP	CDP1823C MAX	UNITS
Minimum Data Retention Voltage, V_{DR}	-	-	-	1.5	2	-	1.5	2	V
Data Retention Quiescent Current, I_{DD}	2	-	-	30	100	-	30	100	µA
Chip Deselect to Data Retention Time	-	5	600	-	-	600	-	-	ns
t_{CDR}	-	10	300	-	-	-	-	-	ns
Recovery to Normal Operation Time t_{RC}	-	5	600	-	-	600	-	-	ns
	-	10	300	-	-	-	-	-	ns
V_{DD} to V_{DR} Rise and Fall Time t_R, t_F	2	5	1	-	-	1	-	-	µs

NOTE:

Typical values are for T_A = 25°C and nominal V_{DD}.

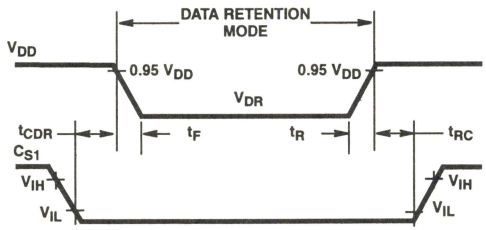


FIGURE 3. LOW V_{DD} DATA RETENTION TIMING WAVEFORMS

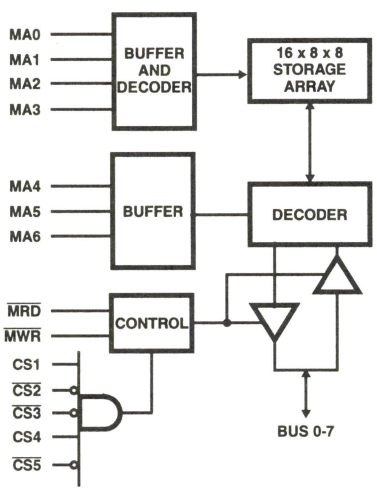


FIGURE 4. FUNCTIONAL DIAGRAM

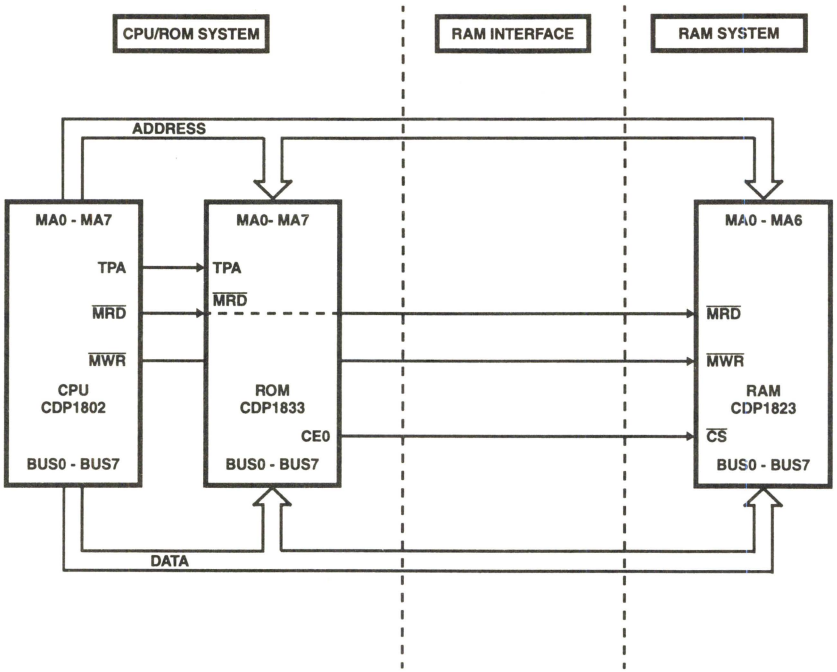


FIGURE 5. CDP1823 (128 x 8) MINIMUM SYSTEM (128 x 8)

HARRIS SEMICONDUCTOR

CDP1823C/3

High-Reliability CMOS 128-Word x 8-Bit Static RAM

March 1997

Features

- For Applications in Aerospace, Military, and Critical Industrial Equipment
- Compatible with CDP1800-Series Microprocessors at Maximum Speed
- Interfaces with CDP1800-Series Microprocessors without Additional Components
- Fast Access Time
- At V_{DD} = 5V, +25°C 275ns
- Single Voltage Supply
- Common Data Inputs and Outputs
- Multiple Chip Select Inputs to Simplify Memory System Expansion
- High Noise Immunity . . . . . 30% of V_{DD}
- Memory Retention for Standby Battery Voltage Down to 2V at 25°C
- Latch-Up-Free Transient Radiation Tolerance

Ordering Information

PACKAGE	TEMP. RANGE	PART NUMBER (5V)	PKG. NO.
SBDIP	-55°C to +125°C	CDP1823CD3	D24.6

Description

The CDP1823C/3 is a 128 word x 8-bit CMOS/SOS static random access memory. It is compatible with the CDP1802, CDP1804, CDP1805, and CDP1806 microprocessors, and will interface directly without additional components. The CDP1823C has a recommended operating voltage range of 4V to 6.5V.

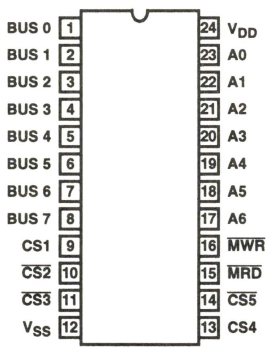
The CDP1823C memory has 8 common data input and data output terminals for direct connection to a bidirectional data bus and is operated from a single voltage supply. Five chip select inputs are provided to simplify memory system expansion. In order to enable the CDP1823C, the chip select inputs $\overline{CS2}$, $\overline{CS3}$, and $\overline{CS5}$ require a low input signal, and the chip select inputs CS1 and CS4 require a high input signal.

The $\overline{MRD}$ signal enables all 8 output drivers when in the low state and should be in a high state during a write cycle.

After valid data appear at the output, the address inputs may be changed immediately. Output data will be valid until either the $\overline{MRD}$ signal goes high, the device is deselected, or t_{AA} (access time) after address changes.

Pinout

CDP1823C/3
(SBDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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OPERATIONAL MODES

FUNCTION	$\overline{MRD}$	$\overline{MWR}$	CS1	$\overline{CS2}$	$\overline{CS3}$	CS4	$\overline{CS5}$	BUS TERMINAL STATE
Read	0	X	1	0	0	1	0	Storage State of Addressed Word
Write	1	0	1	0	0	1	0	Input High Impedance
Standby	1	1	1	0	0	1	0	High Impedance
Not Selected	X X X X X	X X X X X	0 X X X X	X 1 X X X	X X 1 X X	X X X 0 X	X X X X 1	High Impedance

NOTE:

1. Logic 1 = High, Logic 0 = Low, X = Don't Care.

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1823C/3 . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	60	17

Maximum Operating Temperature Range (T_A) . . . -55°C to +125°C
Maximum Storage Temperature Range (T_{STG}) . . . -65°C to +150°C
Maximum Lead Temperature (During Soldering) . . . . . +265°C
Maximum Junction Temperature . . . . . +150°C

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS		UNITS
	MIN	MAX	
Supply Voltage Range	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V

Static Electrical Specifications

V_{DD} = 5V ±5%

PARAMETER		CONDITIONS			LIMITS				UNITS
					-55°C, +25°C		+125°C		
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	MAX	MIN	MAX	
Quiescent Device Current (Note 1)	I_{DD}	-	0, 5	5	-	270	-	1000	µA
Output Low (Sink) Current (Note 1)	I_{OL}	0.4	0, 5	5	2.7	-	1.5	-	mA
Output High (Source) Current (Note 1)	I_{OH}	4.6	0, 5	5	-	-1.3	-	-0.7	mA
Output Voltage Low-Level	V_{OL}	-	0, 5	5	-	0.1	-	0.1	V
Output Voltage High-Level	V_{OH}	-	0, 5	5	V_{DD} - 0.1	-	V_{DD} - 0.1	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	0.3 V_{DD}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	0.7 V_{DD}	-	0.7 V_{DD}	-	V
Input Leakage Current (Note 1)	I_{IN}	-	0, 5	5	-	±2.6	-	±10	µA
Operating Current (Note 1)	I_{DD1}	-	0, 5	5	-	5	-	10	mA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	±2.6	-	±10	µA
Input Capacitance	C_{IN}	-	-	-	-	7.5	-	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	15	-	15	pF

NOTE:

1. Limits designate 100% testing, all other limits are designer's parameters under given test conditions and do not represent 100% testing.

Read Cycle Dynamic Electrical Specifications

t_R, t_F = 10ns, C_L = 50pF

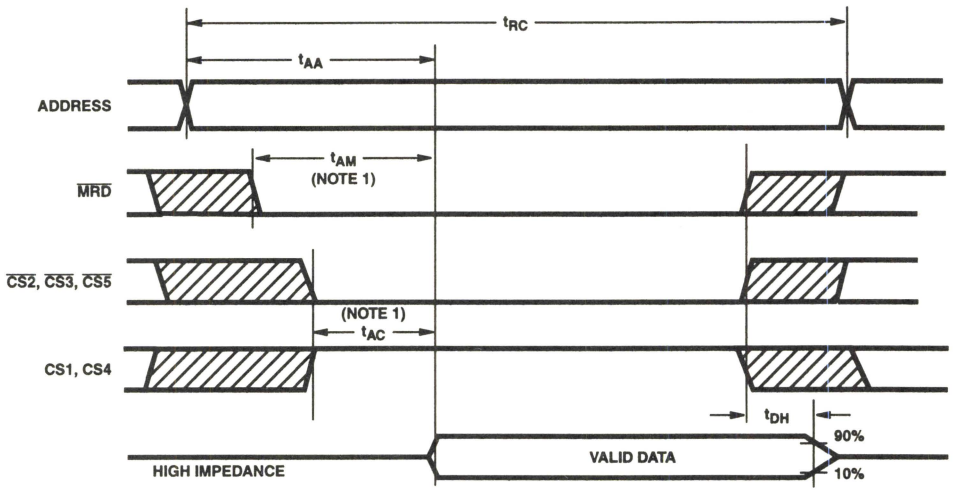
PARAMETER	SYMBOL	V_{DD} (V)	LIMITS				UNITS
			+25°C, -55°C		+125°C		
			MIN	MAX	MIN	MAX	
Read Cycle	t_{RC}	5	360	-	505	-	ns
Access Time from Address Change (Note 1)	t_{AA}	5	-	360	-	505	ns
Access Time from Chip Select	t_{AC}	5	-	360	-	505	ns

Read Cycle Dynamic Electrical Specifications t_R, t_F = 10ns, C_L = 50pF (Continued)

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS				UNITS
			+25°C, -55°C		+125°C		
			MIN	MAX	MIN	MAX	
Access Time from $\overline{MRD}$ (Note 1)	t_{AM}	5	-	310	-	435	ns
Data Hold Time After Read	t_{DH}	5	50	-	70	-	ns

NOTE:

1. Limits designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.



NOTES:

1. Minimum timing for valid data output. Longer times will initiate an earlier but invalid output.
2. $\overline{MWR}$ is high during read operation. Timing measurement reference is $0.5V_{DD}$.

FIGURE 1. READ CYCLE TIMING DIAGRAM

Write Cycle Dynamic Electrical Specifications t_R, t_F = 10ns, C_L = 50pF

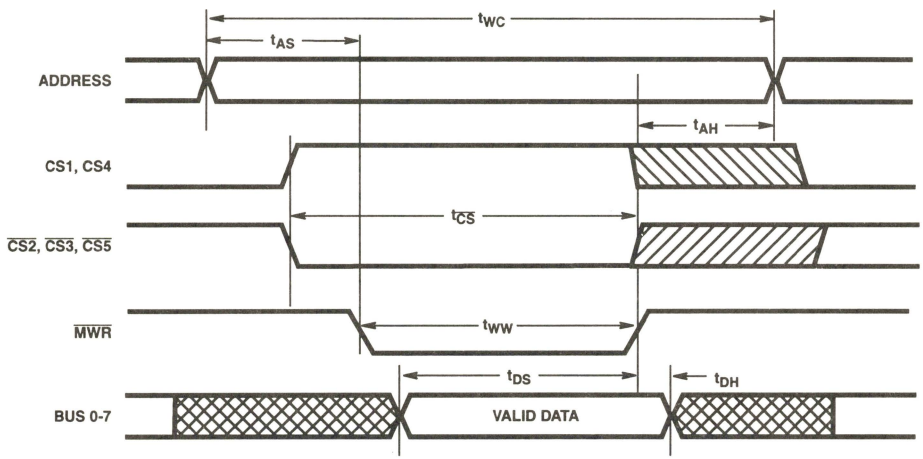
PARAMETER	SYMBOL	V_{DD} (V)	LIMITS				UNITS
			+25°C, -55°C		+125°C		
			(NOTE 2) MIN	MAX	(NOTE 2) MIN	MAX	
Write Cycle	t_{WC}	5	280	-	400	-	ns
Address Setup Time (Note 1)	t_{AS}	5	70	-	100	-	ns
Address Hold Time	t_{AH}	5	70	-	100	-	ns
Write Pulse Width (Note 1)	t_{WW}	5	140	-	200	-	ns
Data to $\overline{MWR}$ Setup Time (Note 1)	t_{DS}	5	70	-	100	-	ns

Write Cycle Dynamic Electrical Specifications t_R, t_F = 10ns, C_L = 50pF (Continued)

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS +25°C, -55°C (NOTE 2) MIN	+25°C, -55°C MAX	+125°C (NOTE 2) MIN	+125°C MAX	UNITS
Data Hold Time from $\overline{MWR}$ (Note 1)	t_{DH}	5	50	-	70	-	ns
Chip Select Setup	$t_{\overline{CS}}$	5	210	-	300	-	ns

NOTES:

1. Limits designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.
2. Minimum timing to allow the indicated function to occur.



NOTE:

1. $\overline{MRD}$ must be high during write operation.

FIGURE 2. WRITE CYCLE TIMING WAVEFORMS

Data Retention Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_{DR} (V)	TEST CONDITIONS V_{DD} (V)	LIMITS +25°C, -55°C MIN	+25°C, -55°C MAX	+125°C MIN	+125°C MAX	UNITS
Minimum Data Retention Voltage (Note 1)	V_{DR}	-	-	-	2	-	2.5	V
Data Retention Quiescent Current	I_{DD}	2	-	-	100	-	400	µA
Chip Deselect to Data Retention Time	t_{CDR}	-	5	450	-	650	-	ns
Recovery to Normal Operation Time	t_{RC}	-	5	450	-	650	-	ns

NOTE:

1. Limits designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

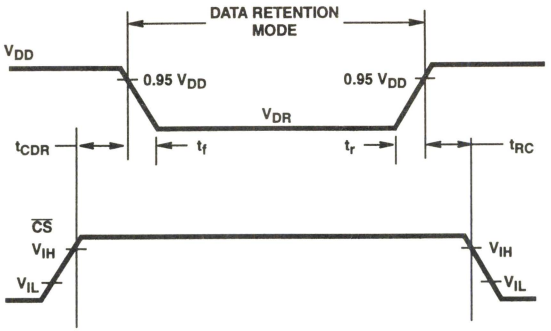
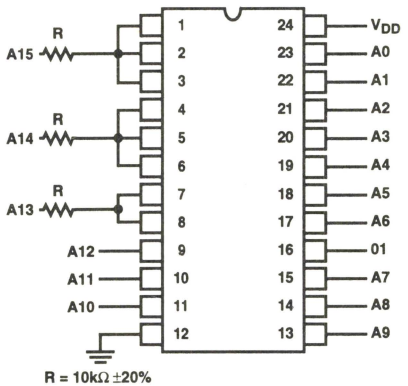
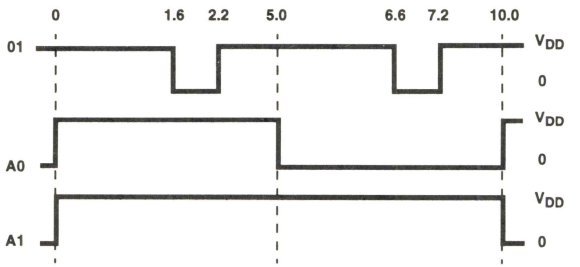


FIGURE 3. LOW V_{DD} DATA RETENTION WAVEFORMS



PACKAGE	TEMPERATURE	DURATION	V_{DD}
D	125°C	160 Hrs	7V



NOTE:

1. A1 - A11 are division by 2 based on A0.

FIGURE 4. DYNAMIC/OPERATING BURN-IN CIRCUIT AND TIMING DIAGRAM

CDP1824, CDP1824C

March 1997

32-Word x 8-Bit Static RAM

Features

- **Fast Access Time**
  - V_{DD} = 5V 710ns
  - V_{DD} = 10V 320ns
- **No Precharge or Clock Required**

Description

The CDP1824 and CDP1824C are 32-word x 8-bit fully static CMOS random-access memories for use in CDP-1800 series microprocessor systems. These parts are compatible with the CDP1802 microprocessor and will interface directly without additional components.

The CDP1824 is fully decoded and does not require a pre-charge or clocking signal for proper operation. It has common input and output and is operated from a single voltage supply. The $\overline{MRD}$ signal (output disable control) enables the three-state output drivers, and overrides the $\overline{MWR}$ signal. A $\overline{CS}$ input is provided for memory expansion.

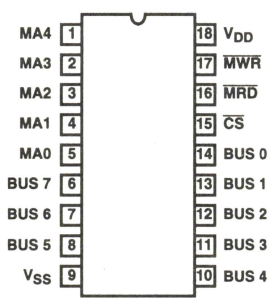
The CDP1824C is functionally identical to the CDP1824. The CDP1824 has an operating range of 4V to 10.5V, and the CDP1824C has an operating voltage range of 4V to 6.5V. The CDP1824 and CDP1824C are supplied in 18 lead hermetic dual-in-line ceramic packages (D suffix), and in 18 lead dual-in-line plastic packages (E suffix).

Ordering Information

5V	10V	PACKAGE	TEMPERATURE RANGE	PKG. NO.
CDP1824CE	CDP1824E	PDIP	-40°C to +85°C	E18.3
CDP1824CEX	CDP1824EX	Burn-In		E18.3
CDP1824CD	CDP1824D	SBDIP	-40°C to +85°C	D18.3

Pinout

CDP1824, CDP1824C (PDIP, SBDIP)
TOP VIEW



OPERATIONAL MODES

FUNCTION	$\overline{CS}$	$\overline{MRD}$	$\overline{MWR}$	DATA PINS STATUS
READ	0	0	X	Output: High/Low Dependent on Data
WRITE	0	1	0	Input: Output Disabled
Not Selected	1	X	X	Output Disabled: High-Impedance State
Standby	0	1	1	Output Disabled: High-Impedance State

Logic 1 = High Logic 0 = Low X = Don't Care

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1824 . . . . . -0.5V to +11V
CDP1824C . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range (T_A)
Package Type D . . . . . -55°C to +125°C
Package Type E . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	75	20
PDIP Package	75	N/A

Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ±1/32 In. (1.59 ± 0.79mm)
from case for 10s max . . . . . +265°C

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	CONDITION	LIMITS				UNITS
		CDP1824D		CDP1824CD		
	V_{DD} (V)	MIN	MAX	MIN	MAX	
Supply Voltage Range	-	4	10.5	4	6.5	V
Recommended Input Voltage Range	-	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise or Fall Time (Note 1)	5	-	5	-	5	µs
t_R, t_F	10	-	2	-	-	µs

NOTE:

1. Input signal rise or fall times longer than these maxima can cause loss of stored data in either the selected or deselected mode.

Static Electrical Specifications

At T_A = -40°C to +85°C, Except as Noted:

PARAMETER	SYMBOL	CONDITIONS			LIMITS						UNITS
					CDP1824			CDP1824C			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	-	5	-	25	50	-	100	200	µA
		-	-	10	-	250	500	-	-	-	µA
Output Low (Sink) Current	I_{OL}	0.4	0, 5	5	1.8	2.2	-	1.8	2.2	-	mA
		0.5	0, 10	10	3.6	4.5	-	-	-	-	mA
Output High (Source) Current	I_{OH}	4.6	0, 5	5	-0.9	-1.1	-	-0.9	-1.1	-	mA
		9.5	0, 10	10	-1.8	-2.2	-	-	-	-	mA
Output Voltage Low-Level	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High-Level	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		1.9	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 9.5	-	5	3.5	-	-	3.5	-	-	V
		1.9	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	±0.1	±1	-	±0.1	±1	µA
			0, 10	10	-	±0.1	±1	-	-	-	µA
Operating Current (Note 2)	I_{DD1}	-	0, 5	5	-	4	8	-	4	8	mA
		-	0, 10	10	-	8	16	-	-	-	mA

Static Electrical Specifications At T_A = -40°C to +85°C, Except as Noted: **(Continued)**

PARAMETER	SYMBOL	CONDITIONS			LIMITS						UNITS
					CDP1824			CDP1824C			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	± 0.2	±2.0	-	± 0.2	± 2	µA
		0, 10	0, 10	10	-	± 0.2	±2.0	-	-	-	µA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

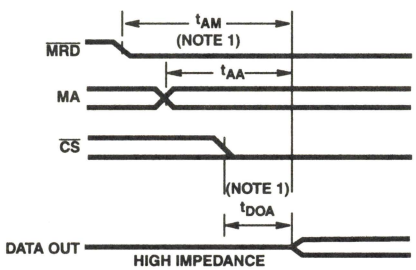
1. Typical values are for T_A = +25°C and nominal V_{DD}.
2. Outputs open circuited; Cycle time = 1µs.

Dynamic Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ±5%, Input t_R, t_F = 10ns, C_L = 50pF, R_L = 200kΩ; See Figure 1

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CDP1824D, CDP1824E			CDP1824CD, CDP1824CE			
		V_{DD} (V)	(NOTE 1) MIN	(NOTE 2) TYP	MAX	(NOTE 1) MIN	(NOTE 2) TYP	MAX	
READ OPERATION									
Access Time From Address Change	t_{AA}	5	-	400	710	-	400	710	ns
		10	-	200	320	-	-	-	ns
Access Time From Chip Select	t_{DOA}	5	-	300	710	-	300	710	ns
		10	-	150	320	-	-	-	ns
Output Active From $\overline{MRD}$	t_{AM}	5	-	300	710	-	300	710	ns
		10	-	150	320	-	-	-	ns

NOTES:

1. Time required by a limit device to allow for the indicated function.
2. Time required by a typical device to allow for the indicated function. Typical values are for T_A = +25°C and nominal V_{DD}.



NOTES:

1. Minimum timing for valid data output longer times will initiate an earlier, but invalid output.

FIGURE 1. READ CYCLE TIMING DIAGRAMS

Dynamic Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ±5%, Input t_R, t_F = 10ns, C_L = 50pF, R_L = 200kΩ; See Figure 2

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CDP1824D, CDP1824E			CDP1824CD, CDP1824CE			
		V_{DD} (V)	(NOTE 1) MIN	(NOTE 2) TYP	MAX	(NOTE 1) MIN	(NOTE 2) TYP	MAX	
WRITE OPERATION									
Write Pulse Width	t_{WRW}	5	390	200	-	390	200	-	ns
		10	180	150	-	-	-	-	ns
Data Setup Time	t_{DS}	5	390	100	-	390	100	-	ns
		10	180	50	-	-	-	-	ns
Data Hold Time	t_{DH}	5	70	40	-	70	40	-	ns
		10	35	20	-	-	-	-	ns
Chip Select Setup Time	t_{CS}	5	425	210	-	425	210	-	ns
		10	215	110	-	-	-	-	ns
Address Setup Time	t_{AS}	5	640	500	-	640	500	-	ns
		10	390	300	-	-	-	-	ns

NOTES:

1. Time required by a limit device to allow for the indicated function.
2. Time required by a typical device to allow for the indicated function. Typical values are for T_A = +25°C and nominal V_{DD}.

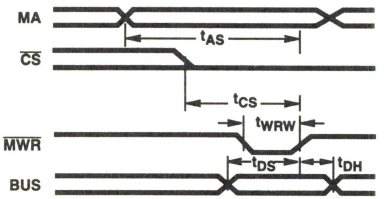
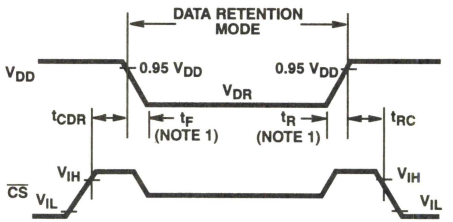


FIGURE 2. WRITE CYCLE TIMING DIAGRAM



NOTE: t_R, t_F > 1µs.

FIGURE 3. LOW V_{DD} DATA RETENTION WAVEFORMS AND TIMING DIAGRAM

Data Retention Specifications at T_A = -40°C to +85°C; See Figure 3

PARAMETER	SYMBOL	TEST CONDITIONS	V_{DD} (V)	LIMITS				UNITS
				CDP1824		CDP1824C		
				MIN	MAX	MIN	MAX	
Data Retention Voltage	V_{DR}		-	2.5	-	2.5	-	V
Data Retention Quiescent Current	I_{DD}	V_{DR} = 2.5V	-	-	10	-	40	µA
Chip Deselect to Data Retention Time	t_{CDR}	V_{DR} = 2.5V	5	600	-	600	-	ns
			10	300	-	-	-	ns
Recovery to Normal Operation Time	t_{RC}	V_{DR} = 2.5V	5	600	-	600	-	ns
			10	300	-	-	-	ns

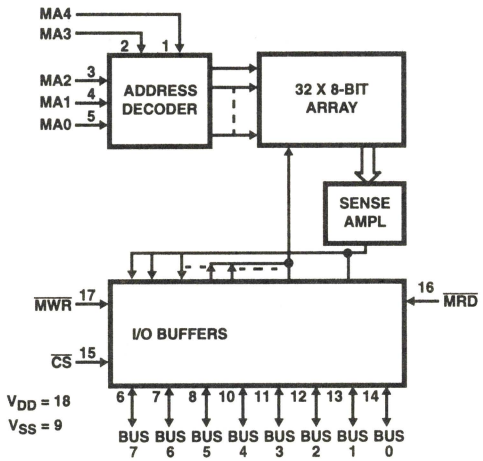


FIGURE 4. FUNCTIONAL DIAGRAM

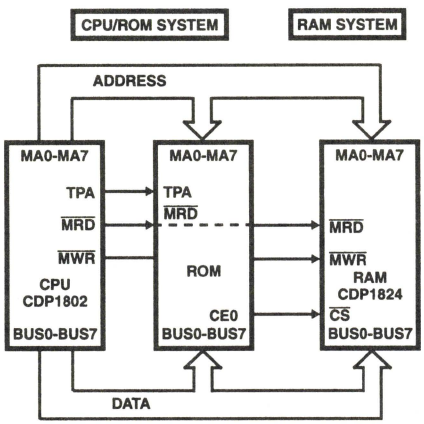


FIGURE 5. CDP1824 (128 X 8) MINIMUM SYSTEM (128 X 8)

HARRIS SEMICONDUCTOR

CDP1824/3, CDP1824C/3

High-Reliability CMOS 32-Word x 8-Bit Static Random-Access Memory

March 1997

Features

- Access Time
  - 610ns . . . . . at V_{DD} = 5V
  - 320ns . . . . . at V_{DD} = 10V
- No Precharge or Clock Required

Ordering Information

5V	10V	PACK-AGE	TEMP. RANGE	PKG. NO.
CDP1824CD3	CDP1824D3	SBDIP	-55°C to +125°C	D18.3

Description

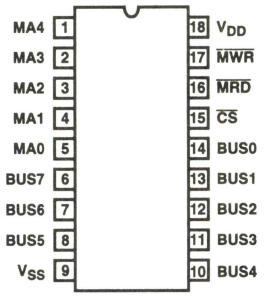
The CDP1824/3 and CDP1824C/3 types are high-reliability CMOS 32-word x 8-bit fully static random-access memories for use in CDP1800-series microprocessor systems. These parts are compatible with the CDP1802 microprocessor and will interface directly without additional components.

The CDP1824/3 is fully decoded and does not require a precharge or clocking signal for proper operation. It has common input and output and is operated from a single voltage supply. The $\overline{MRD}$ signal (output disable control) enables the three-state output drivers, and overrides the $\overline{MWR}$ signal. A $\overline{CS}$ input is provided for memory expansion.

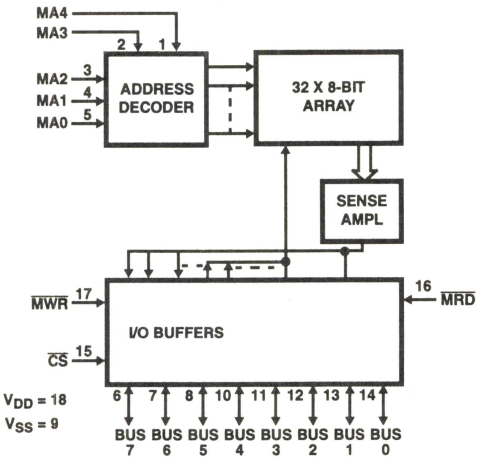
The CDP1824C/3 is functionally identical to the CDP1824/3. The CDP1824/3 has a recommended operating voltage range of 4V to 10.5V, and the CDP1824C/3 has an operating voltage range of 4V to 6.5V.

Pinout

CDP1824/3, CDP1824C/3 (SBDIP)
TOP VIEW



Functional Diagram



OPERATIONAL MODES

FUNCTION	$\overline{CS}$	$\overline{MRD}$	$\overline{MWR}$	DATA PINS STATUS
READ	0	0	X	Output: High/Low Dependent on Data
WRITE	0	1	0	Input: Output Disabled
Not Selected	1	X	X	Output Disabled: High-Impedance State
Standby	0	1	1	Output Disabled: High-Impedance State

Logic 1 = High Logic 0 = Low X = Don't Care

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **1717.2**

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1824/3 . . . . . -0.5V to +11V
CDP1824C/3 . . . . . -0.5 to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input . . . . . ±10mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	75	20

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type D . . . . . -55°C to +125°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ±1/32 In. (1.59 ± 0.79mm)
from case for 10s max . . . . . +265°C

Recommended Operating Conditions

T_A = Full Package-Temperature Range. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS				UNITS
	CDP1824/3		CDP1824C/3		
	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Static Electrical Specifications

PARAMETER	SYMBOL	CONDITIONS			LIMITS				UNITS
					-55°C, +25°C		+125°C		
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	MAX	MIN	MAX	
Quiescent Device Current (Note 1)	I_{DD}	-	0, 5	5	-	50	-	500	µA
		-	0, 10	10	-	500	-	1000	µA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0.1	-	0.2	V
		-		10	-	0.1	-	0.2	V
Output Voltage High-Level (Note 2)	V_{OH}	-	0, 5	5	4.9	-	4.8	-	V
		-	-	10	9.9	-	4.8	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	-	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	V
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	4	-	1.5	-	mA
		0.5	0, 10	10	4	-	2.9	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-	-1	-	-0.75	mA
		9.5	0, 10	10	-	-2	-	-1.5	mA
Input Current	I_{IN}	Any Input	0, 5	5	-	1	-	5	µA
			0, 10	10	-	1	-	5	µA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	2	-	5	µA
		0, 10	0, 10	10	-	2	-	5	µA
Input Capacitance	C_{IN}	(Note 2)			-	10	-	10	pF
Output Capacitance	C_{OUT}	(Note 2)			-	15	-	15	pF

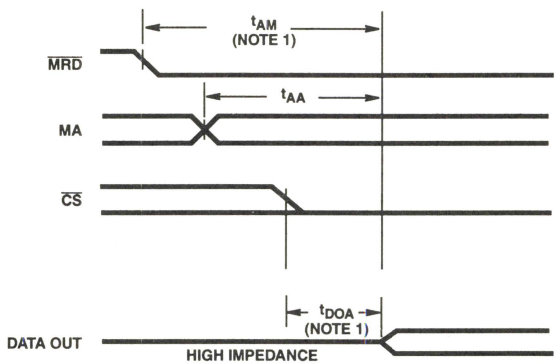
NOTES:

1. The CDP1824C/3 meets all 5V Static Electrical Characteristics of the CDP1824/3 except Quiescent Device Current for which the limits are I_{DD} = 200µA at +25°C/-55°C; I_{DD} = 1000µA at +125°C.
2. Guaranteed, but not tested.

Read Cycle Dynamic Electrical Specifications

Input t_R, $t_F \leq 15ns$, $C_L = 50pF$

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			-55°C, +25°C		+125°C		
		V_{DD} (V)	MIN	MAX	MIN	MAX	
Access Time From Address Change	t_{AA}	5	-	610	-	825	ns
		10	-	320	-	375	ns
Access Time From Chip Select	t_{DOA}	5	-	610	-	825	ns
		10	-	320	-	375	ns
Output Active From $\overline{MRD}$	t_{AM}	5	-	610	-	825	ns
		10	-	320	-	375	ns



NOTE:

1. Minimum timing for valid data output longer times will initiate an earlier, but invalid output.

FIGURE 1. READ CYCLE TIMING DIAGRAM

Write Cycle Dynamic Electrical Specifications

Input t_R, $t_F \leq 15ns$, $C_L = 50pF$

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			-55°C, +25°C		+125°C		
		V_{DD} (V)	(NOTE 1) MIN	MAX	(NOTE 1) MIN	MAX	
Write Pulse Width	t_{WRW}	5	350	-	475	-	ns
		10	180	-	220	-	ns
Data Setup Time	t_{DS}	5	400	-	560	-	ns
		10	190	-	260	-	ns
Data Hold Time	t_{DH}	5	70	-	90	-	ns
		10	35	-	45	-	ns
Chip Select Setup Time	t_{CS}	5	550	-	775	-	ns
		10	340	-	475	-	ns
Address Setup Time	t_{AS}	5	550	-	775	-	ns
		10	340	-	475	-	ns

NOTE:

1. Time required by a device to allow for the indicated function.

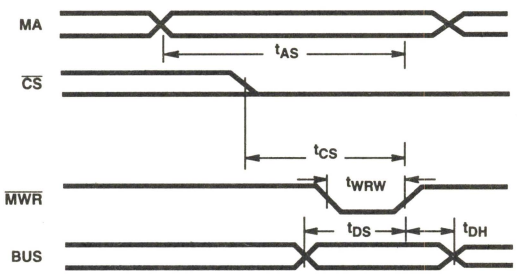
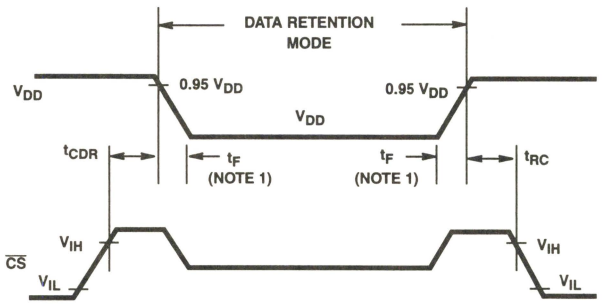


FIGURE 2. WRITE CYCLE TIMING DIAGRAM

Data Retention Specifications At $T_A = +25^oC$

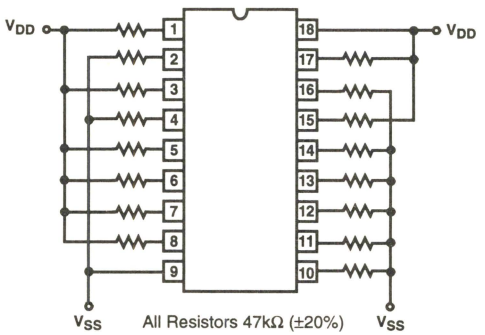
PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS				UNITS
				CDP1824/3		CDP1824C/3		
		V_{DR} (V)	V_{DD} (V)	MIN	MAX	MIN	MAX	
Data Retention Voltage	V_{DR}	-	-	2.5	-	2.5	-	V
Data Retention Quiescent Current	I_{DD}	2.5	-	-	10	-	40	µA
Chip Deselect to Data Retention Time	t_{CDR}	2.5	5	600	-	600	-	ns
		2.5	10	300	-	-	-	ns
Recovery to Normal Operation Time	t_{RC}	2.5	5	600	-	600	-	ns
		2.5	10	300	-	-	-	ns



NOTE: t_r, $t_f > 1\mu s$.

FIGURE 3. LOW V_{DD} DATA RETENTION WAVEFORMS AND TIMING DIAGRAM

Static Burn-In Circuit



TYPE	V_{DD}	TEMPERATURE	TIME
CDP1824	11V	+125°C	160 Hrs., Min.
CDP1824C	7V	+125°C	160 Hrs., Min.

HARRIS SEMICONDUCTOR

CDP1826C

CMOS 64-Word x 8-Bit Static RAM

March 1997

Features

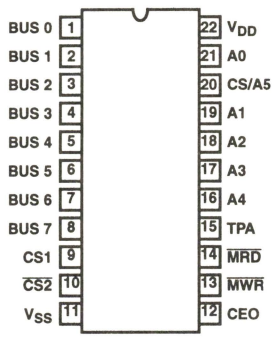
- **Ideal for Small, Low-Power RAM Memory Requirements in Microprocessor and Microcomputer Applications**
- **Interfaces with CDP1800-Series Microprocessors Without Additional Address Decoding**
- **Daisy Chain Feature to Further Reduce External Decoding Needs**
- **Multiple Chip-Select Inputs for Versatility**
- **Single Voltage Supply**
- **No Clock or Precharge Required.**

Ordering Information

PACKAGE	TEMP. RANGE	PART NUMBER	PKG. NO.
PDIP	-40°C to +85°C	CDP1826CE	E22.4

Pinout

CDP1826C (PDIP)
TOP VIEW



Description

The CDP1826C is a general purpose, fully static, 64-word x 8-bit random-access memory, for use in CDP1800-series or other microprocessor systems where minimum component count and/or price performance and simplicity in use are desirable.

The CDP1826C has 8 common data input and data-output terminals with three-state capability for direct connection to a standard bidirectional data bus. Two chip-select inputs - CS1 and $\overline{CS2}$ - are provided to simplify memory-system expansion. An additional select pin, CS/A5, is provided to enable the CDP1826C to be selected directly from the CDP1800 multiplexed address bus without additional latching or decoding. In an 1800 system, the CS/A5 pin can be tied to any MA address line from the CDP1800 processor. A TPA input is provided to latch the high-order bit of this address line as a chip-select for the CDP1826C. If this CS/A5 input is latched high, and if CS = 1 and $\overline{CS2}$ = 0 at the appropriate time in the memory cycle, the CDP1826C will be enabled for writing or reading. In a non-1800 system, the TPA pin can be tied high, and the CS/A5 pin can be used as a normal address input.

The six input-address buffers are gated with the chip-select function to reduce standby current when the device is deselected, as well as to provide for a simplified power down mode by reducing address buffer sensitivity to long fall times from address drivers which are being powered down.

Two memory control signals, $\overline{MRD}$ and $\overline{MWR}$, are provided for reading from the writing to the CDP1826C. The logic is designed so that $\overline{MWR}$ overrides $\overline{MRD}$, allowing the chip to be controlled from a single R/$\overline{W}$.

A CHIP ENABLE OUTPUT is provided for daisy-chaining to additional memories or I/O devices. This output is high whenever the chip-select function selects the CDP1826C, which deselects any other chip which has its $\overline{CS}$ input connected to the CDP1826C CEO output. The connected chip is selected when the CDP1826C is deselected and the $\overline{MRD}$ input is low. Thus, the CEO is only active for a read cycle and can be setup so that a CEO of another device can feed the $\overline{MRD}$ of the CDP1826C, which in turn selects a third chip in the daisy chain.

The CDP1826C has a recommended operating voltage of 4.5V to 5.5V and is supplied in 22 lead dual-in-line plastic packages (E suffix). The CDP1826C is also available in chip form (H suffix).

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1311.2**

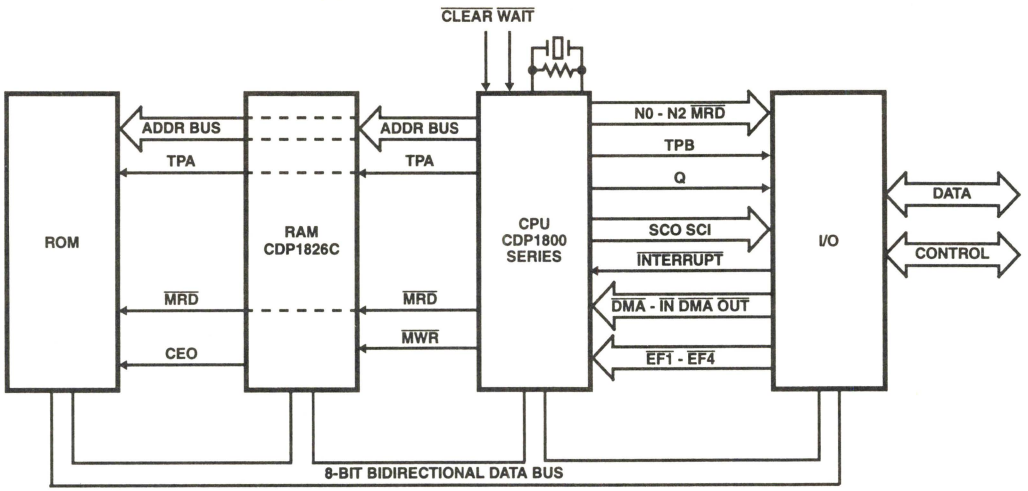


FIGURE 1. TYPICAL CDP1802 MICROPROCESSOR SYSTEM

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1826C . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Power Dissipation Per Package (P_D)
T_A = -40°C to +60°C (Package Type E) 500mW
T_A = +60°C to +85°C (Package Type E) . . . . . Derate Linearly at 12mW/°C to 200mW
T_A = -55°C to +100°C (Package Type D) 500mW
T_A = +100°C to +125°C (Package Type D) . . . . Derate Linearly at 12mW/°C to 200mW

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	75	N/A

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type D . . . . . -55°C to +125°C
Package Type E . . . . . -40°C to +85°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ±1/32 In. (1.59 ±0.79mm)
from case for 10s max . . . . . +265°C

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	SYMBOL	CDP1826C		UNITS
		MIN	MAX	
DC Operating Voltage Range		4	6.5	V
Input Voltage Range		V_{SS}	V_{DD}	V
Input Signal Rise or Fall Time, V_{DD} = 5V	t_R, t_F	-	10	µs

Static Electrical Specifications

At T_A = -40°C to +85°C, V_{DD} = 5V ±5%, Except as Noted:

PARAMETER		SYMBOL	CONDITIONS		LIMITS			UNITS
					CDP1826C			
			V_O (V)	V_{IN} (V)	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current		I_{DD}	-	0, V_{DD}	-	5	50	µA
Output Low (Sink) Current	BUS	I_{OL}	0.4	0, V_{DD}	1.6	3.2	-	mA
	CEO		0.4	0, V_{DD}	0.8	1.6	-	mA
Output High (Source) Current	BUS	I_{OH}	V_{DD} -0.4	0, V_{DD}	-1.0	-1.5	-	mA
	CEO		V_{DD} -0.4	0, V_{DD}	-0.6	-1.0	-	mA
Output Voltage Low-Level		V_{OL}	-	0, V_{DD}	-	0	0.1	V
Output Voltage High-Level		V_{OH}	-	0, V_{DD}	V_{DD} -0.1	V_{DD}	-	V
Input Low Voltage		V_{IL}	-	-	-	-	1.5	V
Input High Voltage		V_{IH}	-	-	3.5	-	-	V
Input Leakage Current		I_{IN}	Any Input	0, V_{DD}	-	±0.1	±1	µA
Operating Device Current (Note 2)		I_{OPER}	-	0, V_{DD}	-	5	10	mA
Three-State Output Leakage Current		I_{OUT}	0, V_{DD}	0, V_{DD}	-	±0.1	±1	µA
Input Capacitance		C_{IN}	-	-	-	5	7.5	pF
Output Capacitance		C_{OUT}	-	0, V_{DD}	-	10	15	pF

NOTES:

1. Typical values are for T_A = +25°C and nominal V_{DD}.
2. Outputs open circuited; Cycle time = 1µs.

Signal Descriptions

A0 - A4, CS/A5 (Address Inputs): These inputs must be stable prior to a write operation, but may change asynchronously during Read operations.

In an 1800 system, the multiplexed high-order address bit at pin CS/A5 can be latched at the end of TPA. A high level will provide a valid chip select for the CDP1826C. The low-order address bit which appears after TPA is used for data word selection. In non-1800 systems, TPA can be tied high to disable the latch and allow the CS/A5 pin to function as a normal address input.

BUS 0 - BUS 7: 8-bit three-state common input/output data bus.

TPA: High-order address strobe input. The high-order address bit at input CS/A5 is latched on the high-to-low transition of the TPA input. Tie TPA high to disable the CS/A5 latch feature.

CS1, $\overline{CS2}$ (Chip Selector): Either chip select (CS1 or $\overline{CS2}$), when not valid, powers down the chip, disables READ and WRITE functions, and gates off the address and output buffers.

$\overline{MRD}$, $\overline{MWR}$: Read and Write control signals. $\overline{MWR}$ overrides $\overline{MRD}$, allowing the CDP1826C to be controlled from a single R/$\overline{W}$ line.

CEO (Chip Enable Output): Allows daisy chaining to additional memories. CEO is high whenever the CDP1826C is selected. CEO is only active (low) for a Read cycle with the CDP1826C deselected and the $\overline{MRD}$ input low.

V_{DD}, V_{SS}: Power supply connections.

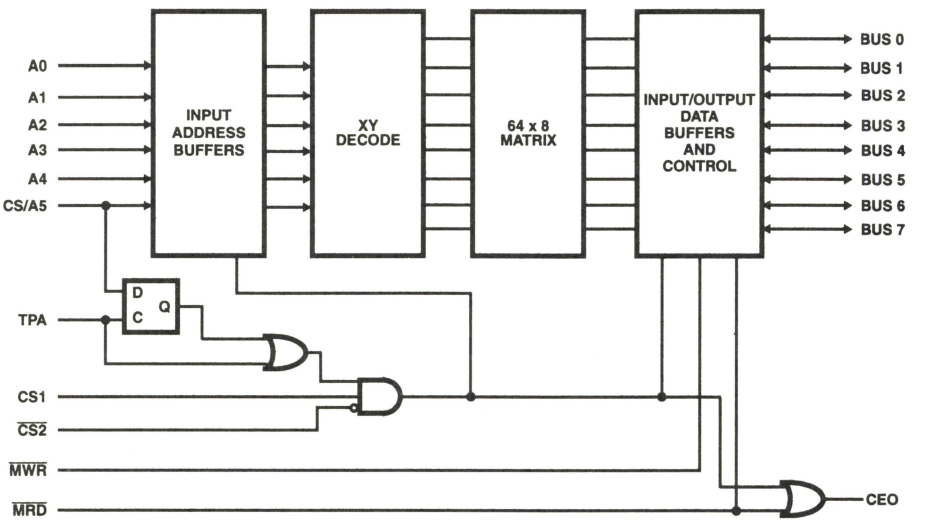
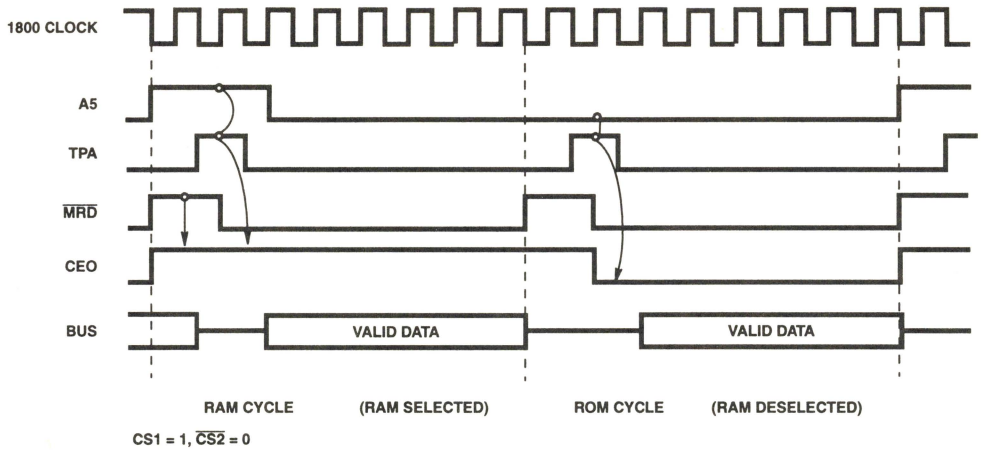


FIGURE 2. FUNCTIONAL DIAGRAM



OPERATING MODES

	FUNCTION	MRD	MWR	CS1 • CS2	TPA	(NOTE 1) CS/A5	CEO
CDP1800 Mode	Write	X	O	I	⎍	I	I
	Read	O	I	I	⎍	I	I
	Deselect	I	I	I	⎍	I	I
	Deselect	I	X	O	X	X	I
	Deselect	O	X	O	X	X	O
	Deselect	I	X	X	⎍	O	I
	Deselect	O	X	X	⎍	O	O
Non-CDP1800 Mode	Write	X	O	I	I	X	I
	Read	O	I	I	I	X	I
	Deselect	I	I	I	I	X	I
	Deselect	I	X	O	I	X	I
	Deselect	O	X	O	I	X	O

NOTE:

1. For CDP1800 Mode, refers to high order memory address bit level at time when TPA ↘ transition takes place.

FIGURE 3. CHIP ENABLE OUTPUT TIMING WAVEFORMS FOR CDP1800 BASED SYSTEMS

Dynamic Electrical Specifications At T_A = -40 to +85°C, V_{DD} = 5V ±5%, Input t_R, t_F = 10ns; C_L = 50pF and 1 TTL Load

PARAMETER		LIMITS CDP1826C (NOTE 1) MIN	(NOTE 2) TYP	MAX	UNITS
READ - CYCLE TIMES (FIGURES 4 AND 5)					
Address to TPA Setup	t_{ASH}	100	-	-	ns
Address to TPA Hold	t_{AH}	100	-	-	ns
Access from Address Change	T_{AA}	-	500	1000	ns
TPA Pulse Width	t_{PAW}	200	-	-	ns
Output Valid from $\overline{MRD}$	t_{AM}	-	500	1000	ns
Access from Chip Select	t_{AC}	-	500	1000	ns
CEO Delay from TPA ↘ Edge	t_{CA}	-	150	300	ns
$\overline{MRD}$ to CEO Delay	t_{MC}	75	-	-	ns
Output High Z from Invalid $\overline{MRD}$	t_{RHZ}	-	-	125	ns
Output High Z from Chip Deselect	t_{SHZ}	-	-	225	ns

NOTES:

1. Time required by a limit device to allow tor the indicated function.
2. Typical values are or T_A = 25°C and nominal V_{DD}.

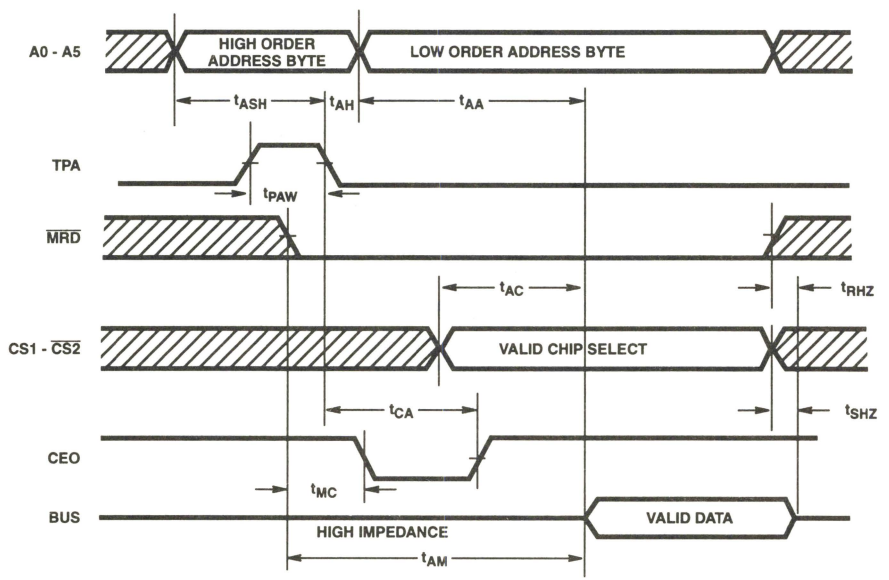


FIGURE 4. TIMING WAVEFORMS FOR READ CYCLE 1

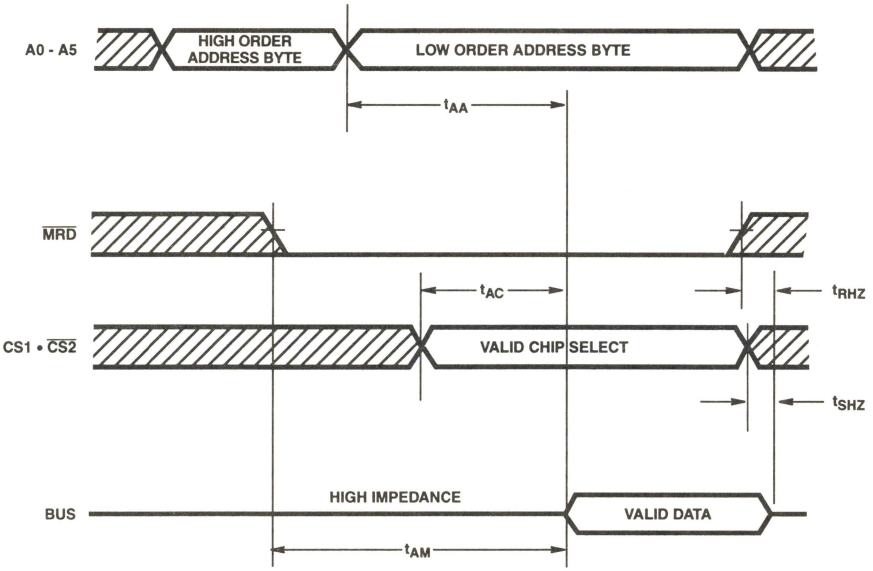


FIGURE 5. TIMING WAVEFORMS FOR READ-CYCLE 2 (TPA HIGH)

Dynamic Electrical Specifications At T_A = -40 to +85°C, V_{DD} = 5V ± 5%,Input t_R, t_F = 10ns; C_L = 50pF and 1 TTL Load

PARAMETER		LIMITS CDP1826C (NOTE 1) MIN	(NOTE 2) TYP	MAX	UNITS
WRITE - CYCLE TIMES (FIGURES 6 AND 7)					
Address to TPA Setup, High Byte	t_{ASH}	100	-	-	ns
Address to TPA Hold	t_{AH}	100	-	-	ns
Address Setup, Low Byte	T_{ASL}	500	250	-	ns
TPA Pulse Width	t_{PAW}	200	-	-	ns
Chip Select Setup	t_{CS}	700	350	-	ns
Write Pulse Width	t_{WW}	300	200	-	ns
Write Recovery	t_{WR}	100	-	-	ns
Data Setup	t_{DS}	400	200	-	ns
Data Hold from End of $\overline{MWR}$	t_{DH1}	100	50	-	ns
Data Hold from End of Chip Select	t_{DH2}	125	50	-	ns

NOTES:

1. Time required by a limit device to allow tor the indicated function.
2. Typical values are for T_A = 25°C and nominal V_{DD}.

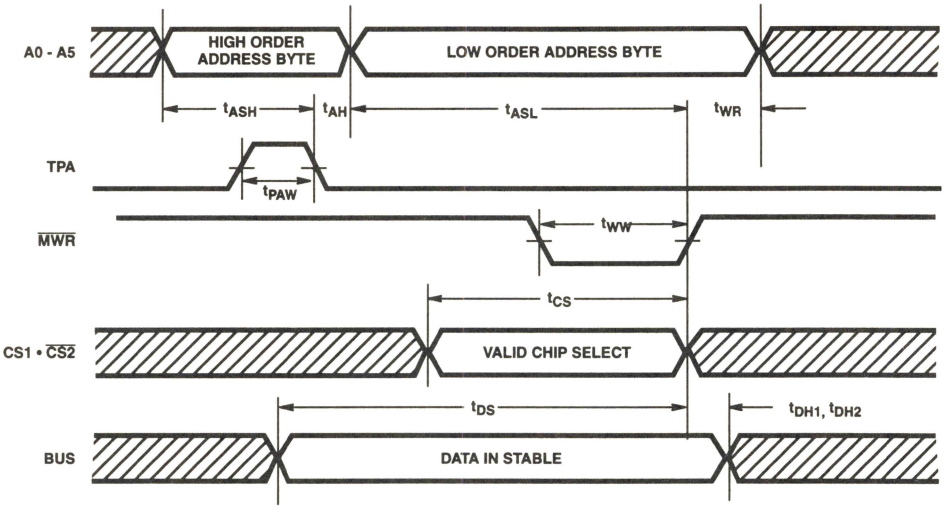


FIGURE 6. TIMING WAVEFORMS FOR WRITE-CYCLE 1

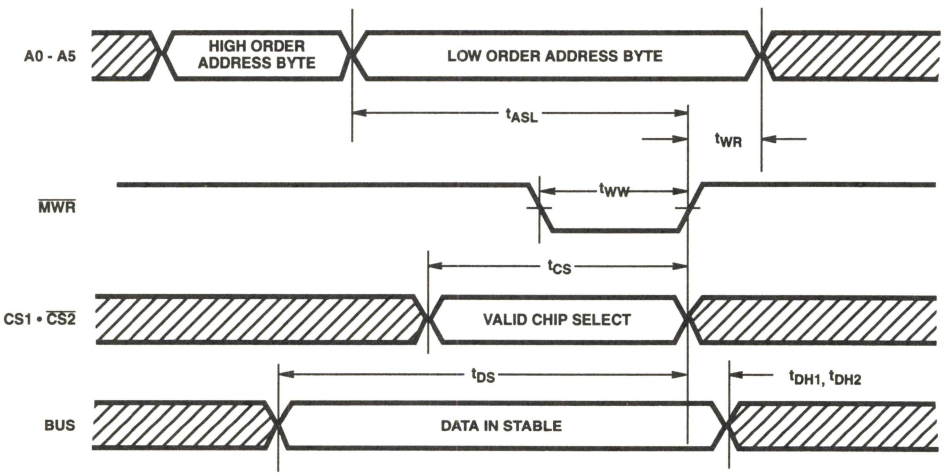


FIGURE 7. TIMING WAVEFORMS FOR WRITE-CYCLE 2 (TPA = HIGH)

Data Retention Specifications At T_A = -40 to +85°C, see Figure 8

PARAMETER	TEST CONDITIONS V_{DR} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	LIMITS CDP1826C MAX	UNITS
Minimum Data Retention Voltage V_{DR}	-	-	-	2	2.5	V
Data Retention Quiescent Current t_{DD}	2.5	-	-	5	25	µA
Chip Deselect to Data Retention Time t_{CDR}	-	5	600	-	-	ns
Recovery to Normal Operation Time t_{RC}	-	5	600	-	-	ns
V_{DD} to V_{DR} Rise and Fall Time t_R, t_F	2.5	5	1	-	-	µA

NOTE:

1. Typical values are or T_A = 25°C and nominal V_{DD}.

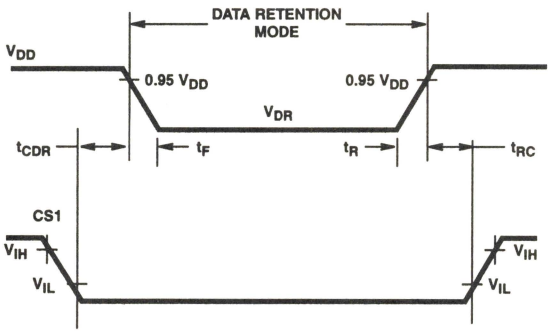


FIGURE 8. LOW V_{DD} DATA RETENTION TIMING WAVEFORMS

HARRIS SEMICONDUCTOR

MWS5101, MWS5101A

256-Word x 4-Bit LSI Static RAM

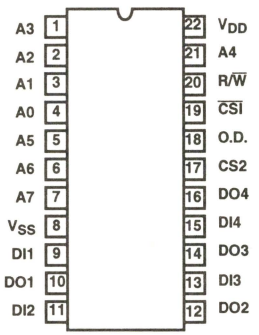
March 1997

Features

- Industry Standard Pinout
- Very Low Operating Current . . . . . 8mA at V_{DD} = 5V and Cycle Time = 1µs
- Two Chip Select Inputs Simple Memory Expansion
- Memory Retention for Standby. . . . . 2V (Min) Battery Voltage
- Output Disable for Common I/O Systems
- Three-State Data Output for Bus Oriented Systems
- Separate Data Inputs and Outputs
- TTL Compatible (MWS5101A)

Pinout

MWS5101, MWS5101A
(PDIP, SBDIP)
TOP VIEW



Description

The MWS5101 and MWS5101A are 256 word by 4-bit static random access memories designed for use in memory systems where high speed, very low operating current, and simplicity in use are desirable. They have separate data inputs and outputs and utilize a single power supply of 4V to 6.5V. The MWS5101 and MWS5101A differ in input voltage characteristics (MWS5101A is TTL compatible).

Two Chip Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems by forcing the output into a high impedance state during a write operation independent of the Chip Select input condition. The output assumes a high impedance state when the Output Disable is at high level or when the chip is deselected by $\overline{CS1}$ and/or CS2.

The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5V operation, excellent system noise margin is preserved by using an external pull-up resistor at each input.

For applications requiring wider temperature and operating voltage ranges, the mechanically and functionally equivalent static RAM, CDP1822 may be used.

The MWS5101 and MWS5101A types are supplied in 22 lead hermetic dual-in-line, sidebrazed ceramic packages (D suffix), in 22 lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Ordering Information

PACKAGE	TEMP. RANGE	MWS5101		MWS5101A		PKG. NO.
		250ns	350ns	250ns	350ns	
PDIP Burn-In	0°C to +70°C	MWS5101EL2	MWS5101ELS	MWS5101AEL2	MWS5101AEL3	E22.4
					MWS5101AEL3X	E22.4
SBDIP Burn-In	0°C to +70°C	-	MWS5101DL3X	-	MWS5101ADL3	D22.4A
						D22.4A

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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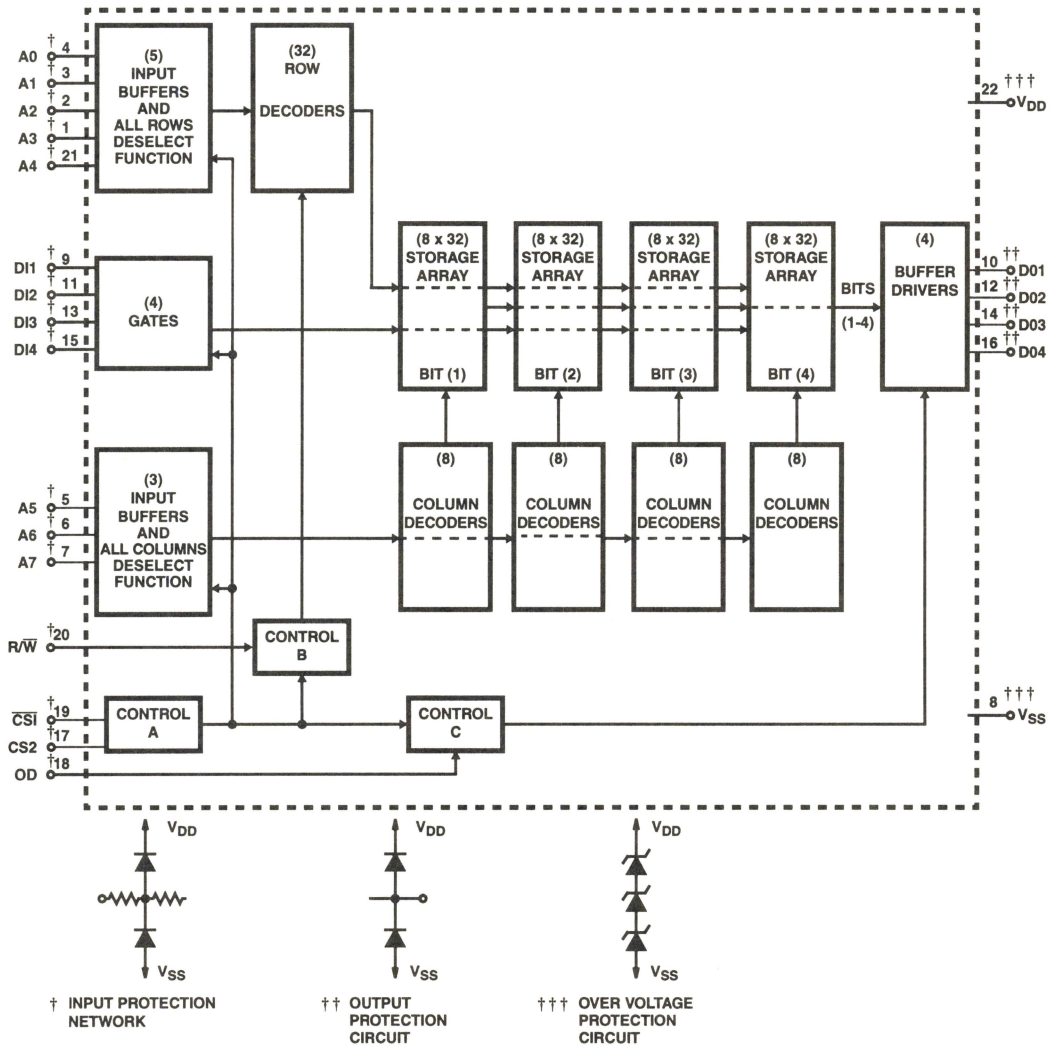
File Number **1106.2**

OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	CHIP SELECT 1 ($\overline{CS_1}$)	CHIP SELECT 2 (CS_2)	OUTPUT DISABLE (OD)	READ/WRITE (R/$\overline{W}$)	
Read	0	1	0	1	Read
Write	0	1	0	0	Data In
Write	0	1	1	0	High Impedance
Standby	1	X	X	X	High Impedance
Standby	X	0	X	X	High Impedance
Output Disable	X	X	1	X	High Impedance

NOTE: Logic 1 = High, Logic 0 = Low, X = Don't Care.

Functional Block Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal) ..... -0.5V to +7V
Input Voltage Range, All Inputs ..... -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input ..... ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	75	N/A
SBDIP Package	80	21

Operating Temperature Range (T_A)
Package Type D ..... -55°C to +125°C
Package Type E ..... -40°C to +85°C
Maximum Storage Temperature Range (T_{STG}) ... -65°C to +150°C
Maximum Junction Temperature
Ceramic Package ..... +175°C
Plastic Package ..... +150°C
Maximum Lead Temperature (During Soldering)
At distance 1/16 ±1/32 In. (1.59 ±0.79mm)
from case for 10s max ..... +265°C

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS MIN	LIMITS MAX	UNITS
DC Operating Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V

Static Electrical Specifications

At T_A = 0°C to +70°C, V_{DD} = 5V ±5%

PARAMETER	SYMBOL	CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	MWS5101 MIN	MWS5101 (NOTE 1) TYP	MWS5101 MAX	MWS5101A MIN	MWS5101A (NOTE 1) TYP	MWS5101A MAX	UNITS
Quiescent Device Current L2 Types	I_{DD}	-	0, 5	-	25	50	-	25	50	µA
Quiescent Device Current L3 Types		-	0, 10	-	100	200	-	100	200	µA
Output Low (Sink) Current	I_{OL}	0.4	0, 5	2	4	-	2	4	-	mA
Output High (Source) Current	I_{OH}	4.6	0, 5	-1	-2	-	-1	-2	-	mA
Output Voltage Low-Level	V_{OL}	-	0, 5	-	0	0.1	-	0	0.1	V
Output Voltage High-Level	V_{OH}	-	0, 5	4.9	5	-	4.9	5	-	V
Input Low Voltage	V_{IL}	-	-	-	-	1.5	-	-	0.65	V
Input High Voltage	V_{IH}	-	-	3.5	-	-	2.2	-	-	V
Input Leakage Current	I_{IN}	-	0, 5	-	-	±5	-	-	±5	µA
Operating Current (Note 2)	I_{DD1}	-	0, 5	-	4	8	-	4	8	mA
Three-State Output Leakage Current L2 Types	I_{OUT}	0, 5	0, 5	-	-	±5	-	-	±5	µA
Three-State Output Leakage Current L3 Types		0, 5	0, 5	-	-	±5	-	-	±5	µA
Input Capacitance	C_{IN}	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = +25°C and nominal V_{DD}.
2. Outputs open circuited; Cycle time = 1µs.

Dynamic Electrical Specifications at $T_A = 0^oC$ to $+70^oC$, $V_{DD} = 5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS (NOTE 1)						UNITS
		L2 TYPES			L3 TYPES			
		(NOTE 2) MIN	(NOTE 3) TYP	MAX	(NOTE 2) MIN	(NOTE 3) TYP	MAX	
READ CYCLE TIMES (FIGURE 1)								
Read Cycle	t_{RC}	250	-	-	350	-	-	ns
Access from Address	t_{AA}	-	150	250	-	200	350	ns
Output Valid from $\overline{\text{Chip Select}}$ 1	t_{DOA1}	-	150	250	-	200	350	ns
Output Valid from Chip Select 2	t_{DOA2}	-	150	250	-	200	350	ns
Output Valid from Output Disable	t_{DOA3}	-	-	110	-	-	150	ns
Output Hold from $\overline{\text{Chip Select}}$ 1	t_{DOH1}	20	-	-	20	-	-	ns
Output Hold from Chip Select 2	t_{DOH2}	20	-	-	20	-	-	ns
Output Hold from Output Disable	t_{DOH3}	20	-	-	20	-	-	ns
WRITE CYCLE TIMES (FIGURE 2)								
Write Cycle	t_{WC}	300	-	-	400	-	-	ns
Address Setup	t_{AS}	110	-	-	150	-	-	ns
Write Recovery	t_{WR}	40	-	-	50	-	-	ns
Write Width	t_{WRW}	150	-	-	200	-	-	ns
Input Data Setup Time	t_{DS}	150	-	-	200	-	-	ns
Data in Hold	t_{DH}	40	-	-	50	-	-	ns
$\overline{\text{Chip Select}}$ 1 Setup	$t_{\overline{CS}1S}$	110	-	-	150	-	-	ns
Chip Select 2 Setup	t_{CS2S}	110	-	-	150	-	-	ns
$\overline{\text{Chip Select}}$ 1 Hold	$t_{\overline{CS}1H}$	0	-	-	0	-	-	ns
Chip Select 2 Hold	t_{CS2H}	0	-	-	0	-	-	ns
Output Disable Setup	t_{ODS}	110	-	-	150	-	-	ns

NOTES:

1. MWS5101: t_R, t_F = 20ns, $V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$; C_L = 100pF and MWS5101A: t_R, t_F = 20ns, V_{IH} = 2.2V, V_{IL} = 0.65V; C_L = 50pF and 1 TTL Load.
2. Time required by a limit device to allow for the indicated function.
3. Typical values are for $T_A = 25^oC$ and nominal V_{DD}.

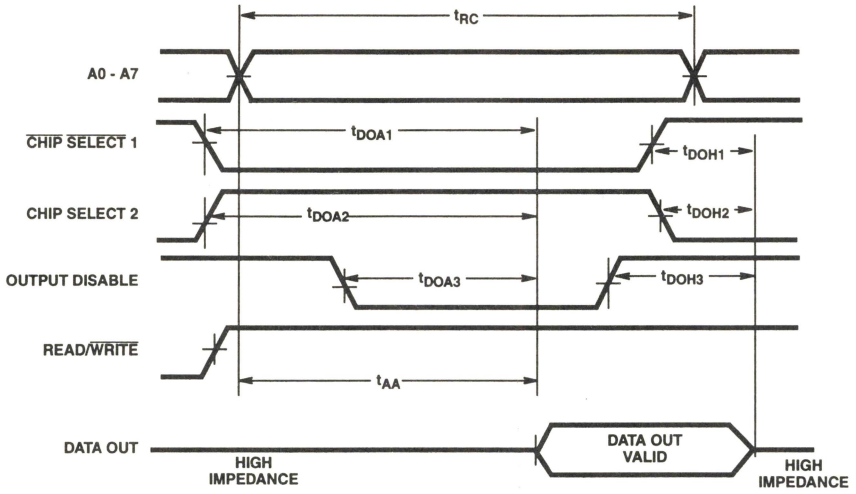
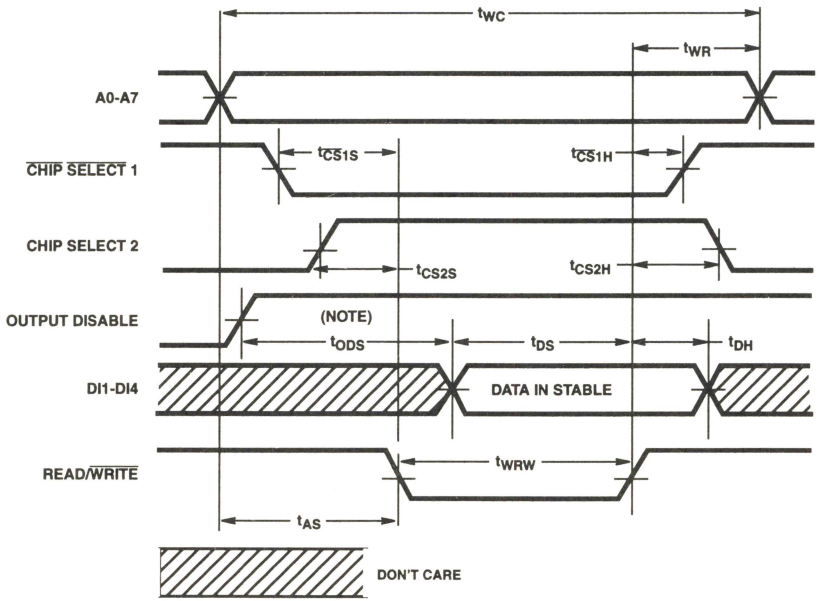


FIGURE 1. READ CYCLE TIMING WAVEFORMS



NOTE: t_{ODS} is required for common I/O operation only; for separate I/O operations, output disable is "don't care".

FIGURE 2. WRITE CYCLE TIME WAVEFORMS

Data Retention Specifications at $T_A = 0^oC$ to $+70^oC$; See Figure 3

PARAMETER		SYMBOL	TEST CONDITIONS		LIMITS			UNITS
					ALL TYPES			
			V_{DR} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	
Minimum Data Retention Voltage		V_{DR}	-	-	-	1.5	2	V
Data Retention Quiescent Current	L2 Types	I_{DD}	2	-	-	2	10	µA
	L3 Types		2	-	-	5	50	µA
Chip Deselect to Data Retention Time		t_{CDR}	-	5	600	-	-	ns
Recovery to Normal Operation Time		t_{RC}	-	5	600	-	-	ns
V_{DD} to V_{DR} Rise and Fall Time		t_R, t_F	2	5	1	-	-	µs

NOTE:

1. Typical Values are for $T_A = 25^oC$ and nominal V_{DD}.

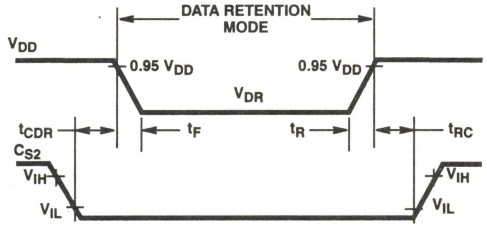


FIGURE 3. LOW V_{DD} DATA RETENTION TIMING WAVEFORMS

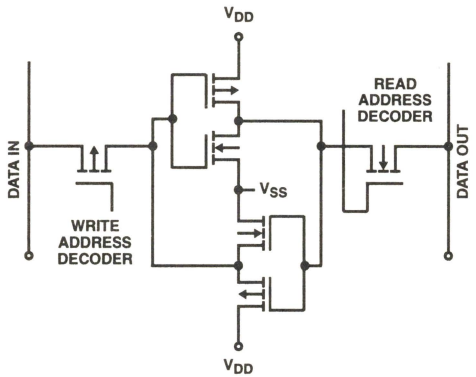


FIGURE 4. MEMORY CELL CONFIGURATION

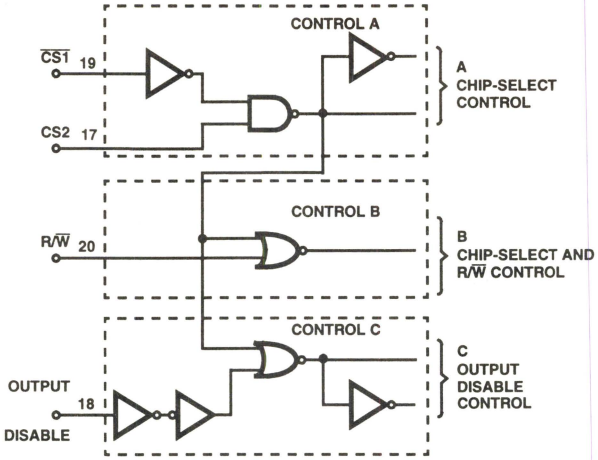


FIGURE 5. LOGIC DIAGRAM OF CONTROLS FOR MWS5101, MWS5101A

HM-6508

March 1997

1024 x 1 CMOS RAM

Features

- Low Power Standby . . . . . 50µW Max
- Low Power Operation . . . . . 20mW/MHz Max
- Fast Access Time. . . . . 180ns Max
- Data Retention . . . . . 2.0V Min
- TTL Compatible Input/Output
- High Output Drive - 2 TTL Loads
- On-Chip Address Register

Description

The HM-6508 is a 1024 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On-Chip latches are provided for address, allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

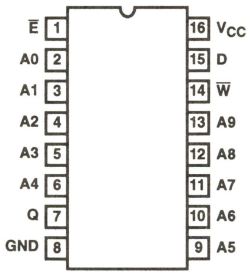
The HM-6508 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

PACKAGE	TEMPERATURE RANGE	180ns	250ns	PKG. NO.
PDIP	-40°C to +85°C	HM3-6508B-9	HM3-6508-9	E16.3
CERDIP	-40°C to +85°C	HM1-6508B-9	HM1-6508-9	F16.3

Pinout

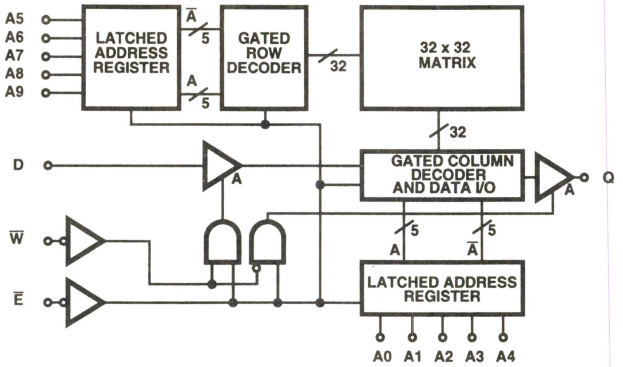
HM-6508
(PDIP, CERDIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Functional Diagram



NOTES:

1. All lines positive logic - active high.
2. Three-state buffers: A high → output active.
3. Address latches and gated decoders: latch on falling edge of $\overline{E}$ and gate on falling edge of $\overline{E}$.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
Typical Derating Factor . . . . . 1.5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
HM-6508B-9, HM-6508-9 . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}	θ_{JC}
PDIP Package	90°C/W	N/A
CERDIP Package	75°C/W	15°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 1925 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6508B-9, HM-6508-9)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		-	10	µA	IO = 0mA, VI = V_{CC} or GND, V_{CC} = 5.0V
ICCOP	Operating Supply Current (Note 1)		-	4	mA	$\overline{E}$ = 1MHz, IO = 0mA, VI = V_{CC} or GND, V_{CC} = 5.5V
ICCDR	Data Retention Supply Current	HM-6508B-9	-	5	µA	V_{CC} = 2.0V, IO = 0mA, VI = V_{CC} or GND, $\overline{E}$ = V_{CC}
		HM-6508-9	-	10	µA	
VCCDR	Data Retention Supply Voltage		2.0	-	V	
II	Input Leakage Current		-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IOZ	Output Leakage Current		-1.0	+1.0	µA	VO = V_{CC} or GND, V_{CC} = 5.5V
VIL	Input Low Voltage		-0.3	0.8	V	V_{CC} = 4.5V
VIH	Input High Voltage		V_{CC} -2.0	V_{CC} +0.3	V	V_{CC} = 5.5V
VOL	Output Low Voltage		-	0.4	V	IO = 3.2mA, V_{CC} = 4.5V
VOH	Output High Voltage		2.4	-	V	IO = -0.4mA, V_{CC} = 4.5V

Capacitance T_A = +25°C

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	6	pF	f = 1MHz, All measurements are referenced to device GND
CO	Output Capacitance (Note 2)	10	pF	

NOTES:

1. Typical derating 1.5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes 1.

AC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6508B-9, HM-6508-9)

SYMBOL	PARAMETER	HM-6508B-9		HM-6508-9		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
(1) TELQV	Chip Enable Access Time	-	180	-	250	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	180	-	250	ns	(Notes 1, 3, 4)
(3) TELQX	Chip Enable Output Enable Time	5	120	5	160	ns	(Notes 2, 3)

AC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6508B-9, HM-6508-9) **(Continued)**

SYMBOL	PARAMETER	HM-6508B-9		HM-6508-9		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
(4) TWLQZ	Write Enable Output Disable Time	-	120	-	160	ns	(Notes 2, 3)
(5) TEHQZ	Chip Enable Output Disable Time	-	120	-	160	ns	(Notes 2, 3)
(6) TELEH	Chip Enable Pulse Negative Width	180	-	250	-	ns	(Notes 1, 3)
(7) TEHEL	Chip Enable Pulse Positive Width	100	-	100	-	ns	(Notes 1, 3)
(8) TAVEL	Address Setup Time	0	-	0	-	ns	(Notes 1, 3)
(9) TELAX	Address Hold Time	40	-	50	-	ns	(Notes 1, 3)
(10) TDVWH	Data Setup Time	80	-	110	-	ns	(Notes 1, 3)
(11) TWHDX	Data Hold Time	0	-	0	-	ns	(Notes 1, 3)
(12) TWLEH	Chip Enable Write Pulse Setup Time	100	-	130	-	ns	(Notes 1, 3)
(13) TELWH	Chip Enable Write Pulse Hold Time	100	-	130	-	ns	(Notes 1, 3)
(14) TWLWH	Write Enable Pulse Width	100	-	130	-	ns	(Notes 1, 3)
(15) TELEL	Read or Write Cycle Time	280	-	350	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0.8V to V_{CC} -2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5V and 5.5V.
4. TAVQV = TELQV + TAVEL.

Timing Waveforms

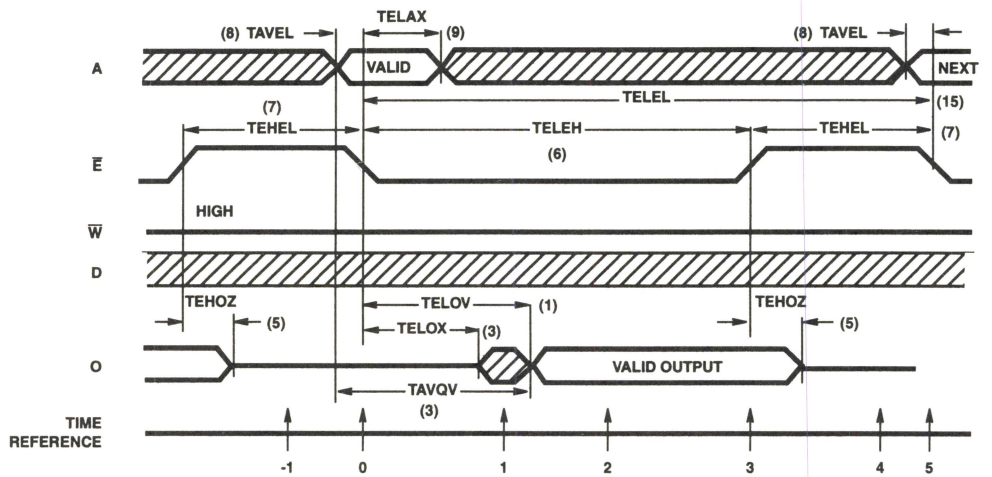


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	X	Output Enabled
2	L	H	X	X	V	Output Valid
3	↗	H	X	X	V	Read Accomplished
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

In the HM-6508 Read Cycle, the address information is latched into the On-Chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation.

During time (T = 1) the data output becomes enabled; however, the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the chip and force the output buffer to a high impedance state. After the required $\overline{E}$ high time (TEHEL) the RAM is ready for the next memory cycle (T = 4).

Timing Wavforms (continued)

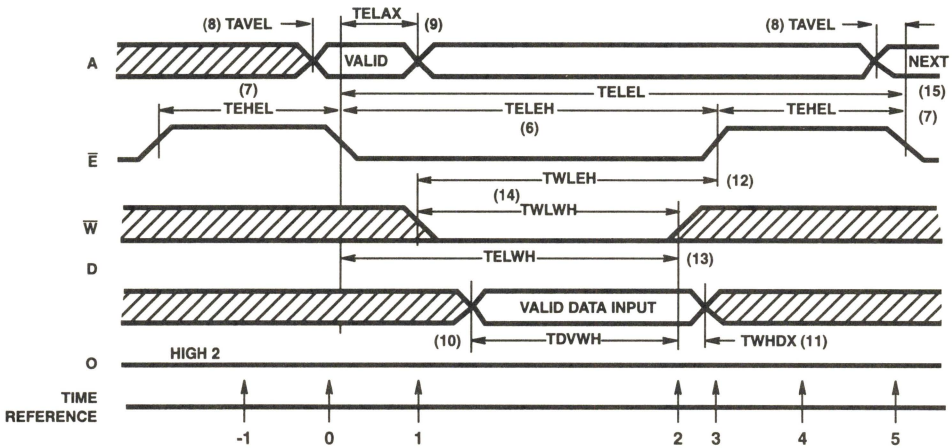


FIGURE 2. WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	X	V	X	Z	Cycle Begins, Addresses are Latched
1	L	↘	X	X	Z	Write Period Begins
2	L	↗	X	V	Z	Data is Written
3	↗	H	X	X	Z	Write Completed
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

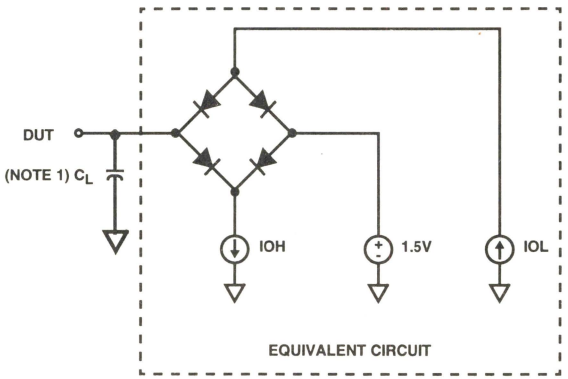
The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the On-Chip registers. The write portion of the cycle is defined as both $\overline{E}$ and $\overline{W}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle, provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$ or $\overline{W}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH), plus an output enable time (TELQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH). The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will ensure that the output buffers are not active.

Test Load Circuit



NOTE:

1. Test head capacitance includes stray and jig capacitance.

HM-6508/883

March 1997

1024 x 1 CMOS RAM

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Power Standby . . . . . 50μW Max**
- **Low Power Operation . . . . . 20mW/MHz Max**
- **Fast Access Time. . . . . 180ns Max**
- **Data Retention . . . . . 2.0V Min**
- **TTL Compatible Input/Output**
- **High Output Drive - 2 TTL Loads**
- **On-Chip Address Register**

Description

The HM-6508/883 is a 1024 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

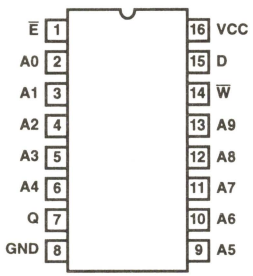
The HM-6508/883 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

PACKAGE	TEMP. RANGE	180ns	250ns	PKG. NO.
CERDIP	-55°C to +125°C	HM1-6508B/883	HM1-6508/883	F16.3

Pinout

HM1-6508/883
(CERDIP)
TOP VIEW



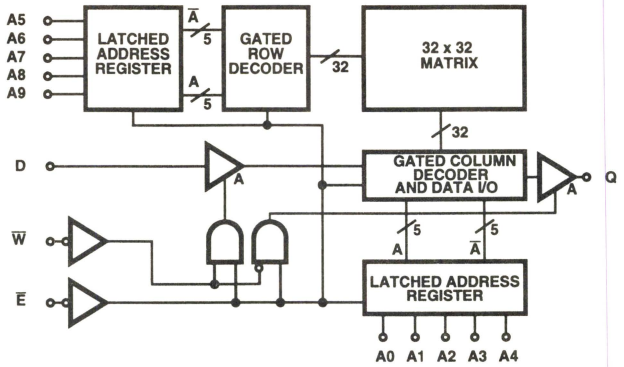
PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2985.1**

Functional Diagram



NOTES:

1. All lines positive logic - active high.
2. Three-state buffers: A high → output active.
3. Address latches and gated decoders: Latch on falling edge of $\overline{E}$ and gate on falling edge of $\overline{E}$.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
Typical Derating Factor . . . . . 1.5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . VCC -2.0V to VCC
Input Rise and Fall Time . . . . . 40ns Max.

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}	θ_{JC}
CERDIP Package	75°C/W	15°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 1925 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. HM-6508/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V, IOL = 3.2mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V, IOH = -0.4mA	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5V, VO = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC, IO = 0mA, VI = VCC or GND	1, 2, 3	$-55°C \le T_A \le +125°C$			
HM-6508B/883					-	5	µA
HM-6508/883					-	10	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 2), $\overline{E}$ = 1MHz, IO = 0mA,	1, 2, 3	$-55°C \le T_A \le +125°C$	-	4	mA
Standby Supply Current	ICCSB	VCC = 5.0V, IO = 0mA, VI = VCC or GND	1, 2, 3	$-55°C \le T_A \le +125°C$	-	10	µA

NOTES:

1. All voltages referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.

TABLE 2. HM-6508/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS				UNITS
					HM-6508B/883		HM-6508/883		
					MIN	MAX	MIN	MAX	
Chip Enable Access Time	(1) TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	180	-	250	ns
Address Access Time	(2) TAVQV	VCC = 4.5 and 5.5V, Note 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	180	-	250	ns
Chip Enable Output Disable Time	(3) TELQX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	5	-	5	-	ns
Write Enable Output Disable Time	(4) TWLQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	160	ns
Chip Enable Output Disable Time	(5) TEHQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	160	ns
Chip Enable Pulse Negative Width	(6) TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	180	-	250	-	ns
Chip Enable Pulse Positive Width	(7) TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	100	-	ns
Address Setup Time	(8) TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Address Hold Time	(9) TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	50	-	ns
Data Setup Time	(10) TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	80	-	110	-	ns
Data Hold Time	(11) TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Chip Enable Write Pulse Setup Time	(12) TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	130	-	ns
Chip Enable Write Pulse Hold Time	(13) TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	130	-	ns
Write Enable Pulse Width	(14) TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	130	-	ns
Read or Write Cycle Time	(15) TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	280	-	350	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC -2.0V; Input rise and fall times: 5ns (max); input and output timing reference level: 1.5V; Output load: 1TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-6508/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	T_A = +25°C	-	6	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	T_A = +25°C	-	10	pF

NOTE:

1. The parameters listed in Table 3 are controlled via design or process; parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Timing Waveforms

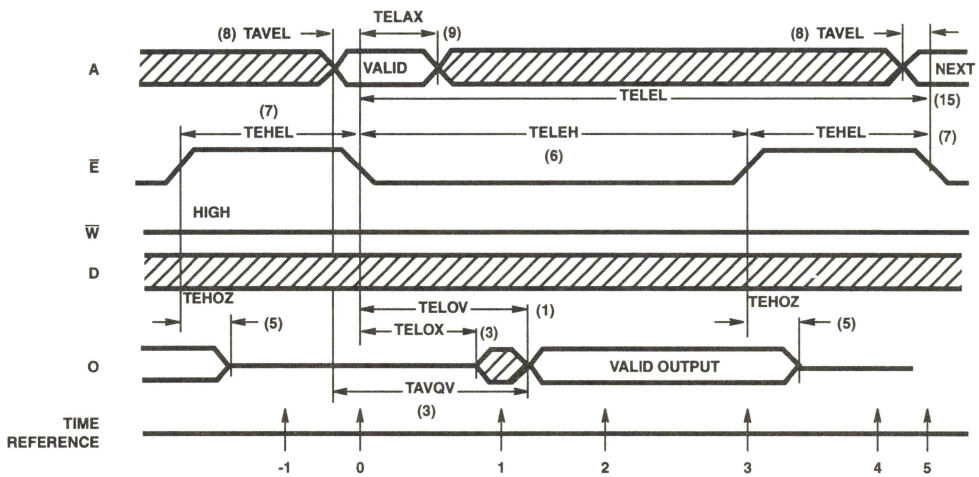


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	X	Output Enabled
2	L	H	X	X	V	Output Valid
3	↗	H	X	X	V	Read Accomplished
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

In the HM-6508/883 Read Cycle, the address information is latched into the on-chip registers on the falling edge of E (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the data output becomes enabled; however, the data is not valid until during time (T = 2).

$\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the chip and force the output buffer to a high impedance state. After the required $\overline{E}$ high time (TEHEL) the RAM is ready for the next memory cycle (T = 4).

Timing Wavforms (continued)

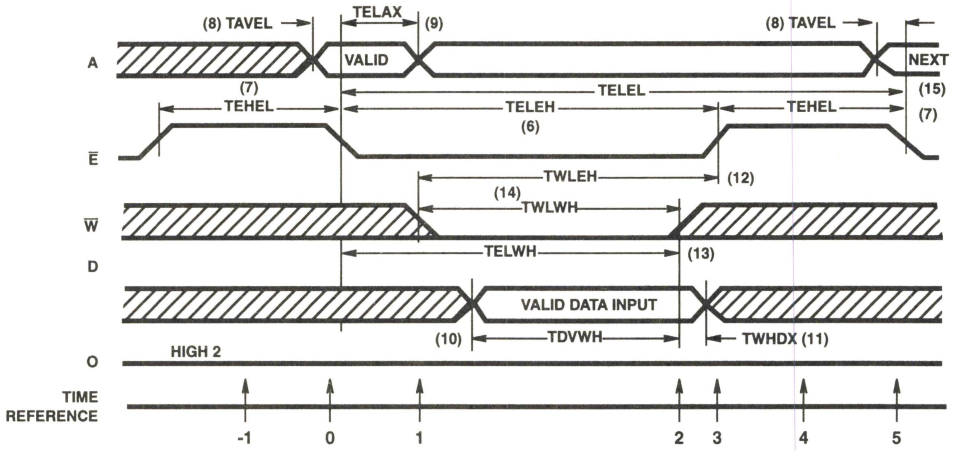


FIGURE 2. WRITE CYCLE

TRUTH TABLE

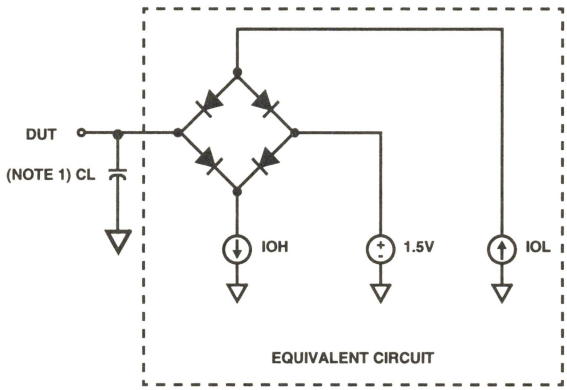
TIME REFERENCE	INPUTS				OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	X	V	X	Z	Cycle Begins, Addresses are Latched
1	L	↘	X	X	Z	Write Period Begins
2	L	↗	X	V	Z	Data is Written
3	↗	H	X	X	Z	Write Completed
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as both $\overline{E}$ and $\overline{W}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle, provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$ or $\overline{W}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH), plus an output enable time (TELQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH). The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method, allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will ensure that the output buffers are not active.

Test Load Circuit

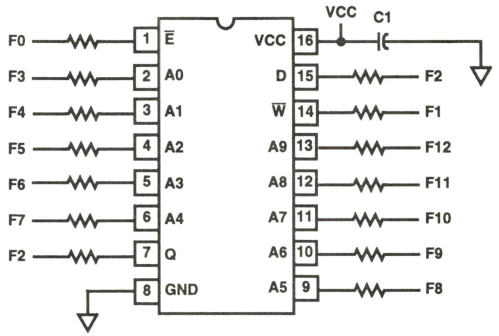


NOTE:

1. Test head capacitance includes stray and jig capacitance.

Burn-In Circuit

HM6508/883 CERDIP



NOTES:

1. All resistors 47kΩ ±5%.
2. F0 = 100kHz ±10%.
3. F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2. . . F12 = F11 ÷ 2.
4. VCC = 5.5V ±0.5V.
5. VIH = 4.5V ±10%.
6. VIL = -0.2V to +0.4V.
7. C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
130 x 150 x 19 ±1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

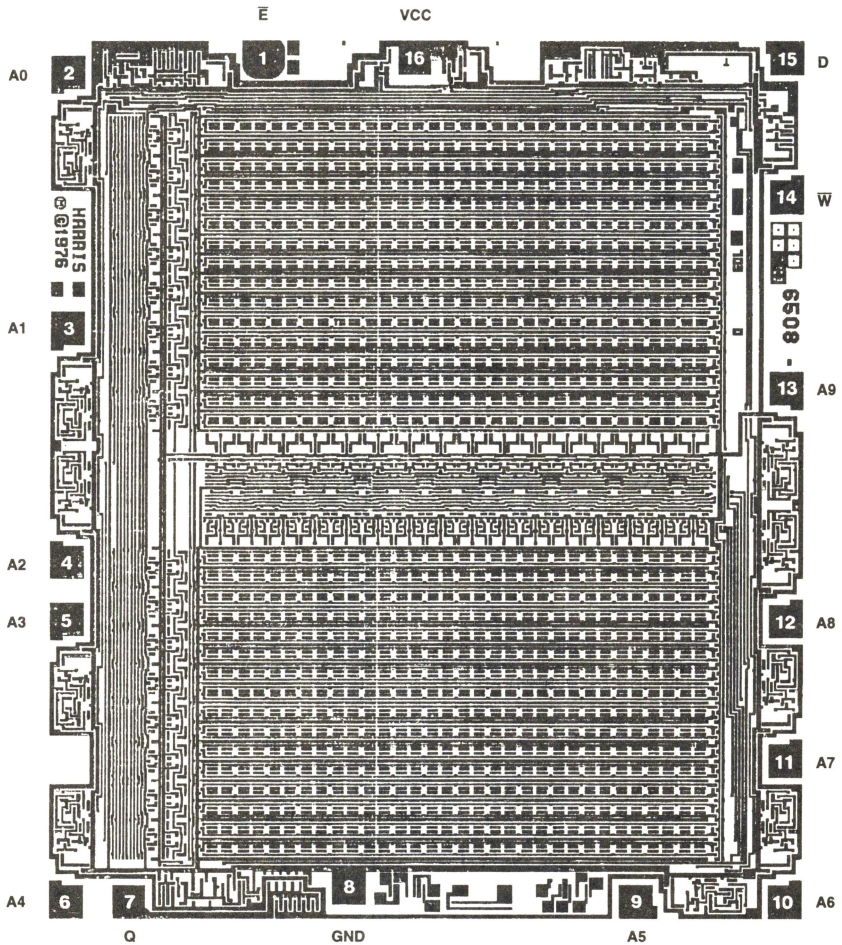
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
1.342×10^5 A/cm^2

LEAD TEMPERATURE (10s soldering):
$\leq 300^{\circ}C$

Metallization Mask Layout

HM-6508/883



HARRIS SEMICONDUCTOR

HM-6518

March 1997

1024 x 1 CMOS RAM

Features

- Low Power Standby . . . . . 50µW Max
- Low Power Operation . . . . . 20mW/MHz Max
- Fast Access Time. . . . . 180ns Max
- Data Retention . . . . . at 2.0V Min
- TTL Compatible Input/Output
- High Output Drive - 2 TTL Loads
- High Noise Immunity
- On-Chip Address Register
- Two-Chip Selects for Easy Array Expansion
- Three-State Output

Description

The HM-6518 is a 1024 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

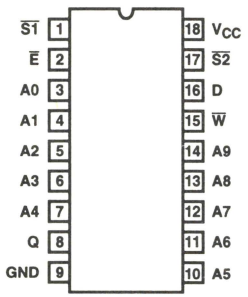
The HM-6518 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over-temperature.

Ordering Information

PACKAGE	TEMP. RANGE	180ns	250ns	PKG. NO.
CERDIP	-40°C to +85°C	HM1-6518B-9	HM1-6518-9	F18.3

Pinout

HM-6518
(CERDIP)
TOP VIEW



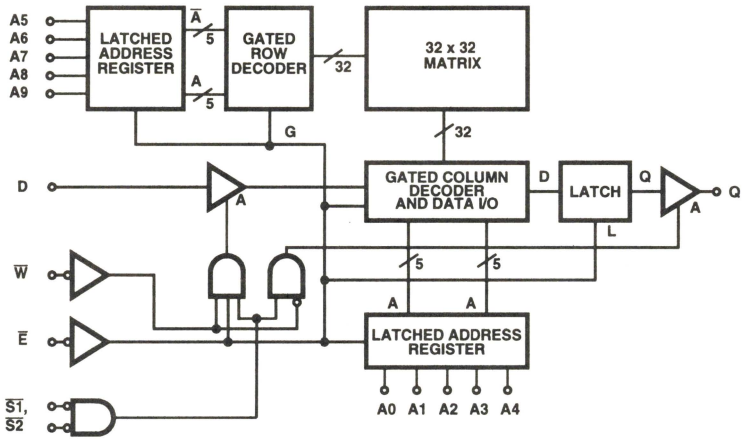
PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
S	Chip Select
D	Data Input
Q	Data Output

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2987.1**

Functional Diagram



NOTES:

1. All lines positive logic - active high.
2. Three-state buffers: A high → output active.
3. Data latches: L high → Q = D; Q Latches on rising edge of L.
4. Address latches and gated decoders: Latch on falling edge of $\overline{E}$ and gate on falling edge of $\overline{E}$.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
HM-6518B-9, HM-6518-9 . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}	θ_{JC}
CERDIP Package	75°C/W	15°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 1936 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6518B-9, HM-6518-9)

PARAMETER		SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
Standby Supply Current		ICCSB	-	10	µA	IO = 0mA, VI = V_{CC} or GND, V_{CC} = 5.5V
Operating Supply Current (Note 1)		ICCOP	-	4	mA	$\overline{E}$ = 1MHz, IO = 0mA, VI = V_{CC} or GND, V_{CC} = 5.5V
Data Retention Supply Current	HM-6518B-9	ICCDR	-	5	µA	V_{CC} = 2.0V, IO = 0mA, VI = V_{CC} or GND, $\overline{E}$ = V_{CC}
	HM-6518-9		-	10	µA	
Data Retention Supply Voltage		VCCDR	2.0	-	V	
Input Leakage Current		II	-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
Output Leakage Current		IOZ	-1.0	+1.0	µA	VO = V_{CC} or GND, V_{CC} = 5.5V
Input Low Voltage		VIL	-0.3	0.8	V	V_{CC} = 4.5V
Input High Voltage		VIH	V_{CC} -2.0	V_{CC} +0.3	V	V_{CC} = 5.5V
Output Low Voltage		VOL	-	0.4	V	IO = 3.2mA, V_{CC} = 4.5V
Output High Voltage		VOH	2.4	-	V	IO = -0.4mA, V_{CC} = 4.5V

Capacitance T_A = +25°C

PARAMETER	SYMBOL	MAX	UNITS	TEST CONDITIONS
Input Capacitance (Note 2)	CI	6	pF	f = 1MHz, All measurements are referenced to device GND
Output Capacitance (Note 2)	CO	10	pF	

NOTES:

1. Typical derating 1.5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

AC Electrical Specifications V_{CC} = 5V ± 10%; T_A = -40°C to +85°C (HM-6518B-9, HM-6518-9)

PARAMETER	SYMBOL	LIMITS				UNITS	TEST CONDITIONS
		HM-6518B-9		HM-6518-9			
		MIN	MAX	MIN	MAX		
Chip Enable Access Time	(1) TELQV	-	180	-	250	ns	(Notes 1, 3)
Address Access Time	(2) TAVQV	-	180	-	250	ns	(Notes 1, 3, 4)
Chip Select Output Enable Time	(3) TSLQX	5	120	5	160	ns	(Notes 2, 3)
Write Enable Output Disable Time	(4) TWLQZ	-	120	-	160	ns	(Notes 2, 3)
Chip Select Output Disable Time	(5) TSHQZ	-	120	-	160	ns	(Notes 2, 3)
Chip Enable Pulse Negative Width	(6) TELEH	180	-	250	-	ns	(Notes 1, 3)
Chip Enable Pulse Positive Width	(7) TEHEL	100	-	100	-	ns	(Notes 1, 3)
Address Setup Time	(8) TAVEL	0	-	0	-	ns	(Notes 1, 3)
Address Hold Time	(9) TELAX	40	-	50	-	ns	(Notes 1, 3)
Data Setup Time	(10) TDVWH	80	-	110	-	ns	(Notes 1, 3)
Data Hold Time	(11) TWHDX	0	-	0	-	ns	(Notes 1, 3)
Chip Select Write Pulse Setup Time	(12) TWLSH	100	-	130	-	ns	(Notes 1, 3)
Chip Enable Write Pulse Setup Time	(13) TWLEH	100	-	130	-	ns	(Notes 1, 3)
Chip Select Write Pulse Hold Time	(14) TSLWH	100	-	130	-	ns	(Notes 1, 3)
Chip Enable Write Pulse Hold Time	(15) TELWH	100	-	130	-	ns	(Notes 1, 3)
Write Enable Pulse Width	(16) TWLWH	100	-	130	-	ns	(Notes 1, 3)
Read or Write Cycle Time	(17) TELEL	280	-	350	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0.8V to V_{CC} - 2.0V; input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; output load: 1 TTL gate equivalent, C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5V and 5.5V.
4. TAVQV = TELQV + TAVEL.

Timing Waveforms

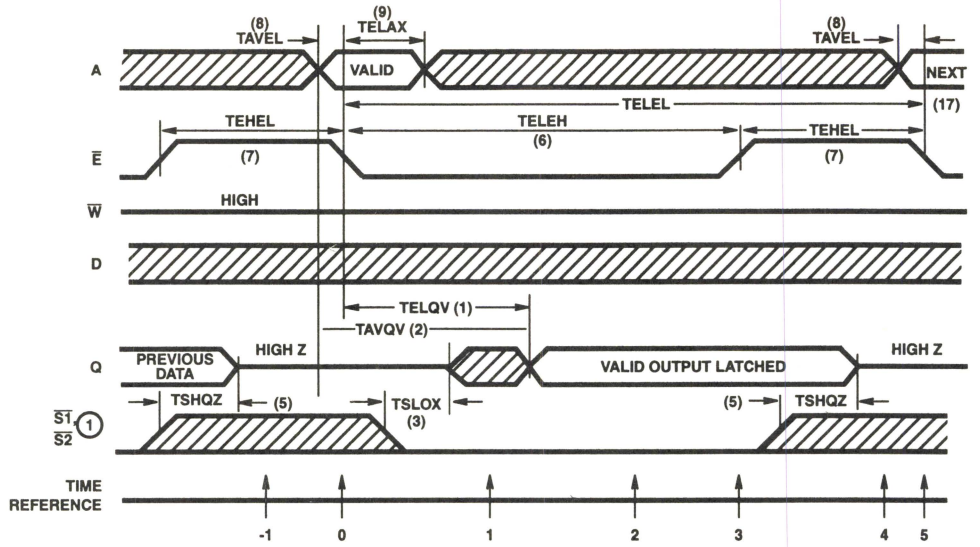


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS					OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	Z	Memory Disabled
0	↘	X	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	L	H	X	X	X	Output Enabled
2	L	L	H	X	X	V	Output Valid
3	↗	L	H	X	X	V	Output Latched
4	H	H	X	X	X	Z	Device Disabled, Prepare for Next Cycle (Same as -1)
5	↘	X	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

In the HM-6518 read cycle the address information is latched into the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. In order for the output to be read $\overline{S1}$, $\overline{S2}$ and $\overline{E}$ must be low, $\overline{W}$ must be high. When $\overline{E}$ goes high, the output data is latched into an on chip register. Taking either or both $\overline{S1}$ or $\overline{S2}$ high, forces the output buffer to a high impedance state. The output data may be re-enabled at any time by taking $\overline{S1}$ and $\overline{S2}$ low. On the falling edge of $\overline{E}$ the data will be unlatched.

Timing Wavforms (Continued)

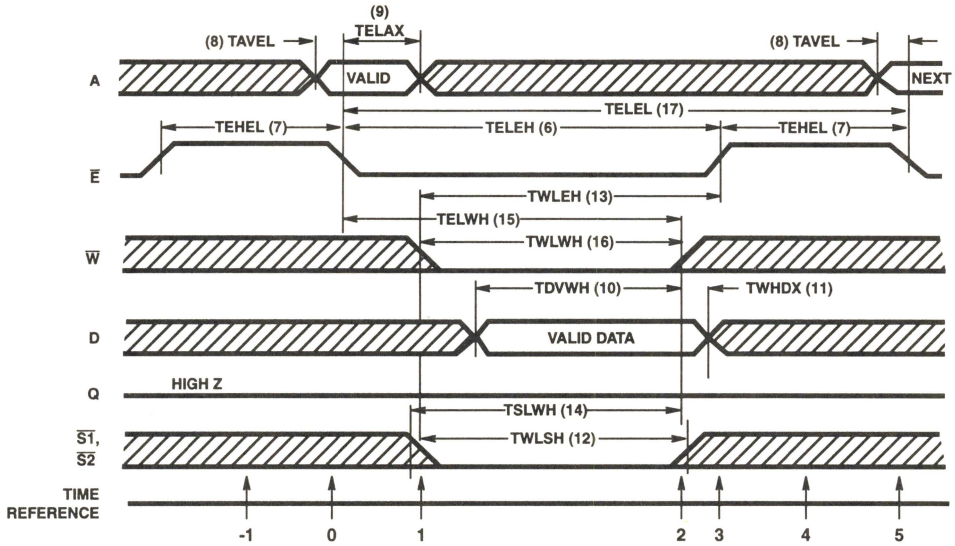


FIGURE 2. WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS					OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	X	Z	Memory Disabled
0	↘	X	X	V	X	Z	Cycle Begins, Addresses are Latched
1	L	L	L	X	V	Z	Write Mode has Begun
2	L	↗	L	X	V	Z	Data is Written
3	↗	X	X	X	X	Z	Write Completed
4	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

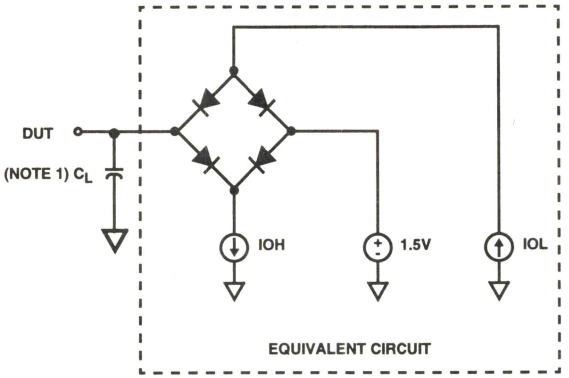
The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ and $\overline{S2}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$, $\overline{W}$, $\overline{S1}$ or $\overline{S2}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TSLQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method, allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will ensure that the output buffers are not active.

Test Load Circuit



NOTE:

1. Test head capacitance includes stray and jig capacitance.

HM-6518/883

March 1997

1024 x 1 CMOS RAM

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Power Standby . . . . . 50μW Max**
- **Low Power Operation . . . . . 20mW/MHz Max**
- **Fast Access Time. . . . . 180ns Max**
- **Data Retention . . . . . .at 2.0V Min**
- **TTL Compatible Input/Output**
- **High Output Drive - 2 TTL Loads**
- **High Noise Immunity**
- **On-Chip Address Register**
- **Two-Chip Selects for Easy Array Expansion**
- **Three-State Output**

Description

The HM-6518/883 is a 1024 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

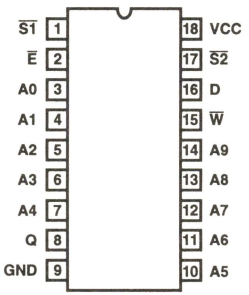
The HM-6518/883 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

PACKAGE	TEMP. RANGE	PART NUMBER	PKG. NO.
CERDIP	-55°C to +125°C	HM1-6518/883	F18.3

Pinout

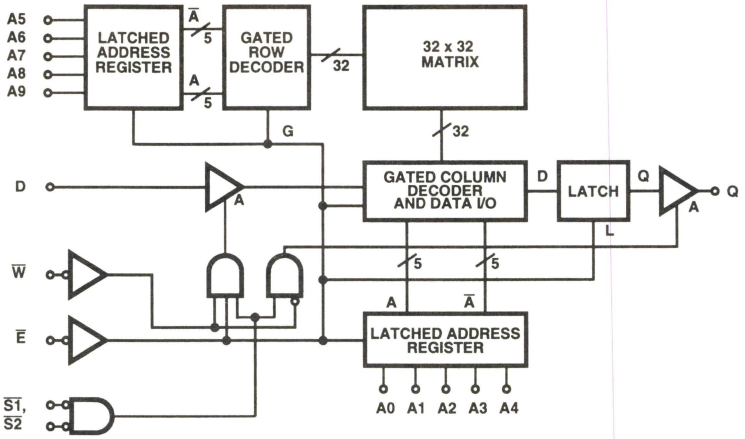
HM-6518/883
(CERDIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
S	Chip Select
D	Data Input
Q	Data Output

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Functional Diagram



NOTES:

1. All lines positive logic - active high.
2. Three-state buffers: A high → output active.
3. Data latches: L high → Q = D; Q Latches on rising edge of L.
4. Address latches and gated decoders: Latch on falling edge of $\overline{E}$ and gate on falling edge of $\overline{E}$.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . VCC -2.0V to VCC
Input Rise and Fall Time . . . . . 40ns Max

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}	θ_{JC}
CERDIP Package	75°C/W	15°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 1936 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. HM-6518/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V, IOL = 3.2mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V, IOH = -0.4mA	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5V, VO = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC, IO = 0mA, VI = VCC or GND	1, 2, 3	$-55°C \le T_A \le +125°C$			
HM-6518B/883					-	5	µA
HM-6518/883					-	10	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 2), $\overline{E}$ = 1MHz, IO = 0mA, VI = VCC or GND	1, 2, 3	$-55°C \le T_A \le +125°C$	-	4	mA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, VI = VCC or GND	1, 2, 3	$-55°C \le T_A \le +125°C$	-	10	µA

NOTES:

1. All voltages referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.

TABLE 2. HM-6518/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS				UNITS
					HM-6518B/883		HM-6518/883		
					MIN	MAX	MIN	MAX	
Chip Enable Access Time	(1) TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	180	-	250	ns
Address Access Time	(2) TAVQV	VCC = 4.5 and 5.5V, Note 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	180	-	250	ns
Chip Select Output Enable Time	(3) TSLQX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	5	-	5	-	ns
Write Enable Output Disable Time	(4) TWLQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	160	ns
Chip Select Output Disable Time	(5) TSHQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	160	ns
Chip Enable Pulse Negative Width	(6) TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	180	-	250	-	ns
Chip Enable Pulse Positive Width	(7) TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	100	-	ns
Address Setup Time	(8) TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Address Hold Time	(9) TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	50	-	ns
Data Setup Time	(10) TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	80	-	110	-	ns
Data Hold Time	(11) TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Chip Select Write Pulse Setup Time	(12) TWLSH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	130	-	ns
Chip Enable Write Pulse Setup Time	(13) TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	130	-	ns
Chip Select Write Pulse Hold Time	(14) TSLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	130	-	ns
Chip Enable Write Pulse Hold Time	(15) TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	130	-	ns
Write Enable Pulse Width	(16) TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	130	-	ns
Read or Write Cycle Time	(17) TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	280	-	350	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC -2.0V; input rise and fall times: 5ns (max); input and output timing reference level: 1.5V; output load: -1TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-6518/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	$T_A = +25^oC$	-	6	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	$T_A = +25^oC$	-	10	pF

NOTE: 1. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Timing Waveforms

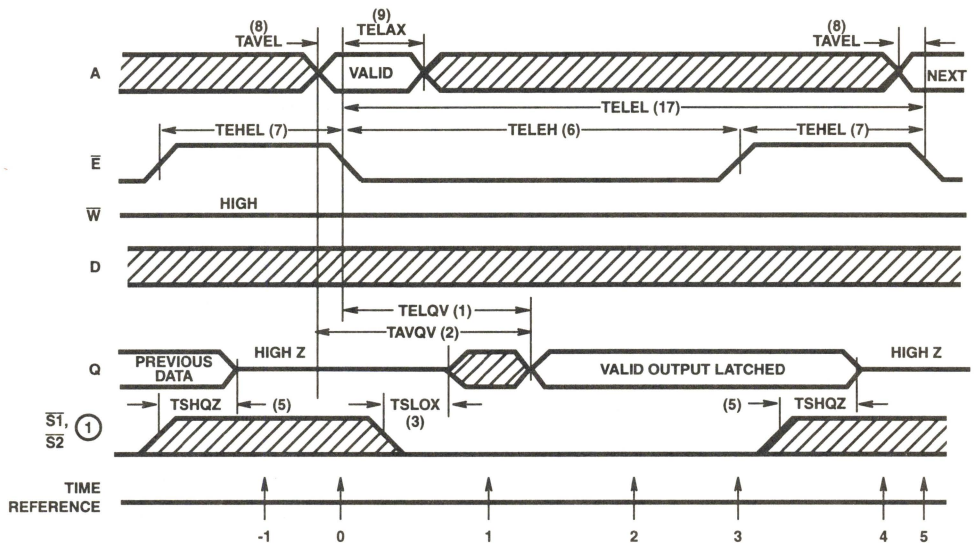


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS					OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	Z	Memory Disabled
0	↘	X	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	L	H	X	X	X	Output Enabled
2	L	L	H	X	X	V	Output Valid
3	↗	L	H	X	X	V	Output Latched
4	H	H	X	X	X	Z	Device Disabled, Prepare for Next Cycle (Same as -1)
5	↘	X	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

In the HM-6518/883 read cycle the address information is latched into the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. In order for the output to be read $\overline{S1}$, $\overline{S2}$ and $\overline{E}$ must be low, $\overline{W}$ must be high. When $\overline{E}$ goes high the output data is latched into an on chip register. Taking either or both $\overline{S1}$ or $\overline{S2}$ high, forces the output buffer to a high impedance state. The output data may be re-enabled at any time by taking $\overline{S1}$ and $\overline{S2}$ low. On the falling edge of $\overline{E}$ the data will be unlatched.

Timing Wavforms (Continued)

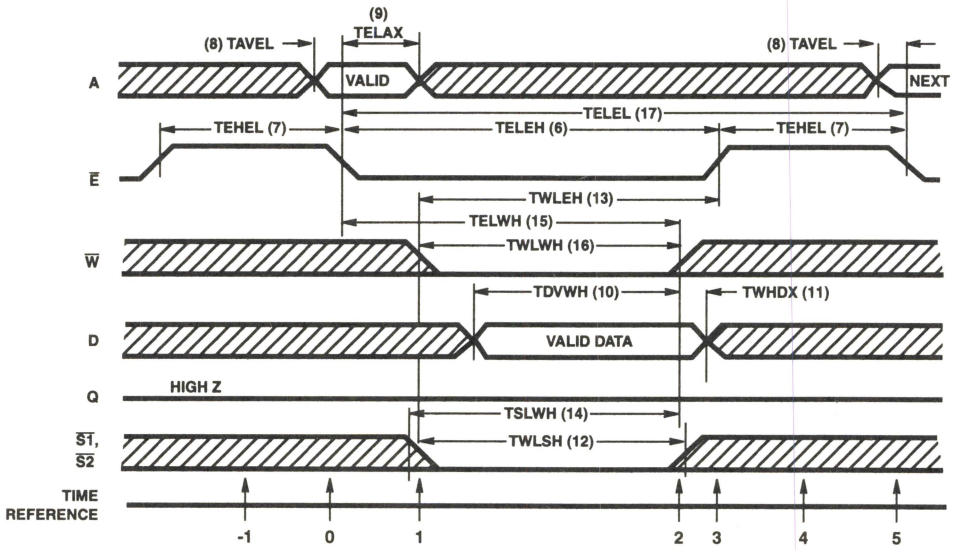


FIGURE 2. WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS					OUTPUTS	FUNCTION
	$\overline{E}$	S1	$\overline{W}$	A	D	Q	
-1	H	X	X	X	X	Z	Memory Disabled
0	↘	X	X	V	X	Z	Cycle Begins, Addresses are Latched
1	L	L	L	X	V	Z	Write Mode has Begun
2	L	↗	L	X	V	Z	Data is Written
3	↗	X	X	X	X	Z	Write Completed
4	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

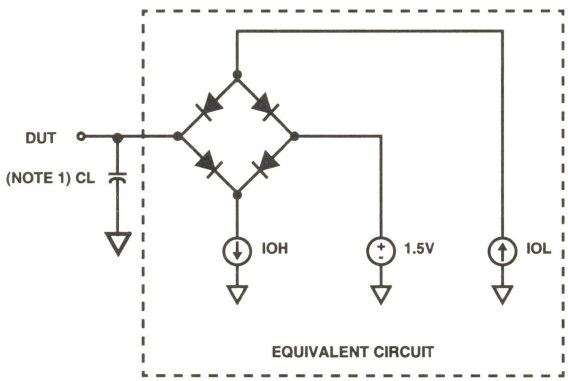
The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ and $\overline{S2}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$, $\overline{W}$, $\overline{S1}$ or $\overline{S2}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{E}$ low time (TELEH) is greater than the W pulse (TWLWH), plus an output enable time (TSLQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will ensure that the output buffers are not active.

Test Load Circuit

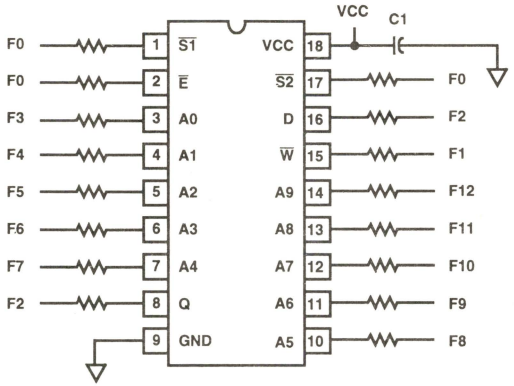


NOTE:

1. Test head capacitance includes stray and jig capacitance.

Burn-In Circuit

HM-6518/883 CERDIP



NOTES:

All resistors 47kΩ ±5%.

F0 = 100kHz ±10%.

F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2. . . . F12 = F11 ÷ 2.

VCC = 5.5V ±0.5V.

VIH = 4.5V ±10%.

VIL = -0.2V to +0.4V.

C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
130 x 150 x 19 ±1mils

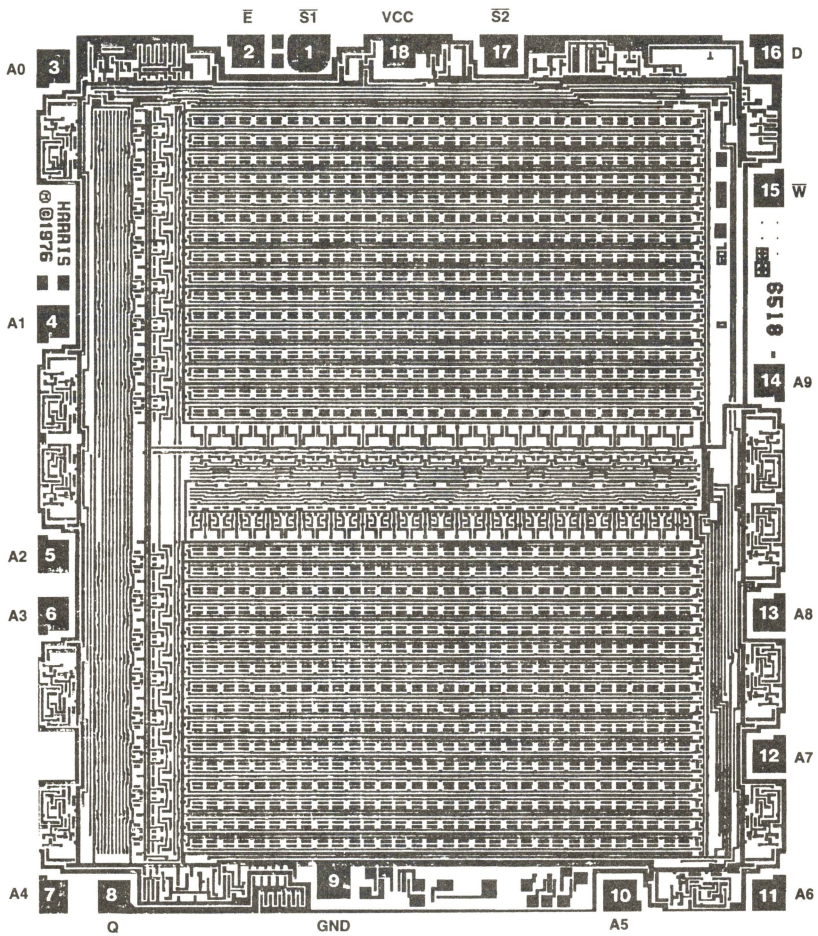
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
1.342 x 10^5 A/cm^2

Metallization Mask Layout

HM-6518/883



NOTE: Pin numbers correspond to DIP package only.

HARRIS SEMICONDUCTOR

HM-6551

March 1997

256 x 4 CMOS RAM

Features

- Low Power Standby . . . . . 50µW Max
- Low Power Operation . . . . . 20mW/MHz Max
- Fast Access Time. . . . . 220ns Max
- Data Retention . . . . . at 2.0V Min
- TTL Compatible Input/Output
- High Output Drive - 1 TTL Load
- Internal Latched Chip Select
- High Noise Immunity
- On-Chip Address Register
- Latched Outputs
- Three-State Output

Description

The HM-6551 is a 256 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

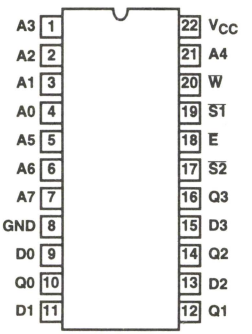
The HM-6551 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over-temperature.

Ordering Information

PACKAGE	TEMPERATURE RANGE	220ns	300ns	PKG. NO.
Plastic DIP	-40°C to +85°C	HM3-6551B-9	HM3-6551-9	E22.4
CERDIP	-40°C to +85°C	HM1-6551B-9	HM1-6551-9	F22.4

Pinout

HM-6551
(PDIP, CERDIP)
TOP VIEW



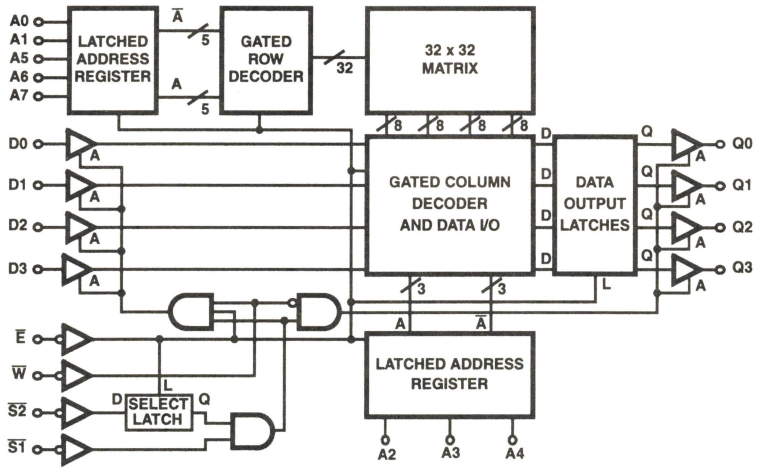
PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write E5able
$\overline{S}$	Chip Select
D	Data Input
Q	Data Output

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2989.1**

Functional Diagram



NOTES:

1. Select Latch: L Low → Q = D and Q latches on rising edge of L.
2. Address Latches And Gated Decoders: Latch on falling edge of $\overline{E}$ and gate on falling edge of $\overline{E}$.
3. All lines positive logic-active high.
4. Three-State Buffers: A high → output active.
5. Data Latches: L High → Q = D and Q latches on falling edge of L.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
HM-6551B-9, HM-6551-9 . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}	θ_{JC}
CERDIP Package	60°C/W	15°C/W
Plastic DIP Package	75°C/W	N/A

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package . . . . . +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 1930 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6551B-9, HM-6551-9)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	10	µA	IO = 0mA, VI = V_{CC} or GND, V_{CC} = 5.5V
ICCOP	Operating Supply Current (Note 1)	-	4	mA	$\overline{E}$ = 1MHz, IO = 0mA, V_{CC} = 5.5V, VI = V_{CC} or GND, $\overline{W}$ = GND
ICCDR	Data Retention Supply Current	-	10	µA	V_{CC} = 2.0V, IO = 0mA, VI = V_{CC} or GND, $\overline{E}$ = V_{CC}
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = V_{CC} or GND, V_{CC} = 5.5V
VIL	Input Low Voltage	-0.3	0.8	V	V_{CC} = 4.5V
VIH	Input High Voltage	V_{CC} -2.0	V_{CC} +0.3	V	V_{CC} = 5.5V
VOL	Output Low Voltage	-	0.4	V	IO = 1.6mA, V_{CC} = 4.5V
VOH	Output High Voltage	2.4	-	V	IO = -0.4mA, V_{CC} = 4.5V

Capacitance T_A = +25°C

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	6	pF	f = 1MHz, All measurements are referenced to device GND
CO	Output Capacitance (Note 2)	10	pF	

NOTES:

1. Typical derating 1.5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

AC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6551B-9, HM-6551-9)

SYMBOL	PARAMETER	LIMITS				UNITS	TEST CONDITIONS
		HM-6551B-9		HM-6551-9			
		MIN	MAX	MIN	MAX		
(1) TELQV	Chip Enable Access Time	-	220	-	300	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	220	-	300	ns	(Notes 1, 3, 4)
(3) TS1LQX	Chip Select 1 Output Enable Time	5	130	5	150	ns	(Notes 2, 3)
(4) TWLQZ	Write Enable Output Disable Time	-	130	-	150	ns	(Notes 2, 3)
(5) TS1HQZ	Chip Select 1 Output Disable Time	-	130	-	150	ns	(Notes 2, 3)
(6) TELEH	Chip Enable Pulse Negative Width	220	-	300	-	ns	(Notes 1, 3)
(7) TEHEL	Chip Enable Pulse Positive Width	100	-	100	-	ns	(Notes 1, 3)
(8) TAVEL	Address Setup Time	0	-	0	-	ns	(Notes 1, 3)
(9) TS2LEL	Chip Select 2 Output Disable Time	0	-	0	-	ns	(Notes 1, 3)
(10) TELAX	Address Hold Time	40	-	50	-	ns	(Notes 1, 3)
(11) TELS2X	Chip Select 2 Hold Time	40	-	50			(Notes 1, 3)
(12) TDVWH	Data Setup Time	100	-	150	-	ns	(Notes 1, 3)
(13) TWHDX	Data Hold Time	0	-	0	-	ns	(Notes 1, 3)
(14) TWLS1H	Chip Select 1 Write Pulse Setup Time	120	-	180	-	ns	(Notes 1, 3)
(15) TWLEH	Chip Enable Write Pulse Setup Time	120	-	180	-	ns	(Notes 1, 3)
(16) TS1LWH	Chip Select 1 Write Pulse Hold Time	120	-	180	-	ns	(Notes 1, 3)
(17) TELWH	Chip Enable Write Pulse Hold Time	120	-	180	-	ns	(Notes 1, 3)
(18) TWLWH	Write Enable Pulse Width	120	-	180	-	ns	(Notes 1, 3)
(19) TELEL	Read or Write Cycle Time	320	-	400	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0.8V to V_{CC} - 2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5V and 5.5V.
4. TAVQV = TELQV + TAVEL.

Timing Waveforms

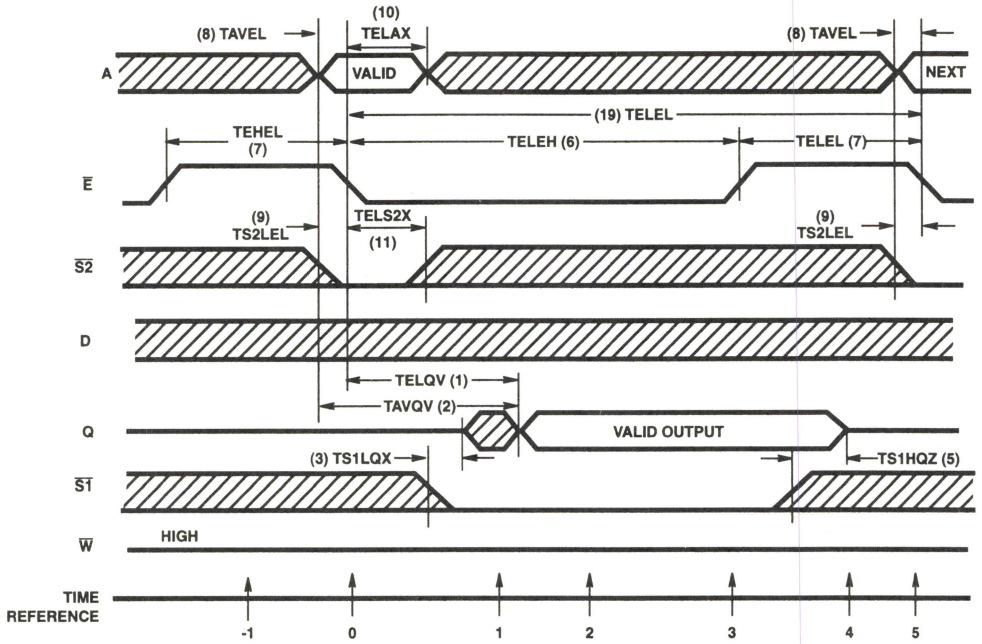


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS						OUTPUTS	FUNCTION
	Ē	S1	S2	W	A	D	Q	
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↘	X	L	H	V	X	Z	Addresses and S2 are Latched, Cycle Begins
1	L	L	X	H	X	X	X	Output Enabled but Undefined
2	L	L	X	H	X	X	V	Data Output Valid
3	↗	L	X	H	X	X	V	Outputs Latched, Valid Data, S2 Unlatches
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	L	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The HM-6551 Read Cycle is initiated by the falling edge of Ē. This signal latches the input address word and S2 into on chip registers, providing the minimum setup and hold times are met. After the required hold time, these inputs may change state without affecting device operation. S2 acts as a high order address and simplifies decoding. For the output to be read, Ē, S1 must be low and W must be high. S2 must have been latched low on the falling edge of Ē. The output data will be valid at access time (TELQV). The HM-6551 has output data latches that are controlled by Ē. On the rising edge of Ē the present data is latched and remains in that state until Ē falls. Also on the rising edge of Ē, S2 unlatches and controls the outputs along with S1. Either or both S1 or S2 may be used to force the output buffers into a high impedance state.

Timing Waveforms (Continued)

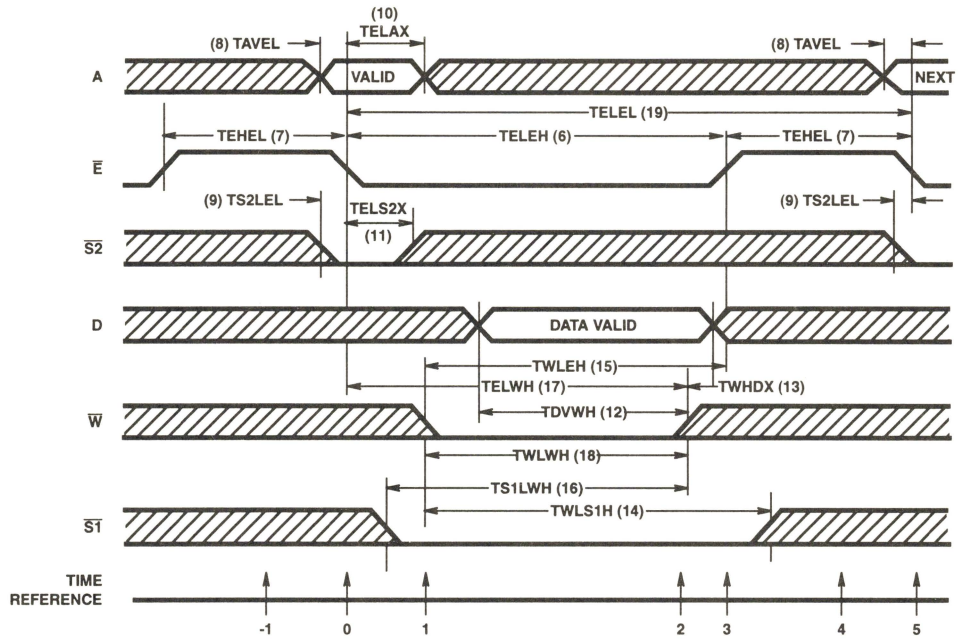


FIGURE 2. WRITE CYCLE

TRUTH TABLE

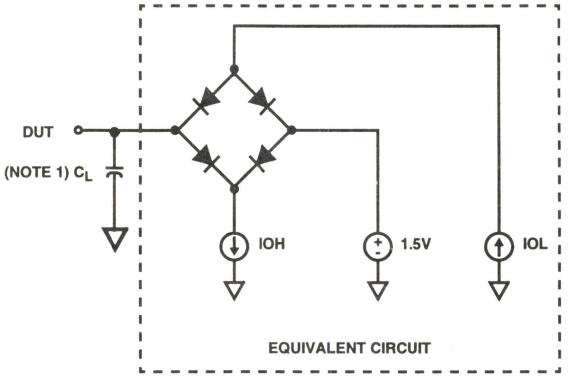
TIME REFERENCE	INPUTS						OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↘	X	L	X	V	X	Z	Cycle Begins, Addresses and $\overline{S2}$ are Latched
1	L	L	X	↘	X	X	Z	Write Period Begins
2	L	L	X	↗	X	V	Z	Data In is Written
3	↗	X	X	H	X	X	Z	Write is Completed
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	L	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses and $\overline{S2}$ into on chip registers. $\overline{S2}$ must be latched in the low state to enable the device. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ being low and $\overline{S2}$ being latched simultaneously. The $\overline{W}$ line may go low at any time during the cycle, providing that the write pulse setup times (TWLEH and TWLS1H) are met. The write portion of the cycle is terminated on the first rising edge of either $\overline{E}$, $\overline{W}$, or $\overline{S1}$.

If a series of consecutive write cycles are to be executed, the $\overline{W}$ line may be held low until all desired locations have been written. If this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$ or $\overline{S1}$. By positioning the write pulse at different times within the $\overline{E}$ and $\overline{S1}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{S1}$ low time (TS1LS1H) is greater than the $\overline{W}$ pulse plus an output enable time (TS1LQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The HM-6551 may be used on a common I/O bus structure by tying the input and output pins together. The multiplexing is accomplished internally by the $\overline{W}$ line. In the write cycle, when $\overline{W}$ goes low, the output buffers are forced to a high impedance state. One output disable time delay (TWLQZ) must be allowed before applying input data to the bus.

Test Load Circuit



NOTE:

1. Test head capacitance includes stray and jig capacitance.

HM-6551/883

March 1997

256 x 4 CMOS RAM

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Power Standby . . . . . 50μW Max**
- **Low Power Operation . . . . . 20mW/MHz Max**
- **Fast Access Time. . . . . 220ns Max**
- **Data Retention . . . . . at 2.0V Min**
- **TTL Compatible Input/Output**
- **High Output Drive - 1 TTL Load**
- **Internal Latched Chip Select**
- **High Noise Immunity**
- **On-Chip Address Register**
- **Latched Outputs**
- **Three-State Output**

Description

The HM-6551/883 is a 256 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation. On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

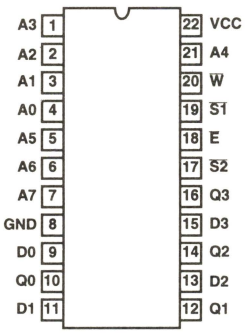
The HM-6551/883 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

PACKAGE	TEMPERATURE RANGE	220ns	300ns	PKG. NO.
CERDIP	-55°C to +125°C	HM-6551B/883	HM1-6551/883	F22.4

Pinout

HM-6551/883 (CERDIP)
TOP VIEW



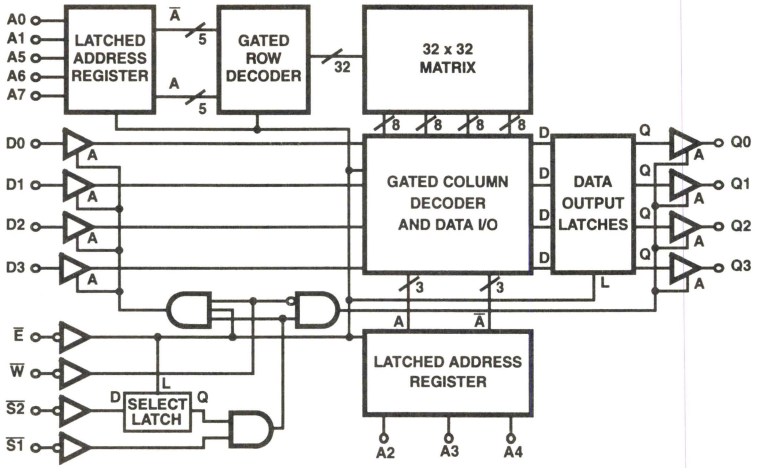
PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
D	Data Input
Q	Data Output

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2988.1**

Functional Diagram



NOTES:

1. Select Latch: L Low → Q = D and Q latches on rising edge of L.
2. Address Latches And Gated Decoders: Latch on falling edge of $\overline{E}$ and gate on falling edge of $\overline{E}$.
3. All lines positive logic-active high.
4. Three-State Buffers: A high → output active.
5. Data Latches: L High → Q = D and Q latches on falling edge of L.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	60°C/W	15°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 1930 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . VCC -2.0V to VCC
Input Rise and Fall Time . . . . . 40ns Max.

TABLE 1. HM-6551/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 1.6mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -0.4mA	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5 V, VO = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC IO = 0mA, VI = VCC or GND	1, 2, 3	$-55°C \le T_A \le +125°C$	-	10	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 2) $\overline{E}$ = 1MHz, IO = 0mA VI = VCC or GND	1, 2, 3	$-55°C \le T_A \le +125°C$	-	4	mA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA VI = VCC or GND	1, 2, 3	$-55°C \le T_A \le +125°C$	-	10	µA

NOTES:

1. All voltages referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.

TABLE 2. HM-6551/883 A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS				UNITS
					HM-6551B/883		HM-6551/883		
					MIN	MAX	MIN	MAX	
Chip Enable Access Time	(1) TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	220	-	300	ns
Address Access Time	(2) TAVQV	VCC = 4.5 and 5.5V, Note 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	220	-	300	ns
Chip Select 1 Output Enable Time	(3) TS1LQX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	5	-	5	-	ns
Write Enable Output Disable Time	(4) TWLQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	130	-	150	ns
Chip Select 1 Output Disable Time	(5) TS1HQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	130	-	150	ns
Chip Enable Pulse Negative Width	(6) TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	220	-	300	-	ns
Chip Enable Pulse Positive Width	(7) TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	100	-	ns
Address Setup Time	(8) TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Chip Select 2 Setup Time	(9) TS2LEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Address Hold Time	(10) TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	50	-	ns
Chip Select 2 Hold Time	(11) TELS2X	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	50	-	ns
Data Setup Time	(12) TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	150	-	ns
Data Hold Time	(13) TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Chip Select 1 Write Pulse Setup Time	(14) TWLS1H	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	180	-	ns
Chip Enable Write Pulse Setup Time	(15) TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	180	-	ns
Chip Select 1 Write Pulse Hold Time	(16) TS1LWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	180	-	ns
Chip Enable Write Pulse Hold Time	(17) TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	180	-	ns
Write Enable Pulse Width	(18) TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	180	-	ns
Read or Write Cycle Time	(19) TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	320	-	400	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-6551B/883 AND HM-6551/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	T_A = +25°C	-	10	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	T_A = +25°C	-	12	pF

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Timing Waveforms

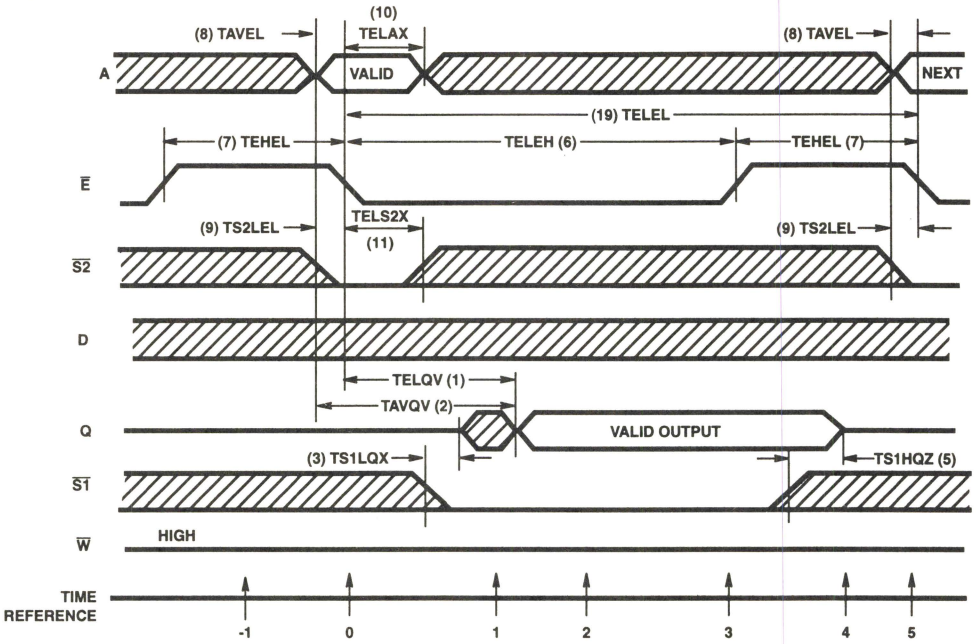


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS						OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↘	X	L	H	V	X	Z	Addresses and $\overline{S2}$ are Latched, Cycle Begins
1	L	L	X	H	X	X	X	Output Enabled but Undefined
2	L	L	X	H	X	X	V	Data Output Valid
3	↗	L	X	H	X	X	V	Outputs Latched, Valid Data, $\overline{S2}$ Unlatches
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	L	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The HM-6551/883 Read Cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word and $\overline{S2}$ into on-chip registers providing the minimum setup and hold times are met. After the required hold time, these inputs may change state without affecting device operation. $\overline{S2}$ acts as a high order address and simplifies decoding. For the output to be read, $\overline{E}$, $\overline{S1}$ must be low and $\overline{W}$ must be high. $\overline{S2}$ must have been latched low on the falling edge of $\overline{E}$. The output data will be valid at access time (TELQV). The HM-6551/883 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains in that state until $\overline{E}$ falls. Also on the rising edge of $\overline{E}$, $\overline{S2}$ unlatches and controls the outputs along with $\overline{S1}$. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Timing Waveforms (Continued)

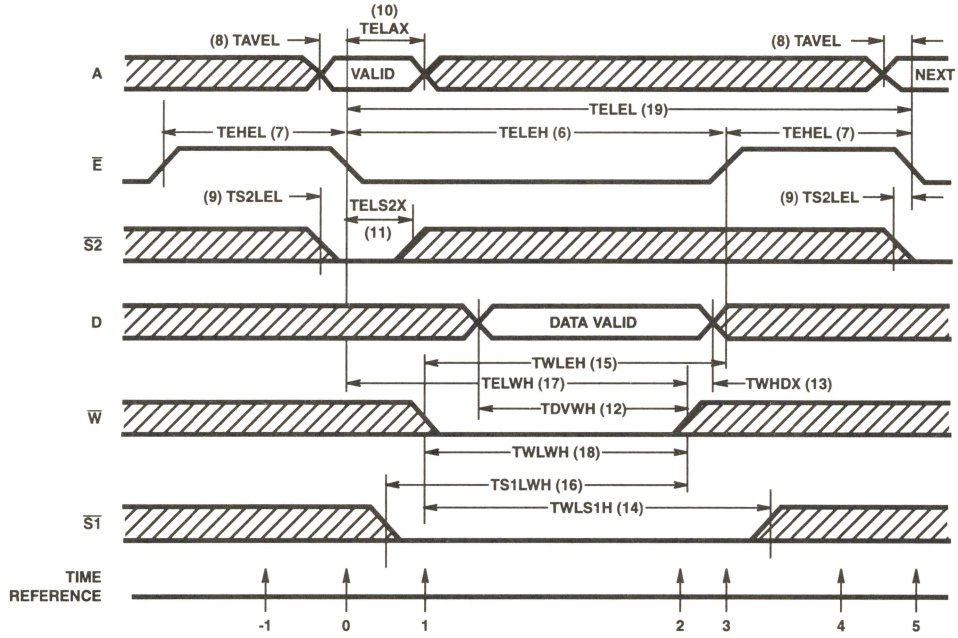


FIGURE 2. WRITE CYCLE

TRUTH TABLE

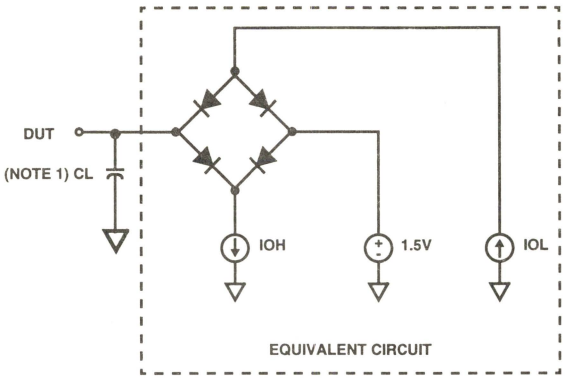
TIME REFERENCE	INPUTS						OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↘	X	L	X	V	X	Z	Cycle Begins, Addresses and $\overline{S2}$ are Latched
1	L	L	X	↘	X	X	Z	Write Period Begins
2	L	L	X	↗	X	V	Z	Data In is Written
3	↗	X	X	H	X	X	Z	Write is Completed
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	L	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses and $\overline{S2}$ into on-chip registers. $\overline{S2}$ must be latched in the low state to enable the device. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ being low and $\overline{S2}$ being latched simultaneously. The $\overline{W}$ line may go low at any time during the cycle providing that the write pulse setup times (TWLEH and TWLS1H) are met. The write portion of the cycle is terminated on the first rising edge of either $\overline{E}$, $\overline{W}$, or $\overline{S1}$.

If a series of consecutive write cycles are to be executed, the $\overline{W}$ line may be held low until all desired locations have been written. If this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$ or $\overline{S1}$. By positioning the write pulse at different times within the $\overline{E}$ and $\overline{S1}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{S1}$ low time (TS1LS1H) is greater than the $\overline{W}$ pulse, plus an output enable time (TS1LQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The HM-6551/883 may be used on a common I/O bus structure by tying the input and output pins together. The multiplexing is accomplished internally by the $\overline{W}$ line. In the write cycle, when $\overline{W}$ goes low, the output buffers are forced to a high impedance state. One output disable time delay (TWLQZ) must be allowed before applying input data to the bus.

Test Load Circuit

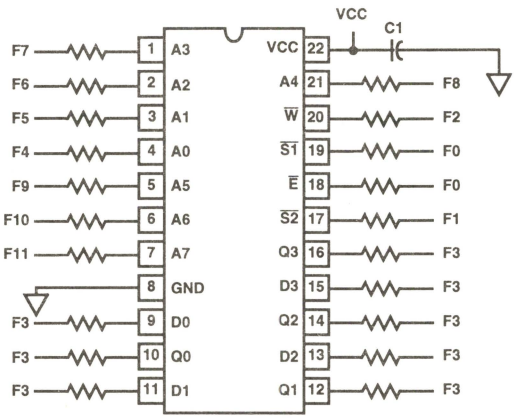


NOTE:

1. Test head capacitance includes stray and jig capacitance.

Burn-In Circuit

HM-6551/883
CERDIP



NOTES:
All resistors 47kΩ ±5%.
F0 = 100kHz ±10%.
F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F12 = F11 ÷ 2.
VCC = 5.5V ±0.5V.
VIH = 4.5V ±10%.
VIL = -0.2V to +0.4V.
C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
132 x 160 x 19 ±1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

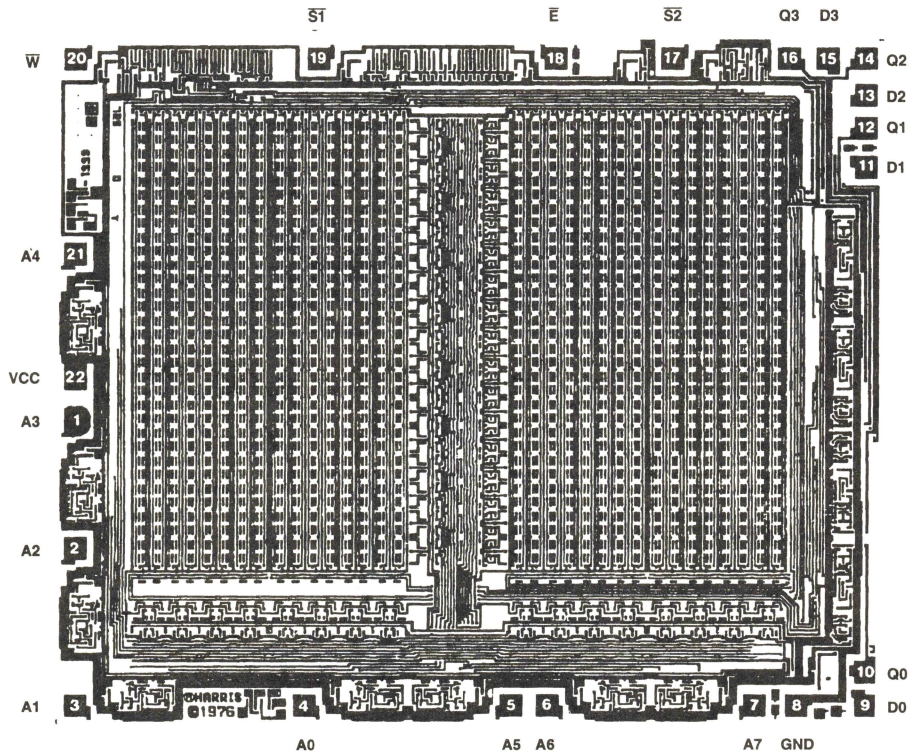
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
1.337×10^5 A/cm^2

LEAD TEMPERATURE (10s soldering):
≤300°C

Metallization Mask Layout

HM-6551/883



NOTE: Pin numbers correspond to DIP Package only.

HARRIS SEMICONDUCTOR

HM-6561

March 1997

256 x 4 CMOS RAM

Features

- Low Power Standby . . . . . 50µW Max
- Low Power Operation . . . . . 20mW/MHz Max
- Fast Access Time. . . . . 200ns Max
- Data Retention . . . . . at 2.0V Min
- TTL Compatible Input/Output
- High Output Drive - 1 TTL Load
- On-Chip Address Registers
- Common Data In/Out
- Three-State Output
- Easy Microprocessor Interfacing

Description

The HM-6561 is a 256 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On-chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

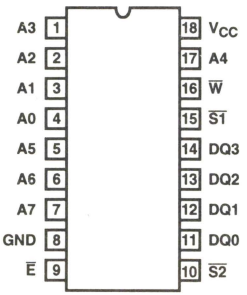
The HM-6561 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

PACKAGE	TEMPERATURE RANGE	220ns	300ns	PKG. NO.
CERDIP	-40°C to +85°C	HM1-6561B-9	HM1-6561-9	F18.3

Pinout

HM-6561
(CERDIP)
TOP VIEW



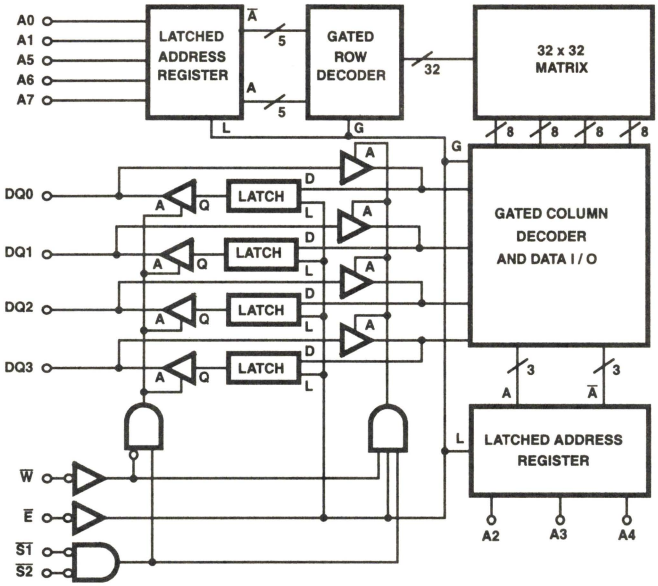
PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
DQ	Data In/Out

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2991.1**

Functional Diagram



NOTES:

1. All lines positive logic-active high.
2. Three-state Buffers: A high → output active.
3. Data Latches: L high → Q = D and Q latches on falling edge of L.
4. Address Latches and Gated Decoders: Latch on falling edge of $\overline{E}$ and gate on falling edge of $\overline{E}$.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage. . . . . GND -0.3V to V_{CC} +0.3V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	74°C/W	18°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 1944 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V

Operating Temperature Range
HM-6561B-9, HM6561-9 . . . . . -40°C to +85°C

DC Electrical Specifications V_{CC} = 5V ± 10%; T_A = -40°C to +85°C (HM-6561B-9, HM-6561-9)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	10	µA	IO = 0mA, VI = V_{CC} or GND, V_{CC} = 5.5V
ICCOP	Operating Supply Current (Note 1)	-	4	mA	$\overline{E}$ = 1MHz, IO = 0mA, V_{CC} = 5.5V, VI = V_{CC} or GND, $\overline{W}$ = GND
ICCDR	Data Retention Supply Current	-	10	µA	V_{CC} = 2.0V, IO = 0mA, VI = V_{CC} or GND, $\overline{E}$ = V_{CC}
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = V_{CC} or GND, V_{CC} = 5.5V
VIL	Input Low Voltage	-0.3	0.8	V	V_{CC} = 4.5V
VIH	Input High Voltage	V_{CC} -2.0	V_{CC} +0.3	V	V_{CC} = 5.5V
VOL	Output Low Voltage	-	0.4	V	IO = 1.6mA, V_{CC} = 4.5V
VOH	Output High Voltage	2.4	-	V	IO = -0.4mA, V_{CC} = 5.5V

Capacitance T_A = +25°C

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	6	pF	f = 1MHz, All measurements are referenced to device GND
CIO	Input/Output Capacitance (Note 2)	10	pF	

NOTES:

1. Typical derating 1.5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

AC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6561B-9, HM-6561-9)

SYMBOL	PARAMETER	LIMITS				UNITS	TEST CONDITIONS
		HM-6561B-9		HM-6561-9			
		MIN	MAX	MIN	MAX		
(1) TELQV	Chip Enable Access Time	-	220	-	300	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	220	-	300	ns	(Notes 1, 3, 4)
(3) TSLQX	Chip Select Output Enable Time	5	120	5	150	ns	(Notes 2, 3)
(4) TSHQZ	Chip Select Output Disable Time	-	120	-	150	ns	(Notes 2, 3)
(5) TELEH	Chip Enable Pulse Negative Width	220	-	300	-	ns	(Notes 1, 3)
(6) TEHEL	Chip Enable Pulse Positive Width	100	-	100	-	ns	(Notes 1, 3)
(7) TAVEL	Address Setup Time	0	-	0	-	ns	(Notes 1, 3)
(8) TELAX	Address Hold Time	40	-	50	-	ns	(Notes 1, 3)
(9) TDVWH	Data Setup Time	100	-	150	-	ns	(Notes 1, 3)
(10) TWHDX	Data Hold Time	0	-	0	-	ns	(Notes 1, 3)
(11) TWLDV	Write Data Delay Time	20	-	30	-	ns	(Notes 1, 3)
(12) TWLSH	Chip Select Write Pulse Setup Time	120	-	180	-	ns	(Notes 1, 3)
(13) TWLEH	Chip Enable Write Pulse Setup Time	120	-	180	-	ns	(Notes 1, 3)
(14) TSLWH	Chip Select Write Pulse Hold Time	120	-	180	-	ns	(Notes 1, 3)
(15) TELWH	Chip Enable Write Pulse Hold Time	120	-	180	-	ns	(Notes 1, 3)
(16) TWLWH	Write Enable Pulse Width	120	-	180	-	ns	(Notes 1, 3)
(17) TELEL	Read or Write Cycle Time	320	-	400	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5V and 5.5V.
4. TAVQV = TELQV + TAVEL.

Timing Waveforms

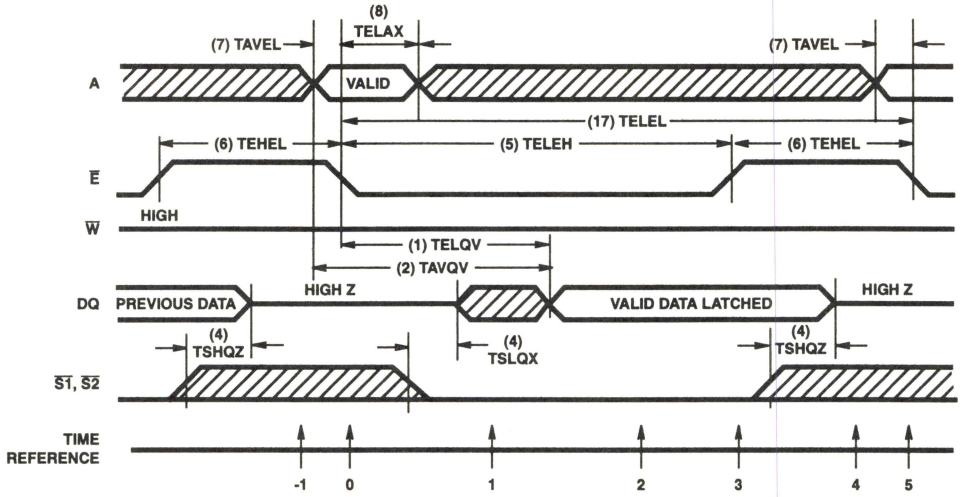


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUT	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{W}$	A	DQ	
-1	H	H	X	X	Z	Memory Disabled
0	↘	X	H	V	Z	Cycle Begins, Addresses are Latched
1	L	L	H	X	X	Output Enabled
2	L	L	H	X	V	Output Valid
3	↗	L	H	X	V	Output Latched
4	H	H	X	X	Z	Device Disabled, Prepare for Next Cycle (Same as -1)
5	↘	X	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE:

1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The HM-6561 Read Cycle is initiated on the falling edge of $\overline{E}$. This signal latches the input address word into on-chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data $\overline{E}$, $\overline{S1}$ and $\overline{S2}$ must be low and $\overline{W}$ must be high. The output data will be valid at access time (TELQV).

The HM-6561 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains latched until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Timing Waveforms (Continued)

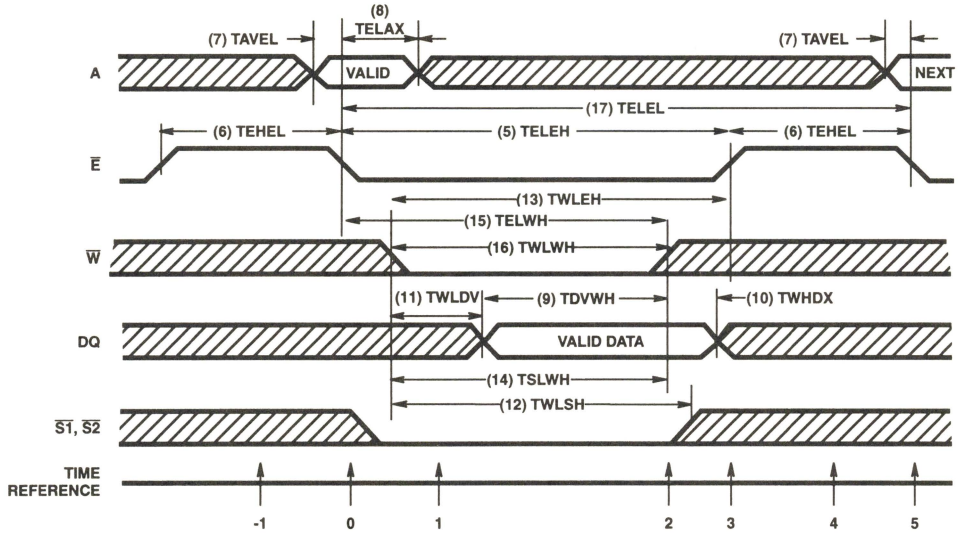


FIGURE 2. WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS					FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{W}$	A	DQ	
-1	H	H	X	X	X	Memory Disabled
0	↓	X	X	V	X	Cycle Begins, Addresses are Latched
1	L	L	L	X	X	Write Period Begins
2	L	L	↑	X	V	Data In is Written
3	↑	X	H	X	X	Write is Completed
4	H	H	X	X	X	Prepare for Next Cycle (Same as -1)
5	↓	X	X	V	X	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE:

1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The write cycle begins with the $\overline{E}$ falling edge latching the address. The write portion of the cycle is defined by $\overline{E}$, $\overline{S1}$, $\overline{S2}$ and $\overline{W}$ all being low simultaneously. The write portion of the cycle is terminated by the first rising edge of any control line, $\overline{E}$, $\overline{S1}$, $\overline{S2}$ or $\overline{W}$. The data setup and data hold times (TDVWH and TWHDX) must be referenced to the terminating signal. For example, if $\overline{S2}$ rises first, data setup and hold times become TDVS2H and TS2HDX; and are numerically equal to TDVWH and TWHDX.

Data input/output multiplexing is controlled by $\overline{W}$. Care must be taken to avoid data bus conflicts, where the RAM outputs become enabled when another device is driving the data inputs. The following two examples illustrate the timing required to avoid bus conflicts.

Case 1: Both $\overline{S1}$ and $\overline{S2}$ Fall Before $\overline{W}$ Falls.

If both selects fall before $\overline{W}$ falls, the RAM outputs will become enabled. $\overline{W}$ is used to disable the outputs, so a disable time (TWLQZ = TWLDV) must pass before any other device can begin to drive the data inputs. This method of operation requires a wider write pulse, because TWLDV + TDVWH is greater than TWLWH. In this case TWLSL + TSHWH are meaningless and can be ignored.

Case 2: $\overline{W}$ Falls Before Both $\overline{S1}$ and $\overline{S2}$ Fall.

If one or both selects are high until W falls, the outputs are guaranteed not to enable at the beginning of the cycle. This eliminates the concern for data bus conflicts and simplifies data input timing. Data input may be applied as early as convenient, and TWLDV is ignored. Since $\overline{W}$ is not used to

disable the outputs it can be shorter than in Case 1; TWLWH is the minimum write pulse. At the end of the write period, if $\overline{W}$ rises before either select, the outputs will enable, reading data just written. They will not disable until either select goes high (TSHQZ).

	IF	OBSERVE	IGNORE
CASE 1	Both $\overline{S1}$ and $\overline{S2}$ = Low Before $\overline{W}$ = Low	TWLQZ TWLDV TDVWH	TWLWH
CASE 2	$\overline{W}$ = Low Before Both $\overline{S1}$ and $\overline{S2}$ = Low	TWLWH TDVWH	TWLQZ TWLDV

If a series of consecutive write cycles are to be performed, W may remain low until all desired locations are written. This is an extension of Case 2.

Read-Modify-Write cycles and Read-Write-Read cycles can be performed (extension of Case 1). In fact data may be modified as many times as desired with $\overline{E}$ remaining low.

HM-6561/883

March 1997

256 x 4 CMOS RAM

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Power Standby . . . . . 50μW Max**
- **Low Power Operation . . . . . 20mW/MHz Max**
- **Fast Access Time . . . . . 200ns Max**
- **Data Retention . . . . . at 2.0V Min**
- **TTL Compatible Input/Output**
- **High Output Drive - 1 TTL Load**
- **On-Chip Address Registers**
- **Common Data In/Out**
- **Three-State Output**
- **Easy Microprocessor Interfacing**

Description

The HM-6561/883 is a 256 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On-chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

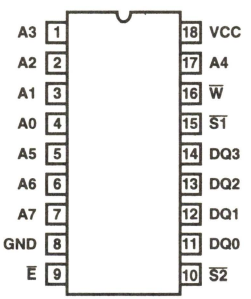
The HM-6561/883 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

PACKAGE	TEMPERATURE RANGE	220ns	300ns	PKG. NO.
CERDIP	-55°C to +125°C	HM1-6561B/883	HM1-6561/883	F18.3

Pinout

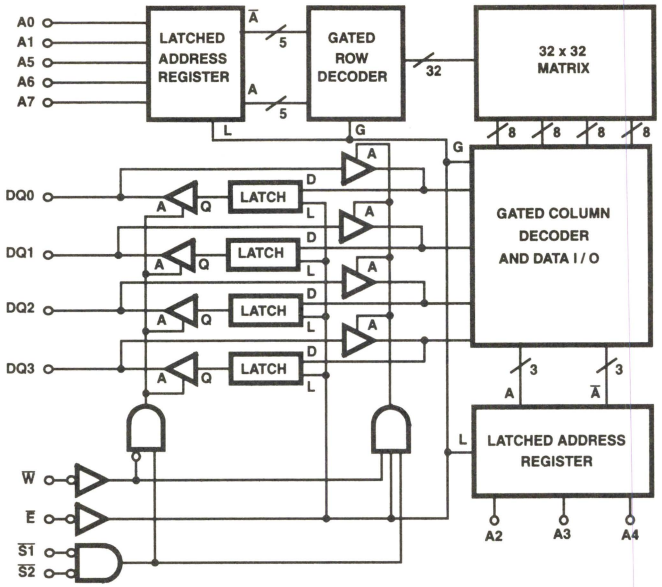
HM-6561/883 (CERDIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
DQ	Data In/Out

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Functional Diagram



NOTES:

1. All lines positive logic-active high.
2. Three-state Buffers: A high → output active.
3. Data Latches: L high → Q = D and Q latches on falling edge of L.
4. Address Latches and Gated Decoders: Latch on falling edge of $\overline{E}$ and gate on falling edge of $\overline{E}$.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage. . . . . GND -0.3V to VCC +0.3V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	74°C/W	18°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 1944 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . VCC - 2.0V to VCC
Input Rise and Fall Time . . . . . 40ns Max

TABLE 1. HM-6561/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V, IOL = 1.6mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V, IOH = -0.4mA	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Input/Output Leakage Current	IIOZ	VCC = 5.5V, VIO = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC, IO = 0mA,	1, 2, 3	$-55°C \le T_A \le +125°C$	-	10	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 2), $\overline{E}$ = 1MHz, $\overline{W}$ = GND, VI = VCC or GND	1, 2, 3	$-55°C \le T_A \le +125°C$	-	4	mA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, VI = VCC or GND	1, 2, 3	$-55°C \le T_A \le +125°C$	-	10	µA

NOTES:

1. All voltages referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.

TABLE 2. HM-6561/883 A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS				UNITS
					HM-6561B/883		HM-6561/883		
					MIN	MAX	MIN	MAX	
Chip Enable Access Time	(1) TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	220	-	300	ns
Address Access Time	(2) TAVQV	VCC = 4.5 and 5.5V, (Note 3)	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	220	-	300	ns
Chip Select Output Enable Time	(3) TSLQX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	5	-	5	-	ns
Chip Select Output Disable Time	(4) TSHQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	150	ns
Chip Enable Pulse Negative Width	(5) TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	220	-	300	-	ns
Chip Enable Pulse Positive Width	(6) TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	100	-	ns
Address Setup Time	(7) TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Address Hold Time	(8) TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	50	-	ns
Data Setup Time	(9) TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	150	-	ns
Data Hold Time	(10) TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Write Data Delay Time	(11) TWLDV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	30	-	
Chip Select Write Pulse Setup Time	(12) TWLSH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	180	-	ns
Chip Enable Write Pulse Setup Time	(13) TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	180	-	ns
Chip Select Write Pulse Hold Time	(14) TSLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	180	-	ns
Chip Enable Write Pulse Hold Time	(15) TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	180	-	ns
Write Enable Pulse Width	(16) TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	180	-	ns
Read or Write Cycle Time	(17) TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	320	-	400	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-6561/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

SYMBOL	PARAMETER	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
CI	Input Capacitance	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	T_A = +25°C	-	8	pF
CO	Output Capacitance	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	T_A = +25°C	-	10	pF

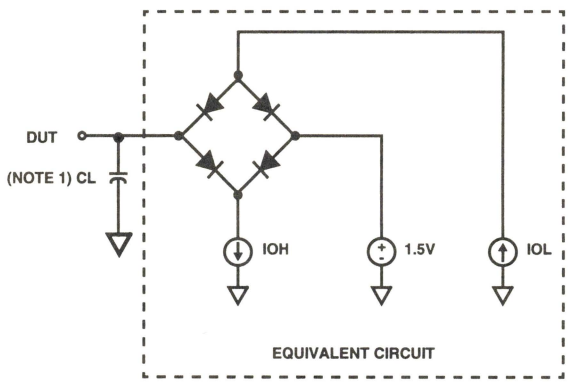
NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Test Load Circuit



NOTE:

1. Test head capacitance includes stray and jig capacitance.

Timing Waveforms

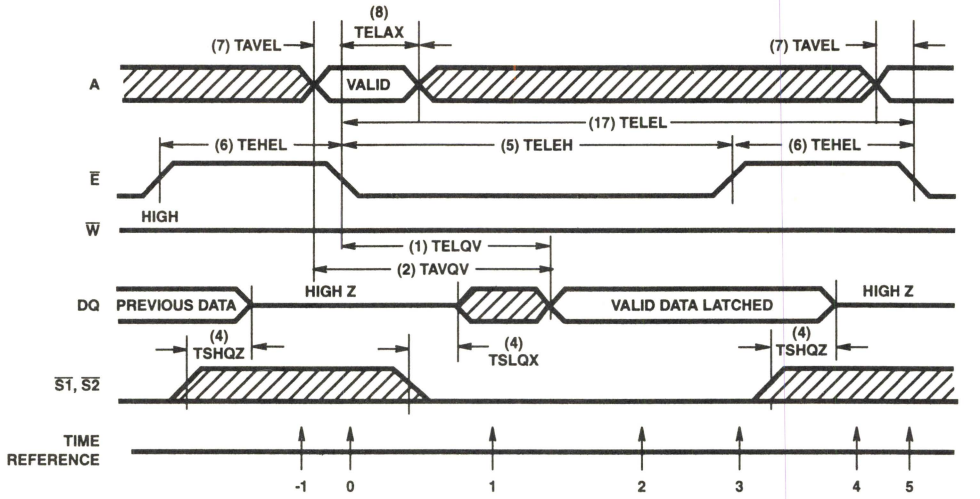


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUT	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{W}$	A	DQ	
-1	H	H	X	X	Z	Memory Disabled
0	↘	X	H	V	Z	Cycle Begins, Addresses are Latched
1	L	L	H	X	X	Output Enabled
2	L	L	H	X	V	Output Valid
3	↗	L	H	X	V	Output Latched
4	H	H	X	X	Z	Device Disabled, Prepare for Next Cycle (Same as -1)
5	↘	X	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The HM-6561/883 Read Cycle is initiated on the falling edge of $\overline{E}$. This signal latches the input address word into on-chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data $\overline{E}$, $\overline{S1}$ and $\overline{S2}$ must be low and $\overline{W}$ must be high. The output data will be valid at access time (TELQV).

The HM-6561/883 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains latched until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Timing Waveforms (Continued)

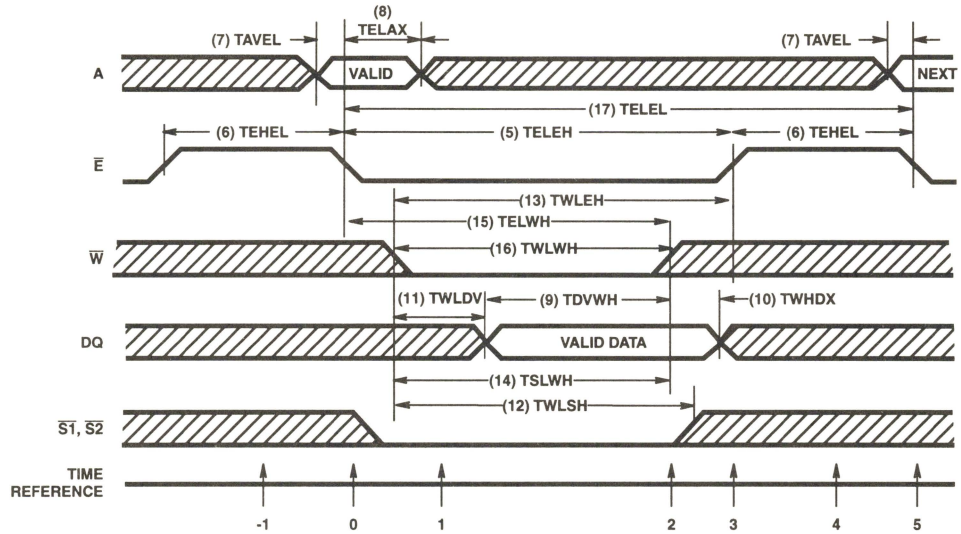


FIGURE 2. WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS					FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{W}$	A	DQ	
-1	H	H	X	X	X	Memory Disabled
0	↓	X	X	V	X	Cycle Begins, Addresses are Latched
1	L	L	L	X	X	Write Period Begins
2	L	L	↑	X	V	Data In is Written
3	↑	X	H	X	X	Write is Completed
4	H	H	X	X	X	Prepare for Next Cycle (Same as -1)
5	↓	X	X	V	X	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The write cycle begins with the $\overline{E}$ falling edge latching the address. The write portion of the cycle is defined by $\overline{E}$, $\overline{S1}$, $\overline{S2}$ and $\overline{W}$ all being low simultaneously. The write portion of the cycle is terminated by the first rising edge of any control line, $\overline{E}$, $\overline{S1}$, $\overline{S2}$ or $\overline{W}$. The data setup and data hold times (TDVWH and TWHDX) must be referenced to the terminating signal. For example, if $\overline{S2}$ rises first, data setup and hold times become TDVS2H and TS2HDX; and are numerically equal to TDVWH and TWHDX.

Data input/output multiplexing is controlled by $\overline{W}$. Care must be taken to avoid data bus conflicts, where the RAM outputs become enabled when another device is driving the data inputs. The following two examples illustrate the timing required to avoid bus conflicts.

Case 1: Both $\overline{S1}$ and $\overline{S2}$ Fall Before $\overline{W}$ Falls.

If both selects fall before $\overline{W}$ falls, the RAM outputs will become enabled. $\overline{W}$ is used to disable the outputs, so a disable time (TWLQZ = TWLDV) must pass before any other device can begin to drive the data inputs. This method of operation requires a wider write pulse, because TWLDV + TDVWH is greater than TWLWH. In this case TWLSL + TSHWH are meaningless and can be ignored.

Case 2: $\overline{W}$ Falls Before Both $\overline{S1}$ and $\overline{S2}$ Fall.

If one or both selects are high until $\overline{W}$ falls, the outputs are guaranteed not to enable at the beginning of the cycle. This eliminates the concern for data bus conflicts and simplifies data input timing. Data input may be applied as early as convenient, and TWLDV is ignored. Since $\overline{W}$ is not used to disable the outputs it can be shorter than in Case 1; TWLWH

is the minimum write pulse. At the end of the write period, if $\overline{W}$ rises before either select the outputs will enable reading data just written. They will not disable until either select goes high (TSHQZ).

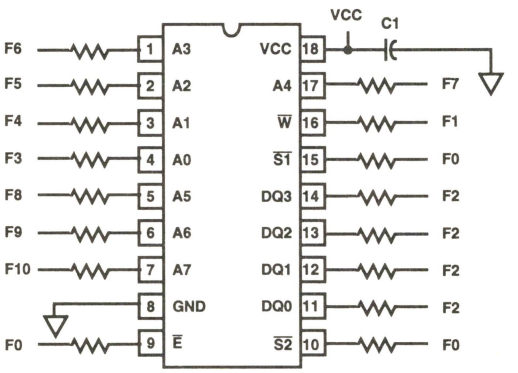
	IF	OBSERVE	IGNORE
CASE 1	Both $\overline{S1}$ and $\overline{S2}$ = Low Before $\overline{W}$ = Low	TWLQZ TWLDV TDVWH	TWLWH
CASE 2	$\overline{W}$ = Low Before Both $\overline{S1}$ and $\overline{S2}$ = Low	TWLWH TDVWH	TWLQZ TWLDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may remain low until all desired locations are written. This is an extension of Case 2.

Read-Modify-Write cycles and Read-Write-Read cycles can be performed (extension of Case 1). In fact data may be modified as many times as desired with $\overline{E}$ remaining low.

Burn-In Circuit

HM-6561/883
CERDIP



NOTES:
All resistors 47kΩ ±5%.
F0 = 100kHz ±10%.
F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F12 = F11 ÷ 2.
VCC = 5.5V ±0.5V.
VIH = 4.5V ±10%.
VIL = -0.2V to +0.4V.
C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
132 x 160 x 19 ±1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

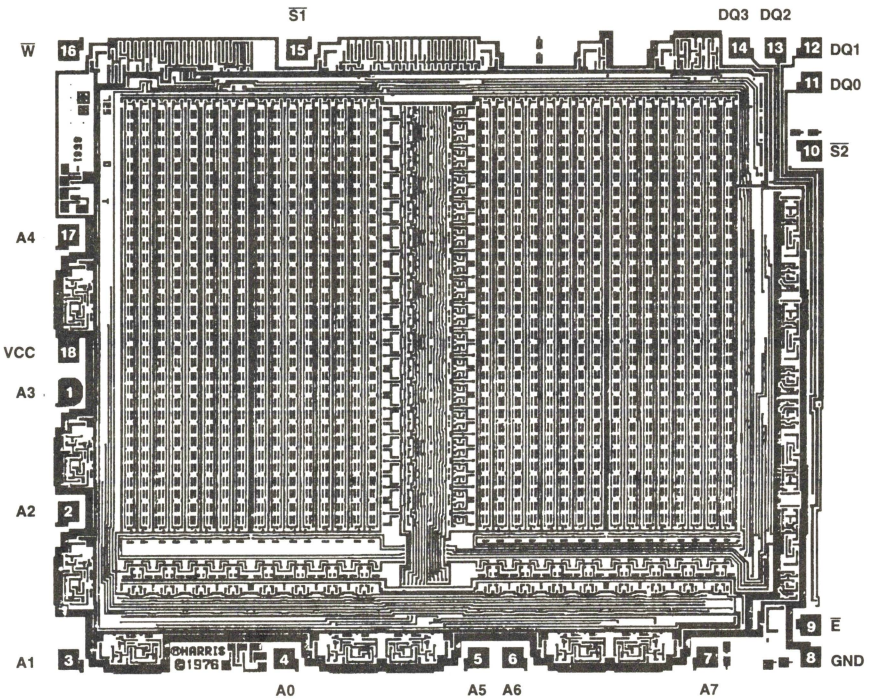
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
1.337×10^5 A/cm^2

LEAD TEMPERATURE (10s soldering):
$\leq 300^oC$

Metallization Mask Layout

HM-6561/883



HARRIS SEMICONDUCTOR

HM-6504

March 1997

4096 x 1 CMOS RAM

Features

- Low Power Standby . . . . . 125µW Max
- Low Power Operation . . . . . 35mW/MHz Max
- Data Retention . . . . . at 2.0V Min
- TTL Compatible Input/Output
- Three-State Output
- Standard JEDEC Pinout
- Fast Access Time. . . . . 120/200ns Max
- 18 Lead Package for High Density
- On-Chip Address Register
- Gated Inputs - No Pull Up or Pull Down Resistors Required

Description

The HM-6504 is a 4096 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays.

Gated inputs allow lower operating current and also eliminate the need for pull up or pull down resistors. The HM-6504 is a fully static RAM and may be maintained in any state for an indefinite period of time.

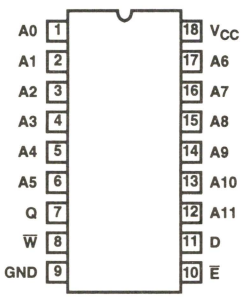
Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

120ns	200ns	300ns	TEMP. RANGE	PACKAGE	PKG. NO.
-	HM3-6504B-9	HM3-6504-9	-40°C to +85°C	PDIP	E18.3
HM1-6504S-9	HM1-6504B-9	HM1-6504-9	-40°C to +85°C	CERDIP	F18.3
24501BVA	-	-	-	JAN #	F18.3
810240IVA	8102403VA	8102405VA	-	SMD #	F18.3
-	-	HM4-6504-9	-40°C to+85°C	CLCC	J18.B

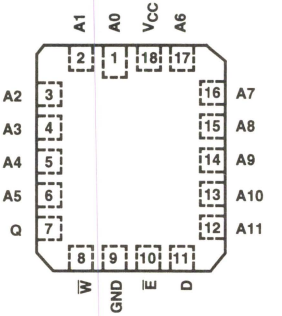
Pinouts

HM-6504 (PDIP, CERDIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

HM-6504 (CLCC)
TOP VIEW

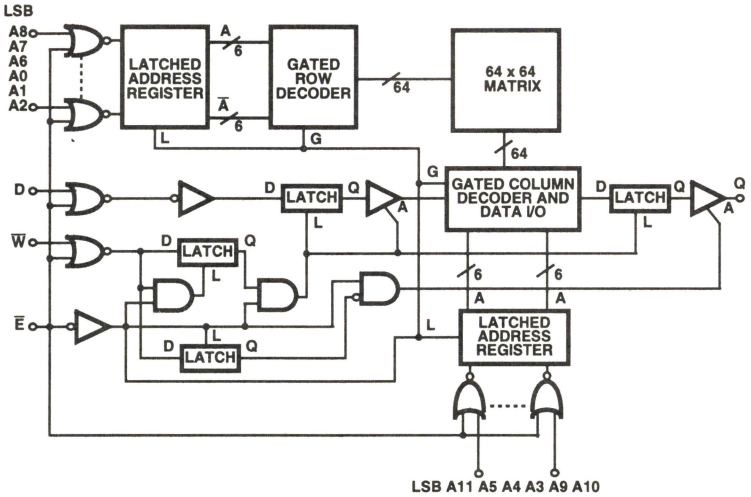


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2994.1**

Functional Diagram



NOTES:

1. All lines active high-positive logic.
2. Three-state Buffers: A high → output active.
3. Control and Data Latches: L low → Q = D and Q latches on rising edge of L.
4. Address Latches: Latch on falling edge of E.
5. Gated Decoders: Gate on rising edge of G.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package	75°C/W	15°C/W
PDIP Package	75°C/W	N/A
CLCC Package	90°C/W	33°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package . . . . . +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 6910 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V

Operating Temperature Range
HM-6504S-9, HM-6504B-9, HM-6504-9 . . . . . -40°C to +85°C
HM-6504B-8, HM-6504-8 . . . . . -55°C to +125°C

DC Electrical Specifications

V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6504B-9, HM-6504-9)
T_A = -55°C to +125°C (HM-6504B-8, HM-6504-8)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	HM-6504-9	-	25	µA	IO = 0mA, $\overline{E}$ = V_{CC} -0.3V, V_{CC} = 5.5V
		HM-6504-8	-	50	µA	
ICCOP	Operating Supply Current (Note 1)		-	7	mA	$\overline{E}$ = 1MHz, IO = 0mA, VI = GND, V_{CC} = 5.5V
ICCDR	Data Retention Supply Current	HM-6504-9	-	15	µA	IO = 0mA, V_{CC} = 2.0V, $\overline{E}$ = V_{CC}
		HM-6504-8	-	25	µA	
VCCDR	Data Retention Supply Voltage		2.0	-	V	
II	Input Leakage Current		-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IOZ	Output Leakage Current		-1.0	+1.0	µA	VO = V_{CC} or GND, V_{CC} = 5.5V
VIL	Input Low Voltage		-0.3	0.8	V	V_{CC} = 4.5V
VIH	Input High Voltage		V_{CC} -2.0	V_{CC} +0.3	V	V_{CC} = 5.5V
VOL	Output Low Voltage		-	0.4	V	IO = 2.0mA, V_{CC} = 4.5V
VOH1	Output High Voltage		2.4	-	V	IO = -1.0mA, V_{CC} = 4.5V
VOH2	Output High Voltage (Note 2)		V_{CC} -0.4	-	V	IO = -100µA, V_{CC} = 4.5V

Capacitance

T_A = +25°C

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	f = 1MHz, All measurements are referenced to device GND
CO	Output Capacitance (Note 2)	10	pF	

NOTES:

1. Typical derating 5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

AC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6504S-9, HM-6504B-9, HM-6504-9)
T_A = -55°C to +125°C (HM-6504B-8, HM-6504-8)

SYMBOL	PARAMETER	HM-6504S		HM-6504B		HM-6504		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
(1) TELQV	Chip Enable Access Time	-	120	-	200	-	300	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	120	-	220	-	320	ns	(Notes 1, 3, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	5	-	5	-	ns	(Notes 2, 3)
(4) TEHQZ	Chip Enable Output Disable Time	-	50	-	80	-	100	ns	(Notes 2, 3)
(5) TELEH	Chip Enable Pulse Negative Width	120	-	200	-	300	-	ns	(Notes 1, 3)
(6) TEHEL	Chip Enable Pulse Positive Width	50	-	90	-	120	-	ns	(Notes 1, 3)
(7) TAVEL	Address Setup Time	0	-	20	-	20	-	ns	(Notes 1, 3)
(8) TELAX	Address Hold Time	40	-	50	-	50	-	ns	(Notes 1, 3)
(9) TWLWH	Write Enable Pulse Width	20	-	60	-	80	-	ns	(Notes 1, 3)
(10) TWLEH	Write Enable Pulse Setup Time	70	-	150	-	200	-	ns	(Notes 1, 3)
(11) TWLEL	Early Write Pulse Setup Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(12) TWHEL	Write Enable Read Mode Setup Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(13) TELWH	Early Write Pulse Hold Time	40	-	60	-	80	-	ns	(Notes 1, 3)
(14) TDVWL	Data Setup Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(15) TDVEL	Early Write Data Setup Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(16) TWLDX	Data Hold Time	25	-	60	-	80	-	ns	(Notes 1, 3)
(17) TELDX	Early Write Data Hold Time	25	-	60	-	80	-	ns	(Notes 1, 3)
(18) TELEL	Read or Write Cycle Time	170	-	290	-	420	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0.8V to V_{CC} - 2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5V and 5.5V.
4. TAVQV = TELQV + TAVEL.

Timing Waveforms

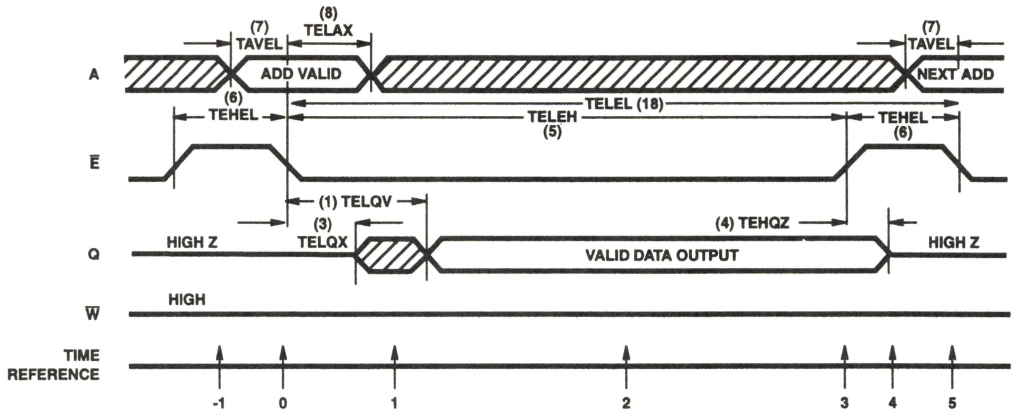


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS			OUTPUT	FUNCTION
	$\overline{E}$	$\overline{W}$	A	Q	
-1	H	X	X	Z	Memory Disabled
0	↘	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↗	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on-chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set-up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all input and ready the RAM for the next memory cycle (T = 4).

Timing Waveforms (Continued)

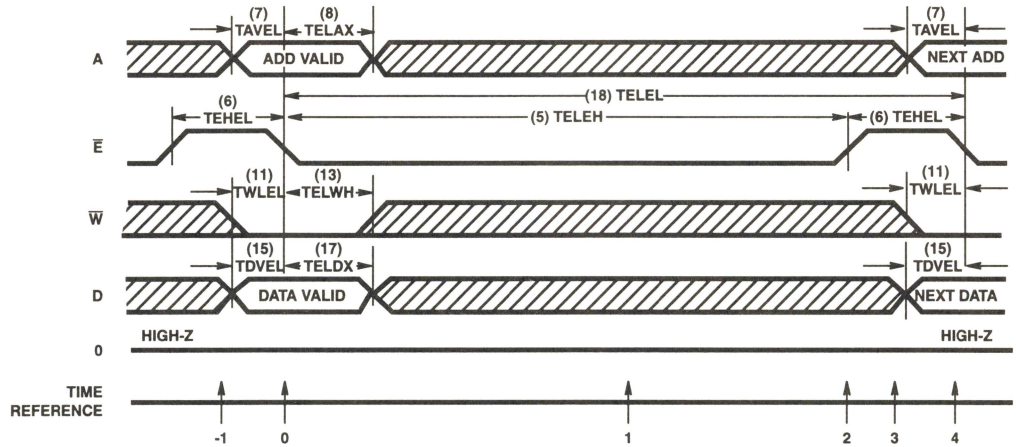


FIGURE 2. EARLY WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUT	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↓	L	V	V	Z	Cycle Begins, Addresses are Latched
1	L	X	X	X	Z	Write in Progress Internally
2	↑	X	X	X	Z	Write Completed
3	H	X	X	X	Z	Prepare for Next Cycle (Same as - 1)
4	↓	L	V	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on-chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls, determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore, data set-up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state, the output buffer and all inputs are disabled and all signals are unlatched. The device is now ready for the next cycle.

Timing Waveforms (Continued)

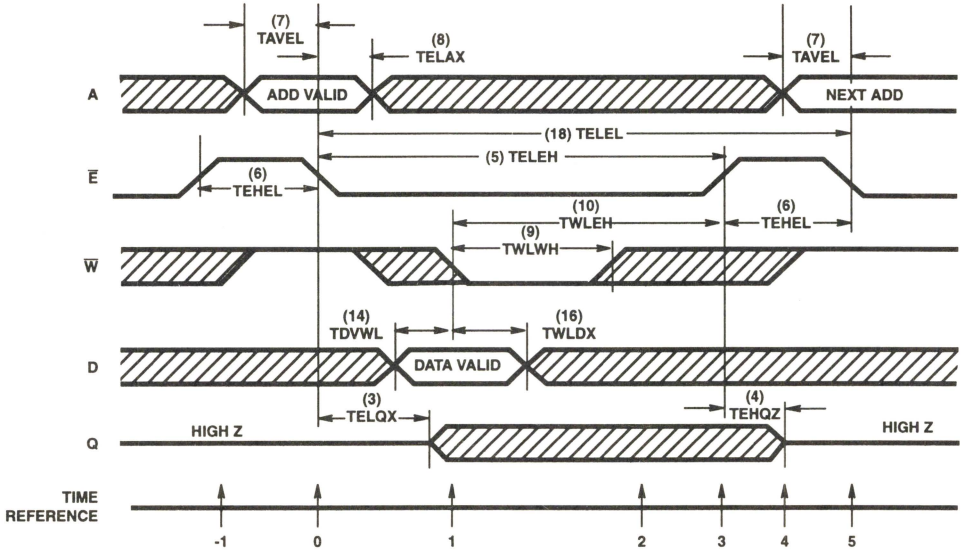


FIGURE 3. LATE WRITE CYCLE

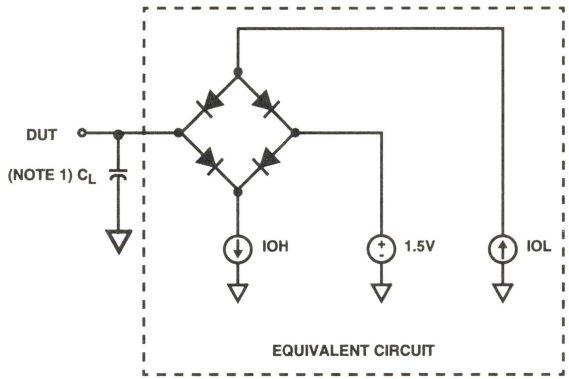
TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	↘	X	V	X	Write Begins, Data is Latched
2	L	H	X	X	X	Write In Progress Internally
3	↗	H	X	X	X	Write Completed
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle.

Recall that in the early write, the output is guaranteed to remain high impedance, and in the read-modify-write the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data setup, data hold, write setup and write pulse widths are observed.

Test Load Circuit



NOTE:

1. Test head capacitance includes stray and jig capacitance.

HARRIS SEMICONDUCTOR

HM-6504/883

March 1997

4096 x 1 CMOS RAM

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Power Standby . . . . . 125μW Max**
- **Low Power Operation . . . . . 35mW/MHz Max**
- **Data Retention . . . . . at 2.0V Min**
- **TTL Compatible Input/Output**
- **Three-State Output**
- **Standard JEDEC Pinout**
- **Fast Access Time. . . . . 120/200ns Max**
- **18 Pin Package for High Density**
- **On-Chip Address Register**
- **Gated Inputs - No Pull Up or Pull Down Resistors Required**

Description

The HM-6504/883 is a 4096 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays.

Gated inputs allow lower operating current and also eliminate the need for pull up or pull down resistors. The HM-6504/883 is a fully static RAM and may be maintained in any state for an indefinite period of time.

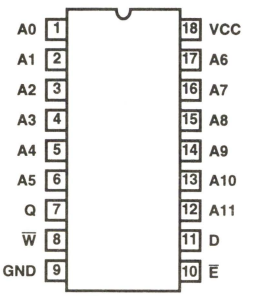
Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

PACKAGE	TEMPERATURE RANGE	200ns	300ns	PKG. NO
CERDIP	-55°C to +125°C	HM1-6504B/883	HM1-6504/883	F18.3

Pinout

HM-6504/883 (CERDIP)
TOP VIEW



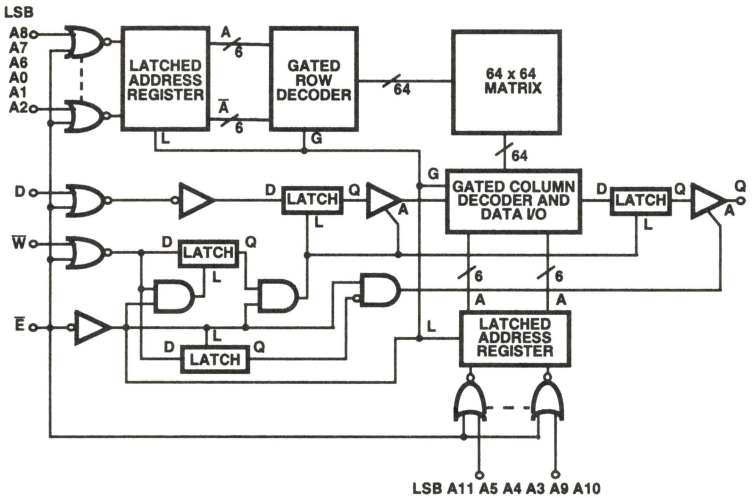
PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2993.1**

Functional Diagram



NOTES:

1. All lines active high-positive logic.
2. Three-state Buffers: A high → output active.
3. Control and Data Latches: L low → Q = D and Q latches on rising edge of L.
4. Address Latches: Latch on falling edge of $\overline{E}$.
5. Gated Decoders: Gate on rising edge of G.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	75°C/W	15°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 6910 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . -0.3V to +0.8V
Input High Voltage . . . . . VCC -2.0V to VCC +0.3V

TABLE 1. HM-6504/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V, IOL = 2mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V, IOH = -1.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5V, VO = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC, IO = 0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	25	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 2), $\overline{E}$ = 1MHz, IO = 0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	7	mA
Standby Supply Current	ICCSB	VCC = 5.0V, $\overline{E}$ = VCC -0.3V, IO = 0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	50	µA

NOTES:

1. All voltage referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.

TABLE 2. HM-6504/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS						UNITS
					HM-6504S/883		HM-6504B/883		HM-6504/883		
					MIN	MAX	MIN	MAX	MIN	MAX	
Chip Enable Access Time	(1) TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	200	-	300	ns
Address Access Time	(2) TAVQV	VCC = 4.5 and 5.5V, Note 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	220	-	320	ns
Chip Enable Pulse Negative Width	(5) TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	200	-	300	-	ns
Chip Enable Pulse Positive Width	(6) TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	50	-	90	-	120	-	ns
Address Setup Time	(7) TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	20	-	20	-	ns
Address Hold Time	(8) TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	50	-	50	-	ns
Write Enable Pulse Width	(9) TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	60	-	80	-	ns
Write Enable Pulse Setup Time	(10) TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	70	-	150	-	200	-	ns
Early Write Pulse Setup Time	(11) TWLEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Early Write Pulse Hold Time	(13) TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	60	-	80	-	ns
Data Setup Time	(14) TDVWL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Early Write Data Setup Time	(15) TDVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Data Hold Time	(16) TWLDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	25	-	60	-	80	-	ns
Early Write Data Hold Time	(17) TELDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	25	-	60	-	80	-	ns
Read or Write Cycle Time	(18) TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	170	-	290	-	420	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-6504/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	HM-6504S/883 LIMITS MIN	HM-6504S/883 LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	T_A = +25°C	-	8	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	T_A = +25°C	-	10	pF
Chip Enable Output Disable Time	(3) TELQX	VCC = 4.5 and 5.5V	1	-55°C ≤ T_A ≤ +125°C	5	-	ns
Chip Enable Output Disable Time	(4) TEHQZ	VCC = 4.5 and 5.5V HM-6504S/883	1	-55°C ≤ T_A ≤ +125°C	-	50	ns
		VCC = 4.5 and 5.5V HM-6504B/883	1	-55°C ≤ T_A ≤ +125°C	-	80	ns
		VCC = 4.5 and 5.5V HM-6504/883	1	-55°C ≤ T_A ≤ +125°C	-	100	ns
Write Enable Read Mode Setup Time	(12) TWHEL	VCC = 4.5 and 5.5V	1	-55°C ≤ T_A ≤ +125°C	0	-	ns
High Level Output Voltage	VOHL	VCC = 4.5V, IO = -100µA	1	-55°C ≤ T_A ≤ +125°C	VCC - 0.4	-	V

NOTE:

1. The parameters listed in Table 3 are controlled via design, or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Timing Waveforms

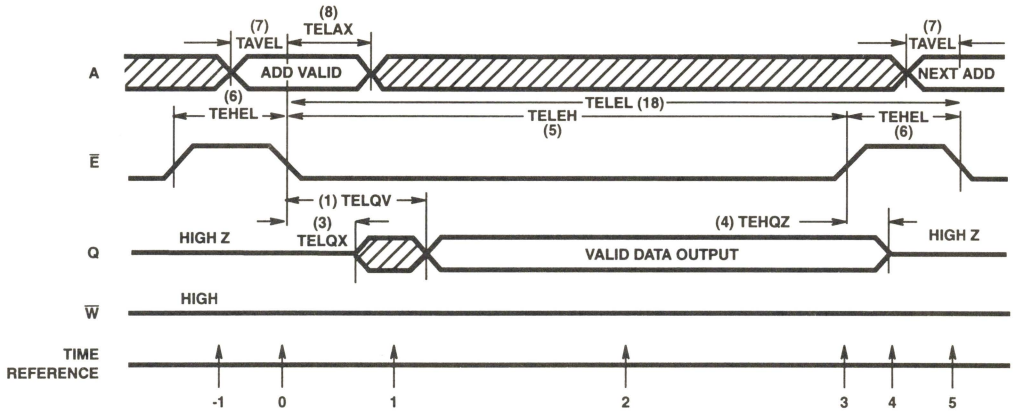


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS			OUTPUT	FUNCTION
	$\overline{E}$	$\overline{W}$	A	Q	
-1	H	X	X	Z	Memory Disabled
0	↘	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↗	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on-chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all input, and ready the RAM for the next memory cycle (T = 4).

Timing Waveforms (Continued)

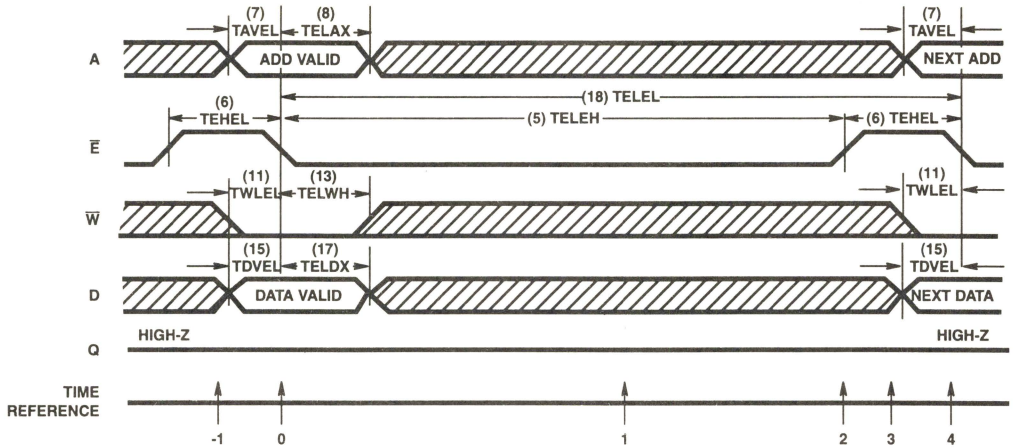


FIGURE 2. EARLY WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUT	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	L	V	V	Z	Cycle Begins, Addresses are Latched
1	L	X	X	X	Z	Write in Progress Internally
2	↗	X	X	X	Z	Write Completed
3	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
4	↘	L	V	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on-chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore, data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state, the output buffer and all inputs are disabled and all signals are unlatched. The device is now ready for the next cycle.

Timing Waveforms (Continued)

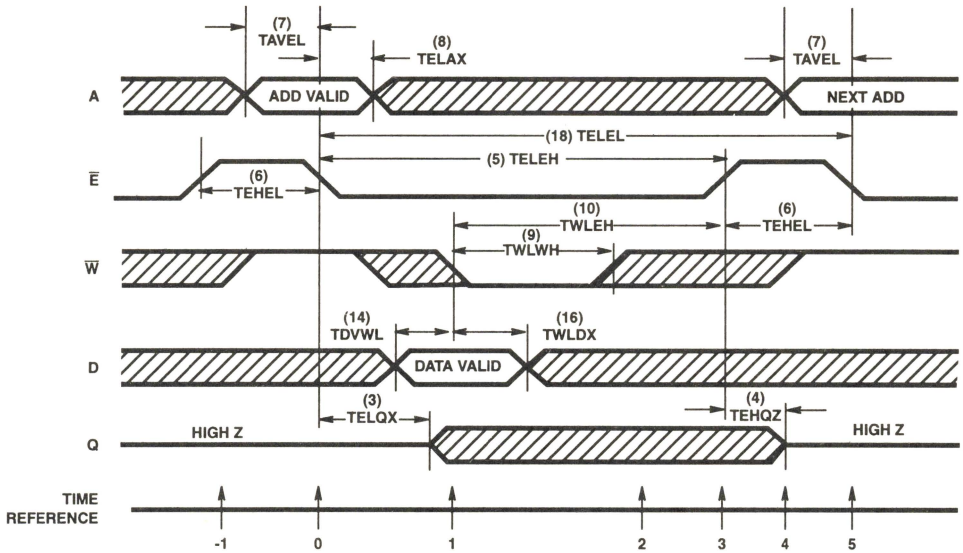


FIGURE 3. LATE WRITE CYCLE

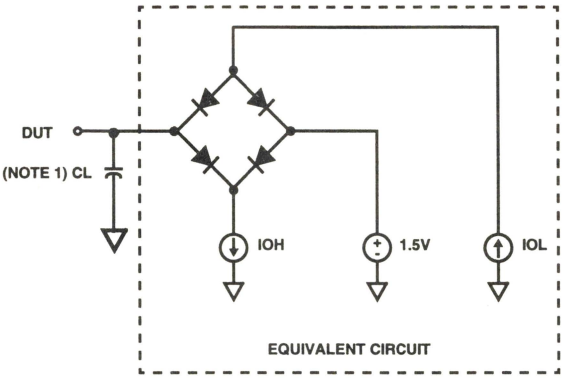
TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	↘	X	V	X	Write Begins, Data is Latched
2	L	H	X	X	X	Write In Progress Internally
3	↗	H	X	X	X	Write Completed
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle.

Recall that in the early write, the output is guaranteed to remain high impedance, and in the read-modify-write, the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data setup, data hold, write setup and write pulse widths are observed.

Test Load Circuit

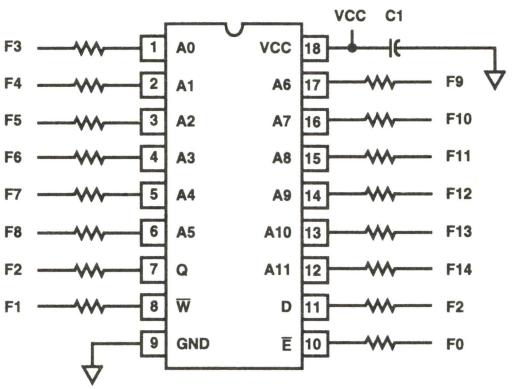


NOTE:

1. Test head capacitance includes stray and jig capacitance.

Burn-In Circuit

HM-6504/883 CERDIP



NOTES:

All resistors 47kΩ ±5%.

F0 = 100kHz ±10%.

F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F12 = F11 ÷ 2.

VCC = 5.5V ±0.5V.

VIH = 4.5V ±10%.

VIL = -0.2V to +0.4V.

C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
136 x 169 x 19 ±1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

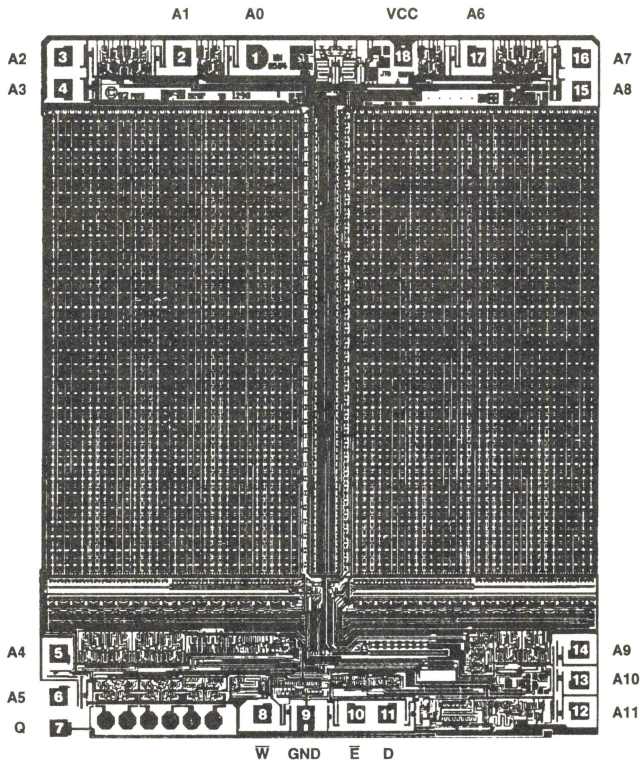
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
1.79×10^5 A/cm^2

LEAD TEMPERATURE (10s soldering):
$\leq 300^{o}C$

Metallization Mask Layout

HM-6504/883



NOTE:

1. Pin numbers correspond to DIP Package only.

HARRIS SEMICONDUCTOR

HM-6514

March 1997

1024 x 4 CMOS RAM

Features

- Low Power Standby . . . . . 125µW Max
- Low Power Operation . . . . . 35mW/MHz Max
- Data Retention . . . . . at 2.0V Min
- TTL Compatible Input/Output
- Common Data Input/Output
- Three-State Output
- Standard JEDEC Pinout
- Fast Access Time. . . . . 120/200ns Max
- 18 Pin Package for High Density
- On-Chip Address Register
- Gated Inputs - No Pull Up or Pull Down Resistors Required

Description

The HM-6514 is a 1024 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On-chip latches are provided for addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays.

Gated inputs allow lower operating current and also eliminate the need for pull up or pull down resistors. The HM-6514 is a fully static RAM and may be maintained in any state for an indefinite period of time.

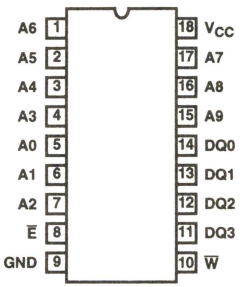
Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

120ns	200ns	300ns	TEMPERATURE RANGE	PACKAGE	PKG. NO.
HM3-6514S-9	HM3-6514B-9	HM3-6514-9	-40°C to +85°C	PDIP	E18.3
HM1-6514S-9	HM1-6514B-9	HM1-6514-9	-40°C to +85°C	CERDIP	F18.3
24502BVA	-	-	-	JAN#	F18.3
8102402VA	8102404VA	8102406VA	-	SMD#	F18.3
-	-	-	-40°C to +85°C	CLCC	J18.B
-	-	HM4-6514-B	-55°C to +125°C		J18.B

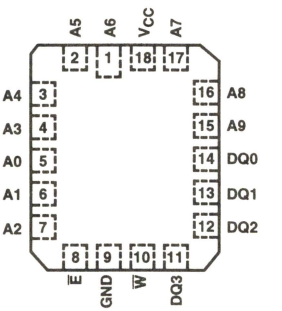
Pinouts

HM-6514 (PDIP, CERDIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

HM-6514 (CLCC)
TOP VIEW

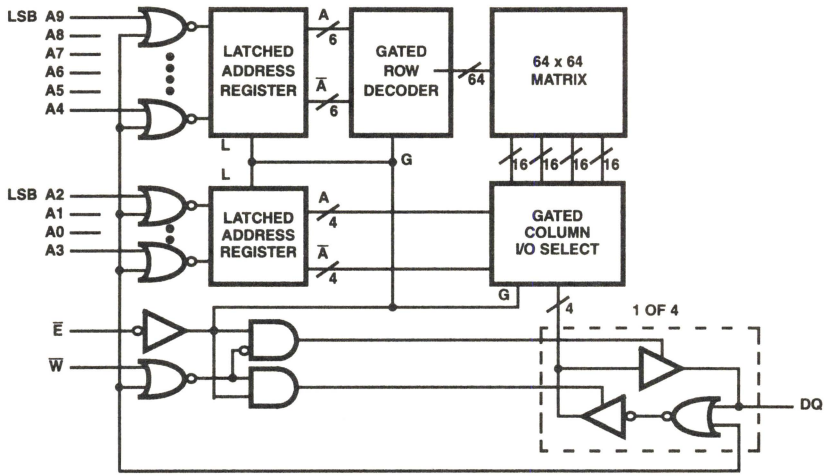


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2995.1**

Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Ranges:
HM-6514S-9, HM-6514B-9, HM-6514-9 . . . . . $-40^{o}C$ to $+85^{o}C$
HM-6514B-8, HM-6514-8 . . . . . $-55^{o}C$ to $+125^{o}C$

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package	$75^{o}C/W$	$15^{o}C/W$
PDIP Package	$75^{o}C/W$	N/A
CLCC Package	$90^{o}C/W$	$33^{o}C/W$

Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $+150^{o}C$
Maximum Junction Temperature
Ceramic Package . . . . . $+175^{o}C$
Plastic Package . . . . . $+150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^{o}C$

Die Characteristics

Gate Count . . . . . 6910 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5V ±10%; T_A = $-40^{o}C$ to $+85^{o}C$ (HM-6514S-9, HM-6514B-9, HM-6514-9)
T_A = $-55^{o}C$ to $+125^{o}C$ (HM-6514B-8, HM-6514-8)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	HM-6514-9	-	25	µA	IO = 0mA, $\overline{E}$ = V_{CC} -0.3V, V_{CC} = 5.5V
		HM-6514-8	-	50	µA	
ICCOP	Operating Supply Current (Note 1)		-	7	mA	$\overline{E}$ = 1MHz, IO = 0mA, VI = GND, V_{CC} = 5.5V
ICCDR	Data Retention Supply Current	HM-6514-9	-	15	µA	IO = 0mA, V_{CC} = 2.0V, $\overline{E}$ = V_{CC}
		HM-6514-8	-	25	µA	
VCCDR	Data Retention Supply Voltage		2.0	-	V	
II	Input Leakage Current		-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IIOZ	Input/Output Leakage Current		-1.0	+1.0	µA	VIO = V_{CC} or GND, V_{CC} = 5.5V
VIL	Input Low Voltage		-0.3	0.8	V	V_{CC} = 4.5V
VIH	Input High Voltage		V_{CC} -2.0	V_{CC} +0.3	V	V_{CC} = 5.5V
VOL	Output Low Voltage		-	0.4	V	IO = 2.0mA, V_{CC} = 4.5V
VOH1	Output High Voltage		2.4	-	V	IO = -1.0mA, V_{CC} = 4.5V
VOH2	Output High Voltage (Note 2)		V_{CC} -0.4	-	V	IO = -100µA, V_{CC} = 4.5V

Capacitance

T_A = $+25^{o}C$

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	f = 1MHz, All measurements are referenced to device GND
CIO	Input/Output Capacitance (Note 2)	10	pF	

NOTES:

1. Typical derating 5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

AC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6514S-9, HM-6514B-9, HM-6514-9)
T_A = -55°C to +125°C (HM-6514B-8, HM-6514-8)

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS
		HM-6514S-9		HM-6514B-9		HM-6514-9			
		MIN	MAX	MIN	MAX	MIN	MAX		
(1) TELQV	Chip Enable Access Time	-	120	-	220	-	300	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	120	-	220	-	320	ns	(Notes 1, 3, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	5	-	5	-	ns	(Notes 2, 3)
(4) TEHQZ	Chip Enable Output Disable Time	-	50	-	80	-	100	ns	(Notes 2, 3)
(5) TELEH	Chip Enable Pulse Negative Width	120	-	200	-	300	-	ns	(Notes 1, 3)
(6) TEHEL	Chip Enable Pulse Positive Width	50	-	90	-	120	-	ns	(Notes 1, 3)
(7) TAVEL	Address Setup Time	0	-	20	-	20	-	ns	(Notes 1, 3)
(8) TELAX	Address Hold Time	40	-	50	-	50	-	ns	(Notes 1, 3)
(9) TWLWH	Write Enable Pulse Width	120	-	200	-	300	-	ns	(Notes 1, 3)
(10) TWLEH	Chip Enable Write Pulse Setup Time	120	-	200	-	300	-	ns	(Notes 1, 3)
(11) TELWH	Chip Enable Write Pulse Hold Time	120	-	200	-	300	-	ns	(Notes 1, 3)
(12) TDVWH	Data Setup Time	50	-	120	-	200	-	ns	(Notes 1, 3)
(13) TWHDX	Data Hold Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(14) TWLDV	Write Data Delay Time	70	-	80	-	100	-	ns	(Notes 1, 3)
(15) TWLEL	Early Output High-Z Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(16) TEHWH	Late Output High-Z Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(17) TELEL	Read or Write Cycle Time	170	-	290	-	420	-	-	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0.8V to V_{CC} - 2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5V and 5.5V.
4. TAVQV = TELQV + TAVEL.

Timing Waveforms

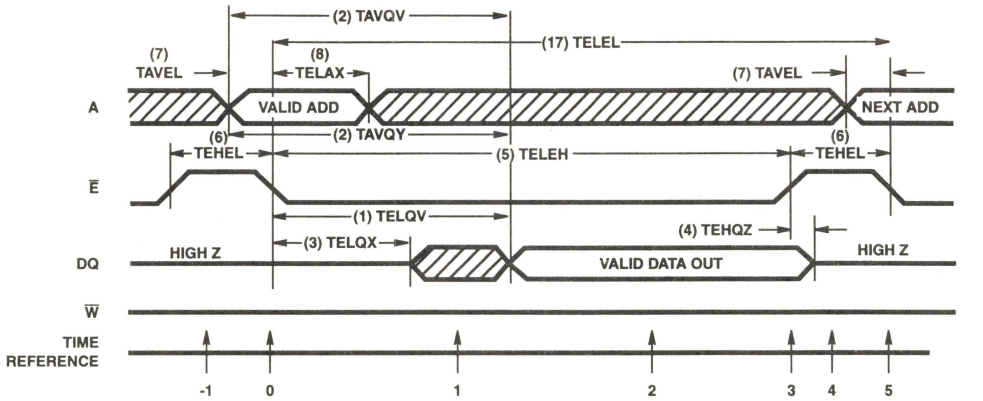


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS			DATA I/O DQ	FUNCTION
	$\overline{E}$	$\overline{W}$	A		
-1	H	X	X	Z	Memory Disabled
0	↘	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↗	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on-chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled, but data is not valid until during time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all inputs, and ready the RAM for the next memory cycle (T = 4).

Timing Waveforms (Continued)

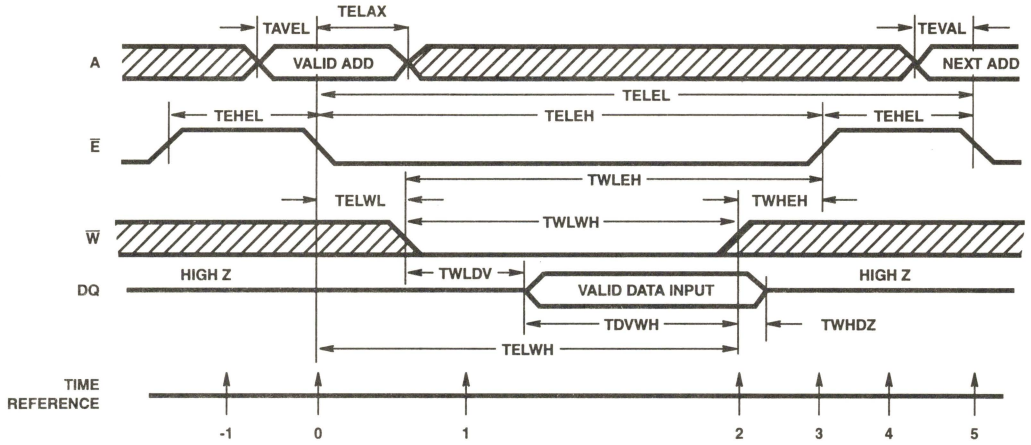


FIGURE 2. WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS			DQ	FUNCTION
	$\overline{E}$	$\overline{W}$	A		
-1	H	X	X	Z	Memory Disabled
0	↓	X	V	Z	Cycle Begins, Addresses are Latched
1	L	L	X	Z	Write Period Begins
2	L	↑	X	V	Data In is Written
3	↑	H	X	Z	Write Completed
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on-chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TWLDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before $\overline{E}$. The RAM outputs and all inputs will three-state after $\overline{E}$ rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

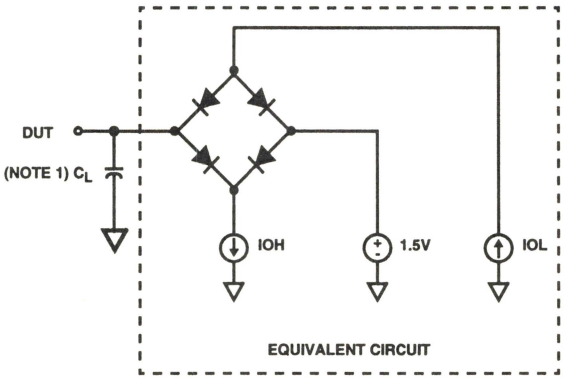
Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rising

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data outputs will stay disabled throughout the cycle, thus, simplifying the data input timing. TWLEL and TEHWH must be met, but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDX become TDVEH and TEHDX. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ and $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDX

If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

Test Load Circuit



NOTE:

1. Test head capacitance.

HM-6514/883

March 1997

1024 x 4 CMOS RAM

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Power Standby . . . . . 125µW Max**
- **Low Power Operation . . . . . 35mW/MHz Max**
- **Data Retention . . . . . at 2.0V Min**
- **TTL Compatible Input/Output**
- **Common Data Input/Output**
- **Three-State Output**
- **Standard JEDEC Pinout**
- **Fast Access Time. . . . . 120/200ns Max**
- **18 Pin Package for High Density**
- **Gated Inputs - No Pull Up or Pull Down Resistors Required**
- **On-Chip Address Register**

Description

The HM-6514/883 is a 1024 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays.

Gated inputs allow lower operating current and also eliminates the need for pull up or pull down resistors. The HM-6514/883 is fully static RAM and may be maintained in any state for an indefinite period of time.

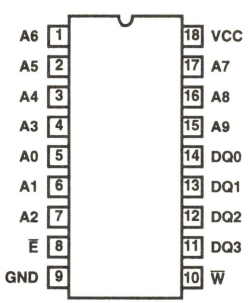
Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

120ns	200ns	300ns	TEMPERATURE RANGE	PACKAGE	PKG. NO.
HM1-6514S/883	HM1-6514B/883	HM1-6514/883	-55°C to 125°C	CERDIP	F18.3

Pinout

HM-6514/883
(CERDIP)
TOP VIEW

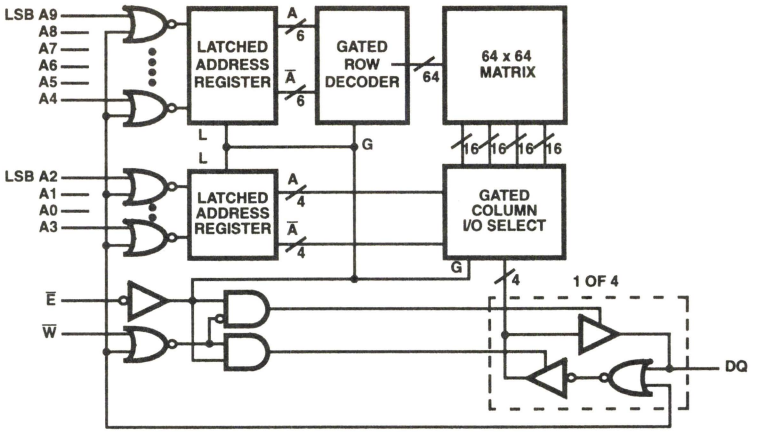


PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	75°C/W	15°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 6910 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . VCC -2.0V to VCC
Input Rise and Fall Time . . . . . 40ns Max

TABLE 1. HM-6514/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 3.2mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -1.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Input/Output Leakage Current	IIOZ	VCC = 5.5 V, VIO = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC -0.3V, IO = 0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	25	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 2) $\overline{E}$ = 1MHz	1, 2, 3	$-55°C \le T_A \le +125°C$	-	7	mA
Standby Supply Current	ICCSB	VCC = 5.5V, $\overline{E}$ = VCC-0.3V, IO = 0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	50	µA

NOTES:

1. All voltages referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.

TABLE 2. HM-6514/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS						UNITS
					HM-6514S/883		HM-6514B/883		HM-6514/883		
					MIN	MAX	MIN	MAX	MIN	MAX	
Chip Enable Access Time	(1) TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	200	-	300	ns
Address Access Time	(2) TAVQV	VCC = 4.5 and 5.5V, Note 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	220	-	320	ns
Chip Enable Pulse Negative Width	(5) TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	200	-	300	-	ns
Chip Enable Pulse Positive Width	(6) TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	50	-	90	-	120	-	ns
Address Setup Time	(7) TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	20	-	20	-	ns
Address Hold Time	(8) TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	50	-	50	-	ns
Write Enable Pulse Width	(9) TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	200	-	300	-	ns
Write Enable Pulse Setup Time	(10) TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	200	-	300	-	ns
Write Enable Pulse Hold Time	(11) TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	200	-	300	-	ns
Data Setup Time	(12) TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	50	-	120	-	200	-	ns
Data Hold Time	(13) TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Write Data Delay Time	(14) TWLDV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	70	-	80	-	100	-	ns
Early Output High-Z Time	(15) TWLEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Late Output High-Z Time	(16) TEHWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Read or Write Cycle Time	(17) TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	170	-	290	-	420	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-6514/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	HM-6514/883 LIMITS MIN	HM-6514/883 LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	$T_A = +25^oC$	-	8	pF
Input/Output Capacitance	CIO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	$T_A = +25^oC$	-	10	pF
Chip Enable Output Disable Time	TELQX	VCC = 4.5 and 5.5V	1	$-55^oC \le T_A \le +125^oC$	5	-	
Chip Enable Output Disable Time	TEHQZ	VCC = 4.5 and 5.5V HM-6514S/883	1	$-55^oC \le T_A \le +125^oC$	-	50	ns
		VCC = 4.5 and 5.5V HM-6514B/883	1	$-55^oC \le T_A \le +125^oC$	-	80	ns
		VCC = 4.5 and 5.5V HM-6514/883	1	$-55^oC \le T_A \le +125^oC$	-	100	ns
High Level Output Voltage	VOH2	VCC = 4.5V, IO = -100µA	1	$-55^oC \le T_A \le +125^oC$	VCC -0.4	-	V

NOTES:

1. The parameters listed in Table 3 are controlled via design, or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Timing Waveforms

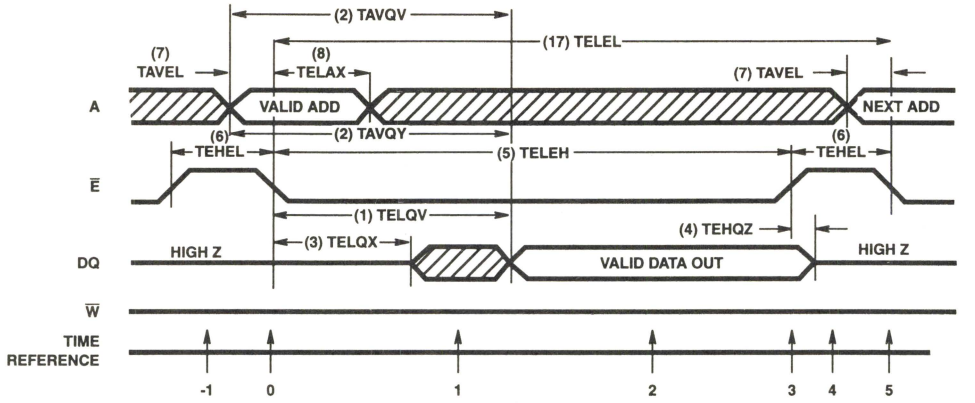


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS			DATA I/O DQ	FUNCTION
	$\overline{E}$	$\overline{W}$	A		
-1	H	X	X	Z	Memory Disabled
0	↘	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↗	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on-chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all inputs, and ready the RAM for the next memory cycle (T = 4).

Timing Waveforms (Continued)

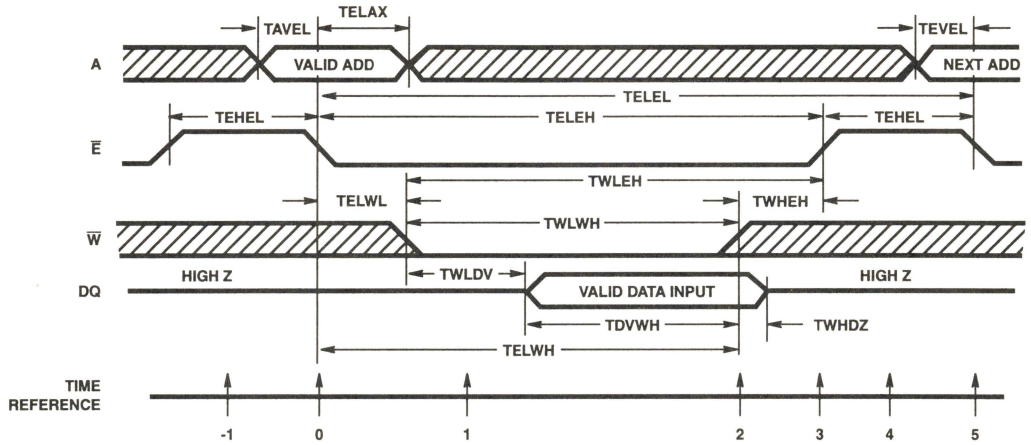


FIGURE 2. WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS			DQ	FUNCTION
	$\overline{E}$	$\overline{W}$	A		
-1	H	X	X	Z	Memory Disabled
0	↓	X	V	Z	Cycle Begins, Addresses are Latched
1	L	L	X	Z	Write Period Begins
2	L	↑	X	V	Data In is Written
3	↑	H	X	Z	Write Completed
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on-chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TWLDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before $\overline{E}$. The RAM outputs and all inputs will three-state after $\overline{E}$ rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

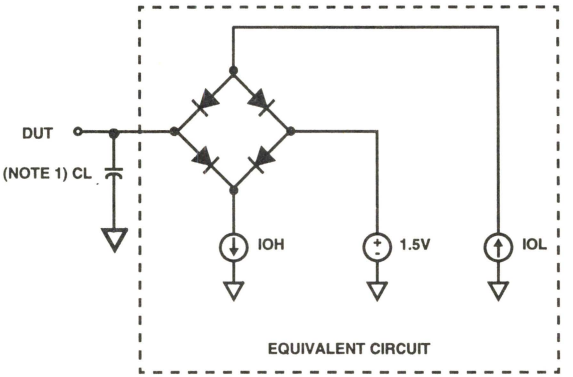
Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rising

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data outputs will stay disabled throughout the cycle, thus simplifying the data input timing. TWLEL and TEHWH must be met, but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDX become TDVEH and TEHDX. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ and $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDX

If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

Test Load Circuit

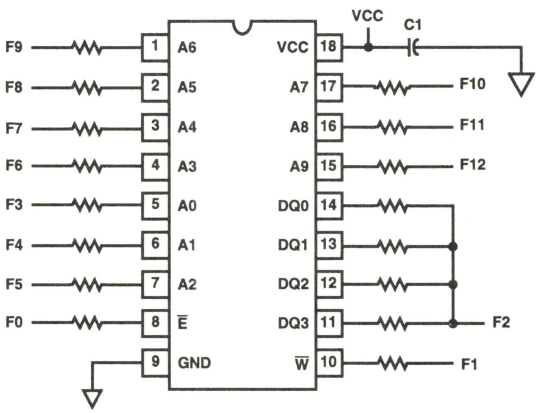


NOTE:

1. Test head capacitance.

Burn-In Circuit

HM6514/883 CERDIP



NOTES:

All resistors 47kΩ ±5%.

F0 = 100kHz ±10%.

F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F12 = F11 ÷ 2.

VCC = 5.5V ±0.5V.

VIH = 4.5V ±10%.

VIL = -0.2V to +0.4V.

C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
136 x 167 x 19 ±1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

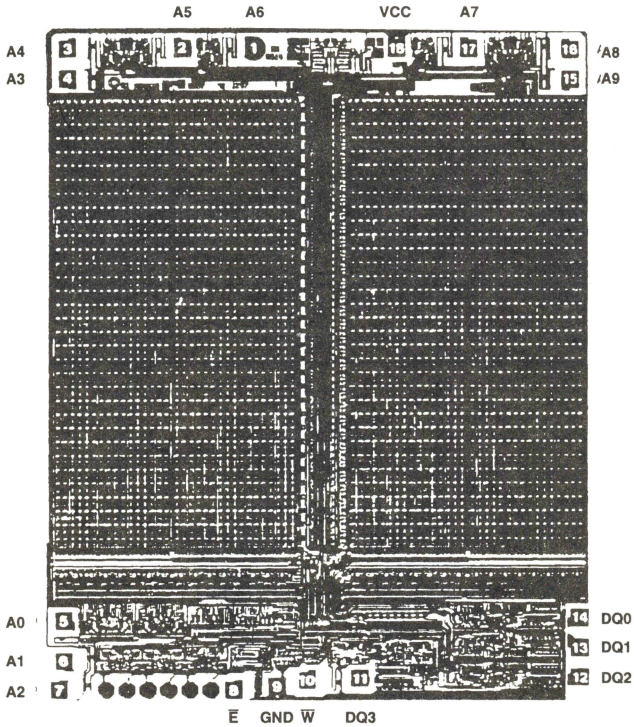
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
1.79×10^5 A/cm^2

LEAD TEMPERATURE (10s soldering):
300°C

Metallization Mask Layout

HM-6514/883



NOTE:

1. Pin numbers correspond to DIP Package only.

HARRIS SEMICONDUCTOR

MWS5114

1024-Word x 4-Bit LSI Static RAM

March 1997

Features

- Fully Static Operation
- Industry Standard 1024 x 4 Pinout (Same as Pinouts for 6514, 2114, 9114, and 4045 Types)
- Common Data Input and Output
- Memory Retention for Standby Battery Voltage as Low as 2V Min
- All Inputs and Outputs Directly TTL Compatible
- Three-State Outputs
- Low Standby and Operating Power

Description

The MWS5114 is a 1024 word by 4-bit static random access memory that uses the ion-implanted silicon gate complementary MOS (CMOS) technology. It is designed for use in memory systems where low power and simplicity in use are desirable. This type has common data input and data output and utilizes a single power supply of 4.5V to 6.5V.

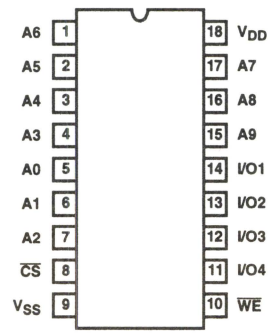
The MWS5114 is supplied in 18 lead, hermetic, dual-in-line sidebrazed ceramic packages (D suffix) and in 18 lead dual-in-line plastic packages (E suffix).

Ordering Information

200ns	250ns	300ns	TEMPERATURE RANGE	PACKAGE	PKG. NO.
MWS5114E3	MWS5114E2 MWS5114E2X	MWS5114E1	0°C to +70°C	PDIP Burn-In	E18.3 E18.3
MWS5114D3 MWS5114D3X	MWS5114D2	MWS5114D1	0°C to +70°C	SBDIP Burn-In	D18.3 D18.3

Pinout

MWS5114
(PDIP, SBDIP)
TOP VIEW



OPERATIONAL MODES

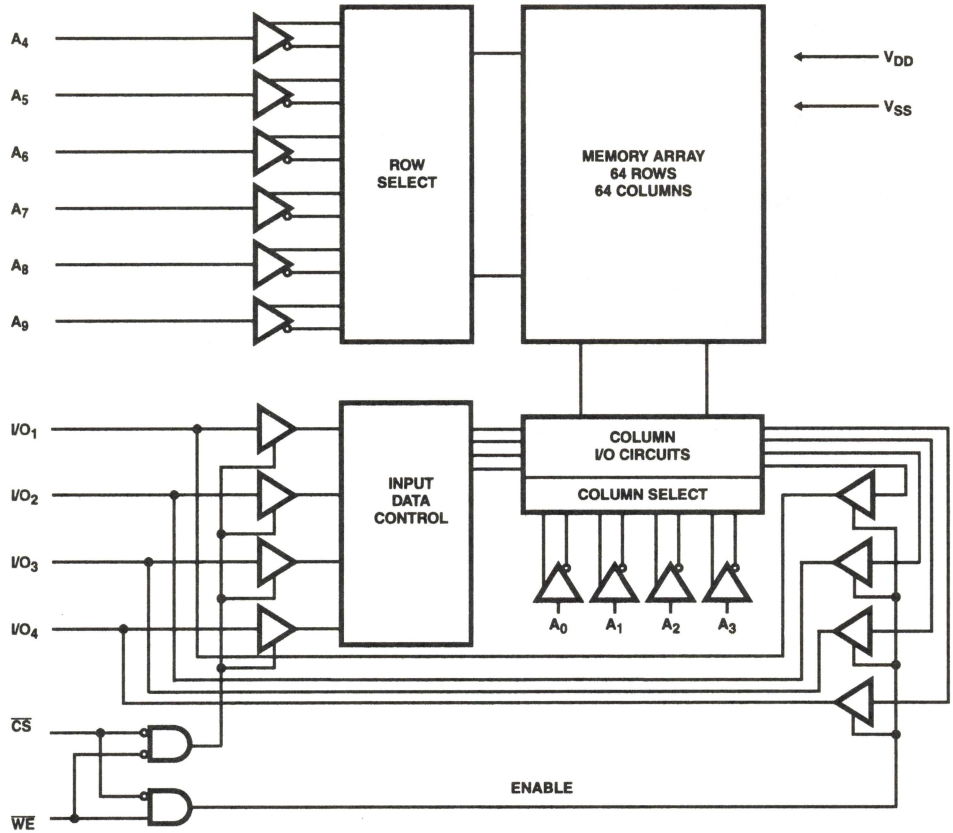
FUNCTION	$\overline{CS}$	$\overline{WE}$	DATA PINS
Read	0	1	Output: Dependent on data
Write	0	0	Input
Not Selected	1	X	High Impedance

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1325.2**

Functional Block Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal) . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input . . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Plastic DIP Package	75	N/A
SBDIP Package	75	20

Operating Temperature Range (T_A)
Package Type D . . . . . -55°C to +125°C
Package Type E . . . . . -40°C to +85°C
Maximum Storage Temperature Range (T_{STG}) . . . -65°C to +150°C
Maximum Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package . . . . . +150°C
Maximum Lead Temperature . . . . . +265°C

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS ALL TYPES MIN	LIMITS ALL TYPES MAX	UNITS
DC Operating Voltage Range	4.5	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V

Static Electrical Specifications

At T_A = 0°C to +70°C, V_{DD} = ±5%, Except as Noted

PARAMETER	SYMBOL	CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS MWS5114-3 MIN	MWS5114-3 (NOTE 1) TYP	MWS5114-3 MAX	MWS5114-2 MIN	MWS5114-2 (NOTE 1) TYP	MWS5114-2 MAX	MWS5114-1 MIN	MWS5114-1 (NOTE 1) TYP	MWS5114-1 MAX	UNITS
Quiescent Device Current	IDD	-	0, 5	5	-	75	100	-	75	100	-	75	250	µA
Output Low (Sink) Current	I_{OL}	0.4	0, 5	5	2	4	-	2	4	-	2	4	-	mA
Output High (Source) Current	I_{OH}	4.6	0, 5	5	-0.4	-1	-	-0.4	-1	-	-0.4	-1	-	mA
Output Voltage Low-Level	VOL	-	0, 5	5	-	0	0.1	-	0	0.1	-	0	0.1	V
Output Voltage High-Level	VOH	-	0, 5	5	4.9	5	-	4.9	5	-	4.9	5	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	1.2	0.8	-	1.2	0.8	-	1.2	0.8	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	2.4	-	-	2.4	-	-	2.4	-	-	V
Input Leakage Current (Note 2)	IIN	-	0, 5	5	-	±0.1	±5	-	±0.1	±5	-	±0.1	±5	µA
Operating Current (Note 3)	IDD1	-	0, 5	5	-	4	8	-	4	8	-	4	8	mA

Static Electrical Specifications At $T_A = 0^oC$ to $+70^oC$, $V_{DD} = \pm5\%$, Except as Noted **(Continued)**

PARAMETER	SYMBOL	CONDITIONS			LIMITS									UNITS
					MWS5114-3			MWS5114-2			MWS5114-1			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Three-State Output Leakage Current (Note 4)	I_{OUT}	0, 5	0, 5	5	-	±0.5	±5	-	±0.5	±5	–	±0.5	±5	µA
Input Capacitance	CI_N	-	-	-	-	5	7.5	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	-	10	15	pF

NOTES:

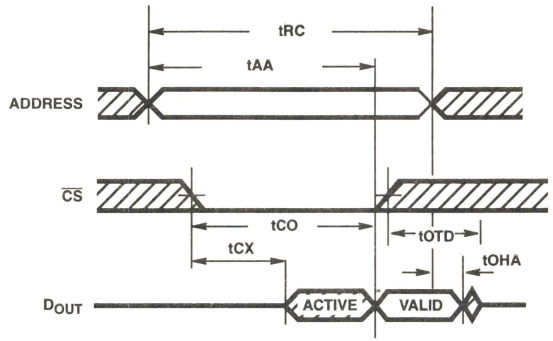
1. Typical values are for $T_A = 25^oC$ and nominal V_{DD}.
2. All inputs in parallel.
3. Outputs open circuited; cycle time = 1µs.
4. All outputs in parallel.

Dynamic Electrical Specifications at $T_A = 0^oC$ to $+70^oC$, $V_{DD} = 5V \pm 5\%$, Input t_R, $t_F = 10ns$; $C_L = 50pF$ and 1 TTL Load

PARAMETER	SYMBOL	LIMITS									UNITS
		MWS5114-3			MWS5114-2			MWS5114-1			
		(NOTE 1) MIN	(NOTE 2) TYP	MAX	(NOTE 1) MIN	(NOTE 2) TYP	MAX	(NOTE 1) MIN	(NOTE 2) TYP	MAX	
READ CYCLE TIMES (FIGURE 1)											
Read Cycle	tRC	200	160	-	250	200	-	300	250	-	ns
Access from Address	tAA	-	160	200	-	200	250	-	250	300	ns
Chip Selection to Output Valid	tCO	-	110	150	-	150	200	-	200	250	ns
Chip Selection to Output Active	tCX	20	100	-	20	100	-	20	100	-	ns
Output Three-State from Deselection	tOTD	-	75	125	-	75	125	-	75	125	ns
Output Hold from Address Change	tOHA	50	100	-	50	100	-	50	100	-	ns
WRITE CYCLE TIMES (FIGURE 2)											
Write Cycle	tWC	200	160	-	250	200	-	300	220	-	ns
Write	tW	125	100	-	150	120	-	200	140	-	ns
Write Release	tWR	50	40	-	50	40	-	50	40	-	ns
Address to Chip Select Setup Time	$t\overline{ACS}$	0	0	-	0	0	-	0	0	-	ns
Address to Write Setup Time	$t\overline{AW}$	25	20	-	50	40	-	50	40	-	ns
Data to Write Setup Time	tDSU	75	50	-	75	50	-	75	50	-	ns
Data Hold from Write	tDH	30	10	-	30	10	-	30	10	-	ns

NOTES:

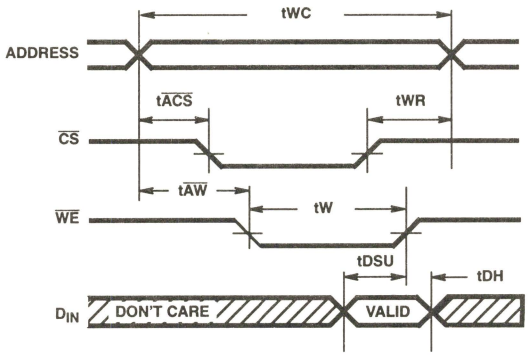
1. Time required by a limit device to allow for the indicated function.
2. Typical values are for $T_A = 25^oC$ and nominal V_{DD}.



NOTE:

1. $\overline{WE}$ is high during the Read Cycle. Timing measurement reference level is 1.5V.

FIGURE 1. READ CYCLE TIMING WAVEFORMS



NOTE:

1. $\overline{WE}$ is low during the Write Cycle. Timing measurement reference level is 1.5V.

FIGURE 2. WRITE CYCLE TIMING WAVEFORMS

Data Retention Specifications at $T_A = 0^oC$ to $+70^oC$; See Figure 3

PARAMETER		SYMBOL	TEST CONDITIONS V_{DR} (V)	TEST CONDITIONS V_{DD} (V)	LIMITS ALL TYPES MIN	LIMITS ALL TYPES (NOTE 1) TYP	LIMITS ALL TYPES MAX	UNITS
Minimum Data Retention Voltage		VDR	-	-	2	-	-	V
Data Retention Quiescent Current	MWS5114-3	IDD	2	-	-	25	50	µA
	MWS5114-2		2	-	-	25	50	µA
	MWS5114-1		2	-	-	60	125	µA
Chip Deselect to Data Retention Time		tCDR	-	5	300	-	-	ns
Recovery to Normal Operation Time		tRC	-	5	300	-	-	ns
V_{DD} to V_{DR} Rise and Fall Time		t_R, t_F	2	5	1	-	-	µs

NOTE:

1. Typical Values are for $T_A = 25^oC$ and nominal V_{DD}.

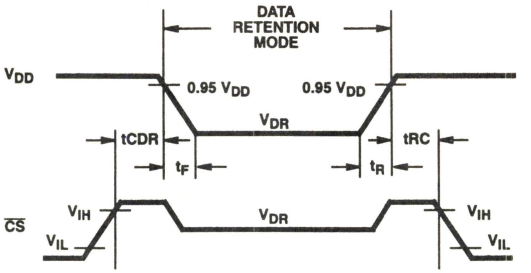


FIGURE 3. LOW V_{DD} DATA RETENTION TIMING WAVEFORMS

HM-6516

March 1997

2K x 8 CMOS RAM

Features

- Low Power Standby . . . . . 275µW Max
- Low Power Operation . . . . . 55mW/MHz Max
- Fast Access Time. . . . . 120/200ns Max
- Industry Standard Pinout
- Single Supply . . . . . 5.0V V_{CC}
- TTL Compatible
- Static Memory Cells
- High Output Drive
- On-Chip Address Latches
- Easy Microprocessor Interfacing

Description

The HM-6516 is a CMOS 2048 x 8 Static Random Access Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, which also gives fast access times. The pinout of the HM-6516 is the popular 24 pin, 8-bit wide JEDEC standard, which allows easy memory board layouts, flexible enough to accommodate a variety of PROMs, RAMS, EPROMs, and ROMs.

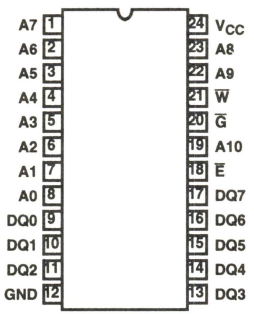
The HM-6516 is ideally suited for use in microprocessor based systems. The byte wide organization simplifies the memory array design, and keeps operating power down to a minimum, because only one device is enabled at a time. The address latches allow very simple interfacing to recent generation microprocessors which employ a multiplexed address/data bus. The convenient output enable control also simplifies multiplexed bus interfacing by allowing the data outputs to be controlled independent of the chip enable.

Ordering Information

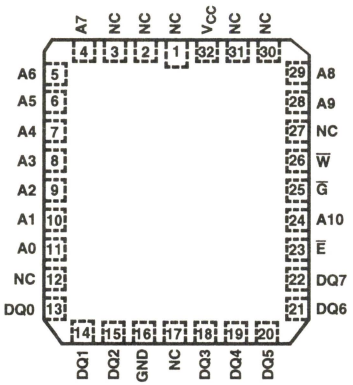
120ns	200ns	TEMP. RANGE	PACKAGE	PKG. NO.
HM1-6516B-9	HM1-6516-9	-40°C to +85°C	CERDIP	F24.6
-	29102BJA	-55°C to +125°C	JAN#	F24.6
8403607JA	8403601JA	-55°C to +125°C	SMD#	F24.6
-	HM4-6516-9	-40°C to +85°C	CLCC	J32.A
8403607ZA	8403601ZA	-55°C to +125°C	SMD#	J32.A

Pinouts

HM-6516
(CERDIP)
TOP VIEW



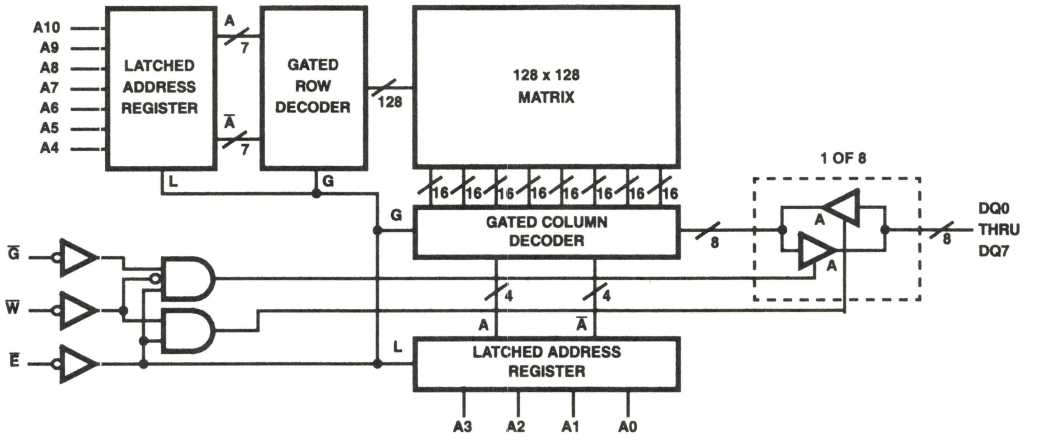
HM-6516
(CLCC)
TOP VIEW



PIN	DESCRIPTION
NC	No Connect
A0 - A10	Address Inputs
$\overline{E}$	Chip Enable/Power Down
V_{SS}/GND	Ground
DQ0 - DQ7	Data In/Data Out
V_{CC}	Power (+5V)
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage Applied for all Grades . . . . . GND -0.3V to V_{CC} +0.3V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Ranges:
HM-6516B-9, HM-6516-9 . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	48°C/W	8°C/W
CLCC Package	66°C/W	12°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 25953 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6516B-9, HM-6516-9)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	50	µA	IO = 0mA, VI = V_{CC} or GND, V_{CC} = 5.5V, HM-6516B-9
		-	100	µA	IO = 0mA, VI = V_{CC} or GND, HM-6516-9
ICCOP	Operating Supply Current (Note 1)	-	10	mA	f = 1MHz, IO = 0mA, $\overline{G}$ = V_{CC}, V_{CC} = 5.5V, VI = V_{CC} or GND
ICCDR	Data Retention Supply Current	-	25	µA	V_{CC} = 2.0V, IO = 0mA, VI = V_{CC} or GND, $\overline{E}$ = V_{CC}, HM-6516B-9
		-	50	µA	V_{CC} = 2.0V, IO = 0mA, VI = V_{CC} or GND, $\overline{E}$ = V_{CC}, HM-6516-9
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = V_{CC} or GND, V_{CC} = 5.5V
V_{IL}	Input Low Voltage	-0.3	0.8	V	V_{CC} = 4.5V
V_{IH}	Input High Voltage	2.4	V_{CC} +0.3	V	V_{CC} = 5.5V
VOL	Output Low Voltage	-	0.4	V	IO = 3.2mA, V_{CC} = 4.5V
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA, V_{CC} = 4.5V
VOH2	Output High Voltage (Note 2)	V_{CC} -0.4	-	V	IO = -100µA, V_{CC} = 4.5V

Capacitance T_A = +25°C

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	f = 1MHz, All measurements are referenced to device GND
CIO	Input/Output Capacitance (Note 2)	10	pF	

NOTES:

1. Typical derating 5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

AC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6516B-9, HM-6516-9)

SYMBOL	PARAMETER	LIMITS				UNITS	TEST CONDITIONS
		HM-6516B-9		HM-6516-9			
		MIN	MAX	MIN	MAX		
(1) TELQV	Chip Enable Access Time	-	120	-	200	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	120	-	200	ns	(Notes 1, 3, 4)
(3) TELQX	Chip Enable Output Enable Time	10	-	10	-	ns	(Notes 2, 3)
(4) TWLQZ	Write Enable Output Disable Time	-	50	-	80	ns	(Notes 2, 3)
(5) TEHQZ	Chip Enable Output Disable Time	-	50	-	80	ns	(Notes 2, 3)
(6) TGLQV	Output Enable Output Valid Time	-	80	-	80	ns	(Notes 1, 3)
(7) TGLQX	Output Enable Output Enable Time	10	-	10	-	ns	(Notes 2, 3)
(8) TGHQZ	Output Enable Output DisableTime	-	50	-	80	ns	(Notes 2, 3)
(9) TELEH	Chip Enable Pulse Negative Width	120	-	200	-	ns	(Notes 1, 3)
(10) TEHEL	Chip Enable Pulse Positive Width	50	-	80	-	ns	(Notes 1, 3)
(11) TAVEL	Address Setup Time	0	-	0	-	ns	(Notes 1, 3)
(12) TELAX	Address Hold Time	30	-	50	-	ns	(Notes 1, 3)
(13) TWLWH	Write Enable Pulse Width	120	-	200	-	ns	(Notes 1, 3)
(14) TWLEH	Write Enable Pulse Setup Time	120	-	200	-	ns	(Notes 1, 3)
(15) TELWH	Write Enable Pulse Hold Time	120	-	200	-	ns	(Notes 1, 3)
(16) TDVWH	Data Setup Time	50	-	80	-	ns	(Notes 1, 3)
(17) TWHDX	Data Hold Time	10	-	10	-	ns	(Notes 1, 3)
(18) TELEL	Read or Write Cycle Time	170	-	280	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0.8V to V_{CC} - 2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5V and 5.5V.
4. TAVQV = TELQV + TAVEL.

Timing Waveforms

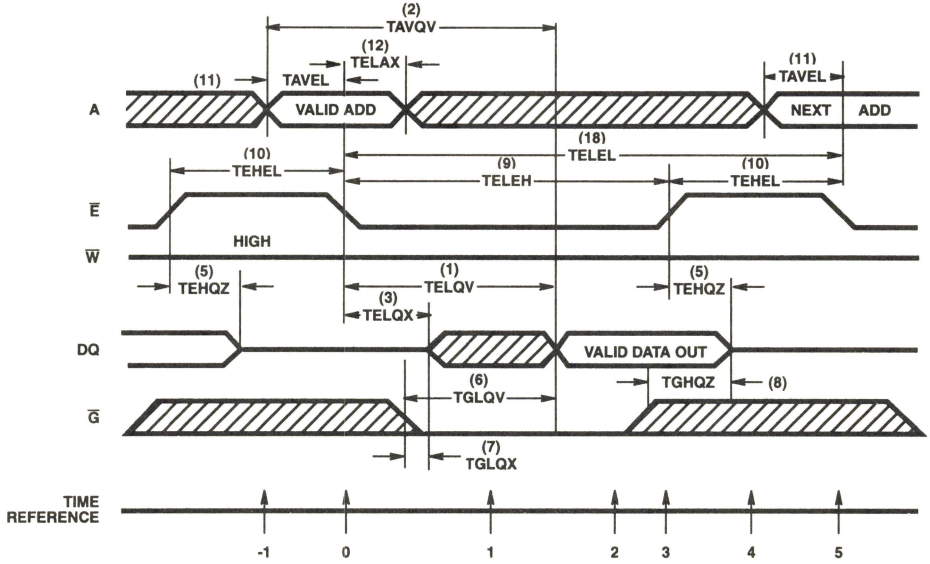


FIGURE 1. READ CYCLE

The address information is latched in the on-chip registers on the falling edge of $\overline{E}$ (T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2), $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical "1" state (T = -1, 0, 3, 4, 5). After (T = 4) time, the memory is ready for the next cycle.

Timing Waveforms (Continued)

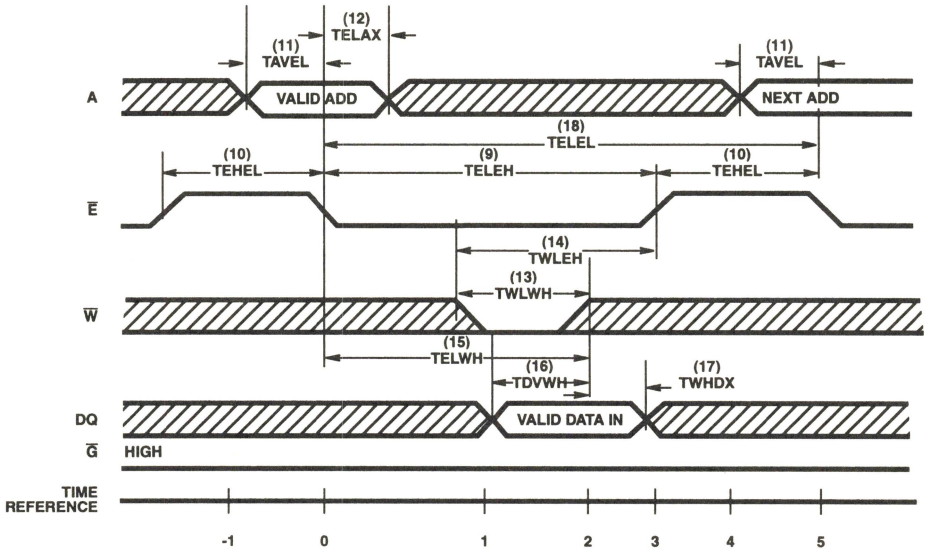


FIGURE 2. WRITE CYCLE

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on-chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$ (T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising of $\overline{E}$.

Typical Performance Curve

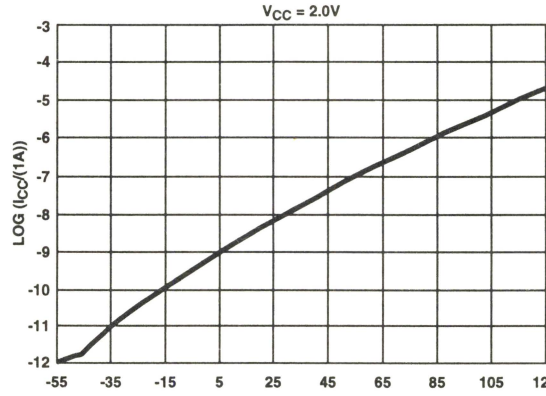


FIGURE 3. TYPICAL ICCDR vs T_A

HARRIS SEMICONDUCTOR

HM-6516/883

March 1997

2K x 8 CMOS RAM

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Power Standby . . . . . 275µW Max**
- **Low Power Operation . . . . . 55mW/MHz Max**
- **Fast Access Time. . . . . 120/200ns Max**
- **Industry Standard Pinout**
- **Single Supply . . . . . 5.0V VCC**
- **TTL Compatible**
- **Static Memory Cells**
- **High Output Drive**
- **On-Chip Address Latches**
- **Easy Microprocessor Interfacing**

Description

The HM-6516/883 is a CMOS 2048 x 8 Static Random Access Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, which also gives fast access times. The pinout of the HM-6516/883 is the popular 24 pin, 8-bit wide JEDEC Standard which allows easy memory board layouts, flexible enough to accommodate a variety of PROMs, RAMS, EPROMs, and ROMs.

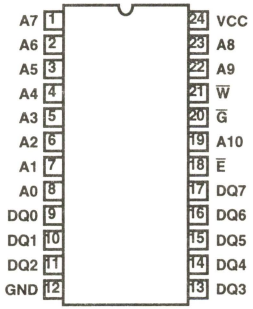
The HM-6516/883 is ideally suited for use in microprocessor based systems. The byte wide organization simplifies the memory array design, and keeps operating power down to a minimum because only one device is enabled at a time. The address latches allow very simple interfacing to recent generation microprocessors which employ a multiplexed address/data bus. The convenient output enable control also simplifies multiplexed bus interfacing by allowing the data outputs to be controlled independent of the chip enable.

Ordering Information

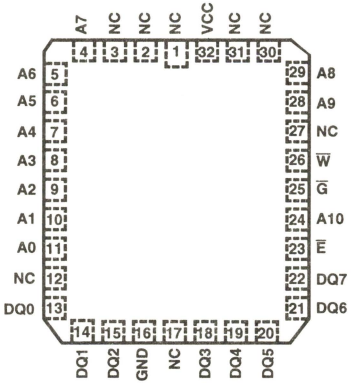
120ns	200ns	TEMPERATURE RANGE	PACKAGE	PKG. NO.
HM1-6516B/883	HM1-6516/883	-55°C to 125°C	CERDIP	F24.6
HM4-6516B/883	-	-55°C to +125°C	CLCC	J32.A

Pinouts

HM-6516/883
(CERDIP)
TOP VIEW



HM-6516/883
(CLCC)
TOP VIEW



PIN	DESCRIPTION
NC	No Connect
A0 - A10	Address Inputs
$\overline{E}$	Chip Enable/Power Down
VSS/GND	Ground
DQ0 - DQ7	Data In/Data Out
VCC	Power (+5V)
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable

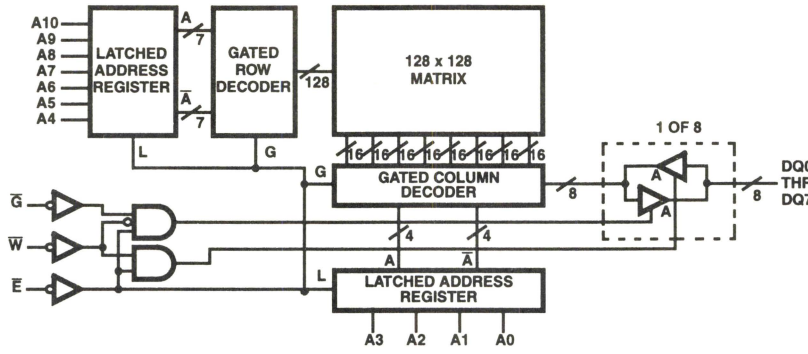
6 CMOS MEMORY

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **2999.1**

Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage Applied for all Grades . . . . . GND -0.3V to VCC +0.3V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	48°C/W	8°C/W
CLCC Package	66°C/W	12°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 25953 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . +2.4V to VCC
Data Retention Supply Voltage . . . . . 2.0V to 4.5V
Input Rise and Fall Time . . . . . 40ns Max

TABLE 1. HM-6516/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH	VCC = 4.5V IO = -1.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V IO = 3.2mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = $\overline{G}$ = 5.5 V, VIO = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	1.0	µA
Operating Supply Current	ICCOP	VCC = $\overline{G}$ = 5.5V, (Note 2) f = 1MHz, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-	10	mA
Standby Supply Current	ICCSB1	VCC = 5.5V, HM-6516/883 $\overline{E}$ = VCC-0.3V, IO = 0mA, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-	100	µA
		VCC = 5.5V, HM-6516B/883 $\overline{E}$ = VCC -0.3V, IO = 0mA, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-	50	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, HM-6516/883 $\overline{E}$ = VCC-0.3V, IO = 0mA, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-	50	µA
		VCC = 2.0V, HM-6516B/883 $\overline{E}$ = VCC-0.3V, IO = 0mA, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-	25	µA
Functional Test	FT	VCC = 4.5V (Note 3)	7, 8A, 8B	$-55°C \le T_A \le +125°C$	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.
3. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH ≥ 1.5V, and VOL ≤ 1.5V.

TABLE 2. HM-6514/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS				UNITS
					HM-6516B/883		HM-6516/883		
					MIN	MAX	MIN	MAX	
Chip Enable Access Time	(1) TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	200	ns
Address Access Time	(2) TAVQV	VCC = 4.5 and 5.5V, (Note 3)	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	200	ns
Chip Enable Pulse Negative Width	(9) TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	200	-	ns
Chip Enable Pulse Positive Width	(10) TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	50	-	80	-	ns
Address Set-up Time	(11) TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Address Hold Time	(12) TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	30	-	50	-	ns
Write Enable Pulse Width	(13) TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	200	-	ns
Write Enable Pulse Set-up Time	(14) TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	200	-	ns
Chip Selection to End of Write	(15) TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	200	-	ns
Data Set-up Time	(16) TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	50	-	80	-	ns
Data Hold Time	(17) TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	10	-	ns
Read or Write Cycle Time	(18) TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	170	-	280	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC -2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-6516/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	8	pF
		VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	12	pF
Input/Output Capacitance	CIO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	10	pF
		VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	14	pF
Chip Enable to Output Valid Time	(3) TELQX	VCC = 4.5 and 5.5V	1	$-55^oC \le T_A \le +125^oC$	10	-	ns
Write Enable Output Disable Time	(4) TWLQZ	VCC = 4.5 and 5.5V HM-6516/883	1	$-55^oC \le T_A \le +125^oC$	-	80	ns
		VCC = 4.5 and 5.5V HM-6516B/883	1	$-55^oC \le T_A \le +125^oC$	-	50	ns
Chip Enable Output Disable Time	(5) TEHQZ	VCC = 4.5 and 5.5V HM-6516/883	1	$-55^oC \le T_A \le +125^oC$	-	80	ns
		VCC = 4.5 and 5.5V HM-6516B/883	1	$-55^oC \le T_A \le +125^oC$	-	50	ns
Output Enable Access Time	(6) TGLQV	VCC = 4.5 and 5.5V	1	$-55^oC \le T_A \le +125^oC$	-	80	ns
Output Enable to Output Valid Time	(7) TGLQX	VCC = 4.5 and 5.5V	1	$-55^oC \le T_A \le +125^oC$	10	-	ns
Output Disable Time	(8) TGHQZ	VCC = 4.5 and 5.5V HM-6516/883	1	$-55^oC \le T_A \le +125^oC$	-	80	ns
		VCC = 4.5 and 5.5V HM-6516B/883	1	$-55^oC \le T_A \le +125^oC$	-	50	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to LCC device types only.
3. Applies to DIP device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Timing Waveforms

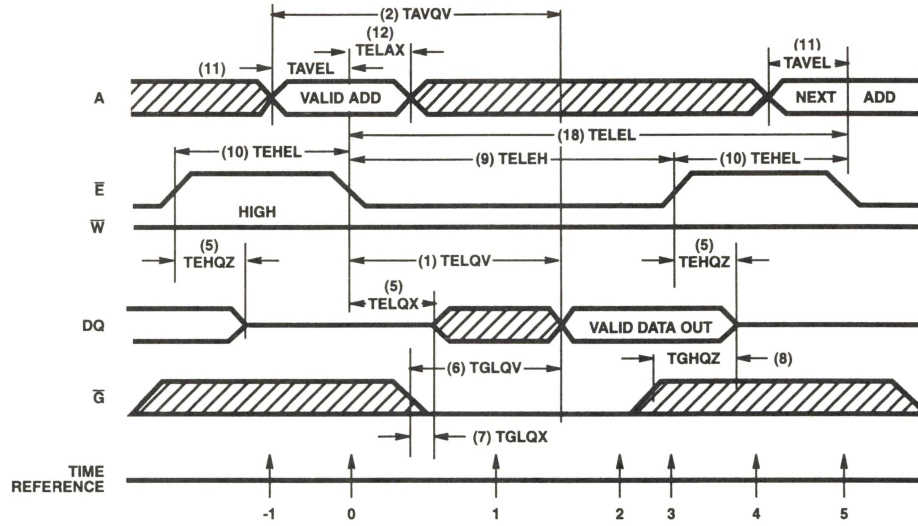


FIGURE 1. READ CYCLE

The address information is latched in the on-chip registers on the falling edge of $\overline{E}$ (T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2), $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical "1" state (T = -1, 0, 3, 4, 5). After (T = 4) time, the memory is ready for the next cycle.

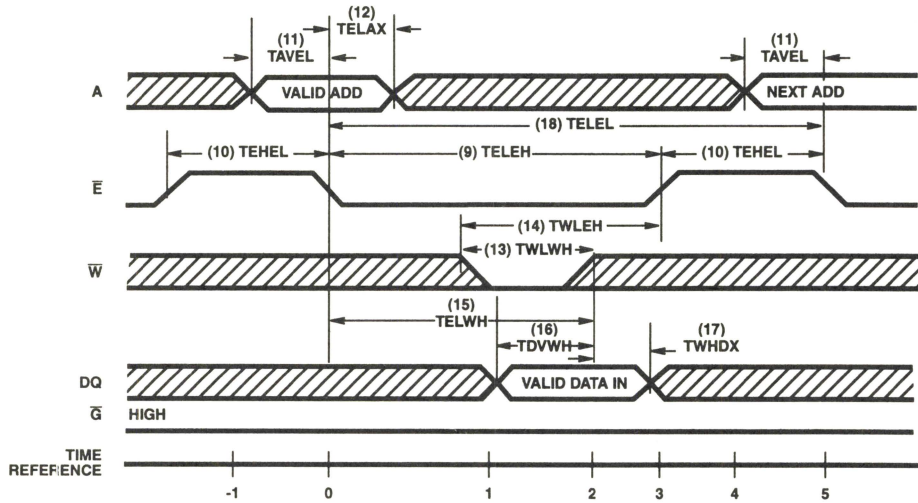
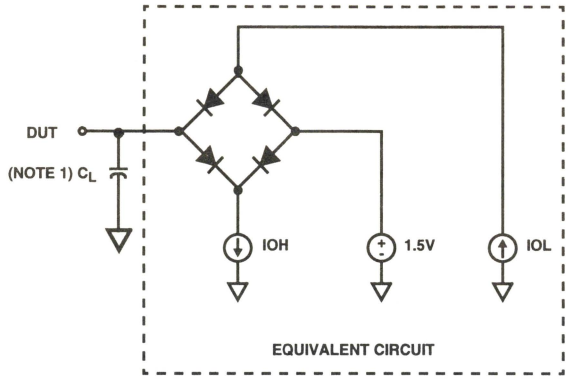


FIGURE 2. WRITE CYCLE

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on-chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or E (T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising of $\overline{E}$.

Test Circuit

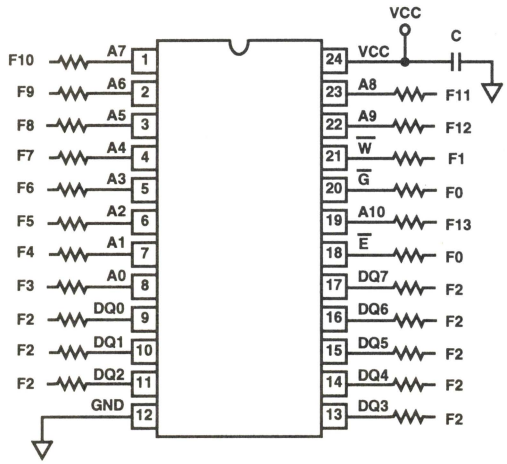


NOTE:

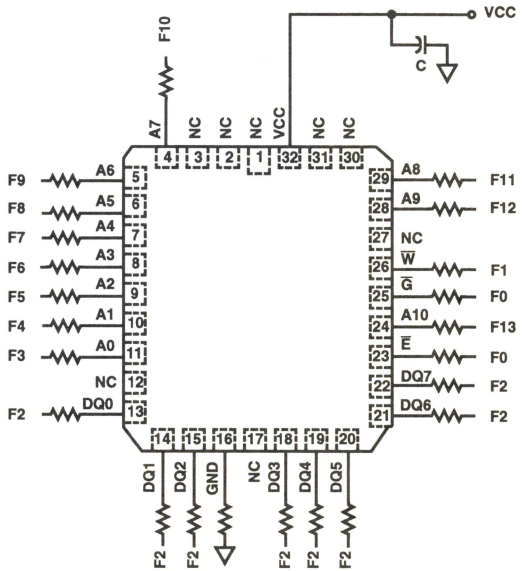
1. Test head capacitance includes stray and jig capacitance.

Burn-In Circuits

HM-6516/883
CERDIP
TOP VIEW



HM-6516/883
CLCC
TOP VIEW



NOTES:

All resistors 47kΩ ±5%.
F0 = 100kHz ±10%.
VCC = 5.5V ±0.5V.
VIH = 4.5V ±10%.
VIL = -0.2V to +0.4V.
C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
186.6 x 199.6 x 19 ±1mils

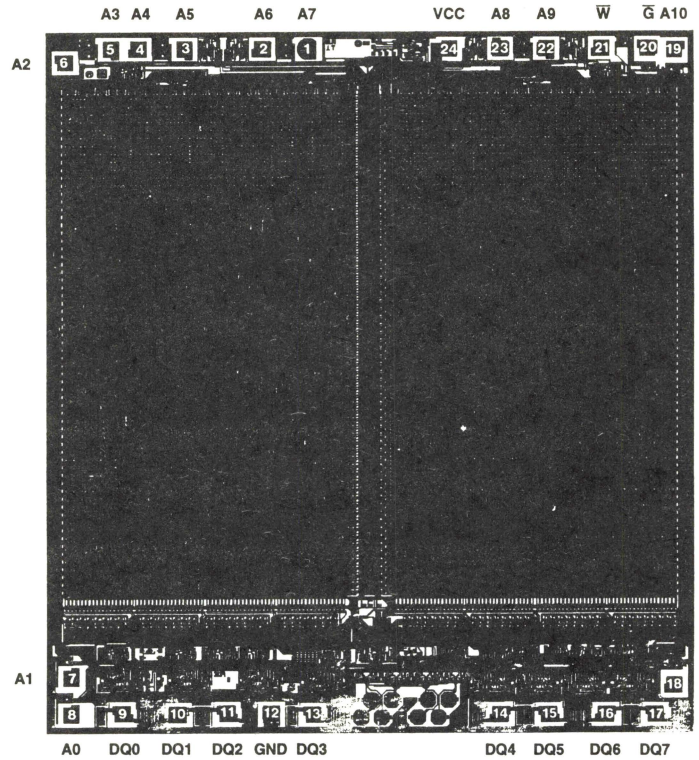
METALLIZATION:
Type: Si - Al
Thickness: 9kÅ - 13kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 7kÅ ±9kÅ

WORST CASE CURRENT DENSITY:
0.5 x 10^5 A/cm^2

Metallization Mask Layout

HM-6516/883



HARRIS SEMICONDUCTOR

HM-65162

2K x 8 Asynchronous CMOS Static RAM

March 1997

Features

- Fast Access Time. . . . . 70/90ns Max
- Low Standby Current. . . . . .50µA Max
- Low Operating Current . . . . . 70mA Max
- Data Retention at 2.0V. . . . . .20µA Max
- TTL Compatible Inputs and Outputs
- JEDEC Approved Pinout (2716, 6116 Type)
- No Clocks or Strobes Required
- Equal Cycle and Access Time
- Single 5V Supply
- Gated Inputs
- No Pull-Up or Pull-Down Resistors Required

Description

The HM-65162 is a CMOS 2048 x 8 Static Random Access Memory manufactured using the Harris Advanced SAJI V process. The device utilizes asynchronous circuit design for fast cycle time and ease of use. The pinout is the JEDEC 24 pin DIP, and 32 pad 8-bit wide standard which allows easy memory board layouts flexible to accommodate a variety of industry standard PROMs, RAMs, ROMs and EPROMs. The HM-65162 is ideally suited for use in microprocessor based systems with its 8-bit word length organization. The convenient output enable also simplifies the bus interface by allowing the data outputs to be controlled independent of the chip enable. Gated inputs lower operating current and also eliminate the need for pull-up or pull-down resistors.

Ordering Information

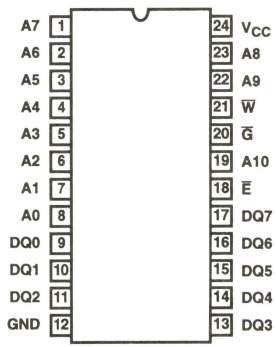
PACKAGE	TEMP. RANGE	70ns/20µA (NOTE 1)	90ns/40µA (NOTE 1)	90ns/300µA (NOTE 1)	PKG. NO.
CERDIP	-40°C to +85°C	HM1-65162B-9	HM1-65162-9	HM1-65162C-9	F24.6
JAN#	-55°C to +125°C	29110BJA	29104BJA	-	F24.6
SMD#	-55°C to +125°C	8403606JA	8403602JA	8403603JA	F24.6
CLCC	-40°C to +85°C	HM4-65162B-9	HM4-65162-9	HM4-65162C-9	J32.A
SMD#	-55°C to 125°C	8403606ZA	8403602ZA	8403603ZA	J32.A

NOTE:

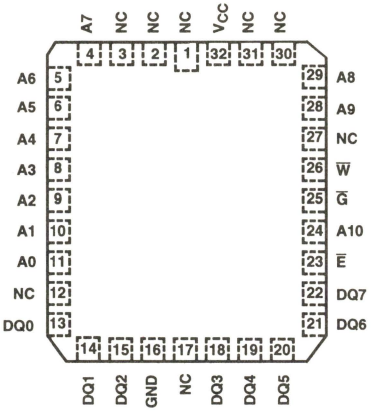
1. Access time/data retention supply current.

Pinouts

HM-65162
(CERDIP)
TOP VIEW



HM-65162
(CLCC)
TOP VIEW



PIN	DESCRIPTION
NC	No Connect
A0 - A10	Address Input
$\overline{E}$	Chip Enable/Power Down
V_{SS}/GND	Ground
DQ0 - DQ7	Data In/Data Out
V_{CC}	Power (+5V)
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable

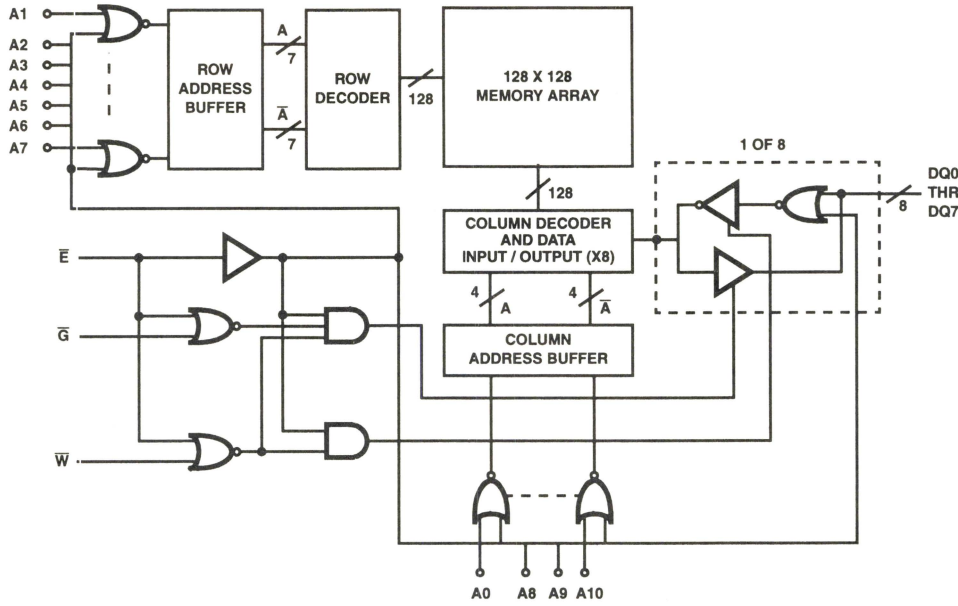
6 CMOS MEMORY

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3000.1**

Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
Typical Derating Factor . . . . . 05mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
HM-65162S-9, HM-65162B-9,
HM-65162-9, HM65162C-9. . . . . -40°C to +85°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	48	8
CLCC Package	66	12

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature. . . . . +175°C
Maximum Lead Temperature (Soldering 10s). . . . . +300°C

Die Characteristics

Gate Count . . . . . 26000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-65162S-9, HM-65162B-9, HM-65162-9, HM-65162C-9)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current	-	50	µA	HM-65162B-9, IO = 0mA, $\overline{E}$ = V_{CC} - 0.3V, V_{CC} = 5.5V
		-	100	µA	HM-65162S-9, HM65162-9, IO = 0mA, $\overline{E}$ = V_{CC} - 0.3V, V_{CC} = 5.5V
		-	900	µA	HM-65162C-9, IO = 0mA, $\overline{E}$ = V_{CC} - 0.3V, V_{CC} = 5.5V
ICCSB	Standby Supply Current	-	8	mA	$\overline{E}$ = 2.2V, IO = 0mA, V_{CC} = 5.5V
ICCEN	Enabled Supply Current	-	70	mA	$\overline{E}$ = 0.8V, IO = 0mA, V_{CC} = 5.5V
ICCOP	Operating Supply Current (Note 1)	-	70	mA	$\overline{E}$ = 0.8V, IO = 0mA, f = 1MHz, V_{CC} = 5.5V
ICCDR	Data Retention Supply Current	-	20	µA	HM-65162B-9, IO = 0mA, V_{CC} = 2.0V, $\overline{E}$ = VCC - 0.3V
		-	40	µA	HM-65162S-9, HM-65162-9, IO = 0mA, V_{CC} = 2.0V, $\overline{E}$ = V_{CC} - 0.3V
		-	300	µA	HM-65162C-9, IO = 0mA, V_{CC} = 2.0V, $\overline{E}$ = V_{CC} - 0.3V
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = V_{CC} or GND, V_{CC} = 5.5V
V_{IL}	Input Low Voltage	-0.3	0.8	V	V_{CC} = 4.5V
V_{IH}	Input High Voltage	2.2	V_{CC} +0.3	V	V_{CC} = 5.5V
VOL	Output Low Voltage	-	0.4	V	IO = 4.0mA, V_{CC} = 4.5V
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA, V_{CC} = 4.5V
VOH2	Output High Voltage (Note 2)	V_{CC} -0.4	-	V	IO = -100µA, V_{CC} = 4.5V

Capacitance T_A = +25°C

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	10	pF	f = 1MHz, All measurements are referenced to device GND
CIO	Input/Output Capacitance (Note 2)	12	pF	

NOTES:

1. Typical derating 5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

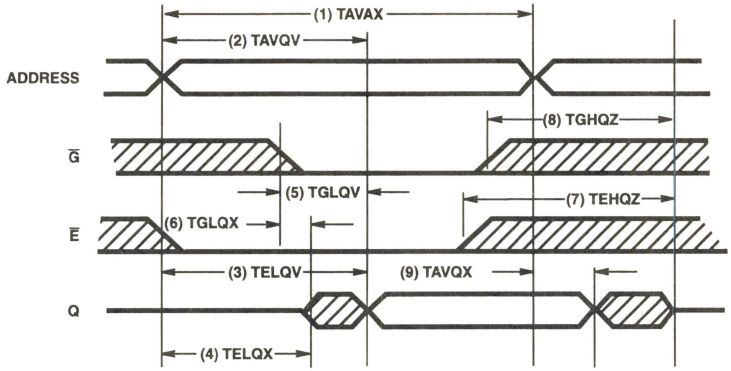
AC Electrical Specifications V_{CC} = 5V ±10%, T_A = -40°C to +85°C (HM-65162S-9, HM-65162B-9, HM65162-9, HM-65162C-9)

SYMBOL	PARAMETER	LIMITS								UNITS	CONDITIONS
		HM-65162S-9		HM-65162B-9		HM-65162-9		HM-65162C-9			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE											
(1) TAVAX	Read Cycle Time	55	-	70	-	90	-	90	-	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	55	-	70	-	90	-	90	ns	(Notes 1, 3, 4)
(3) TELQV	Chip Enable Access Time	-	55	-	70	-	90	-	90	ns	(Notes 1, 3)
(4) TELQX	Chip Enable Output Enable Time	5	-	5	-	5	-	5	-	ns	(Notes 2, 3)
(5) TGLQV	Output Enable Access Time	-	35	-	50	-	65	-	65	ns	(Notes 1, 3)
(6) TGLQX	Output Enable Output Enable Time	5	-	5	-	5	-	5	-	ns	(Notes 2, 3)
(7) TEHQZ	Chip Enable Output Disable Time	-	35	-	35	-	50	-	50	ns	(Notes 2, 3)
(8) TGHQZ	Output Enable Output Disable Time	-	30	-	35	-	40	-	40	ns	(Notes 2, 3)
(9) TAVQX	Output Hold From Address Change	5	-	5	-	5	-	5	-	ns	(Notes 1, 3)
WRITE CYCLE											
(10) TAVAX	Write Cycle Time	55	-	70	-	90	-	90	-	ns	(Notes 1, 3)
(11) TELWH	Chip Selection to End of Write	45	-	45	-	55	-	55	-	ns	(Notes 1, 3)
(12) TAVWL	Address Setup Time	5	-	10	-	10	-	10	-	ns	(Notes 1, 3)
(13) TWLWH	Write Enable Pulse Width	40	-	40	-	55	-	55	-	ns	(Notes 1, 3)
(14) TWHAX	Write Enable Read Setup Time	10	-	10	-	10	-	10	-	ns	(Notes 1, 3)
(15) TGHQZ	Output Enable Output Disable Time	-	30	-	35	-	40	-	40	ns	(Notes 2, 3)
(16) TWLQZ	Write Enable Output Disable Time	-	30	-	40	-	50	-	50	ns	(Notes 2, 3)
(17) TDVWH	Data Setup Time	25	-	30	-	30	-	30	-	ns	(Notes 1, 3)
(18) TWHDX	Data Hold Time	10	-	10	-	15	-	15	-	ns	(Notes 1, 3)
(19) TWHQX	Write Enable Output Enable Time	0	-	0	-	0	-	0	-	ns	(Notes 1, 3)
(20) TWLEH	Write Enable Pulse Setup Time	45	-	40	-	55	-	55	-	ns	(Notes 1, 3)
(21) TDVEH	Chip Enable Data Setup Time	25	-	30	-	30	-	30	-	ns	(Notes 1, 3)
(22) TAVWH	Address Valid to End of Write	45	-	50	-	65	-	65	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5 and 5.5V.
4. TAVQV = TELQV + TAVEL.

Timing Waveforms

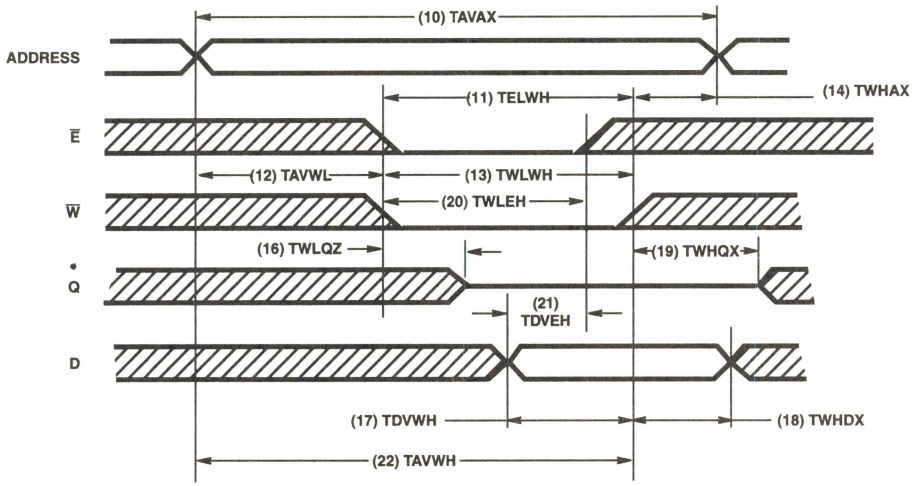


NOTE:

1. $\overline{W}$ is high for a Read Cycle.

FIGURE 1. READ CYCLE

Addresses must remain stable for the duration of the read cycle. To read, $\overline{G}$ and $\overline{E}$ must be $\leq V_{IL}$ and $\overline{W} \geq V_{IH}$. The output buffers can be controlled independently by $\overline{G}$ while $\overline{E}$ is low. To execute consecutive read cycles, $\overline{E}$ may be tied low continuously until all desired locations are accessed. When $\overline{E}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.



NOTE:

1. $\overline{G}$ is low throughout Write Cycle.

FIGURE 2. WRITE CYCLE I

To write, addresses must be stable, $\overline{E}$ low and $\overline{W}$ falling low for a period no shorter than TWLWH. Data in is referenced with the rising edge of $\overline{W}$, (TDVWH and TWHDX). While addresses are changing, $\overline{W}$ must be high. When $\overline{W}$ falls low, the I/O pins are still in the output state for a period of TWLQZ and input data of the opposite phase to the outputs must not be applied, (Bus contention). If $\overline{E}$ transitions low simultaneously with the $\overline{W}$ line transitioning low, or after the $\overline{W}$ transition, the output will remain in a high impedance state. $\overline{G}$ is held continuously low.

Timing Waveforms (Continued)

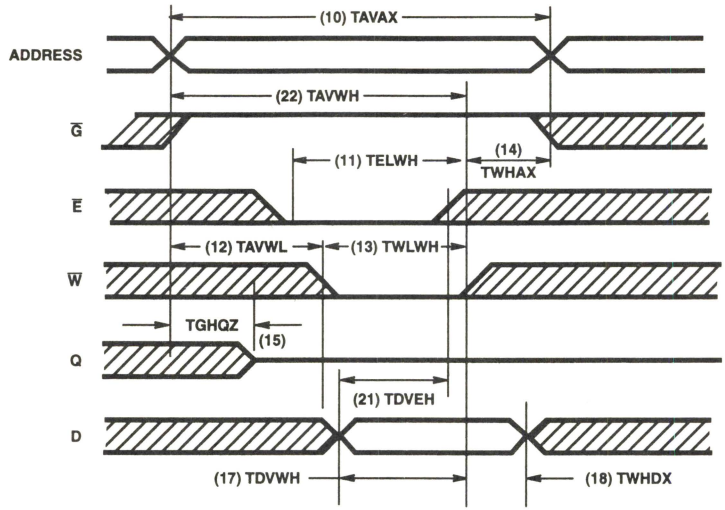


FIGURE 3. WRITE CYCLE II

In this write cycle $\overline{G}$ has control of the output after a period, TGHQZ. $\overline{G}$ switching the output to a high impedance state allows data in to be applied without bus contention after TGHQZ. When $\overline{W}$ transitions high, the data in can change after TWHDX to complete the write cycle.

Low Voltage Data Retention

Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within V_{CC} -0.3V to V_{CC} +0.3V.
2. On RAMs which have selects or output enables (e.g., S, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. Inputs which are to be held high (e.g., $\overline{E}$) must be kept between V_{CC} +0.3V and 70% of V_{CC} during the power up and down transitions.
4. The RAM can begin operation > 55ns after V_{CC} reaches the minimum operating voltage (4.5V).

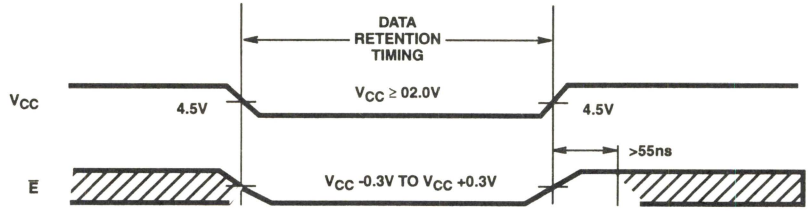


FIGURE 4. DATA RETENTION TIMING

Typical Performance Curve

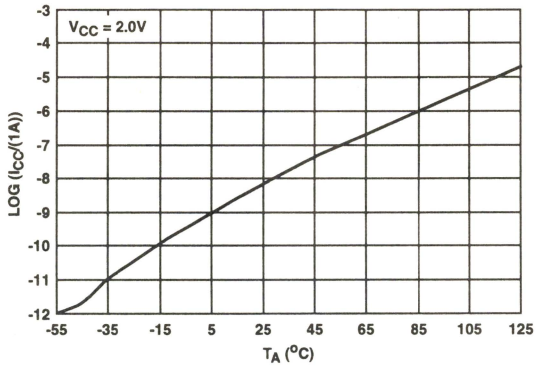


FIGURE 5. TYPICAL ICCDR vs T_A

HARRIS SEMICONDUCTOR

HM-65162/883

2K x 8 Asynchronous CMOS Static RAM

March 1997

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Fast Access Time. . . . . 70/90ns Max
- Low Standby Current. . . . . .50µA Max
- Low Operating Current . . . . . 70mA Max
- Data Retention at 2.0V. . . . . .20µA Max
- TTL Compatible Inputs and Outputs
- JEDEC Approved Pinout (2716, 6116 Type)
- No Clocks or Strobes Required
- Wide Temperature Range . . . . . -55°C to +125°C
- Equal Cycle and Access Time
- Single 5V Supply
- Gated Inputs
  - No Pull-Up or Pull-Down Resistors Required

Description

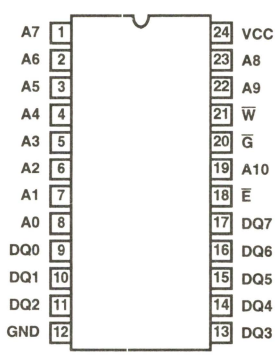
The HM-65162/883 is a CMOS 2048 x 8 Static Random Access Memory manufactured using the Harris Advanced SAJI V process. The device utilizes asynchronous circuit design for fast cycle time and ease of use. The pinout is the JEDEC 24 pin DIP, and 32 pad 8-bit wide standard which allows easy memory board layouts flexible to accommodate a variety of industry standard PROMs, RAMs, ROMs and EPROMs. The HM-65162/883 is ideally suited for use in microprocessor based systems with its 8-bit word length organization. The convenient output enable also simplifies the bus interface by allowing the data outputs to be controlled independent of the chip enable. Gated inputs lower operating current and also eliminate the need for pull-up or pull-down resistors.

Ordering Information

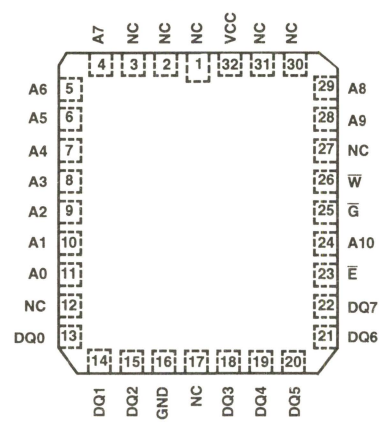
70ns/20µA	90ns/40µA	90ns/300µA	TEMP. RANGE	PACKAGE	PKG. NO.
HM1-65162B/883	HM1-65162/883	HM1-65162C/883	-55°C to 125°C	CERDIP	F24.6
HM4-65162B/883	HM4-65162/883	-	-55°C to 125°C	CLCC	J32.A

Pinouts

HM-65162/883 (CERDIP)
TOP VIEW



HM-65162/883 (CLCC)
TOP VIEW



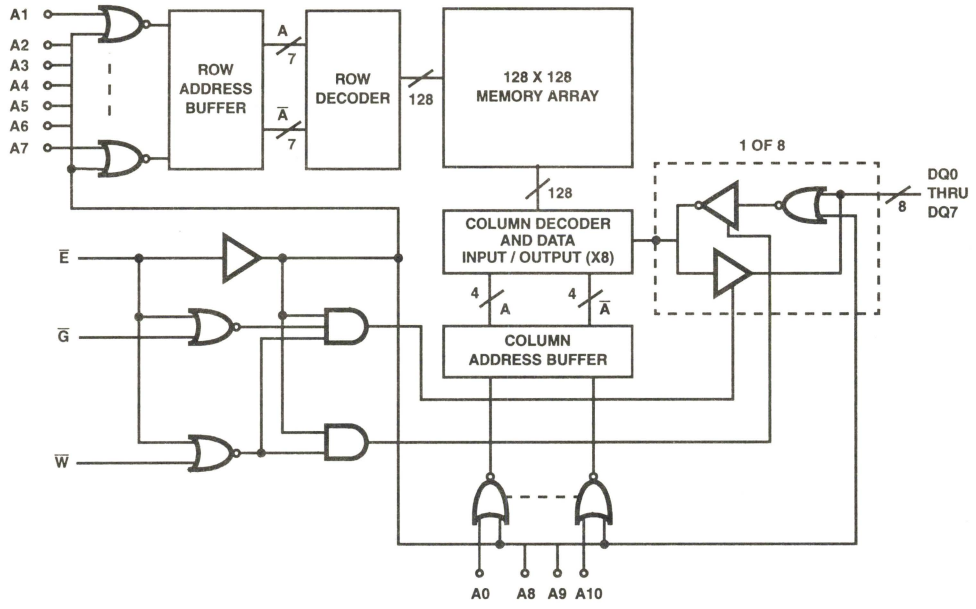
PIN	DESCRIPTION
NC	No Connect
A0 - A10	Address Input
$\overline{E}$	Chip Enable/Power Down
VSS/GND	Ground
DQ0 - DQ7	Data In/Data Out
VCC	Power (+5V)
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3001.1**

Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
Typical Derating Factor . . . . . 1.5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	48°C/W	8°C/W
CLCC Package	66°C/W	12°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 26000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . 0V to +0.8V
Chip Enable High/Low Time . . . . . 40ns (Min)
Input High Voltage . . . . . -2.2V to VCC
Data Retention Supply Voltage . . . . . 2.0V to 4.5V
Input Rise and Fall Time . . . . . 40ns Max

TABLE 1. 65162/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VCC = 4.5V, IO = -1.0mA	1, 2, 3	$-55^{\circ}C \le T_A \le +125^{\circ}C$	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 4.0mA	1, 2, 3	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 2.2V, or $\overline{E}$ = 2.2V, VI/O = GND or VCC	1, 2, 3	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-1.0	1.0	µA
Standby Supply Current	ICCSB1	HM-65162B/883, IO = 0mA, VCC = 5.5V, $\overline{E}$ = VCC -0.3V	1, 2, 3	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	50	µA
		HM-65162/883, IO = 0mA, VCC = 5.5V, $\overline{E}$ = VCC - 0.3V	1, 2, 3	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	100	µA
		HM-65162C/883, IO = 0mA, VCC = 5.5V, $\overline{E}$ = VCC - 0.3V	1, 2, 3	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	900	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 2.2V	1, 2, 3	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	8	mA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = 5.5V, (Note 2), f = 1MHz, $\overline{E}$ = 0.8V	1, 2, 3	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	70	mA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 0.8V	1, 2, 3	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	70	mA
Data Retention Supply Current	ICCDR	HM-65162B/883, IO = 0mA, VCC = 2.0V, $\overline{E}$ = VCC - 0.3V	1, 2, 3	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	20	µA
		HM-65162/883, IO = 0mA, VCC = 2.0V, $\overline{E}$ = VCC - 0.3V	1, 2, 3	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	40	µA
		HM-65162C/883, IO = 0mA, VCC = 2.0V, $\overline{E}$ = VCC - 0.3V	1, 2, 3	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	300	µA
Functional Test	FT	VCC = 4.5V (Note 3)	7, 8A, 8B	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC - 2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 2. HM-65162/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS						UNITS
					HM-65162B /883		HM-65162 /883		HM-65162C /883		
					MIN	MAX	MIN	MAX	MIN	MAX	
Read/Write/ Cycle Time	(1) TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	70	-	90	-	90	-	ns
Address Access Time	(2) TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	70	-	90	-	90	ns
Chip Enable Access Time	(3) TELQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	70	-	90	-	90	ns
Output Enable Access Time	(5) TGLQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	50	-	65	-	65	ns
Chip Selection to End of Write	(11) TELWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	45	-	55	-	55	-	ns
Address Setup Time	(12) TAVWL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	10	-	10	-	ns
Write Enable Pulse Write	(13) TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	55	-	55	-	ns
Write Enable Read Setup Time	(14) TWHAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	10	-	10	-	ns
Data Setup Time	(17) TDVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	30	-	30	-	ns
Data Hold Time	(18) TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	15	-	15	-	ns
Write Enable Pulse Setup Time	(20) TWLEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	55	-	55	-	ns
Chip Enable Data Setup Time	(21) TDVEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	30	-	30	-	ns
Address Valid to End of Write	(22) TAVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	65	-	65	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC -2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-65162/883 ELECTRICAL PERFORMANCE SPECIFICATIONS, AC AND DC

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS						UNITS
					HM-65162B/883		HM-65162/883		HM-65162C/883		
					MIN	MAX	MIN	MAX	MIN	MAX	
Input Capacitance	CIN	VCC = Open, F = 1MHz, All Measurements Referenced To Device Ground	1, 2	+25°C	-	10	-	10	-	10	pF
			1, 3	+25°C	-	8	-	8	-	8	pF
I/O Capacitance	CI/O	VCC = Open, F = 1MHz, All Measurements Referenced To Device Ground	1, 2	+25°C	-	12	-	12	-	12	pF
			1, 3	+25°C	-	10	-	10	-	10	pF
Chip Enable to Output ON	(4) TELQX	VCC = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	5	-	0	-	5	-	ns
Output Enable to Output ON	(6) TGLQX	VCC = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	5	-	5	-	5	-	ns
Chip Enable High to Output In High Z	(7) TEHQZ	VCC = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	-	35	-	50	-	50	ns
Output Disable to Output in High Z	(8) TGHQZ	VCC = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	-	35	-	40	-	40	ns
Output Hold from Address Change	(9) TAVQX	VCC = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	5	-	5	-	5	-	ns
Write Enable to Output in High Z	(16) TWLQZ	VCC = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	-	40	-	50	-	50	ns
Write Enable High to Output ON	(19) TWHQX	VCC = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	0	-	0	-	0	-	ns
Output High Voltage	VOH2	VCC = 4.5V, IO = -100µA	1	-55°C ≤ T_A ≤ +125°C	VCC - 0.4V	-	VCC - 0.4V	-	VCC - 0.4V	-	V

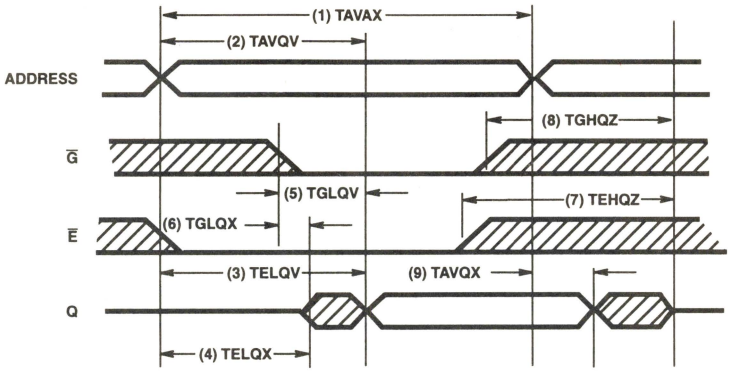
NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to LCC device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 7, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Timing Waveforms

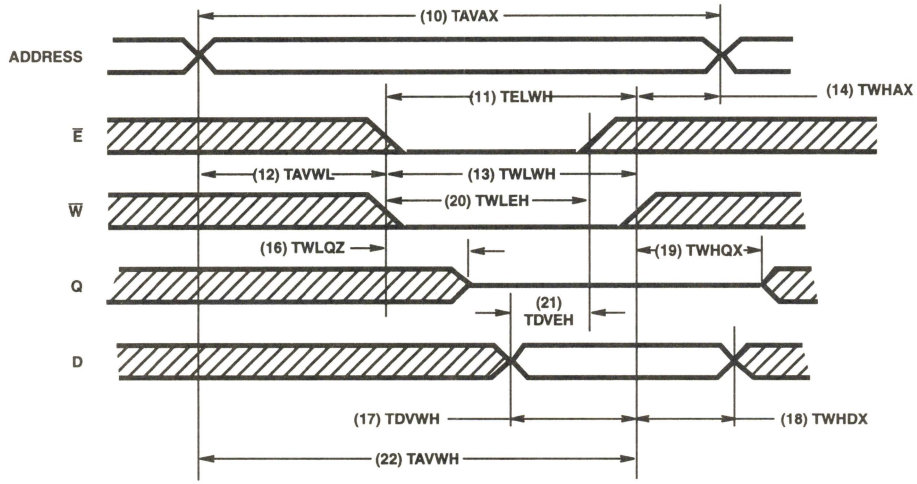


NOTE:

1. $\overline{W}$ is High for a Read Cycle.

FIGURE 1. READ CYCLE

Addresses must remain stable for the duration of the read cycle. To read, $\overline{G}$ and $\overline{E}$ must be ≤ VIL and $\overline{W}$ ≥ VIH. The output buffers can be controlled independently by $\overline{G}$ while $\overline{E}$ is low. To execute consecutive read cycles, $\overline{E}$ may be tied low continuously until all desired locations are accessed. When $\overline{E}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.



NOTE:

1. $\overline{G}$ is Low throughout Write Cycle.

FIGURE 2. WRITE CYCLE I

To write, addresses must be stable, $\overline{E}$ low and $\overline{W}$ falling low for a period no shorter than TWLWH. Data in is referenced with the rising edge of $\overline{W}$, (TDVWH and TWHDX). While addresses are changing, $\overline{W}$ must be high. When $\overline{W}$ falls low, the I/O pins are still in the output state for a period of TWLQZ and input data of the opposite phase to the outputs must not be applied, (Bus contention). If $\overline{E}$ transitions low simultaneously with the $\overline{W}$ line transitioning low or after the $\overline{W}$ transition, the output will remain in a high impedance state. $\overline{G}$ is held continuously low.

Timing Waveforms (Continued)

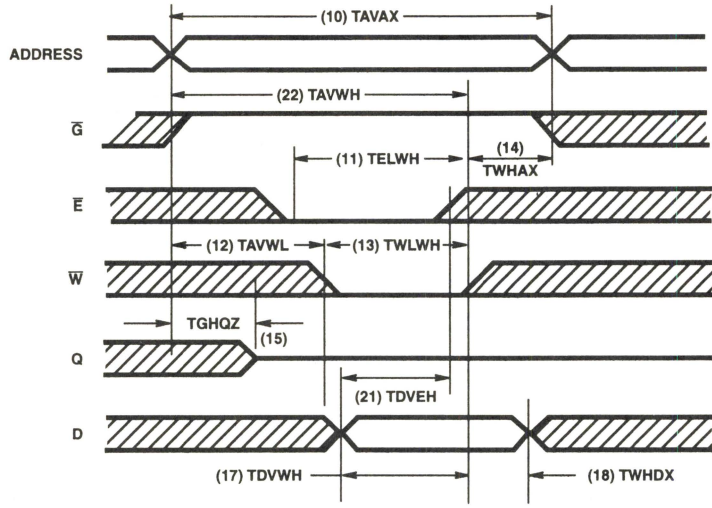


FIGURE 3. WRITE CYCLE II

In this write cycle $\overline{G}$ has control of the output after a period, TGHQZ. $\overline{G}$ switching the output to a high impedance state allows data in to be applied without bus contention after TGHQZ. When $\overline{W}$ transitions high, the data in can change after TWHDX to complete the write cycle.

Low Voltage Data Retention

Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaran teed over temperature. The following rules ensure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC -0.3V to VCC +0.3V.
2. On RAMs which have selects or output enables (e.g., S, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. Inputs which are to be held high (e.g., $\overline{E}$) must be kept between VCC +0.3V and 70% of VCC during the power up and down transitions.
4. The RAM can begin operation > 55ns after VCC reaches the minimum operating voltage (4.5V).

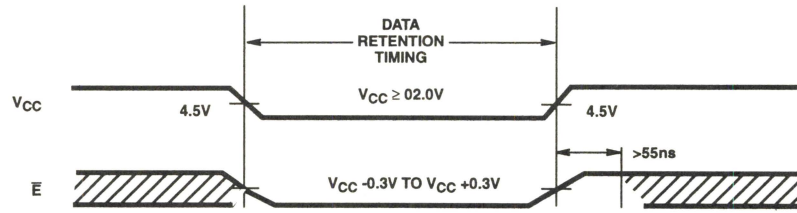
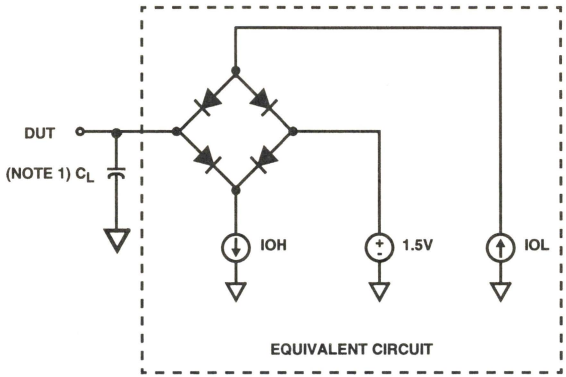


FIGURE 4. DATA RETENTION TIMING

Test Circuit

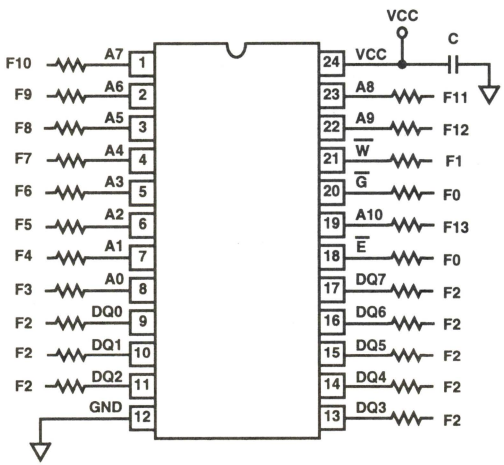


NOTE:

1. Test head capacitance includes stray and jig capacitance.

Burn-In Circuits

HM-65162/883
CERDIP
TOP VIEW



NOTES:

All resistors 47kW ±5%.

F0 = 100kHz ±10%.

F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F13 = F12 ÷ 2.

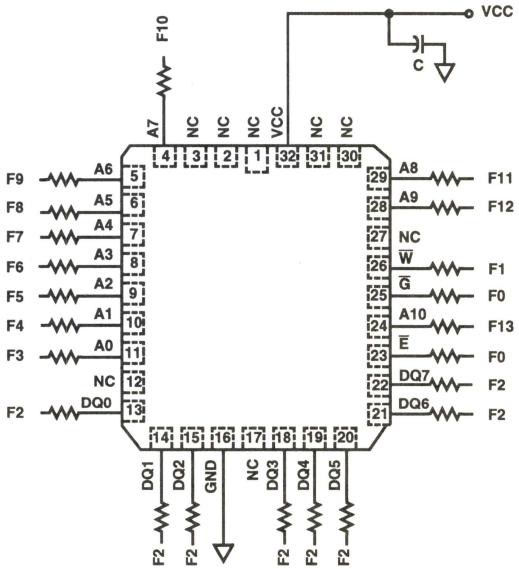
VCC = 5.5V ±0.5V.

VIH = 4.5V ±10%.

VIL = -0.2V to +0.4V.

C = 0.01µF Min.

HM-65162/883
CLCC
TOP VIEW



NOTES:

All resistors 47kW ±5%.

F0 = 100kHz ±10%.

F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F13 = F12 ÷ 2.

VCC = 5.5V ±0.5V.

VIH = 4.5V ±10%.

VIL = -0.2V to +0.4V.

C = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
180.3 x 194.9 x 19 ±1mils

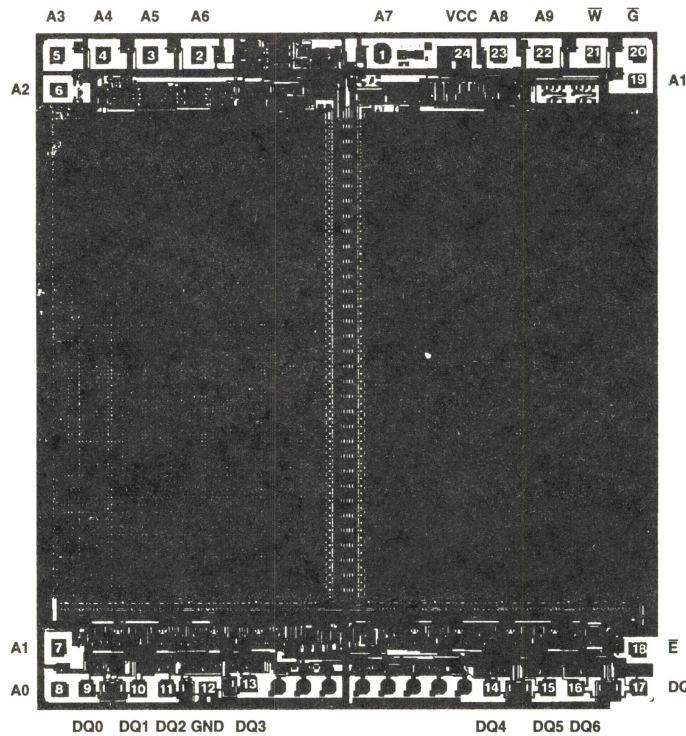
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
1.7×10^5 A/cm^2

Metallization Mask Layout

HM-65162/883



HARRIS SEMICONDUCTOR

HM-65262

16K x 1 Asynchronous CMOS Static RAM

March 1997

Features

- **Fast Access Time. . . . . 70/85ns Max**
- **Low Standby Current. . . . . .50µA Max**
- **Low Operating Current . . . . . 50mA Max**
- **Data Retention at 2.0V. . . . . .20µA Max**
- **TTL Compatible Inputs and Outputs**
- **JEDEC Approved Pinout**
- **No Clocks or Strobes Required**
- **Temperature Range . . . . . +55°C to +125°C**
- **Equal Cycle and Access Time**
- **Single 5V Supply**
- **Gated Inputs-No Pull-Up or Pull-Down Resistors Required**

Description

The HM-65262 is a CMOS 16384 x 1-bit Static Random Access Memory manufactured using the Harris Advanced SAJI V process. The device utilizes asynchronous circuit design for fast cycle times and ease of use. The HM-65262 is available in both JEDEC standard 20 pin, 0.300 inch wide CERDIP and 20 pad CLCC packages, providing high board-level packing density. Gated inputs lower standby current, and also eliminate the need for pull-up or pull-down resistors.

The HM-65262, a full CMOS RAM, utilizes an array of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T RAM cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor (4T) devices.

Ordering Information

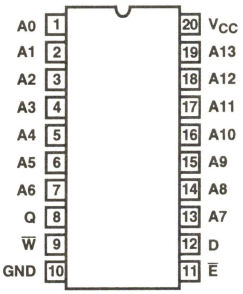
PACKAGE	TEMP. RANGE	70ns/20µA (NOTE 1)	85ns/20µA (NOTE 1)	(NOTE 1) 85ns/400µA	PKG. NO.
CERDIP	-40°C to +85°C	HM1-65262B-9	HM1-65262-9	-	F20.3
JAN #	-55°C to +125°C	29109BRA	29103BRA	-	F20.3
SMD#	-55°C to +125°C	8413203RA	8413201RA	-	F20.3
CLCC (SMD#)	-55°C to +125°C	8413203YA	8413201YA	-	J20.C

NOTE:

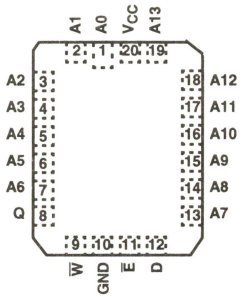
1. Access Time/Data Retention Supply Current.

Pinouts

HM-65262 (CERDIP)
TOP VIEW



HM-65262 (CLCC)
TOP VIEW



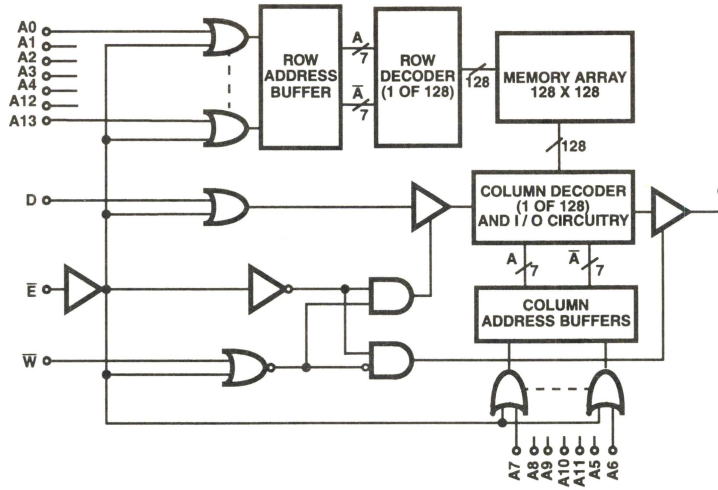
A0 - A13	Address Input
$\overline{E}$	Chip Enable/Power Down
Q	Data Out
D	Data In
V_{SS}/GND	Ground
V_{CC}	Power (+5)
$\overline{W}$	Write Enable

6 CMOS MEMORY

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **3002.2**

Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage Applied for all grades . . . . . -0.3V to V_{CC} +0.3V
Typical Derating Factor . . . . . .5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package	$66^oC/W$	$13^oC/W$
CLCC Package	$75^oC/W$	$18^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature . . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 26256 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V

Operating Temperature Range
HM-65262B-9, HM-65262-9, HM-65262C-9 . . . . . -40^oC to $+85^oC$

DC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40^oC to $+85^oC$ (HM-65262B-9, HM-65262-9, HM-65262C-9)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current	-od	50	µA	HM-65262B-9, HM-65262-9, IO = 0mA, $\overline{E}$ = V_{CC} -0.3V, V_{CC} = 5.5V
		-	900	µA	HM-65262C-9, IO = 0mA, $\overline{E}$ = V_{CC} -0.3V, V_{CC} = 5.5V
ICCSB	Standby Supply Current	-	5	mA	$\overline{E}$ = 2.2V, IO = 0mA, V_{CC} = 5.5V
ICCEN	Enabled Supply Current	-	50	mA	$\overline{E}$ = 0.8V, IO = 0mA, V_{CC} = 5.5V
ICCOP	Operating Supply Current (Note 1)	-	50	mA	$\overline{E}$ = 0.8V, IO = 0mA, f = 1MHz, V_{CC} = 5.5V
ICCDR	Data Retention Supply Current	-	20	µA	HM-65262B-9, HM-65262-9, V_{CC} = 2.0V, $\overline{E}$ = V_{CC}
		-	400	µA	HM-65262C-9, V_{CC} = 2.0V, $\overline{E}$ = V_{CC}
ICCDR1	Data Retention Supply Current	-	30	µA	HM-65262B-9, HM-65262-9, V_{CC} = 3.0V, $\overline{E}$ = V_{CC}
		-	550	µA	HM-65262C-9, V_{CC} = 3.0V, $\overline{E}$ = V_{CC}
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IOZ	Output Leakage Current	-1.0	+1.0	µA	VIO = V_{CC} or GND, V_{CC} = 5.5V
VIL	Input Low Voltage	-0.3	0.8	V	V_{CC} = 4.5V
VIH	Input High Voltage	2.2	V_{CC} +0.3	V	V_{CC} = 5.5V
VOL	Output Low Voltage	-	0.4	V	IO = 8.0mA, V_{CC} = 4.5V
VOH1	Output High Voltage	2.4	-	V	IO = -4.0mA, V_{CC} = 4.5V
VOH2	Output High Voltage (Note 2)	V_{CC} -0.4	-	V	IO = -100µA, V_{CC} = 4.5V

Capacitance T_A = $+25^oC$

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	10	pF	f = 1MHz, All measurements are referenced to device GND
CIO	Input/Output Capacitance (Note 2)	12	pF	

NOTES:

1. Typical derating 5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

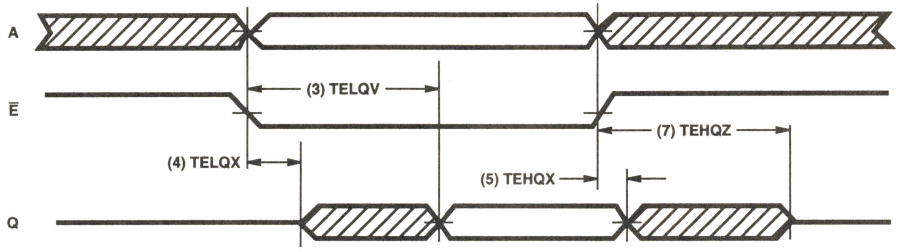
AC Electrical Specifications V_{CC} = 5V 10%, T_A = -40°C to +85°C (HM-65262B-9, HM-65262-9, HM-65262C-9)

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS
		HM-65262B-9		HM-65262-9		HM-65262C-9			
		MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE									
(1) TAVAX	Read/Cycle Time	70	-	85	-	85	-	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	70	-	85	-	85	ns	(Notes 1, 3)
(3) TELQV	Chip Enable Access Time	-	70	-	85	-	85	ns	(Notes 1, 3)
(4) TELQX	Chip Enable Output Enable Time	5	-	5	-	5	-	ns	(Notes 2, 3)
(5) TEHQX	Chip Disable Output Hold Time	5	-	5	-	5	-	ns	(Notes 2, 3)
(6) TAXQX	Address Invalid Output Hold Time	5	-	5	-	5	-	ns	(Notes 2, 3)
(7) TEHQZ	Chip Enable Output Disable Time	-	30	-	30	-	30	ns	(Notes 2, 3)
WRITE CYCLE									
(8) TAVAX	Write Cycle Time	70	-	85	-	85	-	ns	(Notes 1, 3)
(9) TELWH	Chip Selection to End of Write	55	-	65	-	65	-	ns	(Notes 1, 3)
(10) TWLWH	Write Enable Pulse Width	40	-	45	-	45	-	ns	(Notes 1, 3)
(11) TAVWL	Address Setup Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(12) TWHAX	Address Hold Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(13) TDVWH	Data Setup Time	30	-	35	-	35	-	ns	(Notes 1, 3)
(14) TWHDX	Data Hold Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(15) TWLQZ	Write Enable Output Disable Time	-	30	-	30	-	30	ns	(Notes 2, 3)
(16) TWHQX	Write Disable Output Enable Time	0	-	0	-	0	-	ns	(Notes 2, 3)
(17) TAVWH	Address Valid to End of Write	55	-	65	-	65	-	ns	(Notes 1, 3)
(18) TAVEL	Address Setup Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(19) TEHAX	Address Hold Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(20) TAVEH	Address Valid to End of Write	55	-	65	-	65	-	ns	(Notes 1, 3)
(21) TELEH	Enable Pulse Width	55	-	65	-	65	-	ns	(Notes 1, 3)
(22) TWLEH	Write Enable Pulse Setup Time	40	-	45	-	45	-	ns	(Notes 1, 3)
(23) TDVEH	Chip Setup Time	30	-	35	-	35	0	ns	(Notes 1, 3)
(24) TEHDX	Data Hold Time	0	-	0	-	0	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5 and 5.5V.

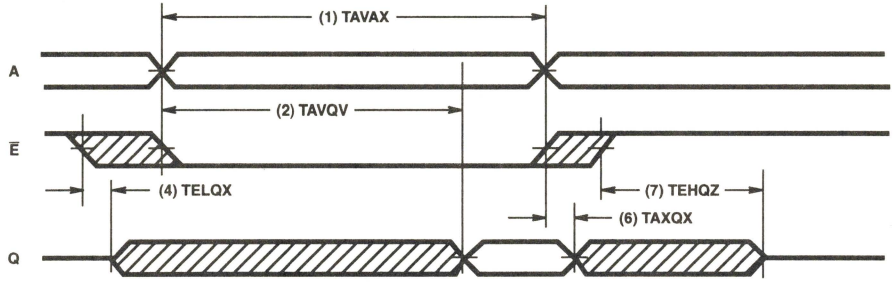
Timing Waveforms



NOTE:

1. $\overline{W}$ is high for entire cycle and D is ignored. Address is stable by the time $\overline{E}$ goes low and remains valid until $\overline{E}$ goes high.

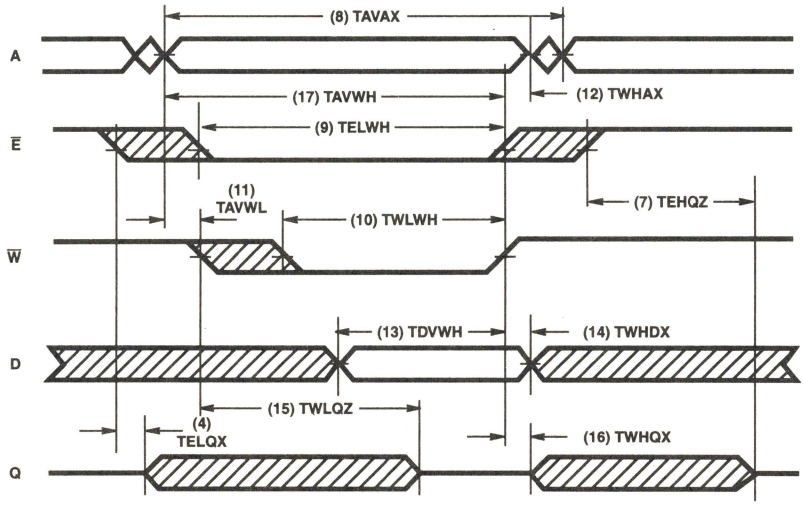
FIGURE 1. READ CYCLE 1: CONTROLLED BY $\overline{E}$



NOTE:

1. $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ is stable prior to A becoming valid and after A becomes invalid.

FIGURE 2. READ CYCLE 2: CONTROLLED BY ADDRESS

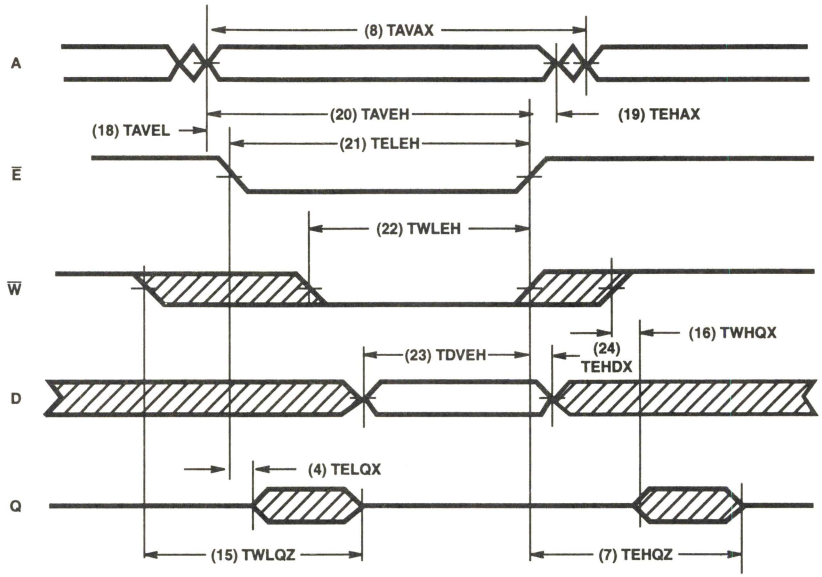


NOTE:

1. In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are low.

FIGURE 3. WRITE CYCLE 1: CONTROLLED BY $\overline{W}$ (LATE WRITE)

Timing Waveforms (Continued)



NOTE:

1. In this mode, $\overline{W}$ rises after $\overline{E}$. If W falls before $\overline{E}$ by a time exceeding TWLQZ (Max) TELQX (Min), and rises after $\overline{E}$ by a time exceeding TEHQZ (Max) TWHQZ (Min), then Q will remain in the high impedance state throughout the cycle.

FIGURE 4. WRITE CYCLE 2: CONTROLLED BY $\overline{E}$ (EARLY WRITE)

Low Voltage Data Retention

Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within V_{CC} to V_{CC} +0.3V.
2. On RAMs which have selects or output enables (e.g., S, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. Inputs which are to be held high (e.g., $\overline{E}$) must be kept between V_{CC} +0.3V and 70% of V_{CC} during the power up and down transitions.
4. The RAM can begin operation > 55ns after V_{CC} reaches the minimum operating voltage (4.5V).

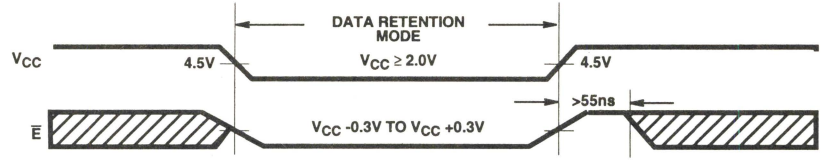


FIGURE 5. DATA RETENTION TIMING

Typical Performance Curve

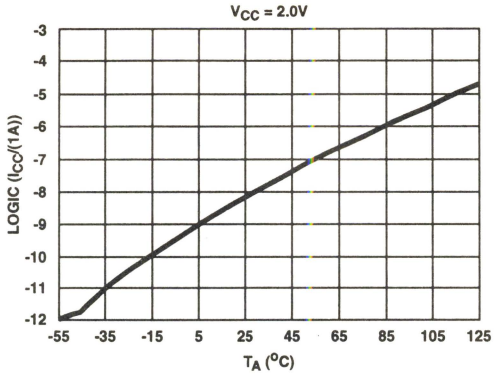


FIGURE 6. TYPICAL ICCDR vs T_A

HARRIS SEMICONDUCTOR

HM-65262/883

16K x 1 Asynchronous CMOS Static RAM

March 1997

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Fast Access Time. . . . . 70/85ns Max**
- **Low Standby Current. . . . . 50µA Max**
- **Low Operating Current . . . . . 50mA Max**
- **Data Retention at 2.0V. . . . . 20µA Max**
- **TTL Compatible Inputs and Outputs**
- **JEDEC Approved Pinout**
- **No Clocks or Strobes Required**
- **Temperature Range . . . . . +55°C to +125°C**
- **Gated Inputs-No Pull-Up or Pull-Down Resistors Required**
- **Equal Cycle and Access Time**
- **Single 5V Supply**

Description

The HM-65262/883 is a CMOS 16384 x 1-bit Static Random Access Memory manufactured using the Harris Advanced SAJI V process. The device utilizes asynchronous circuit design for fast cycle times and ease of use. The HM-65262/883 is available in both JEDEC Standard 20 pin, 0.300 inch wide CERDIP and 20 pad CLCC packages, providing high board-level packing density. Gated inputs lower standby current, and also eliminate the need for pull-up or pull-down resistors.

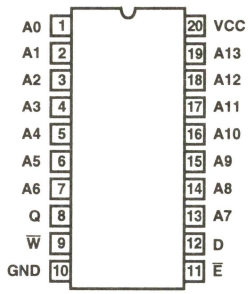
The HM-65262/883, a full CMOS RAM, utilizes an array of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T RAM cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor (4T) devices.

Ordering Information

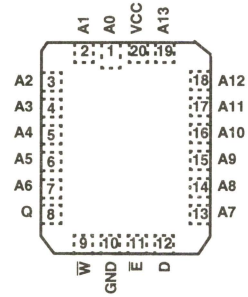
70ns/20µA	85ns/20µA	85ns/400µA	TEMP. RANGE	PACKAGE	PKG. NO.
-	HM1-65262/883	-	-55°C to +125°C	CERDIP	F20.3
HM4-65262B/883	HM4-65262/883	-	-55°C to +125°C	CLCC	J20.C

Pinouts

HM1-65262/883 (CERDIP)
TOP VIEW



HM-65262 (CLCC)
TOP VIEW



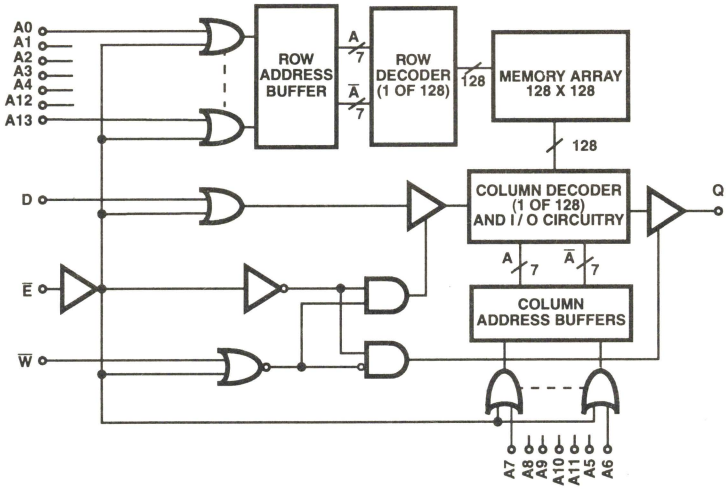
A0 - A13	Address Input
$\overline{E}$	Chip Enable/Power Down
Q	Data Out
D	Data In
VSS/GND	Ground
VCC	Power (+5)
$\overline{W}$	Write Enable

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3003.2**

Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage Applied for all Grades . . . . . -0.3V to VCC +0.3V
Typical Derating Factor . . . . . .5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package	66°C/W	13°C/W
CLCC Package	75°C/W	18°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 26256 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage (VIH) . . . . . ±2.2V to VCC
Data Retention Supply Voltage . . . . . 2.0V to 4.5V
Input Rise and Fall Time . . . . . 40ns Max.

TABLE 1. HM-65262/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

DC PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	MIN	MAX	UNITS
High Level Output Voltage	VOH1	VCC = 4.5V, IO = -4.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 8.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IOZ	VCC = 5.5V, $\overline{E}$ = 5.5V, VO = GND or VCC	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Standby Supply Current	ICCSB1	VCC = 5.5V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	50	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 2.2V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	5	mA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 2), f = 1MHz, $\overline{E}$ = 0.8V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	50	mA
Data Retention Supply Current	ICCDR	VCC = 2.0V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	20	µA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 0.8V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	50	mA
Functional Test	FT	VCC = 4.5V (Note 3)	7, 8A, 8B	-55°C ≤ T_A ≤ +125°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.
3. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH ≥ 1.5V, and VOL ≤ 1.5V.

TABLE 2. HM-65262/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

AC PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	HM-65262B/883 LIMITS		HM-65262/883 LIMITS		UNITS
					MIN	MAX	MIN	MAX	
Read/Write/Cycle Time	(1) TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	70	-	85	-	ns
Address Access Time	(2) TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	70	-	85	ns

TABLE 2. HM-65262/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested

AC PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	HM-65262B/883 LIMITS		HM-65262/883 LIMITS		UNITS
					MIN	MAX	MIN	MAX	
Chip Enable to End of Write	(3) TELWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	55	-	65	-	ns
Chip Enable Access Time	(4) TELQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	70	-	85	ns
Address Hold Time	(5) TWHAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Address Setup Time	(6) TAVWL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Address Valid to End of Write	(7) TAVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	55	-	65	-	ns
Address Setup Time	(8) TAVEL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Address Hold Time	(9) TEHAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Address Valid to End of Writes	(10) TAVEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	55	-	65	-	ns
Write Enable Pulse Write	(11) TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	45	-	ns
Data Setup Time	(12) TDVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	30	-	35	-	ns
Data Hold Time	(13) TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Enable Pulse Width	(14) TELEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	55	-	65	-	ns
Write to End of Write	(15) TWLEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	45	-	ns
Data Setup Time	(16) TDVEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	30	-	35	-	ns
Data Hold Time	(17) TEHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC -2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-65262/883 ELECTRICAL PERFORMANCE SPECIFICATIONS, AC AND DC

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CIN	VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	1, 2	$T_A = +25^oC$	-	10	pF
		VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	1, 3	$T_A = +25^oC$	-	6	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	1, 2	$T_A = +25^oC$	-	12	pF
		VCC = Open, f = 1MHz, All Measurements Referenced To Device Grounds	1, 3	$T_A = +25^oC$	-	8	pF

TABLE 3. HM-65262/883 ELECTRICAL PERFORMANCE SPECIFICATIONS, AC AND DC (Continued)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Write Enable to Output in High Z	(18) TWLQZ	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	-	40	ns
Write Enable High to Output ON	(19) TWHQX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	0	-	ns
Chip Enable to Output ON	(20) TELQX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	5	-	ns
Output Enable High to Output in High Z	(21) TE-HQZ	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	-	40	ns
Chip Disable to Output Hold Time	(22) TE-HQX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	5	-	ns
Address Invalid Output Hold Time	(23) TAX-QX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	5	-	ns
High Level Output Voltage	(24) VOH2	VCC = 4.5V, IO = -100mA	1	$-55^oC \le T_A \le +125^oC$-	VCC -0.4V	-	V

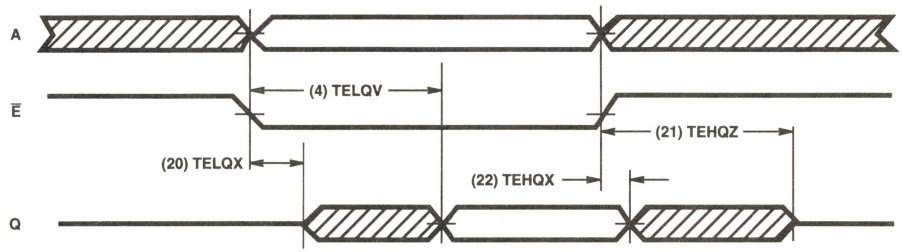
NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to LCC device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

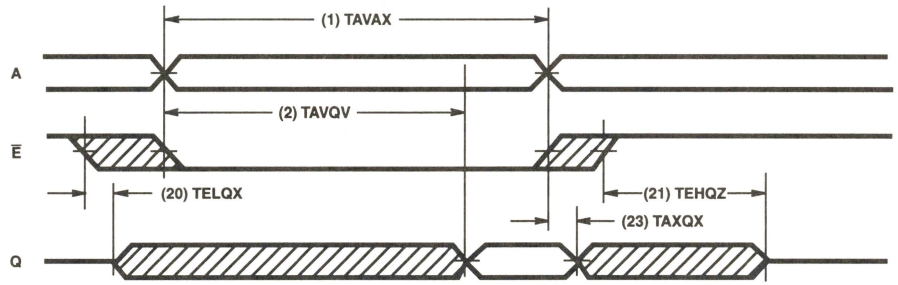
Timing Waveforms



NOTE:

1. $\overline{W}$ is high for entire cycle and D is ignored. Address is stable by the time $\overline{E}$ goes low and remains valid until $\overline{E}$ goes high.

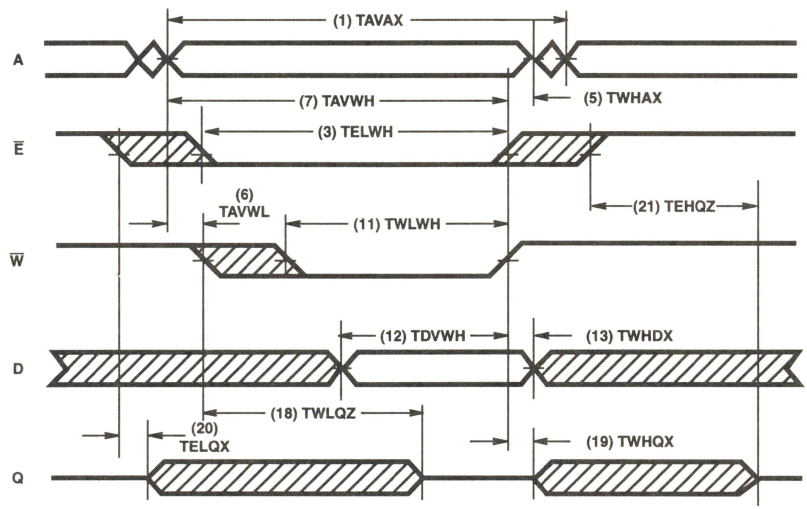
FIGURE 1. READ CYCLE 1: CONTROLLED BY $\overline{E}$



NOTE:

1. $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ is stable prior to A becoming valid and after A becomes invalid.

FIGURE 2. READ CYCLE 2: CONTROLLED BY ADDRESS

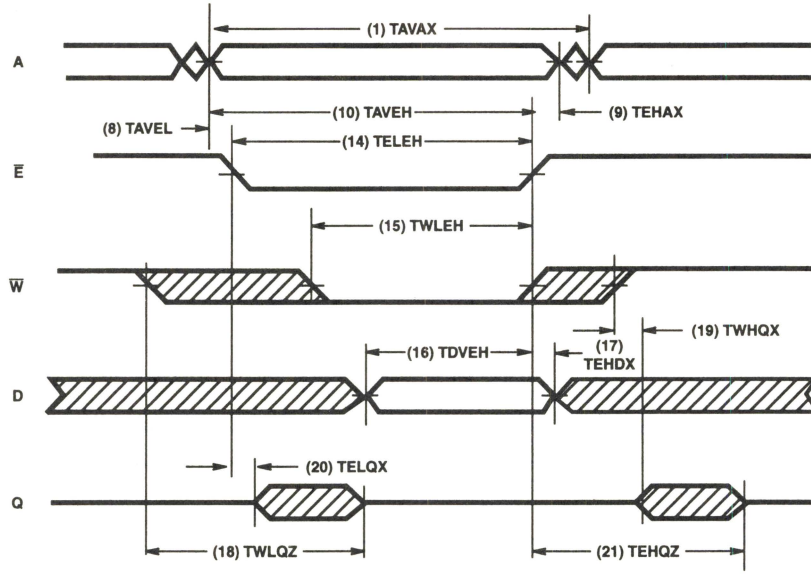


NOTE:

1. In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are low.

FIGURE 3. WRITE CYCLE 1: CONTROLLED BY $\overline{W}$ (LATE WRITE)

Timing Waveforms (Continued)



NOTE:

1. In this mode, $\overline{W}$ rises after $\overline{E}$. If W falls before $\overline{E}$ by a time exceeding TWLQZ (Max) TELQX (Min), and rises after $\overline{E}$ by a time exceeding TEHQZ (Max) TWHQZ (Min), then Q will remain in the high impedance state throughout the cycle.

FIGURE 4. WRITE CYCLE 2: CONTROLLED BY $\overline{E}$ (EARLY WRITE)

Low Voltage Data Retention

Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC to VCC +0.3V.
2. On RAMs which have selects or output enables (e.g., S, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. Inputs which are to be held high (e.g., $\overline{E}$) must be kept between VCC +0.3V and 70% of VCC during the power up and down transitions.
4. The RAM can begin operation >55ns after VCC reaches the minimum operating voltage (4.5V).

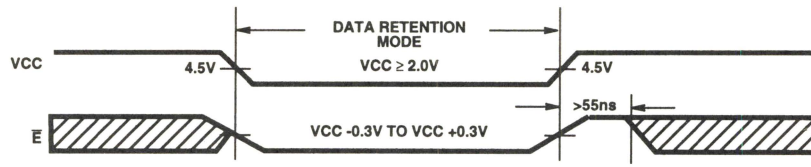
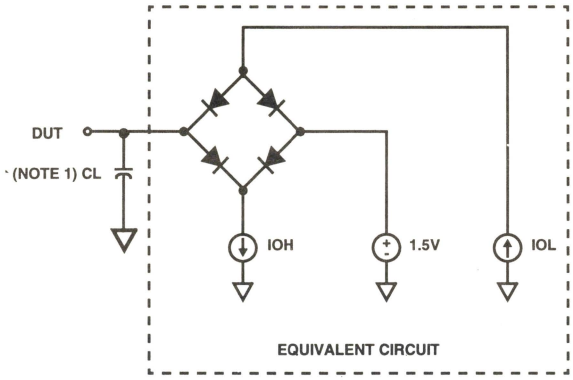


FIGURE 5. DATA RETENTION TIMING

Test Circuit

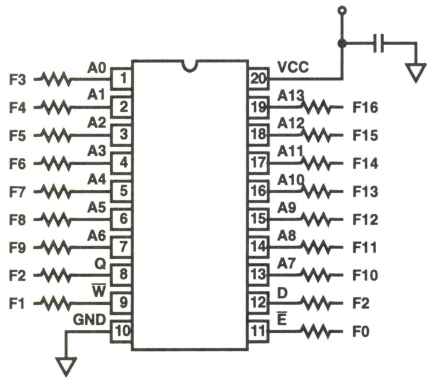


NOTE:

1. Test head capacitance includes stray and jig capacitance.

Burn-In Circuits

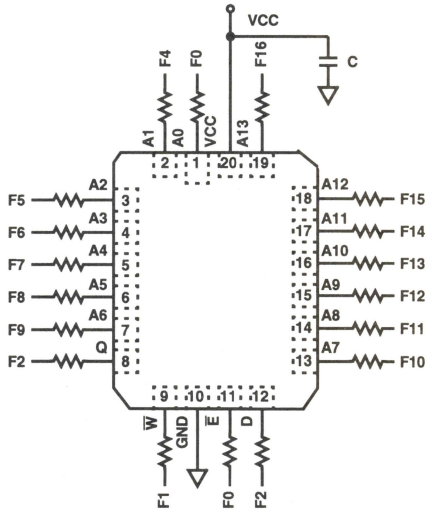
HM-65262/883
CERDIP
TOP VIEW



NOTES:

All resistors 47kΩ ±5%.
F0 = 100kHz ±10%.
F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F13 = F12 ÷ 2.
VCC = 5.5V ±0.5V.
VIH = 4.5V ±10%.
VIL = -0.2V to +0.4V.
C = 0.01µF Min.

HM-65262/883
CLCC
TOP VIEW



NOTES:

All resistors 47kΩ ±5%.
F0 = 100kHz ±10%.
F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F13 = F12 ÷ 2.
VCC = 5.5V ±0.5V.
VIH = 4.5V ±10%.
VIL = -0.2V to +0.4V.
C = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
148 x 187 x 19 mils

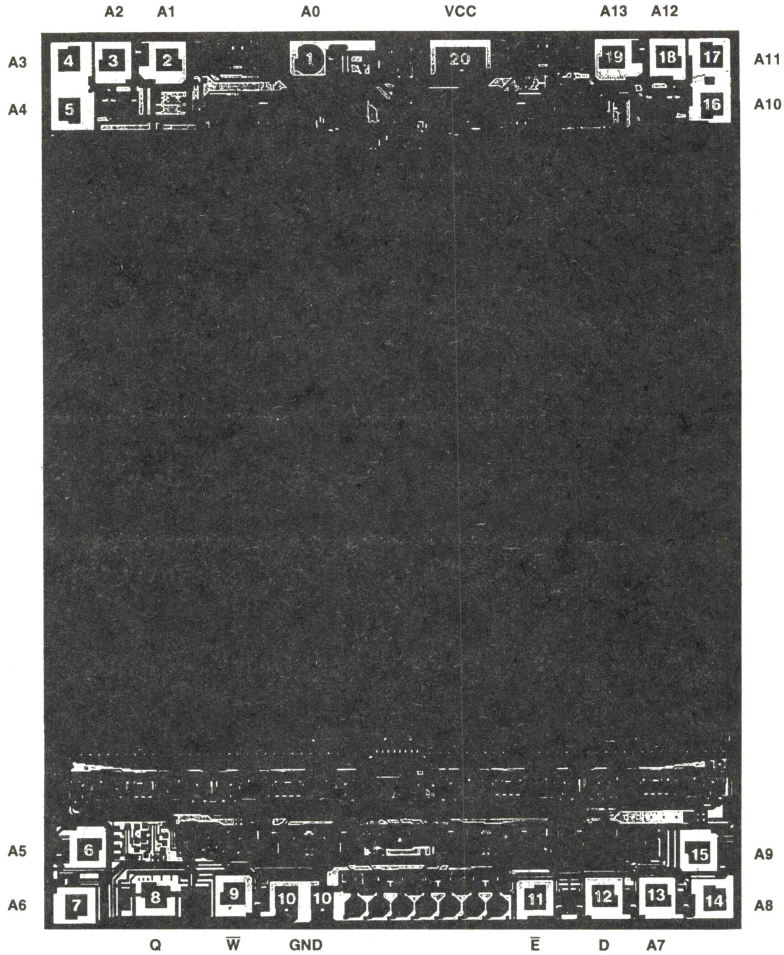
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
1.2×10^5 A/cm^2

Metallization Mask Layout

HM-65262/883



HARRIS SEMICONDUCTOR

HM-65642

8K x 8 Asynchronous CMOS Static RAM

March 1997

Features

- Full CMOS Design
- Six Transistor Memory Cell
- Low Standby Supply Current 100µA
- Low Operating Supply Current. 20mA
- Fast Address Access Time 150ns
- Low Data Retention Supply Voltage. 2.0V
- CMOS/TTL Compatible Inputs/Outputs
- JEDEC Approved Pinout
- Equal Cycle and Access Times
- No Clocks or Strobes Required
- Gated Inputs
- No Pull-Up or Pull-Down Resistors Required
- Easy Microprocessor Interfacing
- Dual Chip Enable Control

Description

The HM-65642 is a CMOS 8192 x 8-bit Static Random Access Memory. The pinout is the JEDEC 28 pin, 8-bit wide standard, which allows easy memory board layouts which accommodate a variety of industry standard ROM, PROM, EPROM, EEPROM and RAMs. The HM-65642 is ideally suited for use in microprocessor based systems. In particular, interfacing with the Harris 80C86 and 80C88 microprocessors is simplified by the convenient output enable ($\overline{G}$) input.

The HM-65642 is a full CMOS RAM which utilizes an array of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T RAM cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor or MIX-MOS (4T) devices.

Ordering Information

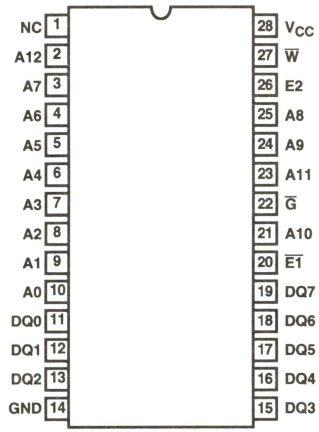
PACKAGE	TEMPERATURE RANGE	(NOTE 1) 150ns/75µA	(NOTE 1) 150ns/150µA	(NOTE 1) 200ns/250µA	PKG. NO.
CERDIP	-40°C to +85°C	-	HM1-65642-9	-	F28.6
JAN#	-55°C to +125°C	29205BXA	-	-	F28.6

NOTE:

1. Access Time/Data Retention Supply Current.

Pinout

HM-65642 (CERDIP)
TOP VIEW



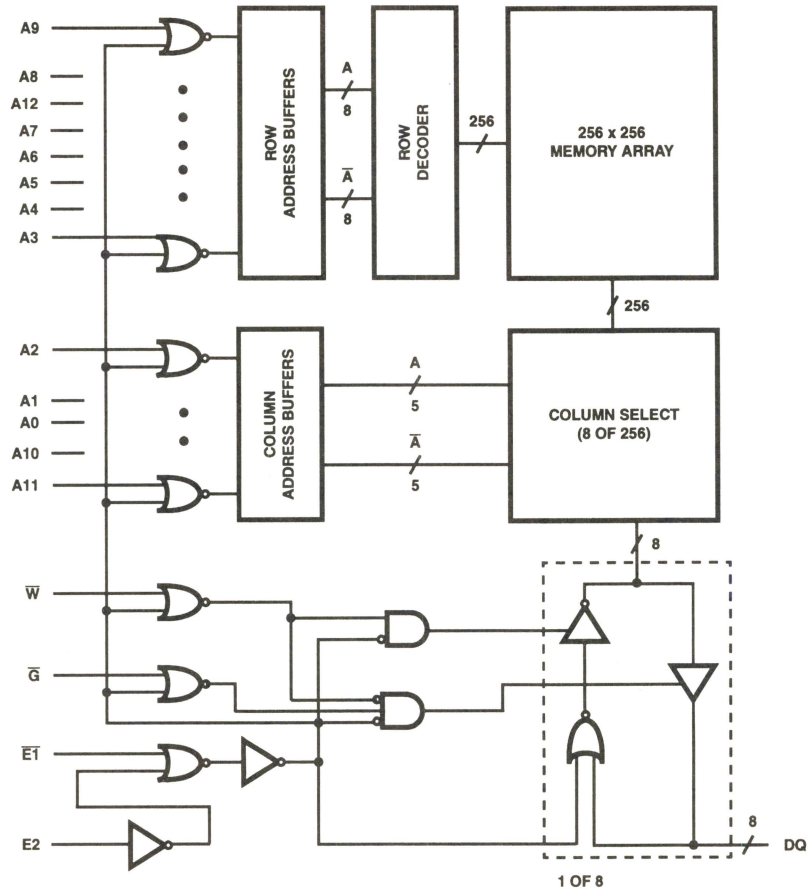
PIN	DESCRIPTION
A	Address Input
DQ	Data Input/Output
$\overline{E1}$	Chip Enable
E2	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
NC	No Connections
GND	Ground
V_{CC}	Power

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3005.1**

Functional Diagram



TRUTH TABLE

MODE	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$
Standby (CMOS)	X	GND	X	X
Standby (TTL)	V_{IH}	X	X	X
	X	V_{IL}	X	X
Enable (High Z)	V_{IL}	V_{IH}	V_{IH}	V_{IH}
Write	V_{IL}	V_{IH}	V_{IL}	X
Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage Applied for All Grades . . . . . GND -0.3V to V_{CC} +0.3V
Typical Derating Factor . . . . . 5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package	45°C/W	8°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 101,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
HM-65642-9 . . . . . -40°C to +85°C
Input Low Voltage . . . . . -0.3V to +0.8V
Input High Voltage . . . . . +2.2V to V_{CC} +0.3V

DC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-65642-9)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	-	250	µA	E2 = GND, V_{CC} = 5.5V
ICCSB2	Standby Supply Current (TTL)	-	5	mA	E2 = 0.8V or $\overline{E1}$ = 2.2V, V_{CC} = 5.5V
ICCDR	Data Retention Supply Current	-	150	µA	E2 = GND, V_{CC} = 2.0V
ICCEN	Enabled Supply Current	-	5	mA	E2 = 2.2V, $\overline{E1}$ = 0.8V, V_{CC} = 5.5V, IIO = 0mA
ICCOP	Operating Supply Current (Note 1)	-	20	mA	f = 1MHz, $\overline{E1}$ = 0.8V, E2 = 2.2V, V_{CC} = 5.5V, IIO = 0mA
II	Input Leakage Current	-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	E2 = GND, VIO = V_{CC} or GND, V_{CC} = 5.5V
VCCDR	Data Retention Supply Voltage	2.0	-	V	
VOH1	Output High Voltage	2.4	-	V	IOH = -1.0mA, V_{CC} = 4.5V
VOH2	Output High Voltage (Note 2)	V_{CC} -0.4	-	V	IOH = -100µA, V_{CC} = 4.5V
VOL	Output Low Voltage	-	0.4	V	IOL = 4.0mA, V_{CC} = 4.5V

Capacitance T_A = +25°C

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	12	pF	f = 1MHz, All measurements are referenced to device GND
CIO	Input/Output Capacitance (Note 2)	14	pF	

NOTES:

1. Typical derating 5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

AC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-65642-9)

SYMBOL	PARAMETER			LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
READ CYCLE							
(1) TAVAX	Read Cycle Time			150	-	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time			-	150	ns	(Notes 1, 3)
(3) TE1LQV	Chip Enable Access Time		$\overline{E1}$	-	150	ns	(Notes 2, 3)
(4) TE2HQV	Chip Enable Access Time		E2	-	150	ns	(Notes 1, 3)
(5) TGLQV	Output Enable Access Time			-	70	ns	(Notes 1, 3)
(6) TE1LQX	Chip Enable Valid to Output On		$\overline{E1}$	10	-	ns	(Notes 2, 3)
(7) TE2HQX	Chip Enable Valid to Output On		E2	10	-	ns	(Notes 2, 3)
(8) TGLQX	Output Enable Valid to Output On			5	-	ns	(Notes 2, 3)
(9) TE1HQZ	Chip Enable Not Valid to Output Off		$\overline{E1}$	-	50	ns	(Notes 2, 3)
(10) TE2LQZ	Chip Enable Not Valid to Output Off		E2	-	60	ns	(Notes 2, 3)
(11) TGHQZ	Output Enable Not Valid to Output Off			-	50	ns	(Notes 2, 3)
(12) TAXQX	Output Hold From Address Change			10	-	ns	(Notes 2, 3)
WRITE CYCLE							
(13) TAVAX	Write Cycle Time			150	-	ns	(Notes 1, 3)
(14) TWLWH	Write Pulse Width			90	-	ns	(Notes 1, 3)
(15) TE1LE1H	Chip Enable to End of Write		$\overline{E1}$	90	-	ns	(Notes 1, 3)
(16) TE2HE2L	Chip Enable to End of Write		E2	90	-	ns	(Notes 1, 3)
(17) TAVWL	Address Setup Time	Late Write		0	-	ns	(Notes 1, 3)
(18) TAVE1L	Address Setup Time	Early Write	$\overline{E1}$	0	-	ns	(Notes 1, 3)
(19) TAVE2H	Address Setup Time	Early Write	E2	0	-	ns	(Notes 1, 3)
(20) TWHAX	Write Recovery Time	Late Write		10	-	ns	(Notes 1, 3)
(21) TE1HAX	Write Recovery Time	Early Write	$\overline{E1}$	10	-	ns	(Notes 1, 3)
(22) TE2LAX	Write Recovery Time	Early Write	E2	10	-	ns	(Notes 1, 3)
(23) TDVWH	Data Setup Time	Late Write		60	-	ns	(Notes 1, 3)
(24) TDVE1H	Data Setup Time	Early Write	$\overline{E1}$	60	-	-	(Notes 1, 3)
(25) TDVE2L	Data Setup Time	Early Write	E2	60	-	ns	(Notes 1, 3)
(26) TWHDX	Data Hold Time	Late Write		5	-	ns	(Notes 1, 3)
(27) TE1HDX	Data Hold Time	Early Write	$\overline{E1}$	10	-	ns	(Notes 1, 3)
(28) TE2LDX	Data Hold Time	Early Write	E2	10	-	ns	(Notes 1, 3)
(29) TWLQZ	Write Enable Low to Output Off			-	50	ns	(Notes 2, 3)
(30) TWHQX	Write Enable High to Output On			5	-	ns	(Notes 2, 3)

NOTES:

1. Input pulse levels: 0V to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5V and 5.5V.

Low Voltage Data Retention

Harris CMOS RAMs are designed with battery backup in mind. Data Retention voltage and supply current are guaranteed over the operating temperature range. The following rules ensure data retention:

1. The RAM must be kept disabled during data retention. This is accomplished by holding the E2 pin between -0.3V and GND.
2. During power-up and power-down transitions, E2 must be held between -0.3V and 10% of V_{CC}.
3. The RAM can begin operating one TAVAX after V_{CC} reaches the minimum operating voltage of 4.5V.

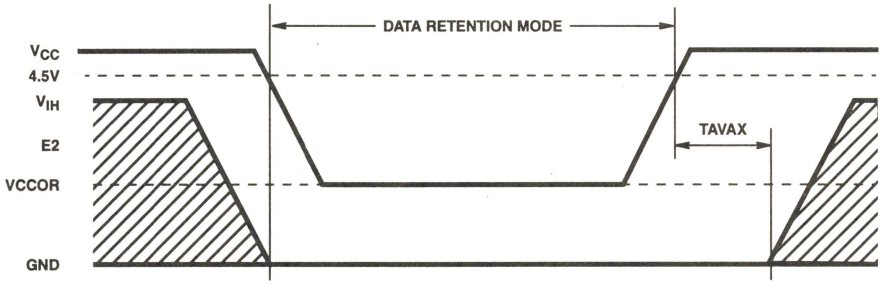


FIGURE 1. DATA RETENTION

Read Cycles

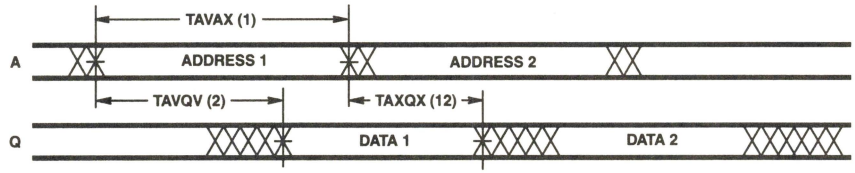


FIGURE 2. READ CYCLE I: $\overline{W}$, E2 HIGH; $\overline{G}$, $\overline{E1}$ LOW

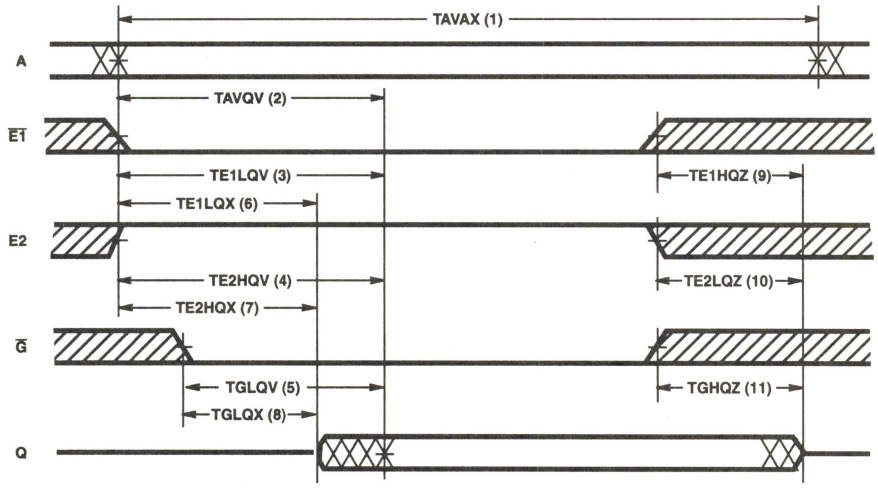


FIGURE 3. READ CYCLE II: $\overline{W}$ HIGH

Write Cycles

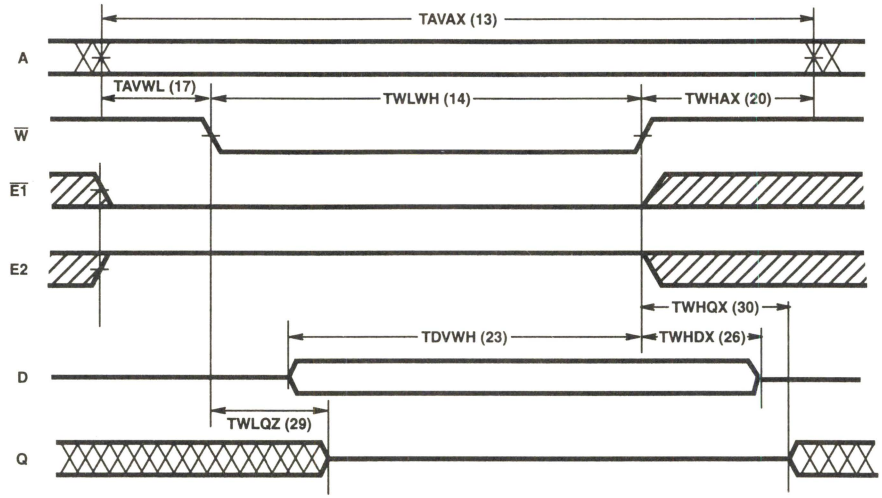


FIGURE 4. WRITE CYCLE I: LATE WRITE

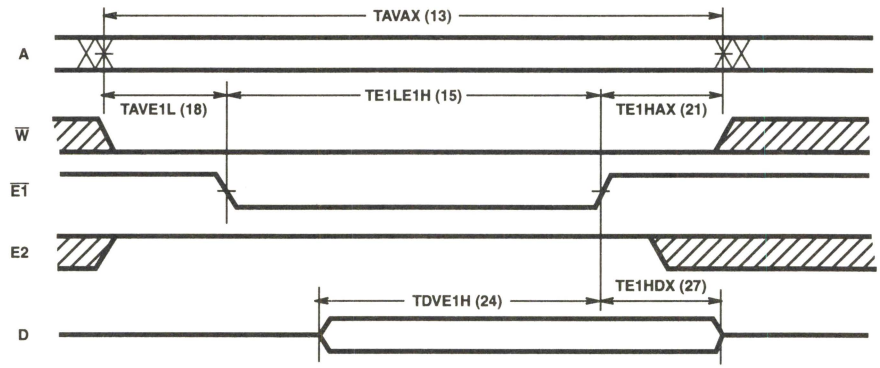


FIGURE 5. WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E1}$

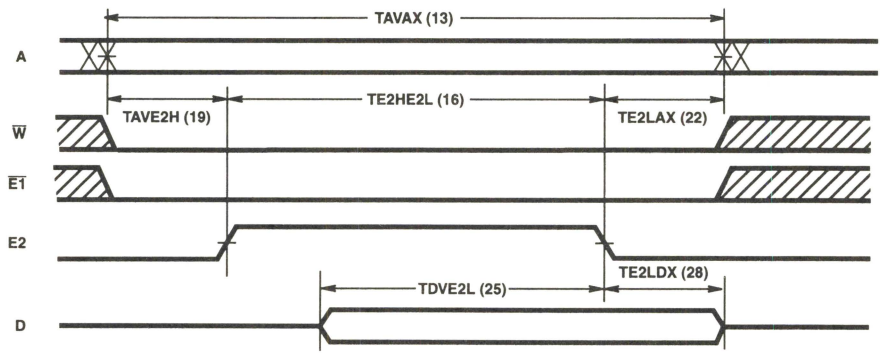


FIGURE 6. WRITE CYCLE III: EARLY WRITE - CONTROLLED BY E2

Typical Performance Curve

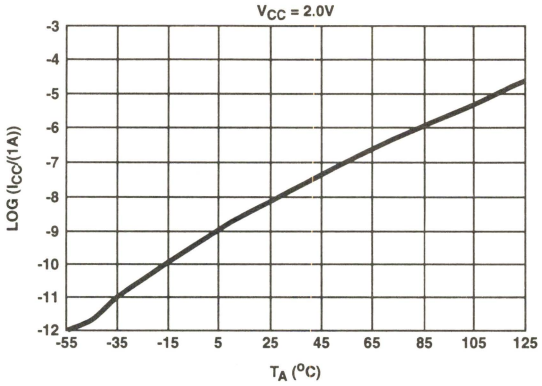


FIGURE 7. TYPICAL ICCDR vs T_A

HARRIS SEMICONDUCTOR

HM-65642/883

8K x 8 Asynchronous CMOS Static RAM

March 1997

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Full CMOS Design
- Six Transistor Memory Cell
- Low Standby Supply Current 100µA
- Low Operating Supply Current. 20mA
- Fast Address Access Time 150ns
- Low Data Retention Supply Voltage. 2.0V
- CMOS/TTL Compatible Inputs/Outputs
- JEDEC Approved Pinout
- Equal Cycle and Access Times
- No Clocks or Strobes Required
- Gated Inputs
  - No Pull-Up or Pull-Down Resistors Required
- Temperature Range -55°C to +125°C
- Easy Microprocessor Interfacing
- Dual Chip Enable Control

Description

The HM-65642/883 is a CMOS 8192 x 8-bit Static Random Access Memory. The pinout is the JEDEC 28 pin, 8-bit wide standard, which allows easy memory board layouts which accommodate a variety of industry standard ROM, PROM, EPROM, EEPROM and RAMs. The HM-65642/883 is ideally suited for use in microprocessor based systems. In particular, interfacing with the Harris 80C86 and 80C88 microprocessors is simplified by the convenient output enable ($\overline{G}$) input.

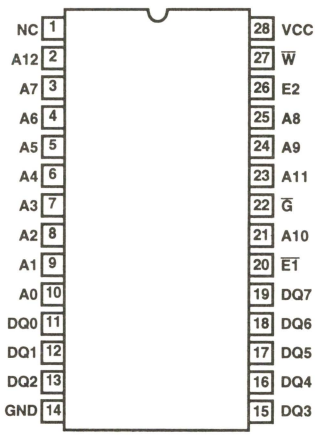
The HM-65642/883 is a full CMOS RAM which utilizes an array of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T RAM cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor or MIX-MOS (4T) devices

Ordering Information

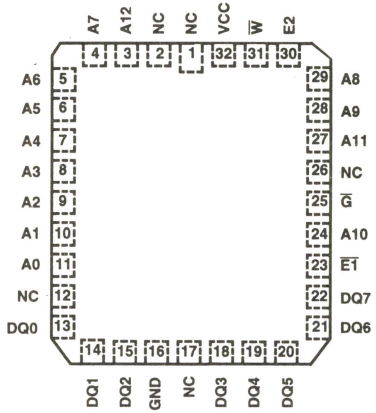
PACKAGE	TEMPERATURE RANGE	150ns/75µA	150ns/150µA	200ns/250µA	PKG. NO.
CERDIP	-55°C to +125°C	HM1-65642B/883	HM1-65642/883	HM1-65642C/883	F28.6
CLCC	-55°C to +125°C	HM4-65642B/883	HM4-65642/883	-	J32.A

Pinouts

HM-65642/883 (CERDIP)
TOP VIEW



HM4-65642/883 (CLCC)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
DQ	Data Input/Output
$\overline{E1}$	Chip Enable
E2	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
NC	No Connections
GND	Ground
VCC	Power

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3004.1**

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage Applied for all Grades . . . . . GND -0.3V to VCC +0.3V
Typical Derating Factor . . . . . 5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package	45°C/W	8°C/W
CLCC Package	55°C/W	10°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 101,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . -0.3V to +0.8V
Input High Voltage . . . . . +2.2V to VCC +0.3V
Data Retention Supply Voltage 2.0V
Input Rise and Fall Time . . . . . 40ns Max.

TABLE 1. HM-65642/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH 1	VCC = 4.5V, IO = -1.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 4.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	HM-65642B/883, HM-65642/883 VCC = 5.5V, $\overline{G}$ = 2.2V, VI/O = GND or VCC	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	+1.0	µA
		HM-65642C/883 VCC = 5.5V, $\overline{G}$ = 2.2V, VI/O = GND or VCC	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-2.0	+2.0	µA
Input Leakage Current	II	HM-65642B/883, HM-65642/883 VCC = 5.5V, VI = GND or VCC	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	+1.0	µA
		HM-65642C/883 VCC = 5.5V, VI = GND or VCC	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-2.0	+2.0	µA
Standby Supply Current	ICCSB1	HM-65642B/883 VCC = 5.5V, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	µA
		HM-65642/883 VCC = 5.5V, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	250	µA
		HM-65642C/883 VCC = 5.5V, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	400	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E1}$ = 2.2V or E2 = 0.8V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	5	mA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E1}$ =0.8V, E2 = 2.2V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	5	mA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = 5.5V, (Note 2), f = 1MHz, $\overline{E1}$ = 0.8V, E2 = 2.2V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	20	mA

TABLE 1. HM-65642/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Data Retention Supply Current	ICCDR	HM-65642B/883 VCC = 2.0V, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	75	µA
		HM-65642/883 VCC = 2.0V, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	150	µA
		HM-65642C/883 VCC = 2.0V, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	250	µA
Functional Test	FT	VCC = 4.5V (Note 3)	7, 8A, 8B	$-55^oC \le T_A \le +125^oC$	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. Typical derating 5mA/MHz increase in ICCOP.
3. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH ≥ 1.5V, and VOL ≤ 1.5V.

TABLE 2. HM-65642/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS HM-65642B/883 MIN	LIMITS HM-65642B/883 MAX	LIMITS HM-65642/883 MIN	LIMITS HM-65642/883 MAX	LIMITS HM-65642C/883 MIN	LIMITS HM-65642C/883 MAX	UNITS
Read/Write/ Cycle Time	TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	150	-	200	-	ns
Address Access Time	TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	150	-	150	-	200	-
Output Enable Access Time	TGLQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	70	-	70	-	70	ns
Chip Enable Access Time	TE1LQV TE2HQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	150	-	150	-	200	ns
Write Recovery Time	TWHAX TE1HAX TE2LAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	10	-	10	-	ns
Chip Enable to End-of-Write	TE1LE1H TE2HE2L	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	90	-	90	-	120	-	ns
Address Setup Time	TAVWL TAVE1L TAVE2H	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Write Enable Pulse Width	TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	90	-	90	-	120	-	ns
Data Setup Time	TDVWH TDVE1H TDVE2L	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	60	-	60	-	80	-	ns

TABLE 2. HM-65642/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS						UNITS
					HM-65642B/883		HM-65642/883		HM-65642C/883		
					MIN	MAX	MIN	MAX	MIN	MAX	
Data Hold Time	TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	5	-	5	-	5	-	ns
	TE1HDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	10	-	10	-	ns
	TE2LDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	10	-	10	-	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL ≥ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.

TABLE 3. HM-65642/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		
					MIN	MAX	UNITS
Output High Voltage	VOH2	VCC = 4.5V, IO = -100µA	1	$-55^oC \le T_A \le +125^oC$	VCC -0.4	-	V
Input Capacitahce	CIN	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	12	pF
		VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	10	pF
I/O Capacitance	CI/O	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	14	pF
		VCC = 4.5V, VI/O = GND or VCC, All Measurements Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	12	pF
Write Enable to Output in High Z	TWLQZ	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	-	50	ns
Write Enable High to Output ON	TWHQX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	5	-	ns
Chip Enable to Output ON	TE1LQX TE2HQX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	10	-	ns
Output Enable to Output ON	TGLQX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	5	-	ns
Chip Enable to Output in High Z	TE1HQZ	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	-	50	ns
	TE2LQZ		1	$-55^oC \le T_A \le +125^oC$	-	60	ns
Output Disable to Output in High Z	TGHQZ	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	-	50	ns
Output Hold from Address Change	TAXQX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	10	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only. For design purposes CIN = 6pF typical and CI/O = 7pF typical.
3. Applies to LCC device types only. For design purposes CIN = 4pF typical and CI/O = 5pF typical.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	GROUPS METHOD	SUBGROUPS
Interim Test 1	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test 1	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

Low Voltage Data Retention

Harris CMOS RAMs are designed with battery backup in mind. Data Retention voltage and supply current are guaranteed over the operating temperature range. The following rules ensure data retention:

1. The RAM must be kept disabled during data retention. This is accomplished by holding the E2 pin between -0.3V and GND.
2. During power-up and power-down transitions, E2 must be held between -0.3V and 10% of VCC.
3. The RAM can begin operating one TAVAX after VCC reaches the minimum operating voltage of 4.5V.

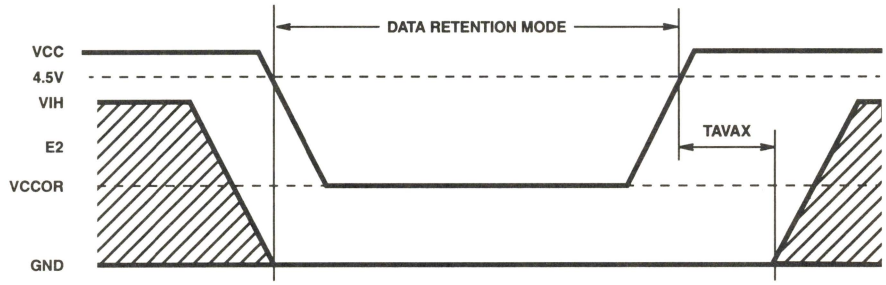


FIGURE 1. DATA RETENTION

Read Cycles

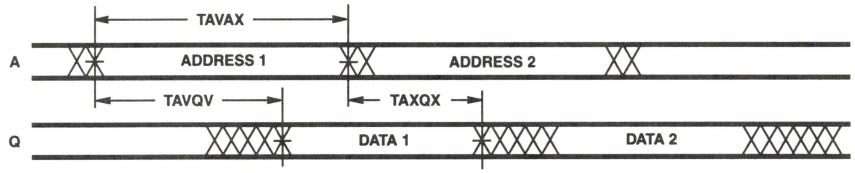


FIGURE 2. READ CYCLE I: $\overline{W}$, E2 HIGH; $\overline{G}$, $\overline{E1}$ LOW

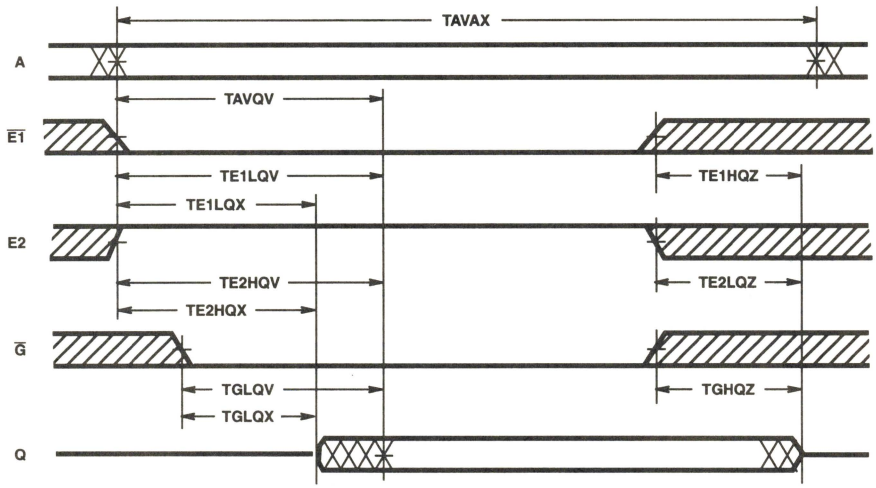


FIGURE 3. READ CYCLE II: $\overline{W}$ HIGH

Write Cycles

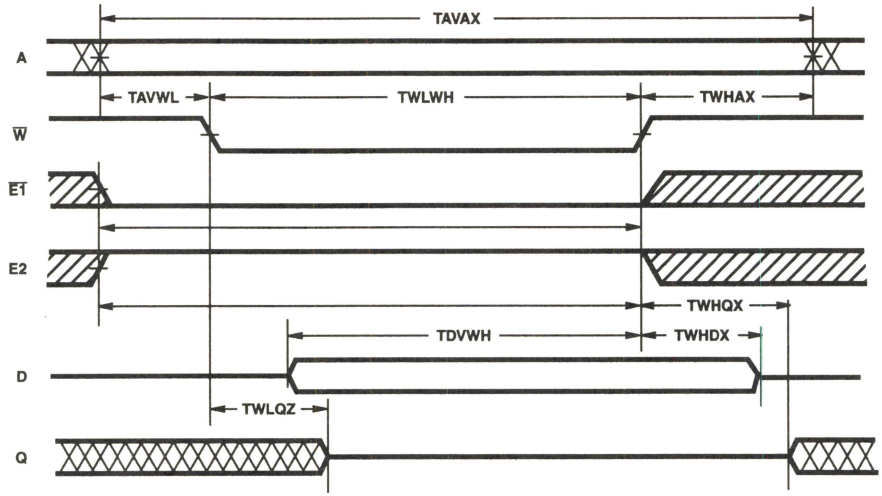


FIGURE 4. WRITE CYCLE I: LATE WRITE

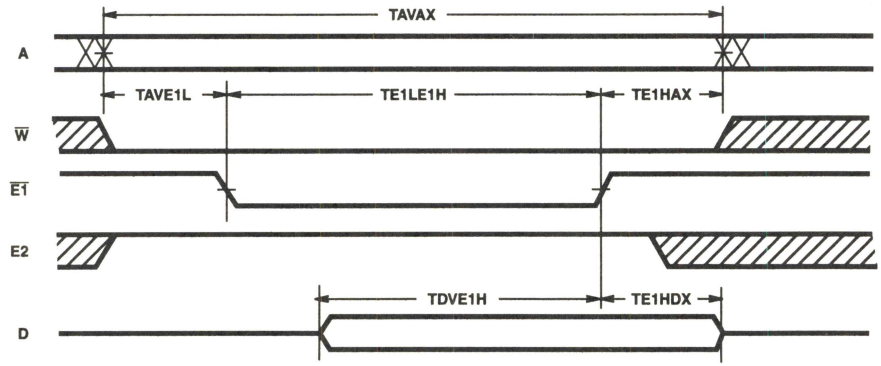


FIGURE 5. WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E1}$

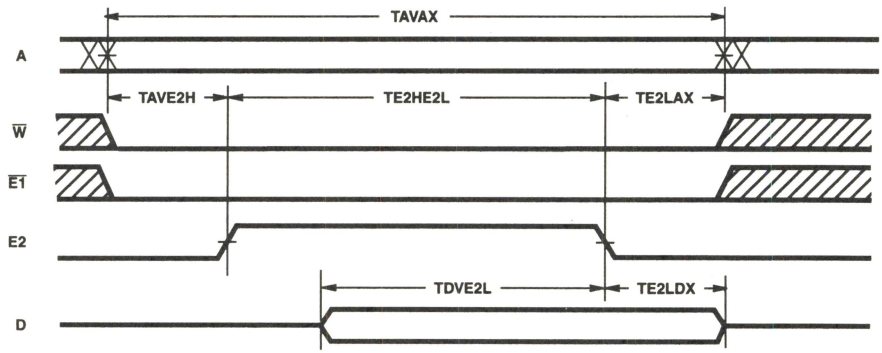
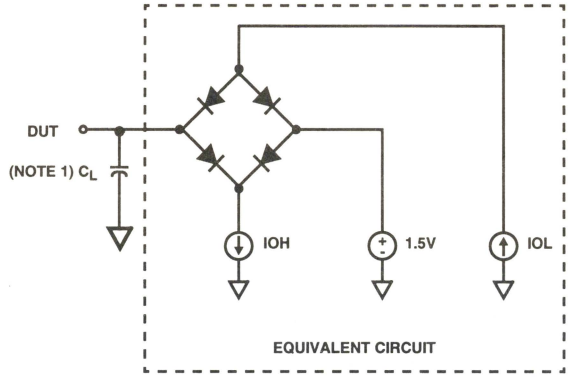


FIGURE 6. WRITE CYCLE III: EARLY WRITE - CONTROLLED BY E2

Test Circuit

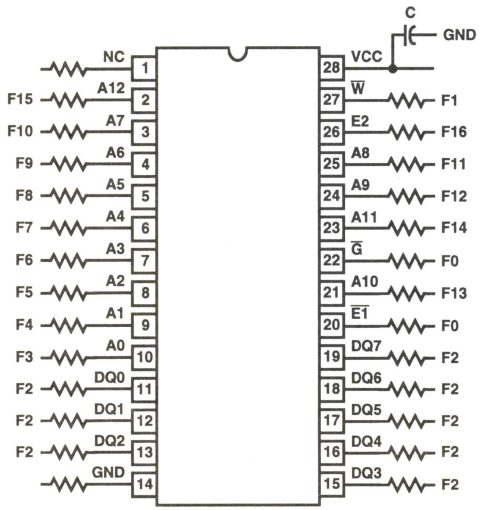


NOTE:

1. Test head capacitance.

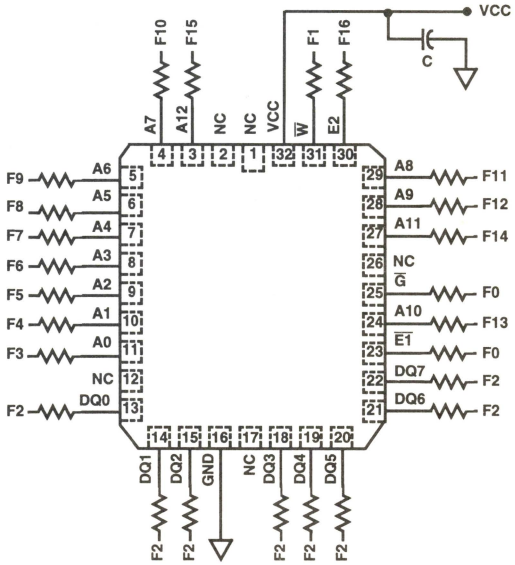
Burn-In Circuits

HM-65642/883
CERDIP
TOP VIEW



NOTES:
F0 = 100kHz ±10%.
All resistors 47kΩ ±5%.
C = 0.01µF Min.
VCC = 5.5V ±0.5V.
VIH = 4.5V ±10%.
VIL = -0.2V to +0.4V.

HM-65642/883
CLCC
TOP VIEW



NOTES:
F0 = 100kHz ±10%.
C = 0.01µF Min.
VCC = 5.5V ±0.5V.
VIH = 4.5V ±10%.
VIL = -0.2V to +0.4V.

Die Characteristics

DIE DIMENSIONS:
274.0 x 302.8 x 19 ±1mils

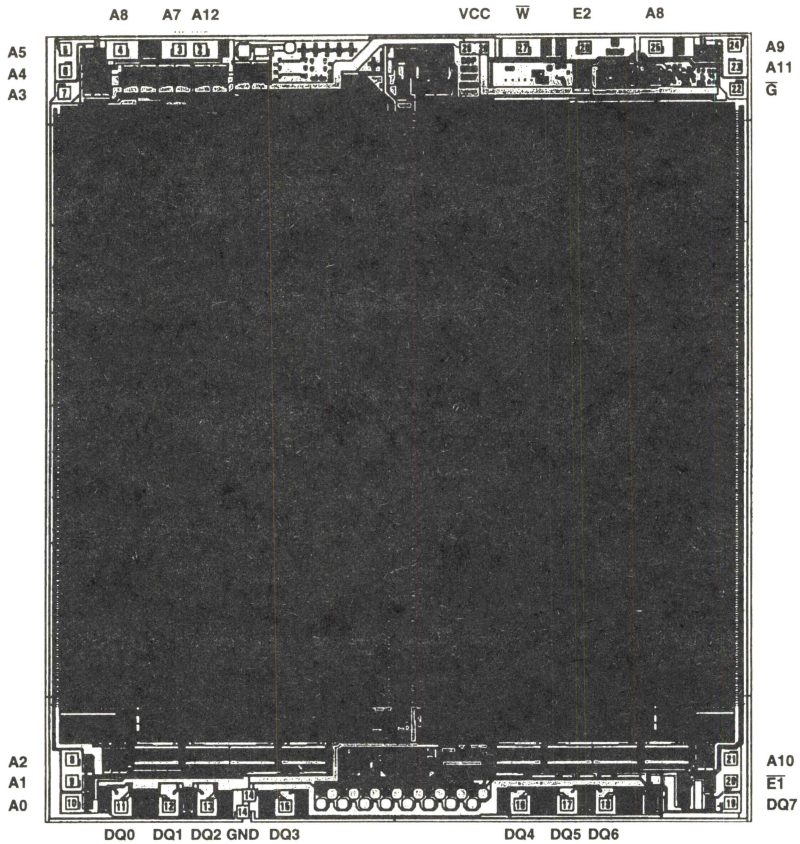
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
0.9 x 10^5 A/cm^2

Metallization Mask Layout

HM-65642/883



HARRIS SEMICONDUCTOR

HM-6642

March 1997

512 x 8 CMOS PROM

Features

- Low Power Standby and Operating Power
  - ICCSB 100µA
  - ICCOP . . . . . 20mA at 1MHz
- Fast Access Time. 120/200ns
- Industry Standard Pinout
- Single 5.0V Supply
- CMOS/TTL Compatible Inputs
- Field Programmable
- Synchronous Operation
- On-Chip Address Latches
- Separate Output Enable

Description

The HM-6642 is a 512 x 8 CMOS NiCr fusible link Programmable Read Only Memory in the popular 24 pin, byte wide pinout. Synchronous circuit design techniques combine with CMOS processing to give this device high speed performance with very low power dissipation.

On-chip address latches are provided, allowing easy interfacing with recent generation microprocessors that use multiplexed address/data bus structures, such as the 8085. The output enable controls, both active low and active high, further simplify microprocessor system interfacing by allowing output data bus control independent of the chip enable control. The data output latches allow the use of the HM-6642 in high speed pipelined architecture systems, and also in synchronous logic replacement functions.

Applications for the HM-6642 CMOS PROM include low power handheld microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, processor control store, and synchronous logic replacement.

All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

Ordering Information

PACKAGE	TEMPERATURE RANGE	120ns	200ns	PKG. NO.
SBDIP	-40°C to +85°C	HM1-6642B-9	HM1-6642-9	D24.6
SMD#	-55°C to +125°C	5962-8869002JA	5962-8869001JA	D24.6
SLIM SBDIP	-40°C to +85°C	HM6-6642B-9	HM6-6642-9	D24.3
SMD#	-55°C to +125°C	5962-8869002LA	5962-8869001LA	D24.3
CLCC	-40°C to +85°C	-	HM4-6642-9	J28.A
SMD#	-55°C to +125°C	5962-88690023A	5962-88690013A	J28.A

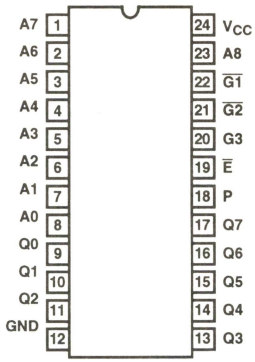
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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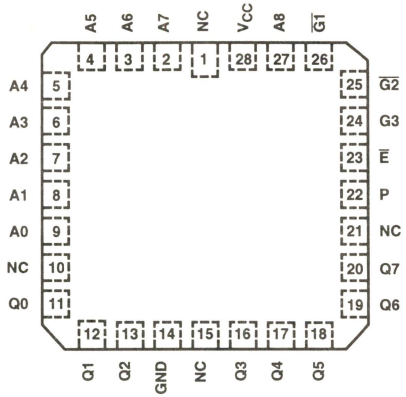
File Number 3012.1

Pinouts

HM-6642 (SBDIP)
TOP VIEW



HM-6642 (CLCC)
TOP VIEW

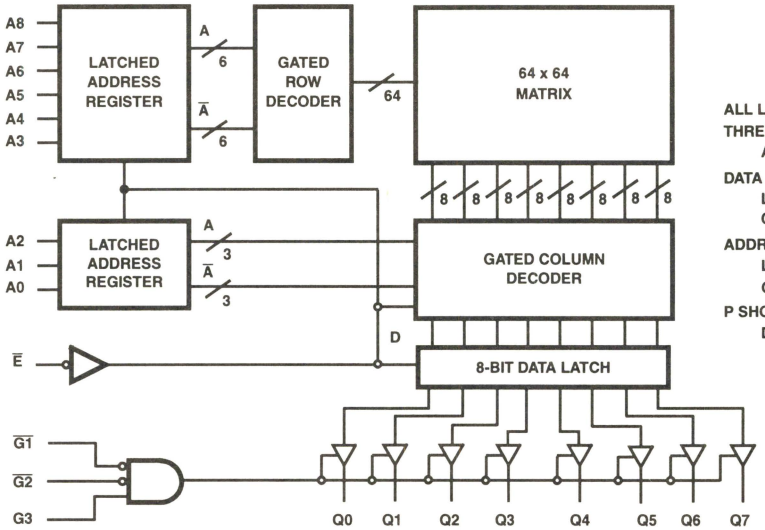


PIN DESCRIPTION

PIN	DESCRIPTION
NC	No Connect
A0-A8	Address Inputs
$\overline{E}$	Chip Enable
Q	Data Output
V_{CC}	Power (+5V)
$\overline{G1}$, $\overline{G2}$, G3	Output Enable
P (Note)	Program Enable

NOTE: P should be hardwired to GND except during programming.

Functional Diagram



ALL LINES POSITIVE LOGIC - ACTIVE HIGH
THREE STATE BUFFERS:
A HIGH ⟶ OUTPUT ACTIVE
DATA LATCHES:
L HIGH ⟶ Q = D
Q LATCHES ON RISING EDGE OF $\overline{E}$
ADDRESS LATCHES AND GATED DECODERS:
LATCH ON FALLING EDGE OF $\overline{E}$
GATE ON FALLING EDGE OF $\overline{E}$
P SHOULD BE HARDWIRED TO GND EXCEPT DURING PROGRAMMING

Programming

Introduction

The HM-6642 is a 512 word by 8-bit field Programmable Read Only Memory utilizing nicrome fusible links as programmable memory elements. Selected memory locations are permanently changed from their manufactured state, of all low (V_{OL}) to a logical high (V_{OH}), by the controlled application of programming potentials and pulses. Careful adherence to the following programming specifications will result in high programming yield. Both high V_{CC} (6.0V) and low V_{CC} (4.0V) verify cycles are specified to assure the integrity of the programmed fuse. This programming specification, although complete, does not preclude rapid programming. The worst case programming time required is 37.4 seconds, and typical programming time can be approximately 4 seconds per device.

The chip ($\overline{E}$) and output enable ($\overline{G}$) are used during the programming procedure. On PROMs which have more than one output enable control G3 is to be used. The other output enables must be held in the active, or enabled, state throughout the entire programming sequence. The programmer designer is advised that all pins of the programmer's socket should be at ground potential when the PROM is inserted into the socket. V_{CC} must be applied to the PROM before any input or output pin is allowed to rise (See Note).

Overall Programming Procedure

1. The address of the first bit to be programmed is presented, and latched by the chip enable ($\overline{E}$) falling edge. The output is disabled by taking the output enable $\overline{G}$ Low: The programming pin is enabled by taking (P) high.
2. V_{CC} is raised to the programming voltage level, 12.5V.
3. All data output pins are pulled up to V_{CC} program. Then the data output pin corresponding to the bit to be programmed is pulled low for 100ms. Only one bit should be programmed at a time.
4. The data output pin is returned to V_{CC}, and the V_{CC} pin is returned to 6.0V.
5. The address of the bit is again presented, and latched by a second chip enable falling edge.
6. The data outputs are enabled, and read, to verify that the bit was successfully programmed.
   a). If verified, the next bit to be programmed is addressed and programmed.
   b). If not verified, the programs verify sequence is repeated up to 8 times total.
7. After all bits to be programmed have been verified at 6.0V, the V_{CC} is lowered to 4.0V and all bits are verified.
   a). If all bits verify, the device is properly programmed.
   b). If any bit fails to verify, the device is rejected.

Programming System Requirements

1. The power supply for the device to be programmed must be able to be set to three voltages: 4.0V, 6.0V, 12.5V. This supply must be able to supply 500mA average, and 1A dynamic, currents to the PROM during programming. The power supply rise fall times when switching between voltages must be no quicker than 1ms.
2. The address drivers must be able to supply a V_{IH} of 4.0V and 6.0V and V_{IL} when the system is at programming voltages. (See Note)
3. The control input buffers must be able to maintain input voltage levels of $\geq$ 70% and $\leq$ 20% V_{CC} for V_{IH} and V_{IL} levels, respectively. Notice that chip enable ($\overline{E}$) and $\overline{G}$ does not require a pull up to programming voltage levels. The program control (P) must switch from ground to VIH and from V_{IH} to the V_{CC} PGM level. (See Note)
4. The data input buffers must be able to sink up to 3mA from the PROM's output pins without rising more than 0.7V above ground, be able to hold the other outputs high with a current source capability of 0.5mA to 2.0mA, and not interfere with the reading and verifying of the data output of the PROM. Notice that a bit to be programmed is changed from a low state (V_{OL}) to high (V_{OH}) by pulling low on the output pin. A suggested implementation is open collector TTL buffers (or inverters) with 4.7kΩ pull up resistors to V_{CC}. (See Note)

NOTE: Never allow any input or output pin to rise more than 0.3V above V_{CC}, or fall more than 0.3V below ground.

Background Information HM-6642 Programming

PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	LIMITS			UNITS
		MIN	TYP	MAX	
VCC PROG	Programming VCC	12.0	12.0	12.5	V
VCCN	Operating VCC	4.5	5.5	5.5	V
VCC LV	Special Verify VCC	4.0	-	6.0	V
ICC	System ICC Capability	500	-	-	mA
ICC Peak	Transient ICC Capability	1.0	-	-	A
PROM INPUT PINS					
VOL	Output Low Voltage (To PROM)	-0.3	GND	20% VCC	V
VOH	Output High Voltage (To PROM)	70% VCC	VCC	VCC +0.3	V
IOL	Output Sink Current (At VOL)	0.01	-	-	mA
IOH	Output Source Current (At VOH)	0.01	-	-	mA
PROM DATA OUTPUT PINS					
VOL	Output Low Voltage (To PROM)	-0.3	GND	0.7	V
VOH	Output High Voltage (To PROM)	70% VCC	VCC	VCC +0.3	V
IOL	Output Sink Current (At VOL)	3.0	-	-	mA
IOH	Output Source Current (At VOH)	0.5	1.0	2.0	mA
tD	Delay Time	1.0	1.0	-	µs
tR	Rise Time	1.0	10.0	10.0	µs
tF	Fall Time	1.0	10.0	10.0	µs
TEHEL	Chip Enable Pulse Width	500	-	-	ns
TAVEL	Address Valid to Chip Enable Low Time	500	-	-	ns
TELQV	Chip Enable Low to Output Valid Time	-	-	500	ns
tpw	Programming Pulse Width	90	100	110	µs
tIP	Input Leakage at VCC = VCC PROG	-10	+1.0	10	µA
TA	Ambient Temperature	-	25	-	°C

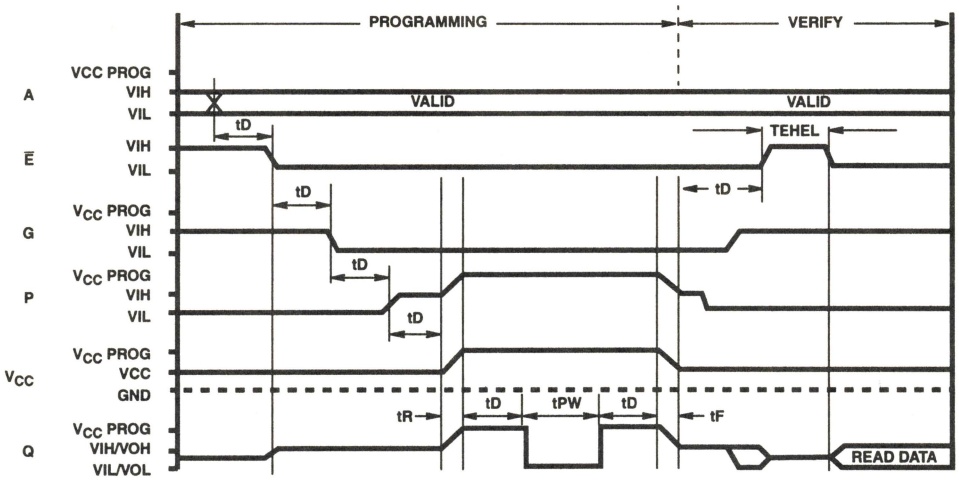


FIGURE 1. HM-6642 PROGRAMMING CYCLE

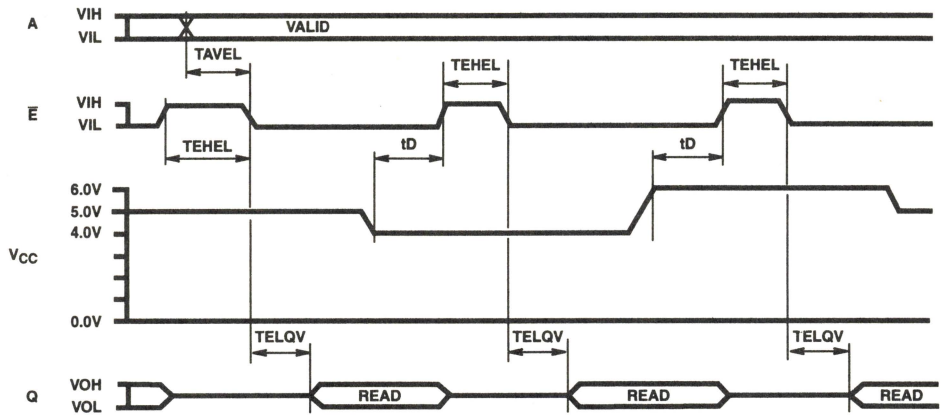


FIGURE 2. HM-6642 POST PROGRAMMING VERIFY CYCLE

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
Typical Derating Factor . . . . . 5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
HM-6642B-9, HM-6642-9 . . . . . -40^oC to $+85^oC$

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	$52^oC/W$	$14^oC/W$
Slim SBDIP	$70^oC/W$	$19^oC/W$
CLCC Package	$58^oC/W$	$14^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature . . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s) $+300^oC$

Die Characteristics

Gate Count . . . . . 1680 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5V ± 10%; T_A = -40^oC to $+85^oC$ (HM-6642B-9, HM-6642-9)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	100	µA	IO = 0, VI = VCC or GND, VCC = 5.5V
ICCOP	Operating Supply Current (Note 3)	-	20	mA	f = 1MHz, IO = 0, VI = VCC or GND, VCC = 5.5V
II	Input Leakage Current	-1.0	+1.0	µA	GND ≤ VI ≤ VCC, VCC = 5.5V
IOZ	Output Leakage Current	-1.0	+1.0	µA	GND ≤ VO ≤ VCC, VCC = 5.5V
VIL	Input Low Voltage	-0.3	0.8	V	VCC = 4.5V
VIH	Input High Voltage	2.4	VCC + 0.3	V	VCC = 5.5V
VOL	Output Low Voltage	-	0.4	V	IOL = 3.2mA, VCC = 4.5V
VOH1	Output High Voltage	2.4	-	V	IOH = -1.0mA, VCC = 4.5V
VOH2	Output High Voltage (Note 2)	VCC - 1.0	-	V	IOH = -100µA, VCC = 4.5V

AC Electrical Specifications

SYMBOL	PARAMETER	LIMITS HM-6642B-9 MIN	LIMITS HM-6642B-9 MAX	LIMITS HM-6642-9 MIN	LIMITS HM-6642-9 MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	120	-	200	ns	Notes 1, 4
(2) TAVQV	Address Access Time (TAVQV = TELQV + TAVEL)	-	140	-	220	ns	Notes 1, 4
(3) TGVQV	Output Enable Access Time	-	50	-	150	ns	Notes 1, 4
(4) TGVQX	Output Enable Time	5	50	5	150	ns	Notes 2, 4
(5) TGXQZ	Output Disable Time	-	50	-	150	ns	Notes 2, 4
(6) TELEH	Chip Enable Pulse Negative Width	120	-	200	-	ns	Notes 1, 4
(7) TELEL	Read Cycle Time	160	-	350	-	ns	Notes 1, 4
(8) TEHEL	Chip Enable Pulse Positive Width	40	-	150	-	ns	Notes 1, 4
(9) TAVEL	Address Setup Time	20	-	20	-	ns	Notes 1, 4
(10) TELAX	Address Hold Time	25	-	60	-	ns	Notes 1, 4

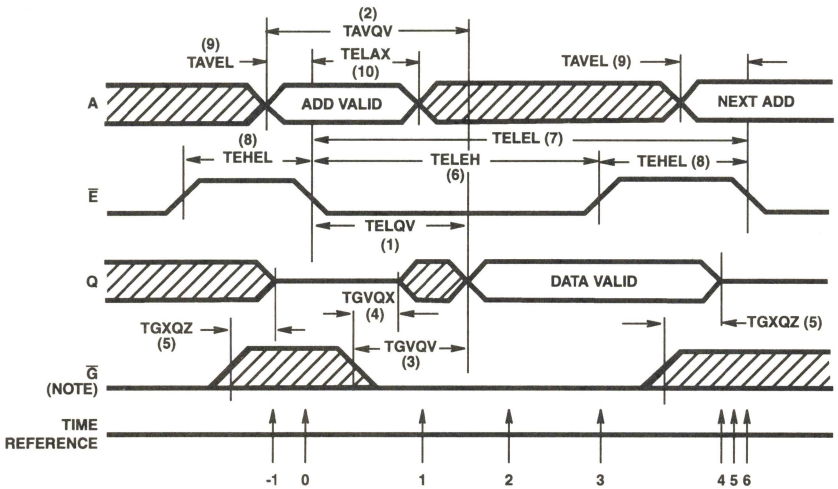
Capacitance $T_A = +25^oC$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	-	10.0	pF	f = 1MHz, All Measurements Reference Device Ground
CO	Output Capacitance (Note 2)	-	12.0	pF	

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. V_{CC} = 4.5V and 5.5V.

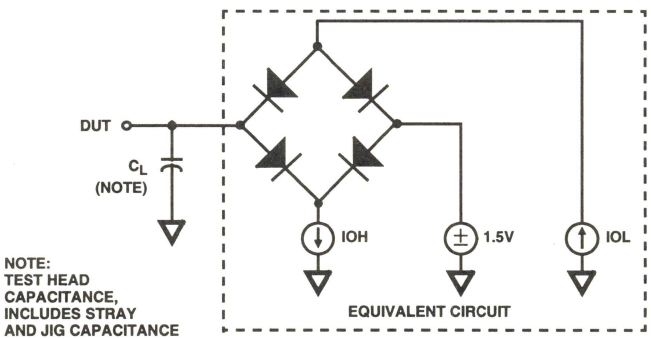
Switching Waveform



NOTE: G has the same timing as $\overline{G}$ except signal is inverted.

FIGURE 3. READ CYCLE

Test Load Circuit



HARRIS SEMICONDUCTOR

HM-6617

March 1997

2K x 8 CMOS PROM

Features

- Low Power Standby and Operating Power
  - ICCSB 100µA
  - ICCOP . . . . . 20mA at 1MHz
- Fast Access Time. 90/120ns
- Industry Standard Pinout
- Single 5.0V Supply
- CMOS/TTL Compatible Inputs
- High Output Drive . . . . . 12 LSTTL Loads
- Synchronous Operation
- On-Chip Address Latches
- Separate Output Enable

Description

The HM-6617 is a 16,384 bit fuse link CMOS PROM in a 2K word by 8-bit/word format with "Three-State" outputs. This PROM is available in the standard 0.600 inch wide 24 pin SBDIP, the 0.300 inch wide slimline SBDIP, and the JEDEC standard 32 pad CLCC.

The HM-6617 utilizes a synchronous design technique. This includes on-chip address latches and a separate output enable control which makes this device ideal for applications utilizing recent generation microprocessors. This design technique, combined with the Harris advanced self-aligned silicon gate CMOS process technology offers ultra-low standby current. Low ICCSB is ideal for battery applications or other systems with low power requirements.

The Harris NiCr fuse link technology is utilized on this and other Harris CMOS PROMs. This gives the user a PROM with permanent, stable storage characteristics over the full industrial and military temperature voltage ranges. NiCr fuse technology combined with the low power characteristics of CMOS provides an excellent alternative to standard bipolar PROMs or NMOS EPROMs.

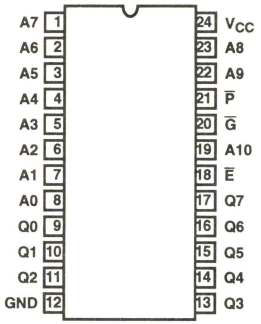
All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

Ordering Information

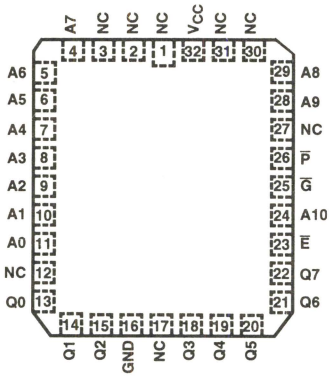
PACKAGE	TEMP. RANGE	90ns	120ns	PKG. NO.
SBDIP	-40°C to +85°C	HM1-6617B-9	HM1-6617-9	D24.6
SMD#	-55°C to +125°C	5962-8954002JA	5962-8954001JA	D24.6
SLIM SBDIP	-40°C to +85°C	HM6-6617B-9	HM6-6617-9	D24.3
SMD#	-55°C to +125°C	5962-8954002LA	5962-8954001LA	D24.3
CLCC	-40°C to +85°C	HM4-6617B-9	HM4-6617-9	J32.A
SMD#	-55°C to +125°C	5962-8954002XA	5962-8954001XA	J32.A

Pinouts

HM-6617 (SBDIP)
TOP VIEW



HM-6617 (CLCC)
TOP VIEW



PIN DESCRIPTION

PIN	DESCRIPTION
NC	No Connect
A0-A10	Address Inputs
$\overline{E}$	Chip Enable
Q	Data Output
V_{CC}	Power (+5V)
$\overline{G}$	Output Enable
$\overline{P}$ (Note)	Output Enable

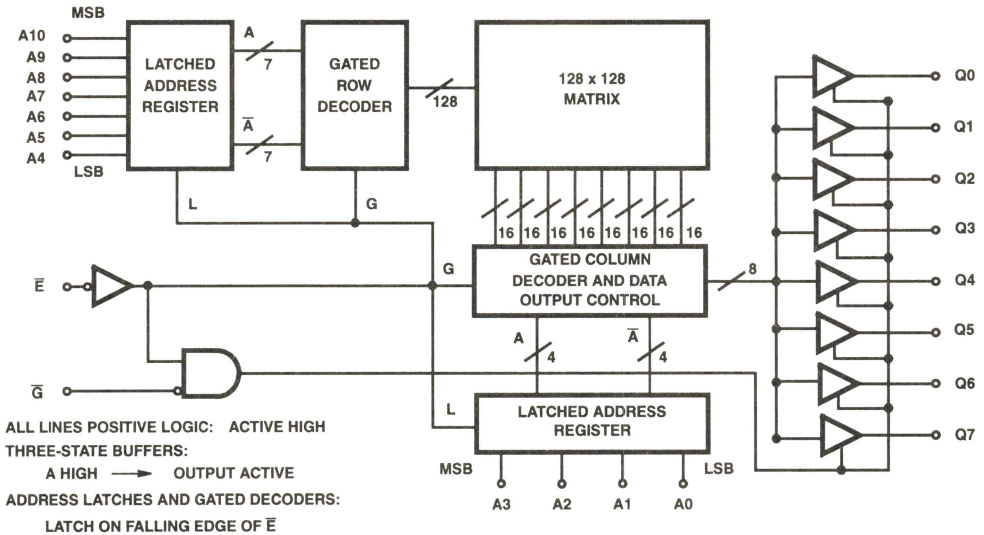
NOTE: $\overline{P}$ should be hardwired to V_{CC} except during programming.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3017.1**

Functional Diagram



ALL LINES POSITIVE LOGIC: ACTIVE HIGH

THREE-STATE BUFFERS:

A HIGH → OUTPUT ACTIVE

ADDRESS LATCHES AND GATED DECODERS:

LATCH ON FALLING EDGE OF $\overline{E}$

GATE ON FALLING EDGE OF $\overline{G}$

Background Information Programming Algorithm

The HM-6617 CMOS PROM is manufactured with all bits containing a logical zero (output low). Any bit can be programmed selectively to a logical one (output high) state by following the procedure shown below. To accomplish this, a programmer can be built that meets the specifications shown, or any of the approved commercial programmers can be used.

Programming Sequence Of Events

1. Apply a voltage of V_{CC1} to V_{CC} of the PROM.
2. Read all fuse locations to verify that the PROM is blank (output low).
3. Place the PROM in the initial state for programming: $\overline{E}$ = V_{IH}, $\overline{P}$ = V_{IH}, $\overline{G}$ = V_{IL}.
4. Apply the correct binary address for the word to be programmed. No inputs should be left open circuit.
5. After a delay of tD, apply voltage of V_{IL} to $\overline{E}$ (pin 18) to access the addressed word.
6. The address may be held through the cycle, but must be held valid at least for a time equal to tD after the falling edge of $\overline{E}$. None of the inputs should be allowed to float to an invalid logic level.
7. After a delay of tD, disable the outputs by applying a voltage of V_{IH} to $\overline{G}$ (pin 20).
8. After a delay of tD, apply voltage of V_{IL} to $\overline{P}$ (pin 21).
9. After delay of tD, raise V_{CC} (pin 24) to VCCPROG with a rise time of tR. All outputs at V_{IH} should track V_{CC} with V_{CC} -2.0V to V_{CC} +0.3V. This could be accomplished by pulling outputs at V_{IH} to V_{CC} through pull-up resistors of value Rn.
10. After a delay of tD, pull the output which corresponds to the bit to be programmed to V_{IL}. Only one bit should be programmed at a time.
11. After a delay of tPW, allow the output to be pulled to V_{IH} through pull-up resistor Rn.
12. After a delay of tD, reduce V_{CC} (pin 24) to V_{CC1} with a fall time of tF. All outputs at V_{IH} should track V_{CC} with V_{CC} 2.0V to V_{CC} +0.3V. This could be accomplished by pulling outputs at V_{IH} to V_{CC} through pull-up resistors of value Rn.
13. Apply a voltage of V_{IH} to $\overline{P}$ (pin 21).
14. After a delay of tD, apply a voltage of V_{IL} to $\overline{G}$ (pin 20).
15. After a delay of tD, examine the outputs for correct data. If any location verifies incorrectly, repeat steps 4 through 14 (attempting to program only those bits in the word which verified incorrectly) up to a maximum of eight attempts for a given word. If a word does not program within eight attempts, it should be considered a programming reject.
16. Repeat steps 3 through 15 for all other bits to be programmed in the PROM.

Post-Programming Verification

17. Place the PROM in the post-programming verification mode: $\overline{E}$ = V_{IH}, $\overline{G}$ = V_{IL}, $\overline{P}$ = V_{IH}, V_{CC} (pin 24) = V_{CC1}.
18. Apply the correct binary address of the word to be verified to the PROM.
19. After a delay of tD, apply a voltage of V_{IL} to $\overline{E}$ (pin 18).
20. After a delay of tD, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
21. Repeat steps 17 through 20 for all possible programming locations

Post-Programming Read

22. Apply a voltage of V_{CC2} = 4.0V to V_{CC} (pin 24).
23. After a delay of tD, apply a voltage of V_{IH} to $\overline{E}$ (pin 18).
24. Apply the correct binary address of the word to be read.
25. After a delay of TAVEL, apply a voltage of V_{IL} to $\overline{E}$ (pin 18).
26. After a delay of TELQV, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
27. Repeat steps 23 through 26 for all address locations.
28. Apply a voltage of V_{CC2} = 6.0V to V_{CC} (pin 24).
29. Repeat steps 23 through 26 for all address locations.

Programming Cycle

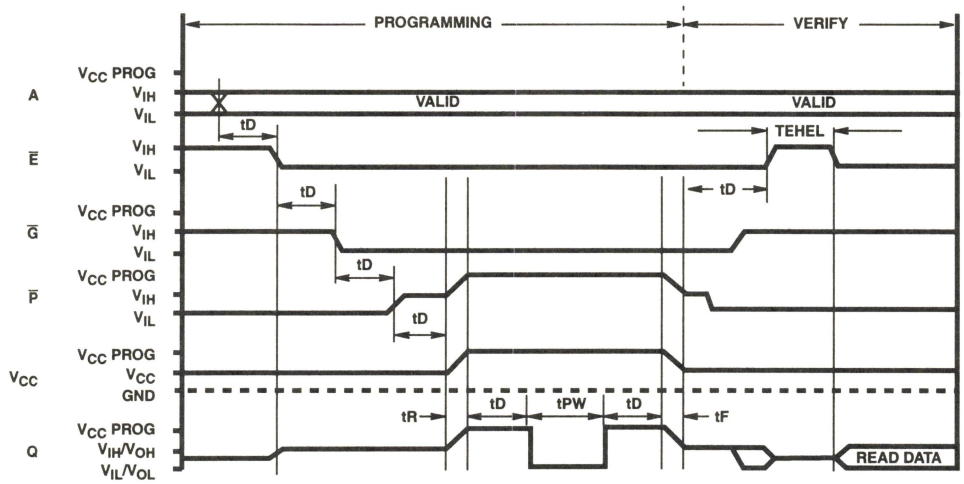


FIGURE 1. HM-6617 PROGRAMMING CYCLE

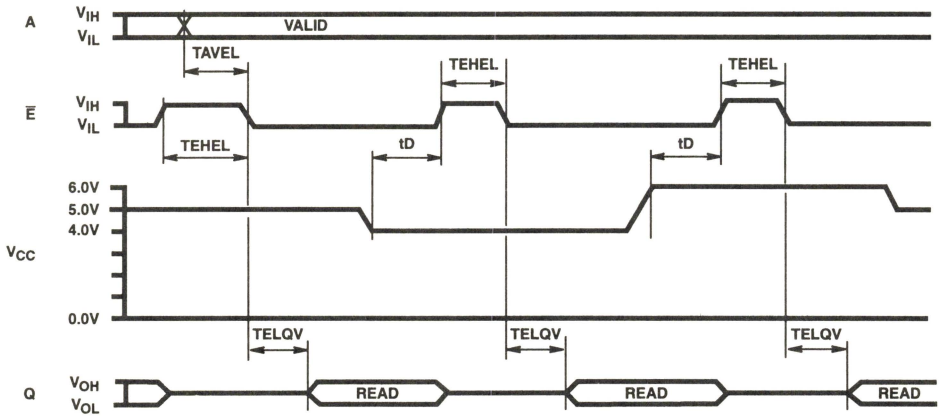


FIGURE 2. HM-6617 POST PROGRAMMING VERIFY CYCLE

Background Information HM-6617 Programming

Programming Specifications

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{IL}	Input "0"	0.0	0.2	0.8	V
V_{IH}	Voltage "1" (Note 6)	VCC-2	V_{CC}	VCC+0.3	V
VCCPROG	Programming V_{CC} (Note 2)	12.0	12.0	12.5	V
V_{CC1}	Operating V_{CC}	4.5	5.5	5.5	V
V_{CC2}	Special Verify V_{CC} (Note 3)	4.0	-	6.0	V
tD	Delay Time	1.0	1.0	-	µs
tR	Rise Time	1.0	10.0	10.0	µs
tF	Fall Time	1.0	10.0	10.0	µs
TEHEL	Chip Enable Pulse Width	50	-	-	ns
TAVEL	Address Valid to Chip Enable Low Time	20	-	-	ns
TELQV	Chip Enable Low to Output Valid Time	-	-	120	ns
tPW	Programming Pulse Width (Note 4)	90	100	110	µs
tIP	Input Leakage at V_{CC} = VCCPROG	-10	+1.0	10	µA
IOP	Data Output Current at V_{CC} = VCCPROG	-	-5.0	-10	mA
Rn	Output Pull-Up Resistor (Note 5)	5	10	15	kΩ
T_A	Ambient Temperature	-	25	-	°C

NOTES:

1. All inputs must track V_{CC} (pin 24) within these limits.
2. VCCPROG must be capable of supplying 500mA.
3. See Steps 22 through 29 of the Programming Algorithm.
4. See Step 11 of the Programming Algorithm.
5. All outputs should be pulled up to V_{CC} through a resistor of value Rn.
6. Except during programming (See Programming Cycle Waveforms).

Absolute Maximum Ratings

Supply Voltage (All Voltages Reference to Device GND) . . . . . +7.0V
Input or Output Voltage Applied for All Grades. . . . . GND -0.3V to V_{CC} +0.3V
Typical Derating Factor . . . . . 5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range: HM-6617-9, B-9 . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
SBDIP Package	48°C/W	9°C/W
Slim SBDIP	65°C/W	14°C/W
CLCC Package	58°C/W	19°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 5473 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications V_{CC} = 5V ±10%; (HM-6617B-9, HM-6617-9)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.4	VCC+0.3	V	V_{CC} = 5.5V
V_{IL}	Logical Zero Input Voltage	-0.3	0.8	V	V_{CC} = 4.5V
VOH1	Logical One Output Voltage	2.4	-	V	I_{OH} = -2.0mA, V_{CC} = 4.5V
VOH2	Logical One Output Voltage (Note 2)	VCC-1.0	-	V	I_{OH} = -100µA, V_{CC} = 4.5V
VOL	Logical Zero Output Voltage	-	0.4	V	I_{OL} = +4.8mA, V_{CC} = 4.5V
II	Input Leakage	-1.0	+1.0	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V
IOZ	Output Leakage	-1.0	+1.0	µA	V_O = V_{CC} or GND, $\overline{G}$ = V_{CC}, V_{CC} = 5.5V
ICCSB	Standby Power Supply Current	-	100	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, I_O = 0
ICCOP	Operating Power Supply Current (Note 3)	-	20	mA	f = 1MHz, V_{CC} = 5.5V, I_O = 0, V_{IN} = V_{CC} or GND

AC Electrical Specifications

SYMBOL		PARAMETER	HM-6617B-9		HM-6617-9		UNITS	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
(1)	TAVQV	Address Access Time	-	105	-	140	ns	(Notes 1, 4)
(2)	TELQV	Chip Enable Access Time	-	90	-	120	ns	(Notes 1, 4)
(3)	TELQX	Chip Enable Time	5	-	5	-	ns	(Notes 2, 4)
(4)	TAVEL	Address Setup Time	15	-	20	-	ns	(Notes 1, 4)
(5)	TELAX	Address Hold Time	20	-	25	-	ns	(Notes 1, 4)
(6)	TELEH	Chip Enable Low Width	95	-	120	-	ns	(Notes 1, 4)
(7)	TEHEL	Chip Enable High Width	40	-	40	-	ns	(Notes 1, 4)
(8)	TELEL	Cycle Time	136	-	160	-	ns	(Notes 1, 4)
(9)	TGLQV	Output Access Time	-	40	-	50	ns	(Notes 1, 4)
(10)	TGLQX	Output Enable Time	5	-	5	-	ns	(Notes 2, 4)
(11)	TGHQZ	Output Disable Time	-	40	-	50	ns	(Notes 2, 4)
(12)	TEHQZ	Chip Enable Disable Time	-	45	-	50	ns	(Notes 2, 4)

Capacitance $T_A = +25^oC$

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CIN	Input Capacitance (Note 2)	10	pF	f = 1MHz, All Measurement are Referenced to Device GND
COUT	Output Capacitance (Note 2)	12	pF	f = 1MHz, All Measurement are Referenced to Device GND

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. V_{CC} = 4.5V and 5.5V.

Switching Waveforms

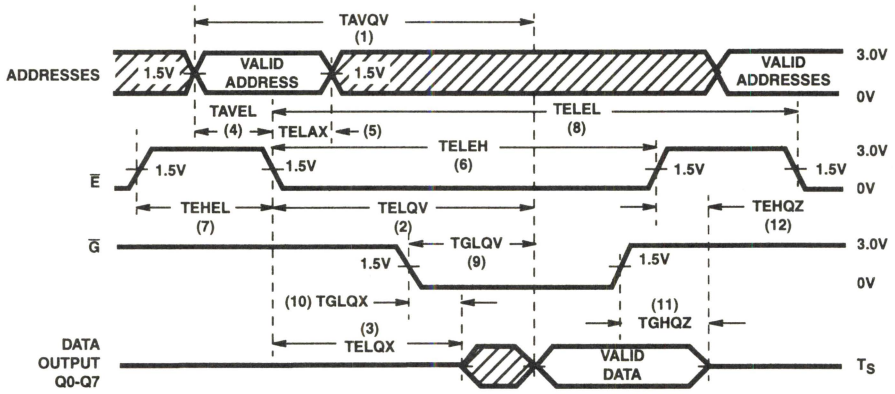


FIGURE 3. READ CYCLE

Test Circuit

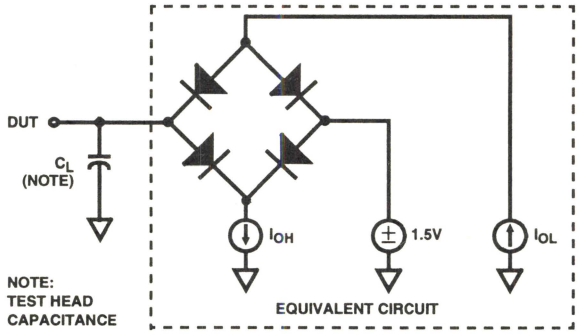


FIGURE 4. TEST CIRCUIT

HM-6642/883

March 1997

512 x 8 CMOS PROM

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Power Standby and Operating Power**
  - **ICCSB 100µA**
  - **ICCOP . . . . . 20mA at 1MHz**
- **Fast Access Time. 120/200ns**
- **Wide Operating . . . . . -55°C to +125°C**
- **Temperature Range**
- **Industry Standard Pinout**
- **Single 5.0V Supply**
- **CMOS/TTL Compatible Inputs**
- **Field Programmable**
- **Synchronous Operation**
- **On-Chip Address Latches**
- **Separate Output Enable**

Ordering Information

PACKAGE	TEMP. RANGE	120ns	200ns	PKG. NO.
SBDIP	-55°C to +125°C	HM1-6642B/883	HM1-6642/883	D24.6
SLIM SBDIP	-55°C to +125°C	HM6-6642B/883	HM6-6642/883	D24.3
CLCC	-55°C to +125°C	-	HM4-6642/883	J28.A

Description

The HM-6642/883 is a 512 x 8 CMOS NiCr fusible link Programmable Read Only Memory in the popular 24 pin, byte wide pinout. Synchronous circuit design techniques combine with CMOS processing to give this device high speed performance with very low power dissipation.

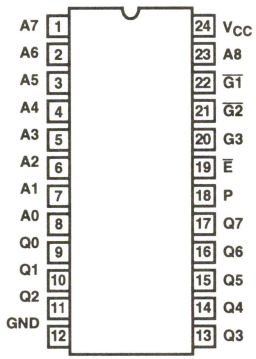
On-chip address latches are provided, allowing easy interfacing with recent generation microprocessors that use multiplexed address/data bus structures, such as the 8085. The output enable controls, both active low and active high, further simplify microprocessor system interfacing by allowing output data bus control independent of the chip enable control. The data output latches allow the use of the HM-6642/883 in high speed pipelined architecture systems, and also in synchronous logic replacement functions.

Applications for the HM-6642/883 CMOS PROM include low power hand held microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, processor control store, and synchronous logic replacement.

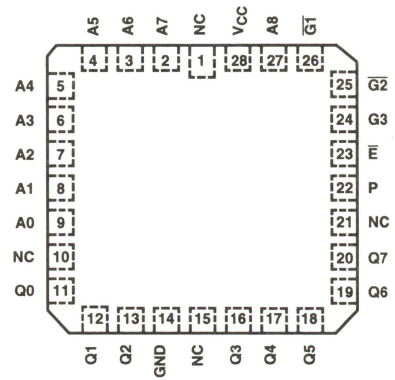
All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

Pinouts

M-6642/883 (BDIP)
TOP VIEW



HM-6642/883 (CLCC)
TOP VIEW



PIN DESCRIPTION

PIN	DESCRIPTION
NC	No Connect
A0-A8	Address Inputs
$\overline{E}$	Chip Enable
Q	Data Output
V_{CC}	Power (+5V)
$\overline{G1}$, $\overline{G2}$, G3	Output Enable
P (Note)	Program Enable

NOTE: P should be hardwired to GND except during programming.

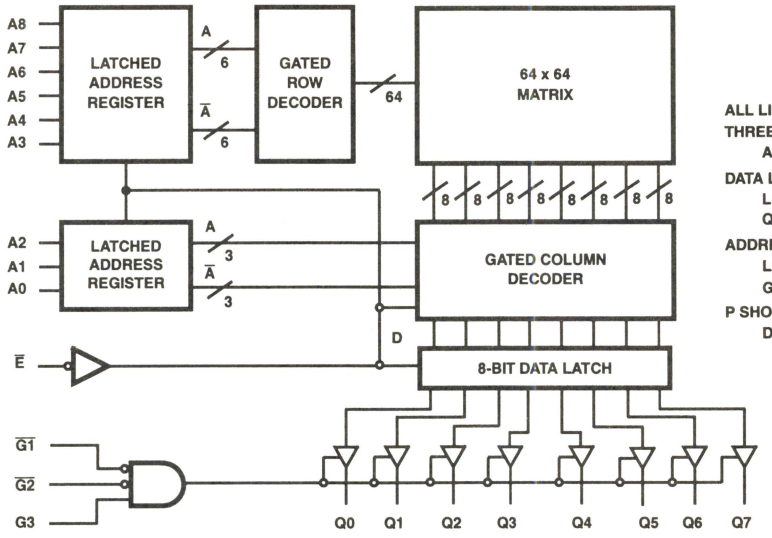
6 CMOS MEMORY

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3013.1**

Functional Diagram



ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

DATA LATCHES:
L HIGH → Q = D
Q LATCHES ON RISING EDGE OF $\overline{E}$

ADDRESS LATCHES AND GATED DECODERS:
LATCH ON FALLING EDGE OF $\overline{E}$
GATE ON FALLING EDGE OF $\overline{E}$

P SHOULD BE HARDWIRED TO GND EXCEPT DURING PROGRAMMING

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND-0.3V to VCC+0.3V
Typical Derating Factor . . . . . 5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . ±4.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . -0.3V to +0.8V
Input High Voltage . . . . . 2.4 to VCC+0.3V

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
SBDIP Package	52°C/W	14°C/W
Slim SBDIP	70°C/W	19°C/W
CLCC Package	58°C/W	14°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 1680 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

TABLE 1. HM-6642/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH	VCC = 4.5V, IO = -1.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = +3.2mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 5.5V, VI/O = GND or VCC	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC, P Not Tested	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Standby Supply Current	ICCSB	VI = VCC or GND, VCC = 5.5V, IO = 0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	µA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = GND, G = VCC, (Note 3), f = 1MHz,IO = 0mA, VI = VCC or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	20	mA
Functional Test	FT	VCC = 4.5V (Note 5)	7, 8A, 8B	-55°C ≤ T_A ≤ +125°C	-	-	-

TABLE 2. HM-6642/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2, 4) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS HM-6642B/883 MIN	LIMITS HM-6642B/883 MAX	LIMITS HM-6642/883 MIN	LIMITS HM-6642/883 MAX	UNITS
Address Access Time	TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	140	-	220	ns
Output Enable Access Time	TGVQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	50	-	150	ns
Chip Enable Access Time	TELQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	120	-	200	ns
Address Setup Time	TAVEL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	20	-	20	-	ns
Address Hold Time	TELAX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	25	-	60	-	ns
Chip Enable Low Width	TELEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	120	-	200	-	ns
Chip Enable High Width	TEHEL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	40	-	150	-	ns

TABLE 2. HM-6642/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2, 4) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS				UNITS
					HM-6642B/883		HM-6642/883		
					MIN	MAX	MIN	MAX	
Read Cycle Time	TELEL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^{o}C \leq T_A \leq +125^{o}C$	160	-	350	-	ns

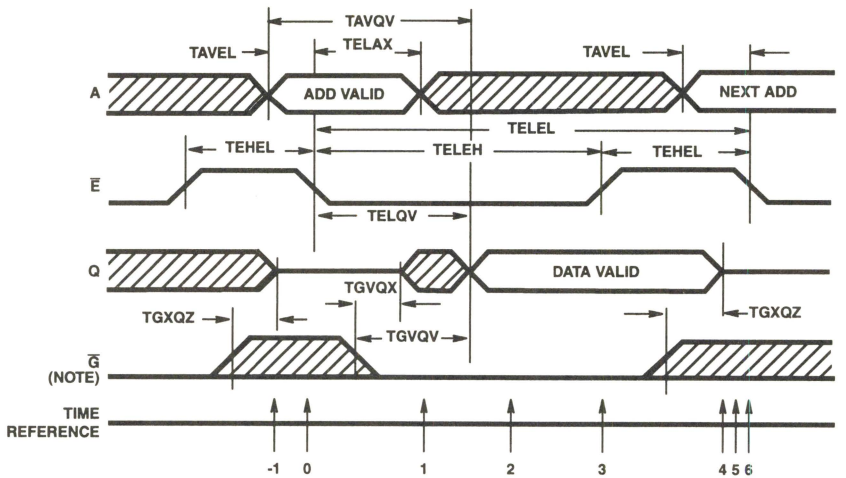
NOTES:

1. All voltages referenced to VSS.
2. A.C. measurements assume transition time < 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL ≅ 50pF.
3. Typical derating = 5mA/MHz increase in ICCOP.
4. All tests performed with P hardwired to GND.
5. Tested as follows: f = 1MHz, VIH = 2.4V, VIL = 0.8V, IOH = -1mA, IOL = +1mA, VOH ≥ 1.5V, VOL ≤ 1.5V.

TABLE 3. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 7, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Switching Waveform



NOTE: G has the same timing as $\overline{G}$ except signal is inverted.

FIGURE 1. READ CYCLE

Test Load Circuit

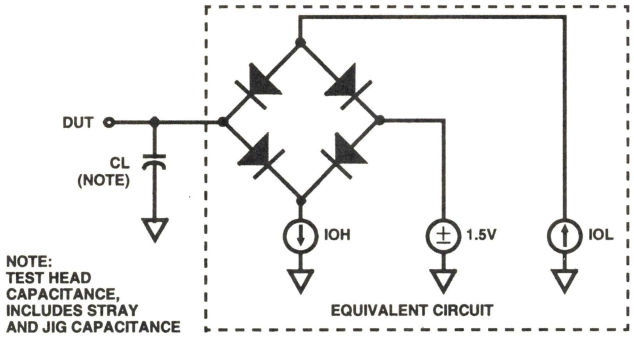
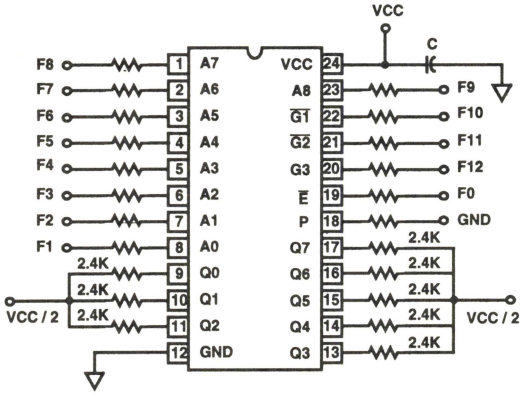


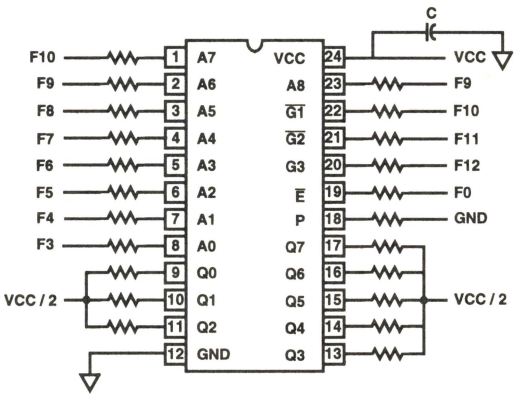
FIGURE 2. TEST LOAD CIRCUIT

Burn-In Circuits

HM-6642/883 (0.300 INCH) SBDIP

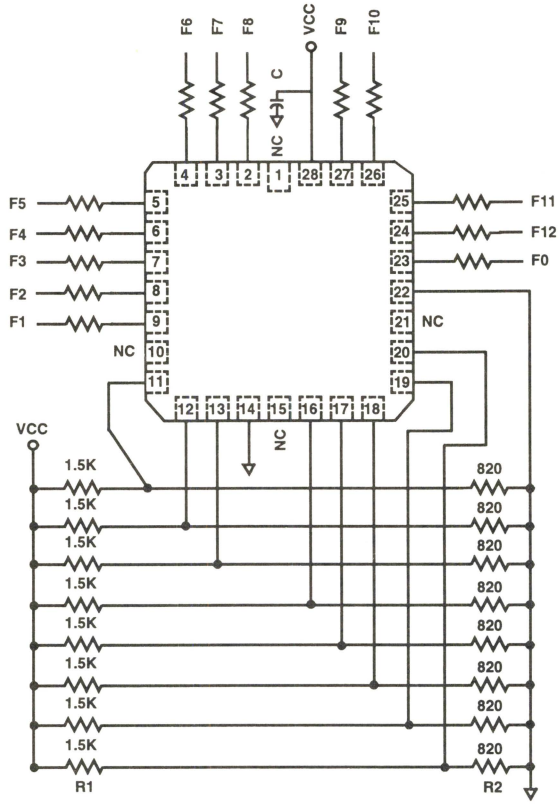


HM-6642/883 (0.600 INCH) SBDIP



Burn-In Circuits (Continued)

HM-6642/883 CLCC



NOTES:

1. F0 = 100kHz ± 10%.
2. All Resistors = 47kΩ.
3. Unless Otherwise Noted.
4. VCC = 5.5V ± 0.5V.
5. VIL = 4.5V ± 10%.
6. C = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
136 x 168 x 19 ± 1mils

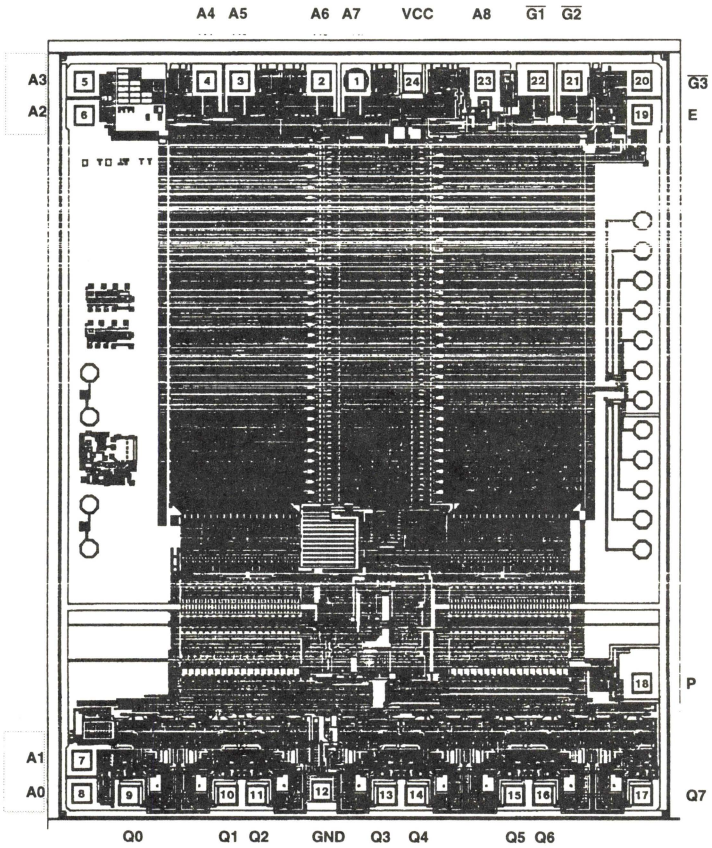
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 15kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
1.7×10^5 A/cm^2

Metallization Mask Layout

HM-6642/883



HARRIS SEMICONDUCTOR

HM-6617/883

March 1997

2K x 8 CMOS PROM

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Power Standby and Operating Power**
  - **ICCSB 100µA**
  - **ICCOP .....20mA at 1MHz**
- **Fast Access Time..... 90/120ns**
- **Industry Standard Pinout**
- **Single 5.0V Supply**
- **CMOS/TTL Compatible Inputs**
- **High Output Drive ..... 12 LSTTL Loads**
- **Synchronous Operation**
- **On-Chip Address Latches**
- **Separate Output Enable**
- **Operating Temperature Range ..... -55°C to +125°C**

Description

The HM-6617/883 is a 16,384-bit fuse link CMOS PROM in a 2K word by 8-bit/word format with "Three-State" outputs. This PROM is available in the standard 0.600 inch wide 24 pin SBDIP, the 0.300 inch wide slim SBDIP, and the JEDEC standard 32 pad CLCC.

The HM-6617/883 utilizes a synchronous design technique. This includes on-chip address latches and a separate output enable control which makes this device ideal for applications utilizing recent generation microprocessors. This design technique, combined with the Harris advanced self-aligned silicon gate CMOS process technology offers ultra-low standby current. Low ICCSB is ideal for battery applications or other systems with low power requirements.

The Harris NiCr fuse link technology is utilized on this and other Harris CMOS PROMs. This gives the user a PROM with permanent, stable storage characteristics over the full industrial and military temperature voltage ranges. NiCr fuse technology combined with the low power characteristics of CMOS provides an excellent alternative to standard bipolar PROMs or NMOS EPROMs.

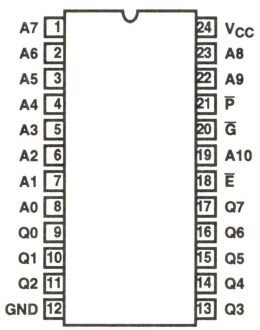
All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

Ordering Information

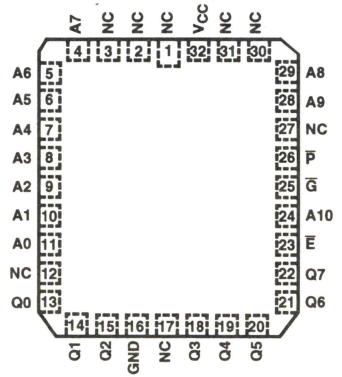
PACKAGE	TEMPERATURE RANGE	90ns	120ns	PACKAGE NO.
SBDIP	-55°C to +125°C	HM1-6617B/883	HM1-6617B/883	D24.6
SLIM SBDIP	-55°C to +125°C	HM6-6617B/883	HM6-6617B/883	D24.3
CLCC	-55°C to +125°C	HM4-6617B/883	HM4-6617B/883	J32.A

Pinouts

HM-6617/883 (SBDIP)
TOP VIEW



HM-6617/883 (CLCC)
TOP VIEW



PIN DESCRIPTION

PIN	DESCRIPTION
NC	No Connect
A0-A10	Address Inputs
$\overline{E}$	Chip Enable
Q	Data Output
V_{CC}	Power (+5V)
$\overline{G}$	Output Enable
$\overline{P}$ (Note)	Program Enable

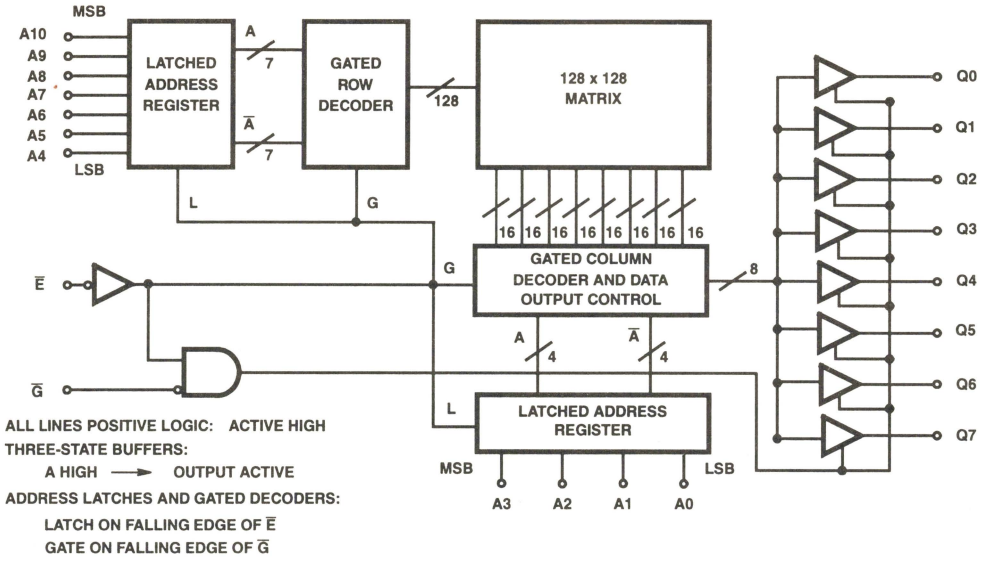
NOTE: $\overline{P}$ should be hardwired to V_{CC} except during programming.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3016.1**

Functional Diagram



ALL LINES POSITIVE LOGIC: ACTIVE HIGH

THREE-STATE BUFFERS:

A HIGH ⟶ OUTPUT ACTIVE

ADDRESS LATCHES AND GATED DECODERS:

LATCH ON FALLING EDGE OF $\overline{E}$

GATE ON FALLING EDGE OF $\overline{G}$

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
Typical Derating Factor . . . . . 5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . -0.3V to +0.8V
Input High Voltage . . . . . +2.4V to VCC +0.3V

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	48°C/W	9°C/W
Slim SBDIP	65°C/W	14°C/W
CLCC Package	58°C/W	19°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 5473 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

TABLE 1. HM-6617/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VCC = 4.5V, IO = -2.0mA	1, 2, 3	-55°C ≤ TA ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = +4.8mA	1, 2, 3	-55°C ≤ TA ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 5.5V, VI/O = GND or VCC	1, 2, 3	-55°C ≤ TA ≤ +125°C	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC, $\overline{P}$ Not Tested	1, 2, 3	-55°C ≤ TA ≤ +125°C	-1.0	1.0	µA
Standby Supply Current	ICCSB	VI = VCC or GND, VCC = 5.5V, IO = 0mA	1, 2, 3	-55°C ≤ TA ≤ +125°C	-	100	µA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = GND, (Note 3), f = 1MHz, IO = 0mA, VI = VCC or GND	1, 2, 3	-55°C ≤ TA ≤ +125°C	-	20	mA
Functional Test	FT	VCC = 4.5V (Note 6)	7, 8A, 8B	-55°C ≤ TA ≤ +125°C	-	-	

TABLE 2. HM-6617/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS HM-6617B/883 MIN	LIMITS HM-6617B/883 MAX	LIMITS HM-6617/883 MIN	LIMITS HM-6617/883 MAX	UNITS
Address Access Time	TAVQV	VCC = 4.5V and 5.5V (Note 5)	9, 10, 11	-55°C ≤ TA ≤ +125°C	-	105	-	140	ns
Output Enable Access Time	TGLQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ TA ≤ +125°C	-	40	-	50	ns
Chip Enable Access Time	TELQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ TA ≤ +125°C	-	90	-	120	ns
Address Setup Time	TAVEL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ TA ≤ +125°C	15	-	20	-	ns
Address Hold Time	TELAX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ TA ≤ +125°C	20	-	25	-	ns
Chip Enable Low Width	TELEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ TA ≤ +125°C	95	-	120	-	ns
Chip Enable High Width	TEHEL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ TA ≤ +125°C	40	-	40	-	ns

TABLE 2. HM-6617/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS HM-6617B/883		LIMITS HM-6617/883		UNITS
					MIN	MAX	MIN	MAX	
Read Cycle Time	TELEL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^{o}C \leq TA \leq +125^{o}C$	136	-	160	-	ns

NOTES:

1. All voltages referenced to Device GND.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL ≅ 50pF.
3. Typical derating = 5mA/MHz increase in ICCOP.
4. All tests performed with $\overline{P}$ hardwired to VCC.
5. TAVQV = TELQV + TAVEL.
6. Tested as follows: f = 1MHz, VIH = 2.4V, VIL = 0.8V, IOH = -1mA, IOL = +1mA, VOH ≥ 1.5V, VOL ≤ 1.5V.

TABLE 3. HM-6617/883 AC AND DC ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	NOTES	TEMPERATURE	LIMITS HM-6617B/883		LIMITS HM-6617/883		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	CIN	VCC = Open, f = 1MHz, All Measurements Referenced to Device GND	2, 3	$+25^{o}C$	-	10	-	10	pF
		VCC = Open, f = 1MHz, All Measurements Referenced to Device GND	2, 4	$+25^{o}C$	-	12	-	12	pF
			2, 5	$+25^{o}C$	-	10	-	10	pF
I/O Capacitance	CI/O	VCC = Open, f = 1MHz, All Measurements Referenced to Device GND	2, 3	$+25^{o}C$	-	12	-	12	pF
		VCC = Open, f = 1MHz, All Measurements Referenced to Device GND	2, 4	$+25^{o}C$	-	14	-	14	pF
			2, 5	$+25^{o}C$	-	12	-	12	pF
Chip Enable Time	TELQX	VCC = 4.5V and 5.5V	2	$-55^{o}C \leq TA \leq +125^{o}C$	5	-	5	-	ns
Output Enable Time	TGLQX	VCC = 4.5V and 5.5V	2	$-55^{o}C \leq TA \leq +125^{o}C$	5	-	5	-	ns
Chip Disable Time	TEHQZ	VCC = 4.5V and 5.5V	2	$-55^{o}C \leq TA \leq +125^{o}C$	-	45	-	50	ns
Output Disable Time	TGHQZ	VCC = 4.5V and 5.5V	2	$-55^{o}C \leq TA \leq +125^{o}C$	-	40	-	50	ns
Output High Voltage	VOH2	VCC = 4.5V, IO = 100μA	2	$-55^{o}C \leq TA \leq +125^{o}C$	VCC-1V	-	VCC-1V	-	V

NOTES:

1. All tests performed with $\overline{P}$ hardwired to VCC.
2. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design changes which would affect these characteristics.
3. Applies to 0.600 inch SBDIP device types only.
4. Applies to 0.300 inch SBDIP device types only.
5. Applies to Ceramic Leadless Chip Carrier (CLCC) device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Switching Waveforms

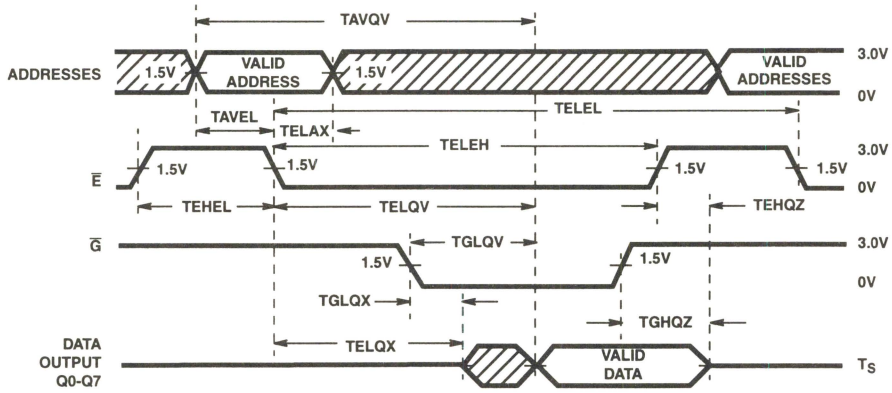


FIGURE 1. READ CYCLE

Test Circuit

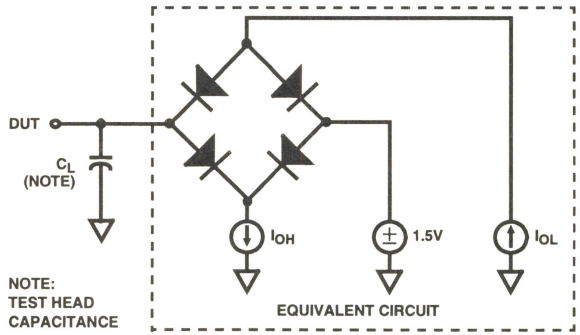
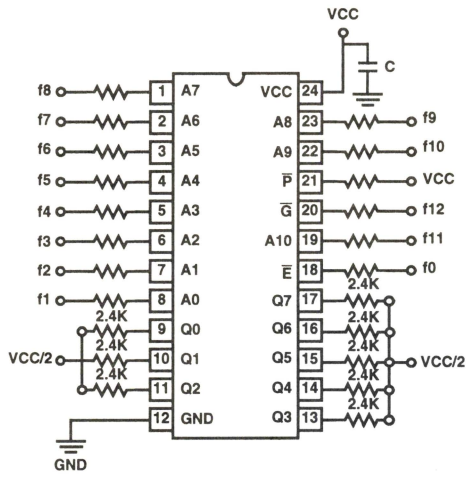


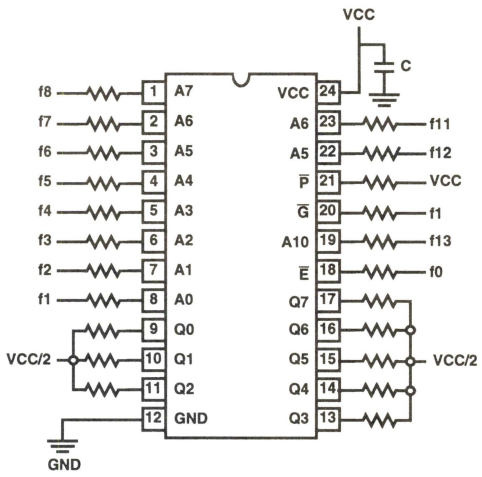
FIGURE 2. TEST CIRCUIT

Burn-In Circuits

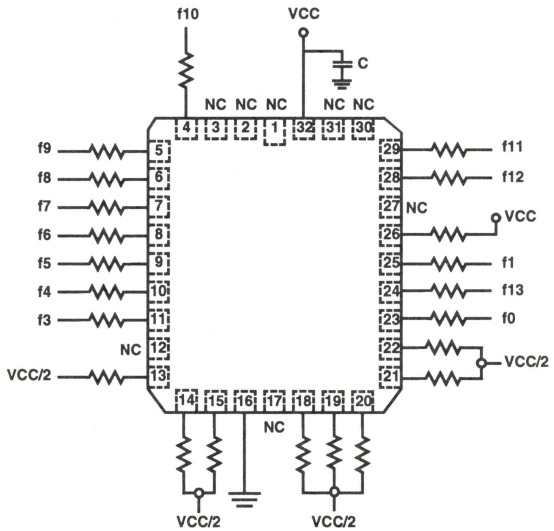
HM-6617/883 (.300 INCH) SBDIP



HM-6617/883 (.600 INCH) SBDIP



HM-6617/883 CLCC



NOTES:
f0 = 100KHz ± 10%.
All resistors = 47kΩ Unless Otherwise Noted.
VCC = 5.5V ± 0.05V.
C = 0.01 µF min.

Die Characteristics

DIE DIMENSIONS:
140 x 232 x 19 ± 1mils

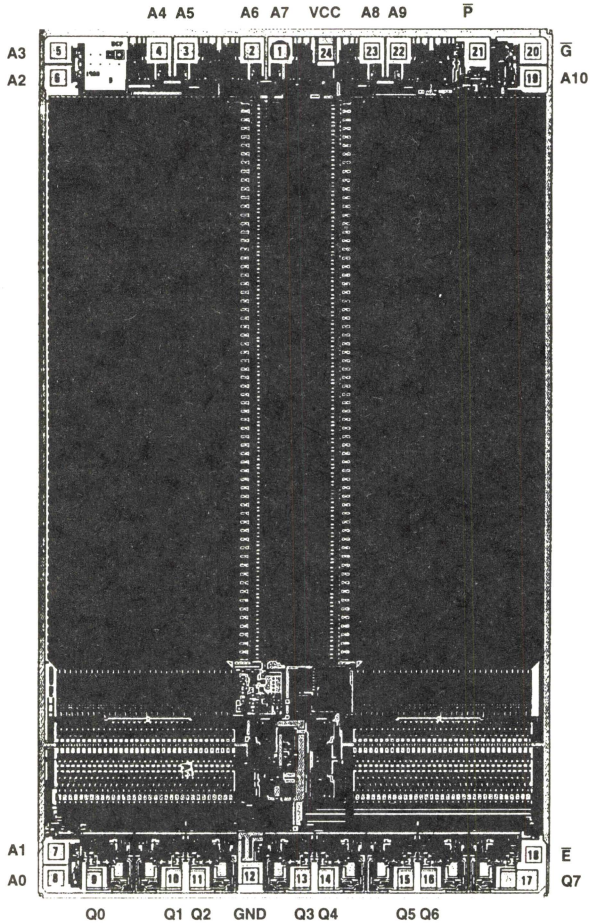
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 15kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 7kÅ ± 9kÅ

WORST CASE CURRENT DENSITY:
1.7×10^5 A/cm^2

Metallization Mask Layout

HM-6617/883



MICROPROCESSOR PRODUCTS 7

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No. AN108.1 March 1997

Harris Digital

82C52 Programmable UART

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Introduction

The 82C52 CMOS Programmable UART can be utilized for serial communications at data rates from DC to 1M baud using clock speeds in the range of 0-16MHz. In addition, the device provides an internal baud rate generator.

In the following discussion, we will look at the functional capabilities of the 82C52, and give information on how the device can be programmed. The following topics will be discussed:

(1) Glossary of communications terms

(2) Control registers

(3) Status registers

(4) Transmit/Receive Buffer Registers

(5) I/O Addressing methods

(6) Reset of the 82C52

(7) Programming the 82C52

1.0 Glossary of Data Communication Terms

1.1 Clear to Send ($\overline{CTS}$):

Clear-to-send is an input signal to the 82C52. It is provided by the device with which the 82C52 is communicating, such as a modem. When this signal is in its active state (active low), the 82C52 is being told that the modem will accept data sent to it from the 82C52 Serial Data Out (SDO) pin.

The $\overline{CTS}$ signal is specified in the RS-232C protocol and is used in conjunction with the Request to Send ($\overline{RTS}$) signal. This signal is used mainly in half-duplex systems. In a half-duplex system communications can be performed in both directions, but in only one direction at a time.

To illustrate this: Suppose we are using the 82C52 to communicate over an RS-232C link to a modem. In half-duplex operation the UART tells the modem that it wishes to transmit a character by putting $\overline{RTS}$ into its active state (active low for the 82C52). The modem, if ready for the data, will respond by driving the 82C52's $\overline{CTS}$ line to its active state (low). When the 82C52 recognizes this, it will then begin data transmission.

1.2 Data Set Ready ($\overline{DSR}$):

This is also an input signal to the 82C52. When in its active state, it signifies that the device with which it is to communicate is powered on and ready for communications. When using a modem, an active state for this signal indicates that the modem is also connected to a communications line (is on line).

1.3 Data Terminal Ready (DTR):

This is an output signal generated by the 82C52. Its purpose is to inform the target (i.e. modem) that it is ready for communications.

1.4 Framing Error:

Each time the 82C52 receives a character of data, it will check for 3 types of errors: (1) Parity error, (2) Framing error, and (3) Overrun error.

When reading characters through the Serial Data In (SDI) pin, the 82C52 will first encounter a start bit. This start bit is a logical zero, and is detected by the first falling edge of the signal on SDI. Next, the 82C52 will see a specified number of data bits followed by the parity bit. The parity bit is checked for a parity error (see 1.8 and 1.9). The stop bits are then checked for a framing error.

A framing error occurs when an incorrect stop bit is found, or if there are too few stop bits. This happens most often when the baud rates between the communicating devices differ. The data will have a tendency to become skewed. For information on this skewing problem, see 1.10.

1.5 Interrupt Driven I/O:

This is a method of handling interaction between a CPU and an I/O device. In this scheme, the I/O device will issue an interrupt to the CPU when it requires attention.

With the 82C52, an interrupt might occur when (1) the device receives a character on its SDI pin, (2) the device completes transmission of a character, (3) an error is found in a received character, or (4) a change was detected in one of the modem control lines.

After the interrupt is recognized by the CPU, it (the CPU) will go to the corresponding Interrupt Service Routine(ISR). This routine decides how the interrupt should be serviced, and then services it. Upon completion of the ISR, execution of the user's software will resume at the point where the interrupt occurred.

1.6 I/O Polling:

A second method for handling interaction between a CPU and an I/O device. Rather than waiting for an I/O device to interrupt the CPU, the software assumes the responsibility of checking to see if an I/O device needs servicing.

When the system software needs to output to the 82C52, it will poll (look at) the device to see if it is ready to accept data. Similarly, in order to receive data from the 82C52, the software will poll to see if there is any data waiting to be read in. Once read, the software must test the status of the 82C52 to see if any errors were detected in the data received. The software must also look for status changes in the modem control lines.

1.7 Overrun Error:

With the 82C52, data is received on the SDI pin. From there it is shifted serially into the Receiver Register. Once in this register, it will be shifted (in parallel) into the Receive Buffer Register (RBR) should this register be empty. Should it not be empty, the data cannot be shifted into the RBR. However, subsequent data coming in on the SDI pin will be shifted into the Receiver Register, overwriting the data already there. This causes the 82C52 to flag an overrun error.

To clear the RBR, data must be read from it by the CPU. This data must be read faster than the data is being received on SDI and written to the Receiver Register. In most cases, this problem must be dealt with in software: (1) Either the receive data routine must be optimized for better performance, or (2) The baud rate must be lowered to compensate for the data loss.

1.8 Parity:

Parity is a form of error detection commonly used in serial communications. In parity checking, the sending device generates and sends an extra bit with each character transmitted. The state of this bit (0 or 1) is determined by (1) the number of 1 bits in the character transmitted, and (2) by whether parity was defined to be even or odd.

With even parity, the parity bit is generated such that the number of one' bits in the character (including the parity bit) is an even number. For example, if a word has 5-bits that are ones, the parity bit must be set to a one so that the total number of 'one' bits is an even number. If a character being sent has 6-bits set to a one, the parity bit will be zero. This still gives an even number of one bits in the character.

Conversely, in odd parity, the parity bit is generated such that the total number of 1 bits (including the parity bit) is an odd number. For a character having 5 one bits, the parity bit generated is a zero. For a character having 6 one bits, the parity bit is set to one

CHARACTER SENT	(EVEN) PARITY BIT	(ODD) PARITY BIT
01101110	1	0
11111010	0	1

FIGURE 1. PARITY

1.9 Parity Error:

This is caused by an invalid parity bit being detected in a character received. The condition occurs when (A) even parity is specified and an odd number of 'one' bits are detected in the character, or (B) odd parity is specified and an even number of 'one' bits are detected.

For example, if the character 6EH (01101110 b) is received by the device, and the parity bit read in is a 1, a parity error would be flagged if parity was defined to be ODD. Should parity be set to EVEN and the parity bit is a 1 for this same character, a parity error will not be flagged.

1.10 Percentage Error in Baud Rate Generation:

When exchanging data between two systems through serial links (i.e., RS-232C) it is important that the baud rates of the two systems be as equal as possible. Roughly speaking, these baud rates should not differ by more than 2%. For example, if system X is using an 82C52 to generate 1200 bits per second (bps), and system Y with which it is communicating is generating 1244bps, there is a 3.67% difference in the baud rates. Errors may occur when data is received by system X.

The 82C52 samples the data being received on the SDI pin beginning from when the receiver detects a start bit. This is denoted by a high-to-low transition on the SDI pin. Based on the specified baud rate, the 82C52 will count and sample such that each bit is read at the center of a bit period. Figure 2 shows a character generated at 1200bps, and sampled for 10-bit periods (S0 - S10). The character is 1B Hex with even parity.

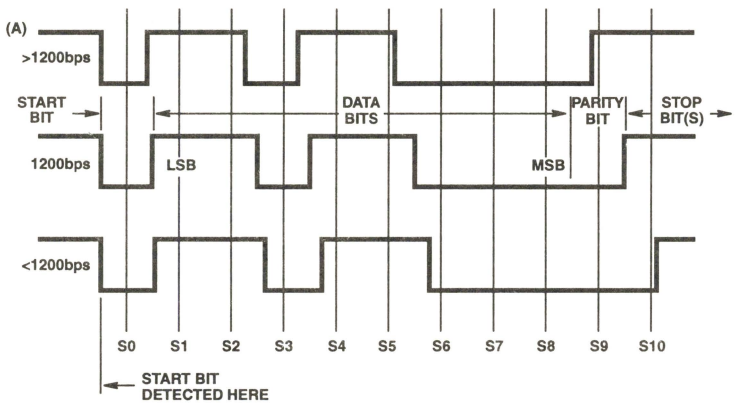


FIGURE 2. PERCENTAGE ERROR

Assume that system X is configured to transmit and receive at 1200bps. The system we are communicating with is running slightly faster as stated above (1244bps). Our sampling rate will still be based upon 1200bps, but the sampling of the incoming signal will be off by a short time period. With each sample this error accumulates. Thus, the skewing to the right becomes greater over time. By the time we normally would be sampling the parity bit (S9), the stop bit(s) would be coming in over the SDI pin (see Figure 2A). In this case, the 82C52 thinks it is sampling the parity bit when in fact, what it is seeing is really the stop bit. This could cause a parity error to be flagged.

Conversely, if data is being received at a baud rate slightly less than our specified baud rate, we would get a skewing of the received data in the opposite direction. From Figure 2C, we see that at S10 we are checking the stop bit, but system Y is still transmitting the parity bit. Therefore, the Framing error will be flagged.

1.11 Request To Send ($\overline{RTS}$):

This signal is an output of the 82C52. It is used to inform a modem or remote system that it wishes to transmit data. The modem (remote system) would then respond by activating the $\overline{CTS}$ signal. As with the $\overline{CTS}$, this signal is of most value in half-duplex communications.

2.0 Control Registers

In order for the 82C52 to properly operate in a system, it must be configured for the desired form of operation. The user must decide how the device will be used in the system, and know the communications protocol of the device it will be communicating with. For example, in a system communicating with a modem we would need to utilize the modem control lines. When using the 82C52 in a local area network these modem control lines may be of no use to us.

The 82C52 is initialized and configured by writing a series of control words from the CPU to various control registers in the device. These registers include the UART Control Register (UCR), the Baud Rate Selector Register(BRSR), and the Modem Control Register (MCR).

UCR: Defines the format of characters being transmitted. The format of the characters includes the number of data bits, parity control, and the number of stop bits.

BRSR: Used in setting up the internal baud rate generator in the 82C52 for a specific baud rate. It will also be used to specify what the CO output is to be.

MCR: Defines which interrupts will be enabled, and will also set the modem control output lines ($\overline{RTS}$ and $\overline{DTR}$). In addition, the MCR allows the user to select one of four modes of communications (normal mode, echo mode, transmit break, and loop test mode).

2.1 UART Control Register

The UART Control Register (UCR) is a write-only register. Writing a command word to the UCR configures the transmission and reception circuitry of the 82C52. The command word essentially describes the format of characters that are to be transmitted or received. The format of these characters are made up of (1) a specific word length, (2) parity information, and (3) a selected number of stop bits, used to indicate transmission of that character is completed.

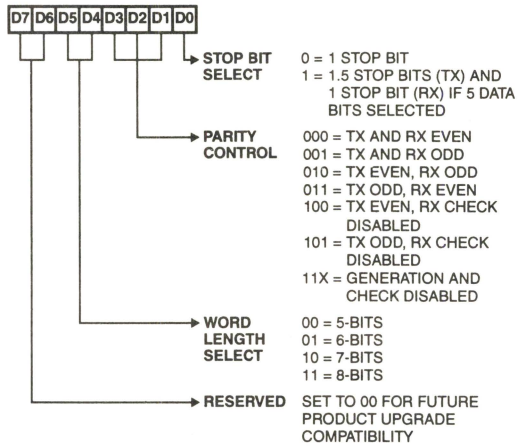


FIGURE 3. UCR FORMAT

D0 – Stop Bit Select. This bit is used to select the number of stop bits that the 82C52 will insert into a character to be transmitted, and the number to look for in received characters. The stop bit(s) denote where the end of a character occurs. The external device must be configured with the same number of stop bits as the 82C52. The setting(s) for this bit are as follows:

0 – If this bit is set to zero, then a single stop bit will be generated and checked for.

1 – Setting this bit to a one will cause either of two configurations. If we select a character length of 5 data bits, the 82C52 will generate 1.5 stop bits during transmission, and will look for a single stop bit when receiving data. If a character length of 6, 7, or 8 data bits is selected, then two (2) stop bits will be generated and checked for.

D3, D2 and D1 – Parity Control. These three bits are used to control the generation and checking of the parity bit. The 82C52 can be configured to perform this function one of seven ways. These are:

000 – Even parity is generated for transmitting data, and will be checked for when receiving data.

001 – Odd parity is generated for transmitting data, and checked for during data reception.

010 – Even parity is generated for data transmission, and odd parity will be checked for during data reception.

011 – Odd parity is generated for data transmission, and even parity will be checked for during data reception.

100 – Even parity is generated for data transmission, however, the 82C52 will do no parity checking on data that has been received.

101 – Odd parity is generated for data transmission. The 82C52 will not check parity on data received.

11X – The generation of a parity bit is disabled. Also, the 82C52 will not check for parity on incoming data. D1 is not used therefore, it can be either a 0 or a 1.

TABLE 1. PARITY SELECTION

	TRANSMITTER	RECEIVER
000	Even	Even
001	Odd	Odd
010	Even	Odd
011	Odd	Even
100	Even	Disabled
101	Odd	Disabled
11X	Disabled	Disabled

D5, D4 – Word Length Select. The state of these bits determines the number of bits that are transmitted as a data word. The word length can be 5, 6, 7, or 8-bits long.

TABLE 2. WORD LENGTH SELECTION

D5	D4	WORD LENGTH
0	0	5-Bits
0	1	6-Bits
1	0	7-Bits
1	1	8-Bits

D7, D6 – Reserved. These bits have been reserved for future product upgrade compatibility. To insure that the future upgrades of the 82C52 will operate with existing software, these bits must both be set to zero (00).

2.2 Baud Rate Select Register

The Baud Rate Select Register (BRSR) is a write-only register used to set the internal 82C52 baud rate generator to the desired data transfer rate. Essentially, this baud rate will depend upon the clock speed of the crystal being used with the device. However, to provide more flexibility, the 82C52 provides two separate counters for selecting a divide ratio to fit the user's needs.

These two counters are the Prescaler, and the Divisor select. The Prescaler allows the input clock rate to be divided by one of four values: 1, 3, 4, and 5. This new data rate can then be further divided by using the values available with the Divisor select. This final clock speed will be 16 times the actual baud rate used by the 82C52.

The 16X clock speed can be output to the CO pin of the device through the CO Select function of the BRSR. If CO select is not selected, the output of the CO pin will reflect the crystal frequency input by the part on the IX pin. Note, this output (CO) is a buffered version of the IX input or 16X baud rate.

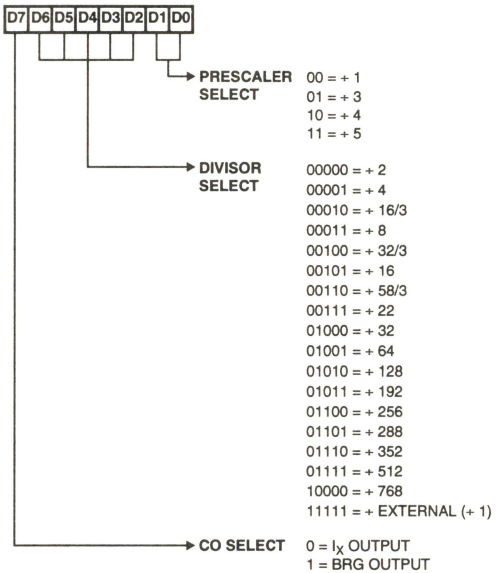


FIGURE 4. BRSR FORMAT

D1 and D0 – Prescaler Select. This allows the user to choose one of four values that the input clock frequency (IX) will be divided by.

TABLE 3. PRESCALER SELECTION

D1	D0	PRESCALER DIVISOR
0	0	÷1
0	1	÷3
1	0	÷4
1	1	÷5

D6, D5, D4, D3, and D2 – Divisor Select. The state of these bits determines the value of the Divisor select. The possible values are as follows in Table 4:

TABLE 4. DIVISOR SELECTION

D6 - D2	DIVISOR
00000	÷2
00001	÷4
00010	÷16/3
00011	÷8
00100	÷32/3
00101	÷16
00110	÷58/3
00111	÷22
01000	÷32
01001	÷64
01010	÷128
01011	÷192
01100	÷256
01101	÷288
01110	÷352
01111	÷512
10000	÷768
11111	÷1

By using a crystal or external frequency with one of the common crystal frequencies (1.8432MHz, 2.4576MHz, or 3.072MHz) and a prescaler of divide by 3, 4, or 5 respectively, standard baud rates can easily be generated by selecting the Divisor as shown in Table 5 below:

TABLE 5. STANDARD DIVISORS

BAUD RATE	DIVISOR
38.4K	External
19.2K	2
9600	4
7200	16/3
4800	8
3600	32/3
2400	16
2000*	58/3
1800*	22
1200	32
600	64
300	128
200	192
150	256
134.5*	288
110*	352
75	512
50	768

NOTE: All baud rates are exact except for:

TABLE 6. PERCENT DIFFERENTIAL

BAUD RATE	ACTUAL	% DIFFERENCE
2000	1986.2	0.69%
800	1745.45	3.03%
134.5	133.33	0.87%
110	109.09	0.83%

To illustrate how a baud rate can be determined, let us look at the following example:

EXAMPLE 2.1:

Assume that we are using a clock frequency of 2.4576MHz with the 82C52, and we wish to configure the device to run at a baud rate of 9600 bits per second (bps). First, select a prescaler of divide-by-four. Therefore, bits D1 and D0 will be set to 1 and 0. This will give an effective clock frequency of 614,400Hz.

Next, look at Table 5 to determine which divisor is needed to generate 9600 bps. The divisor is four (4). Bits 6 through 2 will be set to 0 0 0 0 and 1. The 614,400Hz clock has then been divided by 4 to give the appropriate 16X clock, which is 153,600HZ (16 x 9600).

To determine what the actual baud rate is, take 153,600Hz and divide it by 16. This will give us our 9600 bits per second (bps). A 16X clock rate is required by the internal circuitry of the 82C52. That is why the prescaler and divisor are selected to yield a clock rate that is 16 times the desired baud rate.

Finally, set the CO Select bit to 1 so that the CO output will be the same as the BRG output. This is the 16X frequency calculated above (153,600Hz).

The command word written to the BRSR will be:

10000110 or 86 Hex

D7 – CO Select. This tells the 82C52 what the source will be for the output pin CO.

0 – The output on CO will be a buffered version of the clock input (IX) to the device. The frequency of this signal will be the actual crystal frequency (or external frequency) used to run the 82C52.

1 – The output of CO will be a buffered version of a clock rate that is 16 times the actual baud rate generated by the 82C52. This signal is suitable for driving a second 82C52 or UART in a system.

2.3 Modem Control Register

The Modem Control Register (MCR) is a general purpose register controlling various operation parameters within the device. These parameters include: (1) setting modem control lines $\overline{RTS}$ and $\overline{DTR}$, (2) Enabling the interrupt structure of the device, (3) enabling the receiver on the device, and (4) selecting one of four operating modes in the device.

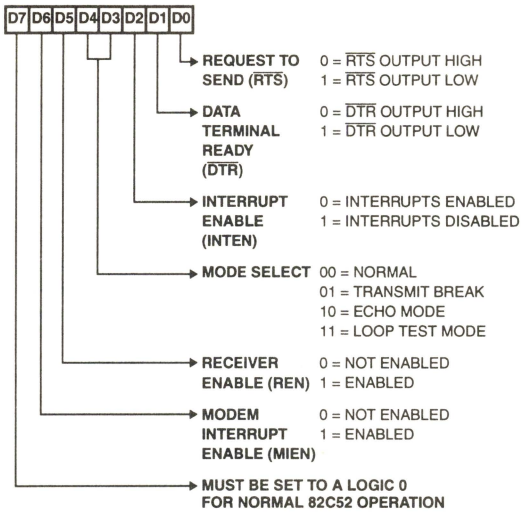


FIGURE 5. MCR FORMAT

D0 – Request to Send. This bit allows the user to set the state of the $\overline{RTS}$ output pin. This pin is used as a modem control line in the RS-232C interface protocol. It is important to remember that the $\overline{RTS}$ output pin is active low.

0 – Setting this bit to a zero causes a one (1) to be output on the $\overline{RTS}$ pin. In effect, this is setting the pin to its logical false state.

1 – If this bit is set to a one, the $\overline{RTS}$ pin will be forced to a zero (0). This puts the $\overline{RTS}$ signal in its logical true state.

D1 – Data Terminal Ready. This is a modem control line for an RS-232C- like interface. It is an output pin and is also active low.

0 – A zero in bit D1 causes $\overline{DTR}$ pin to be put in a logical false state. The $\overline{DTR}$ pin outputs a one (1).

1 – By writing a one to this bit, the 82C52 $\overline{DTR}$ output pin is set to its logical true state (zero).

D2 – Interrupt Enable (INTEN). This bit is an overall control for the INTR pin on the 82C52. With it, all 82C52 interrupts to the processor can either be enabled or disabled. When D2 is reset to disable interrupts, no status changes including modem status changes can cause an interrupt to the processor.

0 – Interrupts are disabled. The INTR pin will be held in a false state (low) so that no interrupt requests to the processor are generated.

1 – Interrupts are enabled. Interrupts will be discussed in more detail later.

D4 and D3 – Mode Select. These two bits allow the user to select one of the four possible operating modes for the 82C52. These are:

00 – Normal mode - The 82C52 is configured for normal full or half duplex communications. Data will not be looped back in any form or fashion between the serial data input pin and the serial data output pin (see Figure 6A).

01 – Transmit break - Selecting this mode of operation will cause the transmitter to transmit break characters only. A break character is composed of all logical zeros for the start, data, parity, and stop bits.

10 – Echo mode - When this is selected, the 82C52 will retransmit data received on the SDI pin out to the SDO pin. In this mode of operation, any data written to the Transmitter Buffer Register will not be sent out on the SDO pin (See Figure 6B).

11 – Loop Test mode - If this mode is selected, the data that normally would be transmitted is internally routed back to the receiver circuitry. The transmitted data will not appear at the SDO pin. Also, data that is received on the SDI pin will be ignored by the device. This mode of operation is useful for performing self test(s) on the device (see Figure 6C).

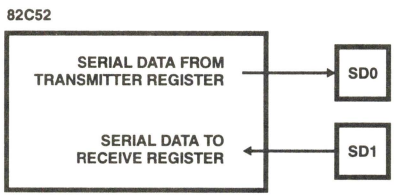


FIGURE 6A. NORMAL MODE

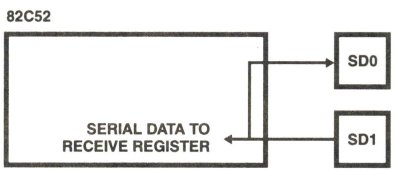


FIGURE 6B. ECHO MODE

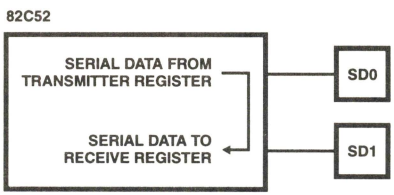


FIGURE 6C. LOOP TEST MODE

FIGURE 6. OPERATING MODES

D5 – Receiver Enable (REN). Controls the reception of data through the SDI pin into the Receiver Register. Disabling the receiver is useful when performing a software reset on the device. This locks out any errant data from being received. This would also prevent interrupts from occurring due to data reception. Other possible reasons for disabling the receiver might be so that sections of software can execute without interruption, so that software only accepts data when ready for it, or so that a software reset/reconfiguration can be performed.

0 - A zero for this bit prevents the device from recognizing data sent to the SDI pin. The receive circuitry will remain in an idle state.

1 - Writing a one to this bit enables the receiver. Data will then be recognized at the SDI pin.

D6 – Modem Interrupt Enable. Enabling this bit will allow any change in the modem status line inputs ($\overline{CTS}$ and $\overline{DSR}$) to cause an interrupt. The Modem Status register (MSR) will contain information pertaining to which condition(s) caused the interrupt.

0 - Modem interrupts not enabled.

1 - Modem interrupts enabled.

D7 – This bit must always be set to a logic zero to insure device compatibility for future product upgrades. Should this bit be set to a one (1) during initialization, the device will not respond to any data at the SDI pin, and no data will be transmitted from the Transmitter Register to the SDO pin.

3.0 Status Registers

In addition to the various Control registers, the 82C52 has two read only status registers that can be accessed by the CPU to determine the status of the device at any given time. These are the UART Status Register (USR), and the Modem Status Register (MSR). The registers are used for keeping track of any changes in (1) the modem lines on the device (2) the status of data transmission or reception, and (3) whether any error(s) were detected in received data.

The USR deals with the different types of data errors, the status of data transmission, as well as data waiting to be read. The MSR, on the other hand, reflects the status of the various modem control lines in the device (i.e. $\overline{CTS}$ and $\overline{DSR}$).

Normally, in an interrupt-driven system, after an interrupt occurs, the user's software would check the status register(s) to determine what caused the interrupt. The software then should deal with the various types of interrupts in an appropriate manner.

3.1 UART Status Register

The UART Status Register (USR) contains information pertaining to the status of the 82C52 operation. The information that is kept in the USR includes: data reception error information, modem status, and the status of data transmission. This register will normally be the first 82C52 register read when servicing an 82C52 interrupt, or when polling the device.

NOTE: The USR will be cleared upon reading its contents.

After reading and clearing the status register, the bits will remain as zeros until a status change occurs to set the proper bit(s).

D0 – Parity error (PE). This bit indicates whether a parity error was detected in the last character read into the Receive Buffer Register. If parity is disabled, this bit will always be a zero.

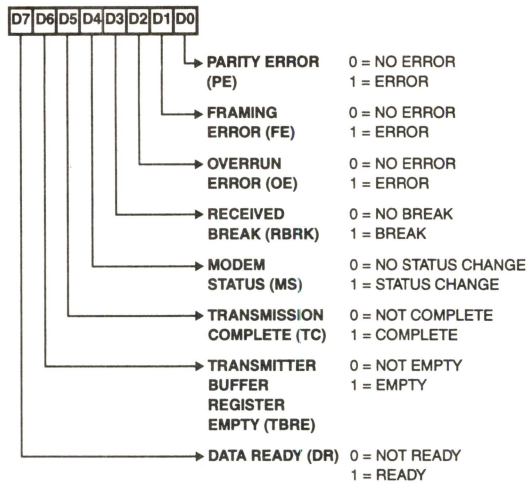


FIGURE 7. USR FORMAT

0 – No error detected.

1 – Parity error detected.

D1 – Framing error (FE). A one in this bit indicates that the last character received contained an improper number of stop bits. This might be caused by no stop bits being sent, or by the length of the stop bits being too short.

0 – No framing error.

1 – Framing error detected.

D2 – Overrun error (OE). When this status bit is set to a one, it indicates that data in the RBR is not being read by the CPU fast enough to permit data in the Receiver Buffer to be shifted to the RBR before the next character comes in on the SDI pin. Data is then lost because it is overwritten by incoming characters.

0 – No overrun error detected.

1 – Overrun error detected.

D3 – Received Break (RBRK). This status bit indicates that the last character received was a break character. A break character consists of all logic zeros including the parity and stop bits. The most common usage of this character is to indicate a special condition in the communications taking place. For example, the device sending information to the 82C52 might send a break character to it to indicate that it has completed transmitting its stream of data.

0 – No break.

1 – Break detected.

D4 – Modem Status (MS). This bit indicates whether or not there has been a change in the states of any of the modem control lines on the device. These lines include: $\overline{CTS}$ and $\overline{DSR}$. To determine which of these lines has changed, the user can read the Modem Status Register (MSR).

Also, should both the MIEN and INTEN bits be set in the MCR register, an interrupt will be generated when the MS bit gets set.

0 – No status change.

1 – Status change detected.

D5 – Transmission Complete (TC). When a character is written to the 82C52 Transmitter Buffer Register (TBR), it will be transferred to the Transmitter Register before actually being shifted out serially through the SDO pin. When the character has finally been transmitted on SDO, and both the TBR and Transmitter Registers are empty, the TC bit will be set.

NOTE: The TC bit getting set does not always mean that an end of transmission has occurred. It indicates that both the TBR and the Transmitter Register are empty. For instance, if we are running the 82C52 at a high baud rate, it could transmit data faster than the user's software can write characters to the device. In this case, the TC bit could get set between each character being transmitted.

Assertion of this bit will cause an interrupt when the INTEN bit of the MCR has been set.

0 – Not complete.

1 – Transmission complete.

D6 – Transmitter Buffer Register Empty (TBRE). When a character written to the TBR has been transferred to the Transmitter Register and the TBR is ready for another character, this bit will get set.

The user should check the TBRE bit before writing another character to the Transmitter Buffer Register. This insures that the previous character written to the TBR no longer resides there, but is being shifted out on the SDO pin.

0 – Not empty.

1 – Empty.

D7 – Data Ready (DR). Is set when the Receive Buffer Register (RBR) has been loaded with a received character through the SDI pin. The CPU can access this data by reading the RBR. For example, if the user wishes to see if there is any data waiting to be read from the Receiver Register, this bit can be checked.

0 – No data ready.

1 – Data ready in RBR.

NOTE: In an interrupt driven system, interrupts caused by the DR signal should have a higher priority than those caused by the TBRE signal. This will guard the software against Overrun errors. You have no control over the information being sent to you, but you can control how and when you are transmitting data.

3.2 Modem Status Register

The Modem Status Register (MSR), a read-only register, allows the user to determine the status of the Modem Status pins. The status of these pins is reflected by the corresponding bit(s) being set to a one if the state of the pin is in its true state (low), and by being set to a zero if the pin is in its false state (high). This will apply regardless of whether the pin is set up to be active high or active low.

A change in any of the status bits will cause an interrupt if the INTEN and MIEN bits of the MCR are enabled.

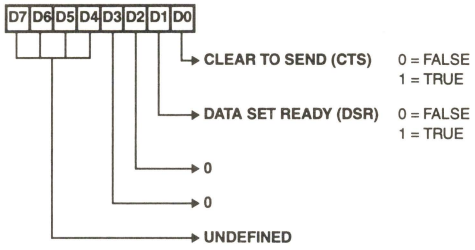


FIGURE 8. MSR FORMAT

D0 – Clear to Send (CTS). This is both a status and control signal from the modem. It tells the 82C52 that the modem is ready to receive data from the 82C52 transmitter output (SDO). If this line is inhibited (false), then the 82C52 will not be able to begin transmission of data. Should this line go false in the middle of a transmission, the UART will only be able to finish transmission of the current character.

0 – CTS in false state.

1 – CTS is true.

D1 – Data Set Ready (DSR). This is a status indicator from the modem to the 82C52 indicating that the modem is ready to provide data to the 82C52.

0 – DSR in false state.

1 – DSR is true.

4.0 Transmit/Receive Buffer Registers

In addition to the control and status registers, the 82C52 has two buffer registers that allow for the actual serial communications to be performed. These registers are used for sending characters out to the SDO pin, and for reading data from the SDI pin.

4.1 Receiver Buffer Register

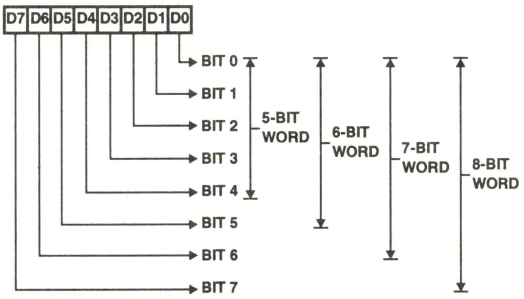
The Receiver Buffer Register (RBR) is a read-only register which contains the character received via the SDI pin. When data is received by the 82C52, it is read serially into the Receiver Register from the SDI pin, and then transferred to the RBR for the CPU's access. This double buffering allows for higher transmission rates without loss of data. However, should additional characters be received by the 82C52 before this register is read, then the Receiver Register will be overwritten with the subsequent characters. This will cause the Overrun Error (OE) flag to be asserted.

The RBR is 8-bits long and can accept data lengths of 5 to 8-bits. The data will be right justified in the register. When selecting data lengths of less than 8-bits, the 82C52 will insert zeros (0) into the RBR for the unused (most significant) bits. For example, if the 82C52 is configured for 6 data bits, and the character 31H is received, the RBR will look as follows when read:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	0	1

FIGURE 9. RECEIVED DATA

Bits D7 and D6 are automatically zeroed out by the 82C52.



NOTE: THE LSB, BIT 0 IS THE FIRST SERIAL DATA BIT RECEIVED

FIGURE 10. RBR FORMAT

4.2 Transmitter Buffer Register

The Transmitter Buffer Register (TBR) is a write only register used for sending characters out through the SDO pin. Characters to be transmitted should only be written to this register when it is empty. This condition can be checked for by reading the UART Status Register (USR) TBRE bit, or waiting for an interrupt to signal this condition.

Like the Receiver circuitry, the Transmitter also uses double buffering. Here, we are taking advantage of the double buffering to increase throughput with the 82C52. The user would first write a character to the TBR. From here it is shifted (in parallel) into a second register known as the Transmit Register. After this transfer has been completed, the TBRE bit is set.

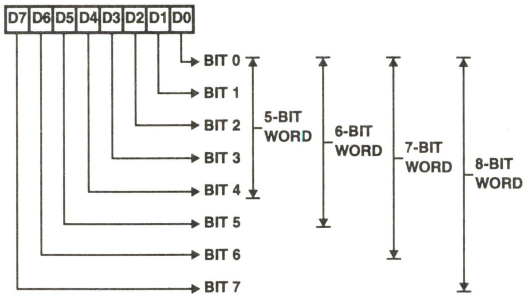
The character shifted into the Transmit Register is then shifted serially out onto the SDO pin. Meanwhile, because the TBR is empty, another character can be written by the CPU to the TBR. In effect, the transmitter circuitry is then performing two operations simultaneously. This double buffering technique allows continuous data flow transmission.

The Transmit Buffer Register is also 8-bits wide. Because we can specify data lengths as being from 5 to 8-bits wide, the 82C52 right justifies the data when it is written to the TBR, and fills the unused bits with zero's. In other words, unused (most significant) bits are truncated. For example, if we set up the device so that 6 data bits are specified and we write the character 71H (01110001 b) to the TBR, we will effectively be transmitting the character:

D7	D6	D5	D 4	D3	D2	D1	D0	
0	0	1	1	0	0	0	1	= 31H

FIGURE 11. TRANSMITTED DATA

The two most significant bits are zeroed out automatically by the 82C52.



NOTE: THE LSB, BIT 0 IS THE FIRST SERIAL DATA BIT TRANSMITTED

FIGURE 12. TBR FORMAT

5.0 I/O Addressing Methods

To utilize the 82C52 in a microprocessor based system, it is necessary for the system to be designed such that we can easily access (address) the device. In the following discussion, we will look at two I/O device addressing schemes that can be applied to the 82C52:

- I/O Mapped Addressing, and

- Memory Mapped I/O Addressing

We will look at these two modes as they apply to an 80C86/80C88-based system.

5.1 I/O Mapped Addressing

In this scheme of I/O addressing, the microprocessor uses one set of instructions for accessing memory, and a different set for accessing I/O devices. The CPU will generate different control signals ($\overline{IO}$/M) to select either memory or I/O based upon the type of instruction it is executing. Because of this, the system needs two sets of control logic for accessing memory and I/O. As we can see in Figure 13, the control logic for each is essentially the same.

When addressing I/O, we would use either the IN instruction or the OUT instruction. The port address specified in the instruction is placed on the address bus, and the $\overline{IO}$/M signal selects and activates the control logic for I/O. If we used one of the memory commands (MOV, CMP, TEST, etc.), the $\overline{IO}$/M signal would activate the control logic for the system memory.

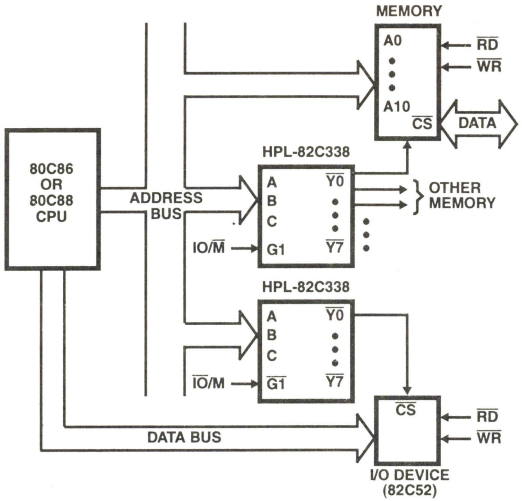
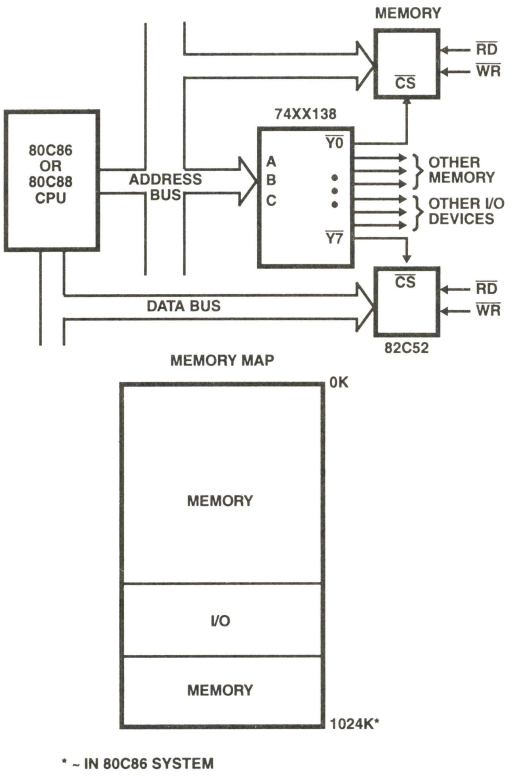


FIGURE 13. I/O MAPPED ADDRESSING



* ~ IN 80C86 SYSTEM

FIGURE 14. MEMORY MAPPED I/O ADDRESSING

5.2 Memory Mapped I/O

Memory Mapped I/O uses the same control logic for accessing both memory and I/O devices within a system. This is illustrated in Figure 14. Because we are using one set of control logic, we reduce the number of devices in the system, and save board space.

When I/O devices are placed within the Memory Space of a system, it is possible to take advantage of the memory instruction set. This would now allow us to utilize the full register set in I/O operations, as opposed to only being able to use the accumulator (AX/AL) for the I/O instructions. Also, conditional testing can be applied to the I/O devices (i.e. TEST, CMP). When using memory mapped I/O, it should be noted that the I/O devices can no longer be accessed through the I/O instructions (IN and OUT). There are disadvantages to using memory mapped I/O as well:

- The I/O devices are treated as memory, therefore the amount of available memory in the system is reduced.
- Memory instructions will execute slower than the I/O commands (IN and OUT). In certain situations (i.e. I/O polling), this could lead to loss of data during communications (overrun errors).

5.3 I/O Addressing For The 82C52

The actual addressing of the 82C52 internal registers takes place through the address pins A0 and A1. These two signals are taken from the address bus. In the following example(s), address lines AD0 and AD1 from the 80C86/88 drive A0 and A1, respectively, on the 82C52. Control logic will decode the remaining address lines from the CPU to generate a 'chip select' for enabling the 82C52. The control logic consists of a 74XX138 Chip Select Decoder.

The addresses for the 82C52 set up as described above are shown in Table 7.

TABLE 7. EXAMPLE ADDRESSES

REGISTER	ADDRESS	REGISTER TYPE
Transmit Buffer Register	10H	Write only register
Receiver Buffer Register	10H	Read only register
UART Control Register	11H	Write only register
UART Status Register	11H	Read only register
Modem Control Register	12H	Write/Read register
Baud Rate Selector Register	13H	Write only register
Modem Status Register	13H	Read only register

6.0 Reset Of The 82C52

There are two distinct ways in which the 82C52 can be reset to a known initial state: (1) By applying a reset pulse for at least two clock cycles on the RST pin, or (2) through software.

A hardware reset is accomplished by forcing the RST pin to a high state for a minimum of two clock cycles. This should be for two cycles of the 82C52's IX clock input as opposed to

the system clock. This reset will cause the UART Status Register (USR) to be set to 60H (TC and TBRE bits will be set), and the Modem Control Register(MCR) will be cleared. Any lines associated with the bits in the USR and MCR will be cleared or disabled.

During the reset of the device, the Baud Rate Select Register (BRSR) and the UART Control Register (UCR) will not be affected. However, if the reset comes due to power on, these registers will have an indeterminate value associated with them. After this reset, the 82C52 will remain in an idle state until programmed to its desired configuration.

A second method of resetting the 82C52 is through a software reset. This will allow the device to be set to a known state. The procedure for performing a software reset is outlined below:

(1) MCR = 00H. Write a zero to the MCR. This will disable the receiver as well as the modem control lines, and interrupts.

(2) Read the RBR to clear out any residual data.

(3) Read the USR to reset status, thus keeping status lines from causing possible interrupts to the CPU.

(4) Reconfigure the device for the desired mode of operation.

7.0 Programming The 82C52

In order to configure the 82C52 for proper operation, three separate command words need to be written to the command (control) registers that were specified earlier.

These registers include (1) the UART Control Register, (2) the Baud Rate Select Register, and (3) the Modem Control Register. When programming the device, these registers can be written to in any order. It is advisable to initialize the Modem Control Register last because it controls the enabling of interrupts, and the receiver circuitry. Once initialized, the 82C52 can be reconfigured at any time by writing new command word(s) to the control registers. However, the device should not be actively transmitting or receiving data when reconfiguring the control registers.

Addressing of the internal registers on the 82C52 occurs by using the address lines A1 and A0, as well as the $\overline{WR}$ and $\overline{RD}$ lines. A more complete description of this is shown in Table 8.

82C52 Polling Operation

When utilizing a polling scheme for communications with the 82C52, it is important to note that the UART status register will be cleared of its contents when it is read by the processor. Therefore, subsequent reads of this register will show the contents to be 00H unless the status of the device has changed between reads. Because of this, it would be necessary for a copy of the status to be saved so that the proper status can be seen.

Interrupt Driven Operation

In this example, the 82C59A Interrupt Controller is being used to handle interrupts generated by the 82C52. The 82C59A then communicates this interrupt information to the CPU so that it may be properly serviced. An example of how the 82C59A and 82C52 are interfaced to the CPU is shown in Figure 15.

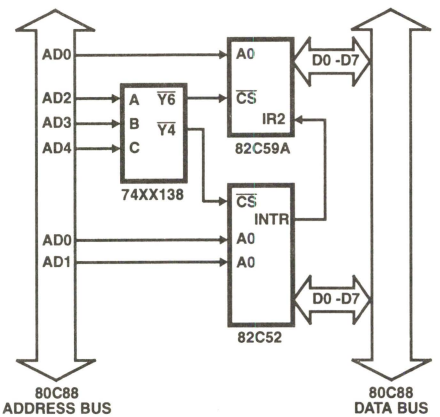


FIGURE 15. INTERRUPT DRIVEN SYSTEM

TABLE 8. ADDRESSING THE 82C52

ALE	$\overline{CSO}$	CS1	A1	A0	$\overline{WR}$	$\overline{RD}$	OPERATION
1 or ↓	0	1	0	0	↓	1	Data bus → TBR
1 or ↓	0	1	0	0	1	↓	RBR → Data bus
1 or ↓	0	1	0	1	↓	1	Data bus → UCR
1 or ↓	0	1	0	1	1	↓	USR → Data bus
1 or ↓	0	1	1	0	↓	1	Data bus → MCR
1 or ↓	0	1	1	0	1	↓	MCR → Data bus
1 or ↓	0	1	1	1	↓	1	Data bus → BRSR
1 or ↓	0	1	1	1	1	↓	MSR → Data bus

Harris Semiconductor

APPNOTE

No. AN109.1 March 1997

Harris Digital

82C59A Priority Interrupt Controller

Author: J.A. Goss

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Introduction

The Harris 82C59A is a CMOS Priority Interrupt Controller, designed to relieve the system CPU from the task of polling in a multi-level priority interrupt system. The 82C59A is compatible with microprocessors such as the 80C86, 80C88, 8086, 8088, 8080/85 and NSC800.

In the following discussion, we will look at the initialization and operation process for the 82C59A. We will focus our attention on 80C86/80C88-based systems. However, the information presented will also be applicable to use of the 82C59A in 8080 and 8085-based systems as well.

Let us look at the sequence of events that occur with the 82C59A during an interrupt request and service. In an 8080/85 based system:

(1) One or more of the INTERRUPT REQUEST lines (IR0 - IR7) are raised high, setting the corresponding bits in the Interrupt Request Register (IRR).

(2) The interrupt is evaluated in the priority resolver. If appropriate, an interrupt is sent to the CPU via the INT line (pin 17).

(3) The CPU acknowledges the interrupt by sending a pulse on the $\overline{INTA}$ line. Upon reception of this pulse, the 82C59A responds by forcing the opcode for a call instruction (0CDH) onto the data bus.

(4) A second $\overline{INTA}$ pulse is sent from the CPU. At this time, the device will respond by placing the lower byte of the address of the appropriate service routine onto the data bus. This address is derived from ICW1.

(5) A final (third) pulse of $\overline{INTA}$ occurs, and the 82C59A responds by placing the upper byte of the address onto the data bus. This address is taken from ICW2.

(6) The three byte call instruction is then complete. If the AEOI mode has been chosen, the bit set during the first $\overline{INTA}$ pulse in the ISR is reset at the end of the third $\overline{INTA}$ pulse. Otherwise, it will not get reset until an appropriate EOI command is issued to the 82C59A.

For 80C86- and 80C88-based systems:

(1) and (2) same as above.

(3) The CPU responds to the interrupt request by pulsing the $\overline{INTA}$ line twice. The first pulse sets the appropriate ISR bit and resets the IRR bit while the second pulse causes the interrupt vector to be placed on the data bus. This byte is composed of the interrupt number in bits 0 through 2, and bits 3 through 7 are taken from bits 3 - 7 of ICW2.

(4) The interrupt sequence is complete. If using the AEOI mode, the bit set earlier in the ISR will be reset. Otherwise, the interrupt controller will await an appropriate EOI command at the end of the interrupt service routine.

1.0 Glossary of Terms for the 82C59A

1.1 Automatic End of Interrupt (AEOI):

When the 82C59A is programmed to operate in the Automatic EOI mode, the device will produce its own End-of-Interrupt (EOI) at the trailing edge of the last Interrupt Acknowledge pulse ($\overline{INTA}$) from the CPU. Using this mode of operation frees the software (service routines) from needing to send an EOI manually to the 82C59A.

However, using the Automatic EOI mode will upset the priority structure of the 82C59A. When the AEOI is generated, the bit that was set in the In-Service Register (ISR) to indicate which interrupt is being serviced, will be cleared. Because of this, while an interrupt is being serviced there will be no record in the ISR that it is being serviced. Unless interrupts are disabled by the CPU, there is a risk that interrupt requests of lower or equal priority will interrupt the current request being serviced. If this mode of operation is not desired, interrupts should not be re-enabled by the CPU when executing interrupt service routines.

1.2 Automatic Rotation:

During normal operation of the 82C59A, we have an assigned order of priorities for the IR lines. There are however, instances when it might be useful to assign equal priorities to all interrupts. Once a particular interrupt has been serviced, all other equal priority interrupts should have an opportunity to be serviced before the original peripheral can be serviced again. This priority equalization can be achieved through Automatic Rotation of priorities.

Assume, for example, that the assigned priorities of interrupts has IR0 as the highest priority interrupt and IR7 as the lowest. Figure 1A shows interrupt requests occurring on IR7 as well as IR3. Because IR3 is of higher priority, it will be serviced first. Upon completion of the servicing of IR3, rotation occurs and IR3 then becomes the lowest priority interrupt. IR4 will now have the highest priority (See Figure 1B).

There are two methods in which Automatic Rotation can be implemented. First, if the 82C59A is operating in the AEOI mode as described above, the 82C59A can be programmed for "Rotate in Automatic EOI mode". This is done by writing a command word to OCW2. The second method occurs when using normal EOIs. When an EOI is issued by the service routine, the software can specify that rotation be performed.

	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
IRR STATUS	1	0	0	0	1	0	0	0
PRIORITY	7	6	5	4	3	2	1	0
	LOWEST PRIORITY							HIGHEST PRIORITY

FIGURE 1A. IR PRIORITIES (BEFORE ROTATION)

	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
IRR STATUS	1	0	0	0	0	0	0	0
PRIORITY	3	2	1	0	7	6	5	4
	HIGHEST PRIORITY						LOWEST PRIORITY	

FIGURE 1B. IR PRIORITIES (AFTER ROTATION)

1.3 Buffered Mode

When using the 82C59A in a large system, it may be necessary to use bus buffers to guarantee data integrity and guard against bus contention.

By selecting buffered mode when initializing the device, the $\overline{SP}/\overline{EN}$ pin (pin 16) will generate an enable signal for the buffers whenever the data outputs from the 82C59A are active. In this mode, the dual function $\overline{SP}/\overline{EN}$ pin can no longer be used for specifying whether a particular 82C59A is being used as a master or a slave in the system. This specification must be made through setting the proper bit in ICW4 during the device initialization.

1.4 Cascade Mode

More than one 82C59A can be used in a system to expand the number of priority interrupts to a maximum of 64 levels without adding any additional hardware. This method of expansion is known as "cascading". An example of cascading 82C59A is shown in Figure 2.

In a cascaded interrupt scheme, a single 82C59A is utilized as the "master" interrupt controller. As many as 8 "slave" 82C59As can be connected to the IR inputs of the "master" 82C59A. Each of these slaves can support up to 8 interrupt inputs, yielding 64 possible prioritized interrupts.

When in cascade mode, the determination of whether a device is a master or a slave can take either of two forms. The state of the $\overline{SP}/\overline{EN}$ pin will select "master" or "slave" mode for a device when the buffered mode is not being used. Should buffered mode be used, then it is necessary that bit D2 (M/S) of ICW4 be set to indicate if the particular 82C59A is being used as a "master" or "slave" interrupt controller in the system.

The CAS0-2 pins on the interrupt controllers serve to provide a private bus for the cascaded 82C59As. These lines allow the "master" to inform the slaves which is to be serviced for a particular interrupt.

1.5 End of Interrupt (EOI):

When an interrupt is recognized and acknowledged by the CPU, its corresponding bit will be set in the In-Service Register (ISR). If the AEOI mode is in use, the bit will be cleared automatically through the interrupt acknowledge signal from the CPU. However, if AEOI is not in effect, it is the task of software to notify the 82C59A when servicing of an interrupt is completed. This is done by issuing an End-of-Interrupt (EOI).

There are 2 different types of EOIs that can be issued to the device; non-specific EOI and specific EOI. In most cases, when the device is operating in a mode that does not disturb the fully nested mode such as Special Fully Nested Mode, we will issue a non-specific EOI. This form of the EOI will automatically reset the highest priority bit set in the ISR. This is because for full nested operation, the highest priority IS bit set is the last interrupt level acknowledged and serviced.

The "specific" EOI is used when the fully nested structure has not been preserved. The 82C59A may not be able to determine the last level acknowledged. Thus, the software must specify which interrupt level is to be reset. This is done by issuing a "specific" EOI.

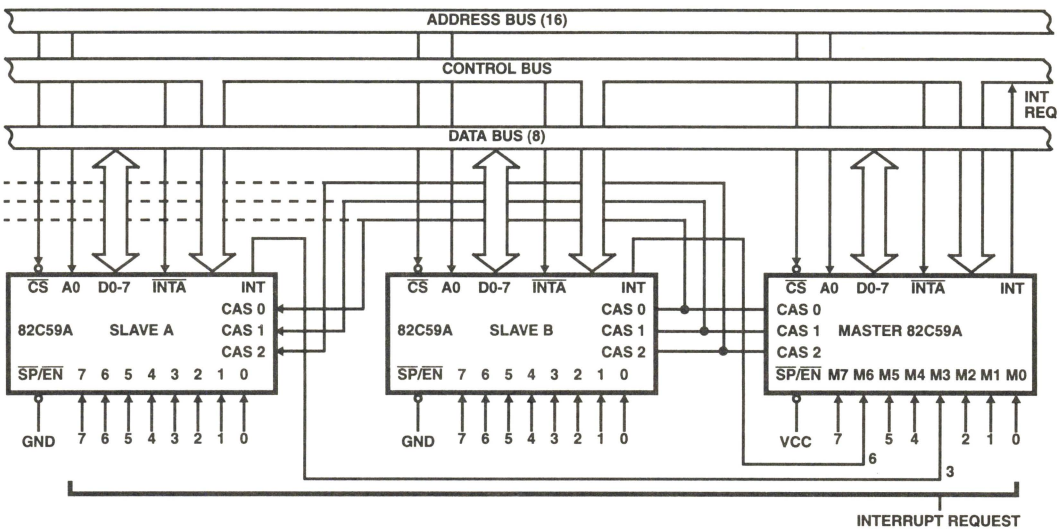


FIGURE 2. CASCADING THE 82C59A

7 APPLICATION NOTES

1.6 Fully Nested Mode:

By default, the 82C59A operates in the Fully Nested Mode. It will remain in this mode until it is programmed otherwise. In the Fully Nested Mode, interrupts are ordered by priority from highest to lowest. Initially, the highest priority level is IR0 with IR7 having the lowest. This ordering can be changed through the use of priority rotation (see 1.2).

In the Fully Nested Mode, when an interrupt occurs, its corresponding bit will get set in the Interrupt Request Register (IRR). When the processor acknowledges the interrupt, the 82C59A will look to the IRR to determine the highest priority interrupt requesting service. The bit in the In-service Register (ISR) corresponding to this interrupt will then be set. This bit remains set until an EOI is sent to the 82C59A.

While an interrupt is being serviced, only higher priority interrupts will be allowed to interrupt the current interrupt being serviced. However, lower priority interrupts can be allowed to interrupt higher priority requests if the 82C59A is programmed for operation in the Special Mask Mode.

When using the 82C59A in an 80C86- or 80C88-based system, interrupts will automatically be disabled when the processor begins servicing an interrupt request. The current address and the state of the flags in the processor will be pushed onto the stack. The interrupt-enable flag is then cleared. To allow interrupts to occur at this point, the STI instruction can be used. Upon exiting the service routine using the IRET instruction, execution of the program is resumed at the point where the interrupt occurred, and the flags are restored to their original values, thus re-enabling interrupts.

A configuration in which the Fully Nested structure is not preserved occurs when one or more of the following conditions occur:

(a) The Automatic EOI mode is being used.

(b) The Special Mask Mode is in use.

(c) A slave 82C59A has a master that is not programmed to the Special Fully Nested Mode.

Cases (a) and (b) differ from case (c) in that the 82C59A would allow lower priority interrupt requests the opportunity to be serviced before higher priority interrupt requests.

1.7 Master:

When using multiple 82C59As in a system, one 82C59A has control over all other 82C59As. This is known as the "master" interrupt controller. Communication between the master and the other (slave) 82C59As occurs via the CAS0 - 2 lines. These lines form a private bus between the multiple 82C59As. Also, the INT lines from the slaves are routed to the master's IR input pin(s). See Figure 2.

1.8 Slave:

A "slave" 82C59A in a system is controlled by a master 82C59A. There is but one "master" in the system, but there can be up to 8 slave 82C59As. The INT outputs from the slaves act as inputs to the master through it's IR inputs. Communications between the master and slaves occurs via the CAS0 - 2 lines. See Figure 2.

1.9 Special Fully Nested Mode:

The Special Fully Nested Mode (SFNM) is used in a system having multiple 82C59As where it is necessary to preserve the priority of interrupts within a slave 82C59A. Only the master is programmed for the Special Fully Nested Mode through ICW4. This mode is similar to the Fully Nested Mode with the following exceptions:

(a) When an interrupt from a particular slave is being serviced, additional higher priority interrupts from that slave can cause an interrupt to the master. Normally, a slave is masked out when its request is in service.

(b) When exiting the Interrupt Service routine, the software should first issue a non-specific EOI to the slave. The Inservice Register (ISR) should then be read and checked to see if its contents are zero. If the register is empty, the software should then write a non-specific EOI to the master. Otherwise, a second EOI need not be written because there are interrupts from that slave still being processed.

NOTE: Because the Master 82C59A and its slave 82C59As must be in Fully Nested Mode for this mode to be functional, we could not utilize Automatic EOIs. These would disturb the Fully Nested structure, as described in section 1.6.

1.10 Special Mask Mode:

The Special Mask Mode is utilized in order to allow interrupts from all other levels (higher and lower as well) to interrupt the IR level that is currently being serviced. Invoking this mode of operation will disturb the fully nested priority structure.

Generally, the Special Mask Mode is selected during the servicing of an interrupt. The software should first set the bit corresponding to the IR level being serviced, in the Interrupt Mask Register (OCW1). The Special Mask Mode and interrupts should then be enabled. This will allow any of the IR levels except for those masked off by OCW1 to interrupt the IR level currently being serviced.

Because this disturbs the Fully Nested Structure, it is required that a Specific EOI be issued when servicing interrupts while the Special Mask Mode is in effect. Before exiting the original interrupt routine, the Special Mask Mode should be disabled.

1.11 Specific Rotation:

By issuing the proper command word to OCW2, the priority structure of the 82C59A can be dynamically altered. The command word written to OCW2 would specify which is to be the lowest priority IR level.

This specific rotation can be accomplished one of two ways. The first is through a specific EOI. The software can specify that rotation is to be applied to the IR level provided with the EOI. The second method is a simple "set priority" command, in which the lowest priority level is specified with the command word.

2.0 Initialization Control Words

The following section gives a description of the Initialization Control Words (ICW) used for configuring the 82C59A Interrupt controller. There are four (4) control words used for initialization of the 82C59A. These ICWs must be programmed in the proper sequence beginning with ICW1. If at any time during the course of operation the configuration of the 82C59A needs to be changed, the user must again write out the control words to the device in their proper order. The initialization sequence is shown in Figure 3.

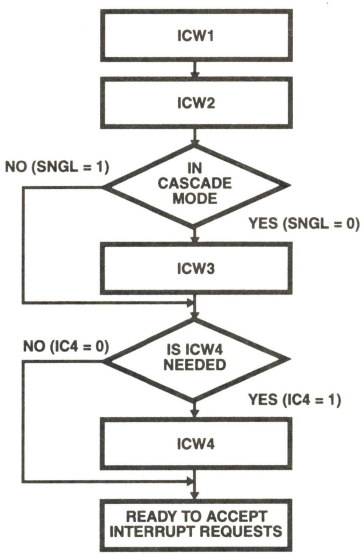


FIGURE 3. 82C59A INITIALIZATION SEQUENCE

ICW1: The 82C59A recognizes the first Initialization Control Word (ICW) written to it based on two criteria: (1) the A0 line from the address bus must be a zero, and (2) the D4 bit must be a one. If the D4 bit is set to a zero, we would be programming either OCW2 or OCW3 (these are explained later). The function of ICW1 is to tell the 82C59A how it is being used in the system (i.e. Single or cascaded, edge or level triggered interrupts etc.).

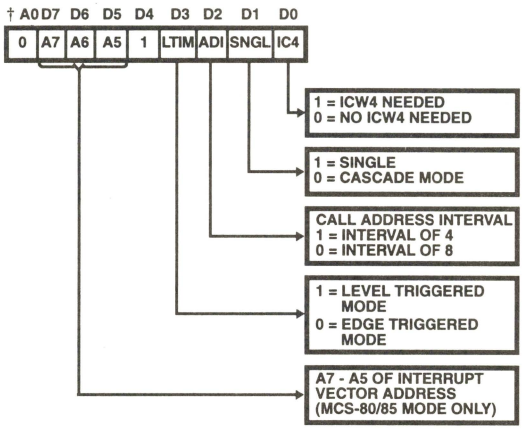
ICW2: This control word is always issued directly after ICW1. When addressing this ICW, the A0 line from the address bus must be a one (high). ICW2 is utilized in providing the CPU with information on where to vector to in memory when servicing an interrupt.

ICW3: This control word is issued only if the SNGL (D1) bit of the ICW1 has been programmed with a zero. When addressing this word, the A0 line from the CPU must be high (1). This control word is for cascaded 82C59As. It allows the master and slave 82C59As to communicate via the CAS0-2 lines. With the master, this word indicates which IR lines have slaves connected to them. For the slave 82C59A(s), this word indicates to which IR line on the master it is connected.

ICW4: Issuance of this ICW is selectable through the IC4 (D0) bit of ICW1. If ICW4 is to be written to the 82C59A, A0 from the CPU must be high (1) when writing to it. This word needs to be written only when the 82C59A is operating in modes other than the default modes. Instances when we would want to write to ICW4 are one or more of the following: An 80C86(80C88) processor is being used, buffered outputs (D0 - D7) are to be used, Automatic EOIs are desired, or the Special Fully Nested mode is to be used.

2.1 ICW1:

ICW1 is the first control word that is written to the 82C59A during the initialization process. To access this word, the value of A0 must be a zero (0) in the addressing, and bit D4 of ICW1 must be a one (1). The format of the command word is as follows:



† A0 is an address bit, and not part of the ICW.

FIGURE 4. ICW1 FORMAT

D7 thru D5 - A7, A6, A5: These bits are used in the 8080/85 mode to form a portion of the low byte call address. When using the 4 byte address interval, all 3 bits are utilized. When using the 8 byte interval, only bits A7 and A6 are used. Bit A5 becomes a "don't care" bit. If using an 80C86(80C88) system, the value of these bits can be set to either a one or zero.

D3 - LTIM:

0: The 82C59A will operate in an edge triggered mode. An interrupt request on one of the IR lines (IR0 - IR7) is recognized by a low to high transition on the pin. The IR signal must remain high at least until the falling edge of the first $\overline{INTA}$ pulse. Subsequent interrupts on the IR pin(s) will not occur until another low-to-high transition occurs.

1: Sets up the 82C59A to operate in the level triggered mode. Interrupts occur when a "high" level is detected on one or more of the IR pins. The interrupt request must be removed from this pin before the EOI command is issued by the CPU. Otherwise, the 82C59A will see the IR line still in a high state, and consider this to be another interrupt request.

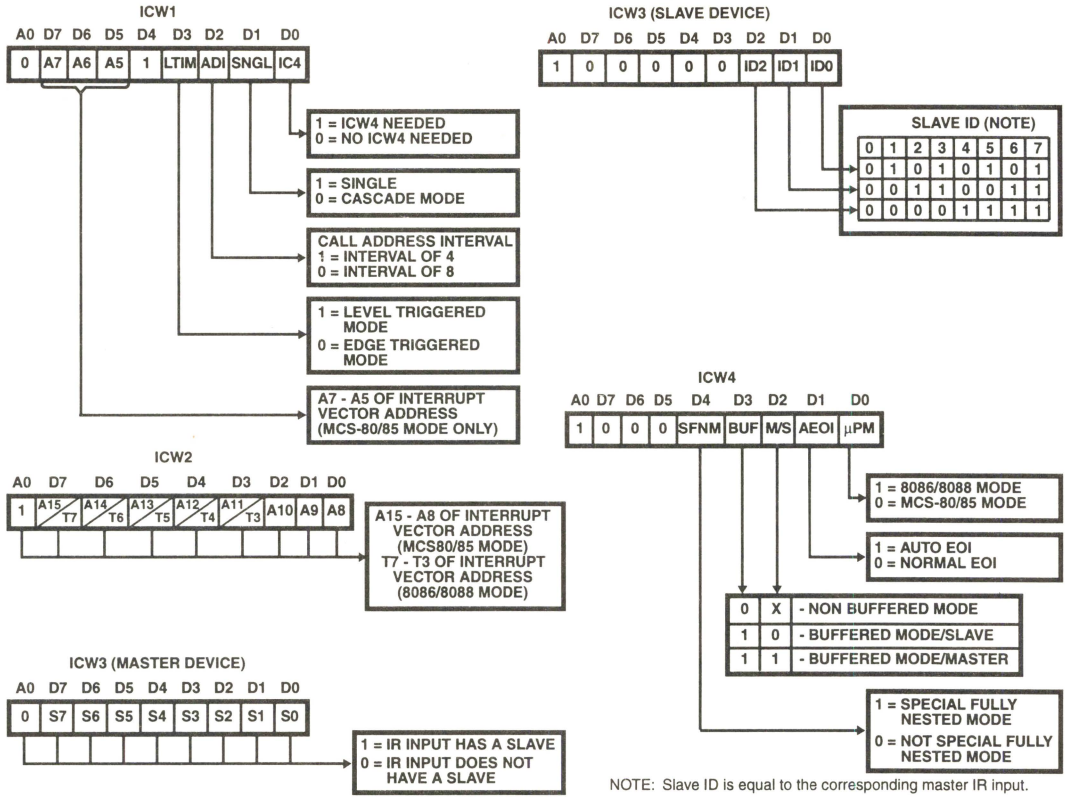


FIGURE 5. 82C59A INITIALIZATION COMMAND WORD FORMAT

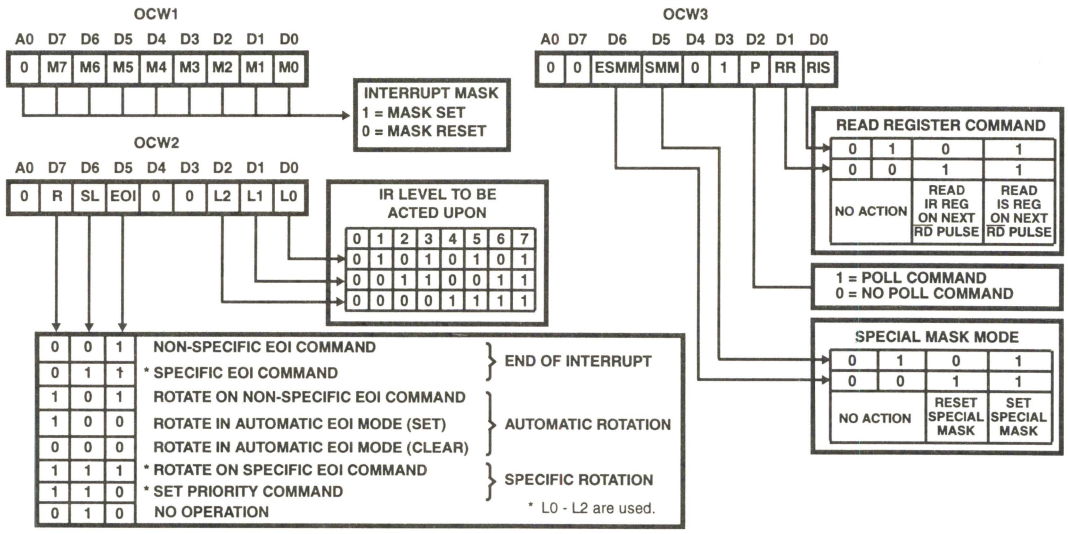


FIGURE 6. 82C59A OPERATION COMMAND WORD FORMAT

D2 - ADI: Call Address Interval (for 8080/8085 use only). If using the 82C59A in an 80C86/88 based system, the value of this bit can be either a 0 or 1.

0: The address interval generated by the 82C59A is 8 bytes. This option provides compatibility with the RST interrupt vectoring in 8080/8085 systems since the vector locations are 8 bytes apart. This vector will be combined with the values specified in bits D7 and D6 of ICW1. The addresses generated are shown in Table 1.

TABLE 1. ADDRESS INTERVAL (8 BYTES)

D7	D6	D5	D4	D3	D2	D1	D0	
A7	A6	1	1	1	0	0	0	IR7
A7	A6	1	1	0	0	0	0	IR6
A7	A6	1	0	1	0	0	0	IR5
A7	A6	1	0	0	0	0	0	IR4
A7	A6	0	1	1	0	0	0	IR3
A7	A6	0	1	0	0	0	0	IR2
A7	A6	0	0	1	0	0	0	IR1
A7	A6	0	0	0	0	0	0	IR0

1: The address interval generated by the interrupt controller will be 4 bytes. This provides the user with a compact jump table for 8080/8085 systems. The interrupt number is effectively multiplied by four and combined with bits D7, D6, and D5 to form the lower byte of the call instruction generated and sent to the 8080 and 8085. Table 2 shows how these addresses are generated for the various interrupt request (IR) levels.

TABLE 2. ADDRESS INTERVAL (4 BYTES)

D7	D6	D5	D4	D3	D2	D1	D0	
A7	A6	A5	1	1	1	0	0	IR7
A7	A6	A5	1	1	0	0	0	IR6
A7	A6	A5	1	0	1	0	0	IR5
A7	A6	A5	1	0	0	0	0	IR4
A7	A6	A5	0	1	1	0	0	IR3
A7	A6	A5	0	1	0	0	0	IR2
A7	A6	A5	0	0	1	0	0	IR1
A7	A6	A5	0	0	0	0	0	IR0

D1 - SNGL:

0: This tells the 82C59A that more than one 82C59A is being used in the system, and it should expect to receive ICW3 following ICW2. How the particular 82C59A is being used in the system will be determined either through ICW4 for buffered mode, or through the $\overline{SP}/\overline{EN}$ pin for non-buffered mode operation.

1: Tells the 82C59A that it is being used alone in the system. Therefore, there will be no need to issue ICW3 to the device.

D0 - IC4: Specifies to the 82C59A whether or not it can expect to receive ICW4. If this device is being used in an 80C86/80C88 system, ICW4 must be issued.

0: ICW4 will not be issued. Therefore, all of the parameters associated with ICW4 will default to the zero (0) state. This should only be done when using the 82C59A in an 8080 or 8085 based system.

1: ICW4 will be issued to the 82C59A.

2.2 ICW2:

ICW2 is the second control word that must be sent to the 82C59A. This byte is used in one of two ways by the 82C59A, depending on whether it is being used in an 8080/85 or an 80C86/88 based system.

When used in conjunction with the 8080/85 microprocessor, the value given to this register is taken as being the high byte of the address in the CALL instruction sent to the CPU.

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

FIGURE 7. ICW2 FORMAT

In an 80C86- or 80C88-based system, ICW2 is used to send the processor an interrupt vector. This vector is formed by taking the value of bits D7 through D3 and combining them with the interrupt request level to get an eight bit number. The processor will multiply this number by four and go to that absolute location in memory to find a starting address for the interrupt service routine corresponding to the interrupt request.

For example, if we set ICW2 to "00011000" and an interrupt is recognized on IR1, the vector sent to the 80C86(80C88) will be 00011001 (19H). The processor will then look to the memory location 64H to find the starting address of the corresponding interrupt service routine. It is the responsibility of the software to provide this address in the interrupt table.

D7	D6	D5	D4	D3	D2	D1	D0
A7	A6	A5	A4	A3	X	X	X

FIGURE 8. ICW2 FORMAT (80C86 MODE)

2.3 ICW3:

ICW3 is only issued when the SNGL bit in ICW1 has been set to zero. If not set, the next word written to the 82C59A will be interpreted as ICW4 if A0 = 1 and IC4 from ICW4 was set to one, or it could see it as one of the Operation Command Words based upon the state of the A0 line.

Like ICW2, this control word can be interpreted in two ways by the 82C59A. However the interpretation of this word depends on whether the 82C59A is being used as a "master" or "slave" in the system. The definition of the particular device's role in the system is assigned through ICW4 (which will be discussed later), or through the state of the $\overline{SP}/\overline{EN}$ pin (pin 16).

82C59A as a MASTER:

If a given 82C59A is being used as a master, the eight (8) bits in this command word are used to indicate which of the IR lines are being driven by a slave 82C59A.

D7	D6	D5	D4	D3	D2	D1	D0
S7	S6	S5	S4	S3	S2	S1	S0

FIGURE 9. ICW3 FORMAT (MASTER)

D7 thru D0:

0: The corresponding IR line to this bit is not being driven by a slave 82C59A. This line can however then be connected to the interrupt output of another interrupting device such as a UART. If there are unused bits in this byte because not all eight of the IR lines are used, set them to zero.

1: The corresponding IR line to this bit is being driven by a slave 82C59A.

The bits in this command word are directly related to the IR lines. For example, to tell the 82C59A that there is a slave device connected to IR5 (pin 23), bit D5 of the command word should be set to a one (1).

82C59A as a SLAVE device:

When the device is being used as a slave device, we must use ICW3 to inform itself as to which IR line it will be connected to in the master. Therefore, only the three (3) least significant bits of ICW3 will be used to specify this value.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	ID2	ID1	ID0

FIGURE 10. ICW3 FORMAT (SLAVE)

These bits are coded as follows:

TABLE 3. SLAVE IDENTIFICATION WITH ICW3

MASTER IR NUMBER	ID2	ID1	ID0
IR7	1	1	1
IR6	1	1	0
IR5	1	0	1
IR4	1	0	0
IR3	0	1	1
IR2	0	1	0
IR1	0	0	1
IR0	0	0	0

For example, if the INT output of a "slave" 82C59A is connected to the input pin IR5 on the "master" 82C59A, ICW3 of the "slave" would be programmed with the value 00000101b, or 05H. This informs the "slave" as to which priority level it holds with the "master".

D7 thru D3: These bits must be set to zeros (0) for proper operation of the device.

2.4 ICW4:

This control register is written to only when the IC4 bit is set in ICW1. The purpose of this command word is to set up the 82C59A to operate in a mode other than the default mode of operation. The default mode of operation is the same as if a value of 00H were to be written to ICW4 (i.e. all bits set to zero).

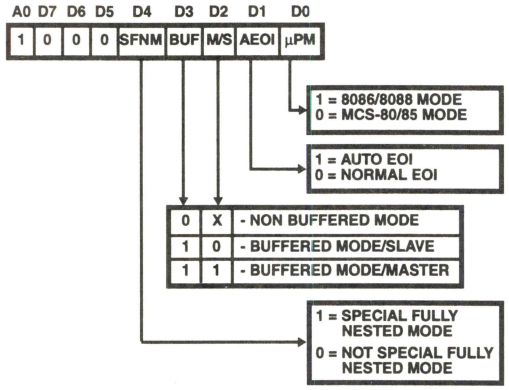


FIGURE 11. ICW4 FORMAT

D7 thru D5: These bits must be set to zero for proper operation.

D4-SFNM: This bit is used in the selection of the Special Fully Nested Mode (SFNM) of operation. This mode should only be used when multiple 82C59As are cascaded in a system. It needs only to be programmed in the Master 82C59A in the system.

0: Special Fully Nested Mode is not selected.

1: Special Fully Nested Mode is selected.

D3 - BUF: This bit tells the 82C59A whether or not the outputs from the data pins (D0 - D7) will be buffered. If they are buffered, this bit will cause the $\overline{SP}/\overline{EN}$ pin to become an output signal that can be used to control the "enable" pin on a buffering device(s).

0: The device will be used in a non-buffered mode. Therefore, (1) the M/S bit in ICW4 is a don't care, and (2) the $\overline{SP}/\overline{EN}$ pin becomes an input pin telling the device if it is being used as a master (pin 16 = High) or a slave (pin 16 = low). For systems using a single 82C59A, the $\overline{SP}/\overline{EN}$ input should be tied high.

1: The device is used in buffered mode. An enable output signal will be generated on pin 16, and the M/S bit will be used for determining whether the particular 82C59A is a "master" or a "slave".

D2 - M/S: This bit is of significance only when the BUF bit is set (BUF =1). The purpose of this bit is to determine whether the particular 82C59A is being used as a "master" or a "slave" in the target system.

0: The 82C59A is being used as slave.

1: The 82C59A is the master interrupt controller in the system.

D1 - AEOI: This bit is used to tell the 82C59A to automatically perform a non-specific End-of-Interrupt on the trailing edge of the last Interrupt Acknowledge pulse. Users should note that when this is selected, the nested priority interrupt structure is lost.

0: Automatic End-of-Interrupt will not be generated.

1: Automatic End-of-Interrupt will be generated on the trailing edge of the last Interrupt Acknowledge pulse.

D0 - μPM: This bit tells the Interrupt Controller which microprocessor is being used in the system. An 8080/8085, or an 80C86/80C88.

0: The 82C59A will be used in an 8080/8085 based system.

1: 82C59A to be used in the 80C86/88 mode of operation.

3.0 Operation Command Words

Once the Initialization Command Words, described in the previous section, have been written to the 82C59A, the device is ready to accept interrupt requests. While the 82C59A is operating, we have the ability to select various options that will put the device in different operating modes, by writing Operation Command Words (OCWs) to the 82C59A. These OCWs can be sent at any time after the device has been initialized and in any order. These words can be changed at any time as well. Note: If A0 = 0 and D4 of the command word = 1, the 82C59A will begin the ICW initialization sequence.

There are three different OCWs for the 82C59A. Each has a different purpose. The first control word (OCW1) is used for masking out interrupt lines that are to be inactive or ignored during operation. OCW2 is used to select from various priority resolution algorithms in the device. Finally, OCW3 is used for (1) controlling the Special Mask Mode, and (2) telling the 82C59A which Register will be read on the next RD pulse; the ISR (In-service Register) or the IRR (Interrupt Request Register).

3.1 OCW1:

This control word is used to set or clear the masking of the eight (8) interrupt lines input to the 82C59A. This control word performs this function via the Interrupt Mask Register (IMR). In it's initial state, the value of this register is 00H. In other words, all of the interrupt lines are enabled. Therefore, we need only write this control word when we wish to disable specific interrupt lines.

A direct mapping occurs between the bits in this control word and the actual interrupt pins on the device. For example bit 7 (D7) controls interrupt line IR7 (pin 25), bit 6 controls IR6, and so on.

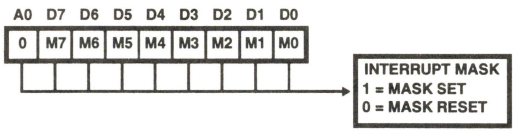


FIGURE 12. OCW1 FORMAT

Even though the user can mask off any of the IR lines, any interrupt occurring during that time will not be lost. The request for an interrupt is retained in the IRR; therefore when that IR is unmasked by issuing a new mask value to OCW1, the interrupt will be generated when it becomes the highest requesting priority.

D7 thru D0:

0: When any of the bits in the control word are reset (0), the corresponding interrupt is enabled.

1: By setting a bit(s) to a one in the control word, the corresponding interrupt line(s) is disabled.

For example, if the value 34H (00110100b) were written to OCW1, interrupts would be disabled from being serviced on lines IR2, IR4, and IR5.

3.2 OCW2:

In ICW4 bit D1 was used to specify whether the 82C59A should wait for an EOI (End of Interrupt) from the CPU, or generate its own EOI (Automatic EOI). If bit D1 of ICW4 had been programmed to be zero, OCW2 would be used for sending the EOI to the 82C59A. Conversely, if this bit had been set to a one, OCW2 would be used for specifying whether or not the 82C59A should perform a priority rotation on the interrupts when the AEOI is detected.

OCW2 has several EOI options. The EOI issued can be either specific or non-specific. For each of these EOIs, the user can specify whether or not priority rotation should be performed.

D7	D6	D5	D4	D3	D2	D1	D0
R	SL	EOI	0	0	L2	L1	L0

FIGURE 13.

R, SL, and EOI:

These three bits are used for specifying how the device should handle AEOIs, or for issuing one of several different EOIs. They are programmed as shown in the following table:

TABLE 4. ROTATE AND EOI MODES

R	SL	EOI	
0	0	1	Non-specific EOI command
0	1	1	*Specific EOI command
1	0	1	Rotate on non-specific EOI command
1	0	0	Rotate in Automatic EOI mode (set)
0	0	0	Rotate in Automatic EOI mode (clear)
1	1	1	*Rotate on specific EOI command
1	1	0	*Set priority command
0	1	0	No operation

* L0 - L2 are used.

L2, L1, and L0:

These three bits of the control word are used in conjunction with the issuance of specific EOIs or when specifically establishing a different priority structure. The bits tell the 82C59A which interrupt level is to be acted upon. Therefore, the software needs to know which interrupt is being serviced by the 82C59A

TABLE 5. INTERRUPT LEVEL TO ACT UPON

L2	L1	L0	
0	0	0	IR level 0
0	0	1	IR level 1
0	1	0	IR level 2
0	1	1	IR level 3
1	0	0	IR level 4
1	0	1	IR level 5
1	1	0	IR level 6
1	1	1	IR level 7

3.3 OCW3:

There are two main functions that OCW3 controls: (1) Interrupt Status, and (2) Interrupt Masking. Interrupt status can be checked by looking at the ISR or IRR registers, or by issuing a Poll Command to manually identify the highest priority interrupt requesting service.

D7	D6	D5	D4	D3	D2	D1	D0
0	ESMM	SMM	0	1	P	RR	RIS

FIGURE 14.

D7: Must be set to zero for proper operation of the 82C59A.

D6 - ESMM: Enable Special Mask Mode - The ESMM bit when enabled allows the SMM bit to set or clear the Special Mask Mode. When disabled this bit causes the SMM bit to have no effect on the 82C59A.

0: Disables the effect of the SMM bit.

1: Enable the SMM bit to control the Special Mask Mode.

D5 - SMM: Special Mask Mode - The SMM bit is used to enable or disable the Special Mask Mode. This bit will only affect the 82C59A when the ESMM bit is set to 1.

0: Disable the Special Mask Mode.

1: Put the 82C59A into the Special Mask Mode.

D4, D3: These bits are used to differentiate between OCW2, OCW3, and ICW1. To properly select OCW3, D4 must be set to zero and D3 must be set to one.

D2 - P: Poll Command - This bit is used to issue the poll command to the 82C59A. The next read of the 82C59A will cause a poll word to be returned which tells if an interrupt is pending, and if so, which is the highest requesting level.

Note: The poll command must be issued each time the poll operation is desired.

0: No poll command issued to the 82C59A.

1: Issue the poll command.

D1 - RR: Read Register - This bit is used to execute the "read register" command. When this bit is set, the 82C59A will look at the RIS bit to determine whether the ISR or IRR register is to be read. When issuing this command, the next instruction executed by the CPU should be an input from this same port to get the contents of the specified register.

0: No "Read Register" command will be performed.

1: The next input instruction by the CPU will read either the contents of the ISR or the IRR as specified by the RIS bit.

D0 - RIS: This bit is used in conjunction with the RR bit to select which register is to be read when the "Read Register" command is issued.

0: The next input instruction will read the contents of the Interrupt Request Register (IRR).

1: The next input instruction will read the contents of the In-Service Register (ISR).

The two registers that can be accessed through the Read Register command are used to determine which interrupts are requesting service, and which one(s) are currently being serviced.

The IRR bits get set when corresponding Interrupt requests are received. For instance, when IR4 is detected, bit D4 of the IRR will get set. When an interrupt acknowledge comes back from the CPU, the priority resolution logic will determine which interrupt request will be serviced. The corresponding bit in the In-service Register (ISR) will then be set. Clearing of the correct bits in the ISR occurs through out use of the AEOI, or by issuing an EOI to the device.

4.0 Addressing the 82C59A

There are two factors that must be taken into account when addressing the 82C59A in a system. To begin with, the 82C59A is accessed only when the $\overline{CS}$ pin (chip select) sees an active signal (low). This signal is generated using control circuitry in the system. Secondly, the various registers within the 82C59A are selected based upon the state of the A0 (address pin) as well as specific bits in the command words (i.e. for ICW1, OCW2, and OCW3 A0 must be a zero).

The circuit in Figure 15 shows that the $\overline{CS}$ signal is generated using an HPL-82C338 Programmable Chip Select Decoder (PCSD). This device is being used as a 3-to-8 decoder. Note that the G1 input is active high and G2 thru G5 have been programmed to be active low. The A, B, and C inputs to the 82C338 correspond to address lines AD2, AD3, and AD4 respectively, from the 80C88. The A0 input to the 82C59A is also taken from the CPUs address bus: AD0 is used. It should be noted that address line AD1 from the 80C88 is not being used in the addressing of this particular peripheral. This is done to allow other peripheral devices that require two address inputs for internal register selection, to use address lines AD0 and AD1 from the processor.

Because the AD1 address line from the 80C88 is not being used, the 82C59A will be addressed regardless of whether AD1 is high or low (1 or 0). The remainder of the address lines from the 80C88 can either be a zero or one when addressing the 82C59A. For the examples to be presented, it can be assumed that all unused address lines will be set to zero when addressing the 82C59A.

In Figure 15, output $\overline{Y6}$ from the HPL-82C338 is being used as the $\overline{CS}$ input to the 82C59A. This line is enabled when the inputs on A, B, and C are: A = 0, B = 1, and C = 1. Combining this with the A0 input to the 82C59A, we get the addresses 18H and 19H for accessing the 82C59A.

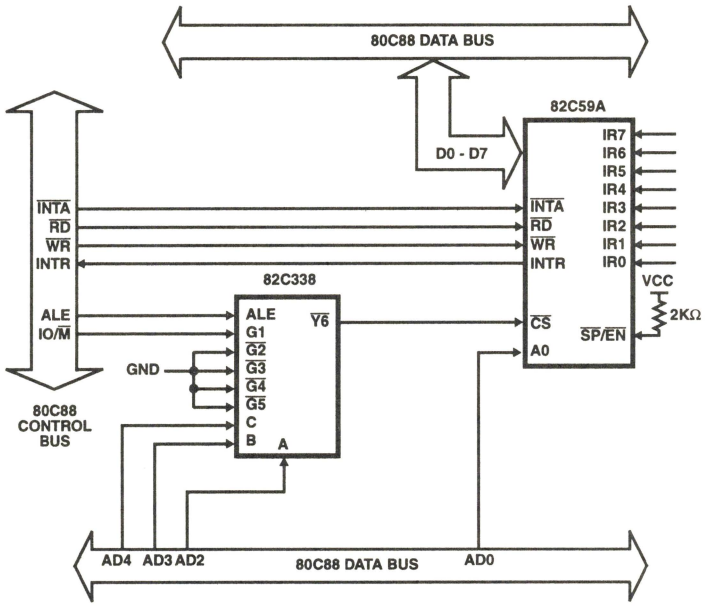


FIGURE 15. ADDRESSING THE 82C59A

5.0 Programming the 82C59A

As described earlier, there are two different types of command words that are used for controlling 82C59A operation; the Initialization Command Words (ICWs) and the Operation Command Words (OCWs). To properly program the 82C59A, it is essential that the ICWs be written first. When writing the ICWs to the 82C59A, they must be written in the following sequence:

(1) Write ICW1 to the 82C59A, A0 = 0.

(2) Write ICW2 to the 82C59A, A0 = 1.

(3) If using cascaded 82C59As in system, write ICW3 to the 82C59A, A0 = 1.

(4) If IC4 bit was set in ICW1, write ICW4 to the 82C59A.

NOTE: When using multiple 82C59As in the system (cascaded), each one must be initialized following the above sequence.

Once the 82C59A(s) has been configured through the ICWs, the OCWs can be used to select from the various operation mode options. These include: masking of interrupt lines, selection of priority rotation, issuance of EOIs, reading of the ISR and/or IRR etc. These OCWs can be written to the 82C59A at any time during operation of the 82C59A. The various command words are identified by the state of selected bits in the words, rather than by the sequence that they are written to the 82C59A; as with the ICWs. Therefore, it is imperative that the fixed bit values in the command words be written as such to insure proper operation of the device(s).

5.1 Example 1: Single 82C59A

In Example 1, we are using a single 82C59A in a system to handle the interrupts caused by an 82C52 Programmable UART. The system is driven using a 80C86 microprocessor. The system configuration is shown in Figure 16.

Interrupts are initiated by the 82C52 anytime it receives data on its Serial Data in pin (SDI), or when it is ready to transmit more data via its Serial Data Out pin (SDO).

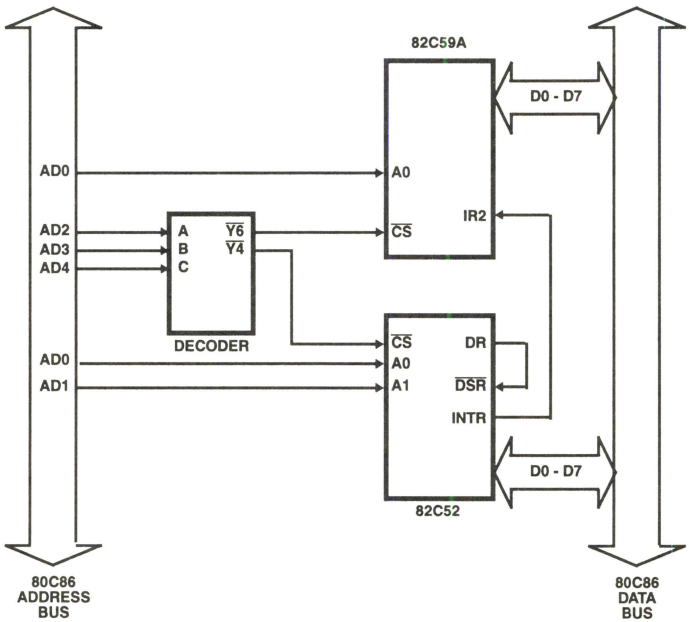


FIGURE 16. EXAMPLE 1: SINGLE 82C59A

5.2 Example 2: Cascaded 82C59As

Example 2 illustrates how we can use multiple 82C59As in Cascade Mode. Figure 17 shows the interconnections between the master and slave interrupt controllers. In this example, only one interrupt can occur. This is generated by the 82C52 UART. Except for the fact that this system is configured with a Master-Slave interrupt scheme, it is the same as that in Example 1.

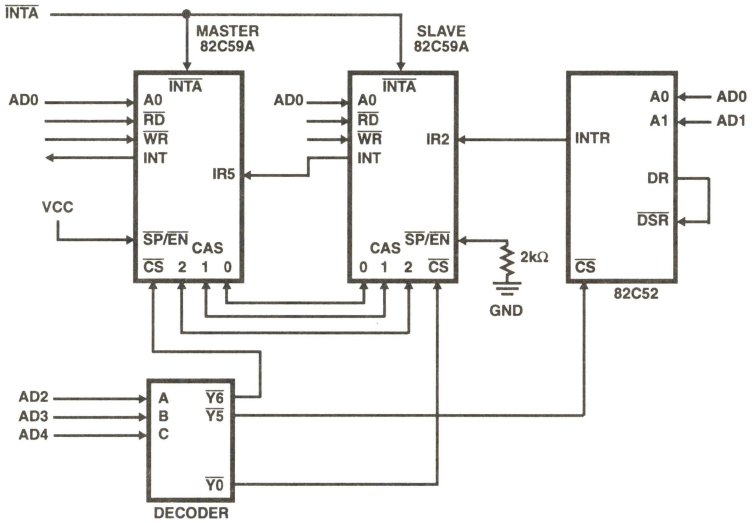


FIGURE 17. EXAMPLE 2: CASCADED 82C59As

6.0 Expansion Past 64 Interrupts

In some instances, it may be desirable to expand the number of available interrupts in a system past the maximum of 64 imposed when using cascaded 82C59As. The easiest way to accomplish this is through the use of the Poll command with the 82C59A. Figure 18 illustrates one example of how this expansion can be accomplished. Notice that we are using two 3 - to -8 decoders to address up to 16 82C59As. Selection of which decoder is active takes place using the $\overline{OE}$ pin driven by AD5 from the CPU's address bus.

With this type of interrupt structure, we are not using the INT and $\overline{INTA}$ lines from our processor (80C88 for this example). Because of this, no interrupts will break execution of the system software. Therefore, it is the task of the software to poll the various 82C59As in the system to see if any interrupts are pending. Once it has been established which interrupt requires servicing, the software can take appropriate action.

There are disadvantages to using the poll mode for the systems interrupt structure: (1) the overhead of polling each of the 82C59As reduces the systems efficiency, and (2) realtime interrupt servicing cannot be guaranteed.

There are several advantages to using the poll mode in this manner: (1) there can be more than 64 priority interrupts in the system, and (2) memory in the system is freed because no interrupt vector table is required.

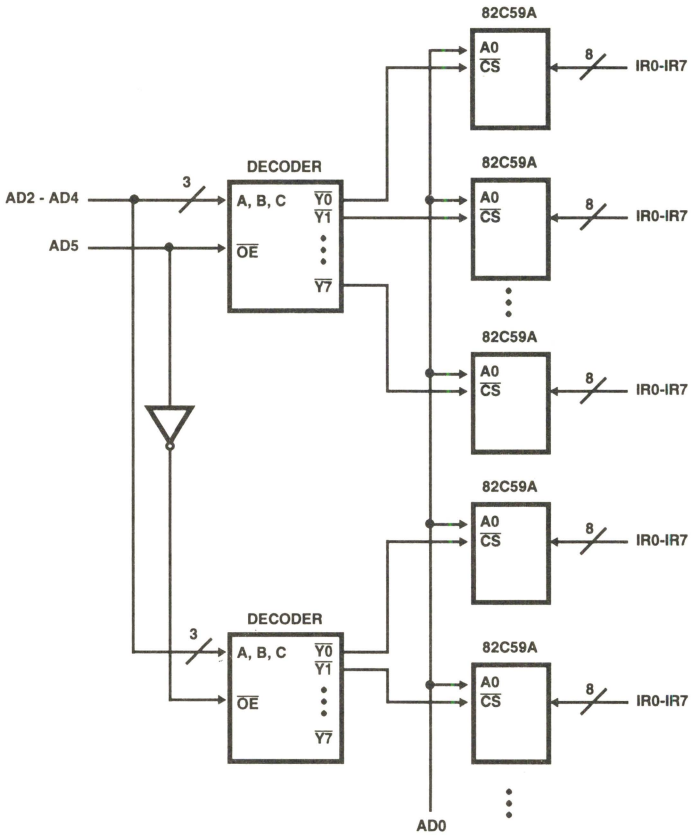


FIGURE 18. EXPANDING PAST 64 INTERRUPTS

Harris Semiconductor

APPNOTE

No. AN111.1 March 1997

Harris Digital

Harris 80C286 Performance Advantages Over the 80386

Author: Ted Dimbero

Introduction

The Harris 80C286, operating at the same frequency as the 80386, has performance advantages over the 80386 when executing 16-bit industry standard 80C86 or 80C286 code. This is evident in the following areas:

(1) Input/Output Handling

(2) Interrupt Handling

(3) Control Transfer (Loop, Jump, Call)

(4) 286 Protected Mode Systems

(5) Multi-Tasking and Task Switching Operations.

This advantage is due to the 80C286 requirement of fewer clock cycles to execute the same instructions. In addition to these areas, the 80C286 executes many other instructions in the same number of clock cycles as the 80386.

This results in an 80C286 performance advantage in areas including:

- Multi-Tasking Systems.
- Control Applications - utilizing interrupt and I/O instructions.
- Structured Software - utilizing many Control transfer instructions.
- Operating Systems that rely on interrupts to perform functions.
- Upgrading 16-bit 80C86 applications for increased performance.

The 80C286 can be effectively used as a fast 80C86. However, the 80386 is not a fast 80C286. This study shows that software written for the 80C86/80C286 can execute more efficiently on the 80C286 than on the 80386. There is not significant performance advantage to be gained by simply moving a system design from an 80C286 to an 80386 at either 16MHz or 20MHz. The 80C286 is the processor best suited for executing 16-bit 80C86/80C286 code, which represents the world's largest base of microprocessor software.

Architecture Background

The 80C286 Harris' newest static CMOS microprocessor combines low operating and standby power with high performance. The Harris 80C286 is available in speeds of 12.5MHz, 16MHz, 20MHz and 25MHz.

The 80C286 evolved from the industry standard 80C86 microprocessor. The 80C286 has vast architectural enhancements over its predecessor that allow the 80C286 to execute the same code with a significant performance increase. Disregarding the clock speed increase, when upgrading from an 80C86 to an 80C286, the 80C286 can execute the same code with an increase in throughput of up to 4 times that of the 80C86. This increase is solely due to the architectural enhancements.

It is common belief that replacing an 80C286 with the 32-bit 80386 microprocessor will yield similar performance increases. This is not the case. The new architecture gives the 80386 32-bit capability and increased protection features, but it does not significantly increase the throughput of a 16-bit 8086 or 80286 code. In most cases, when executing industry standard 8086 or 80286 code, replacing the 80C286 with an 80386 does not result in a significant performance increase. In some cases, such a replacement will actually cause a performance degradation.

Figure 1 illustrates a comparison of the number of clock cycles needed to execute several instructions available on all three microprocessors (80C86, 80C286, and 80386). This illustrates the dramatic effect of 80C286 architectural enhancements on performance when compared to the 80C86 and the lack of similar performance improvement when executing 8086/80286 code on the 80386.

With an 80C86 to 80C286 upgrade, system designers can execute existing 8086 code on the 80C286 and take advantage of an immediate performance upgrade. This same benefit is not realized when switching from an 80C286 to an 80386. This comparison illustrates that changing from an 80C286 to an 80386 does not yield throughput when executing the same industry standard 80C86/80C286 code (the world's largest base of microprocessor software).

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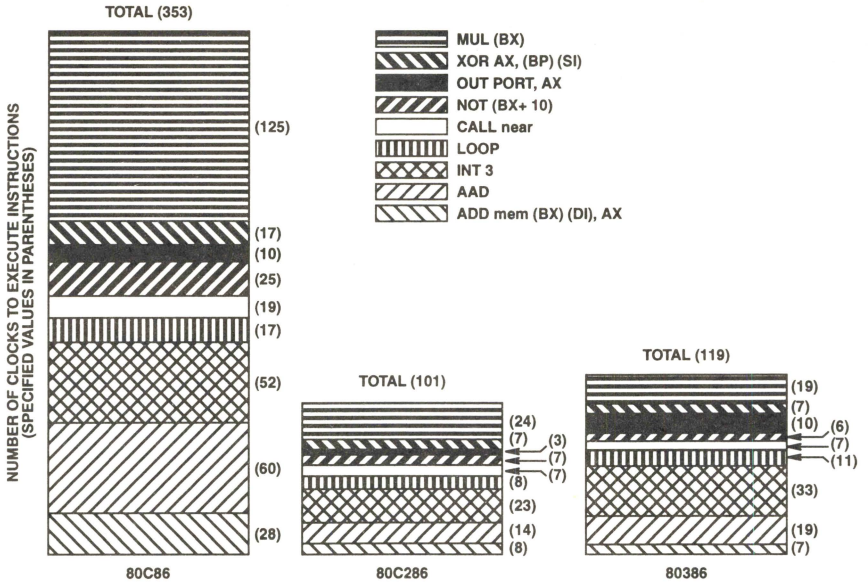


FIGURE 1. ARCHITECTURAL COMPARISON

Instruction Comparison

The Appendix in this document illustrates a direct comparison of the number of clock cycles needed to execute the same instructions on the 80C286 and the 80386. The table includes examples of instruction timing for all instructions available on both processors. Several addressing modes of each instruction type are included.

Of the 190 instruction examples analyzed, 74 of the instructions execute faster on the 80C286 than on the 80386; 66 of the instructions analyzed execute in the same number of clock cycles on both processors. This leaves only 50 instructions with improved performance on the 80386 (See Figure 2). Over 70% of the instructions analyzed execute as fast or faster on the 80C286 than on the 80386.

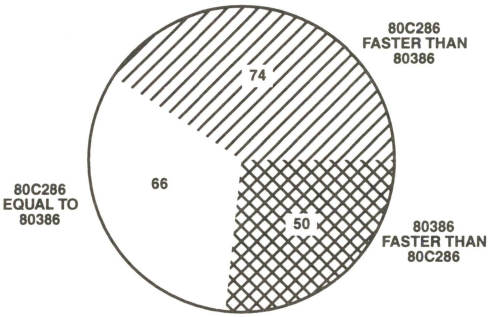


FIGURE 2. EXECUTION SPEED COMPARISON (NUMBER OF INSTRUCTIONS)

This is vastly different than the previous 86-286 upgrade. With that upgrade, the 80C286 exhibits equal or better performance than the 80C86 with 100% of the instructions. This clearly indicates the 80C286 is the processor best suited for executing industry standard 8086 family code.

The following discussion groups each of the instructions into one of several categories to analyze which applications will benefit from utilizing the 80C286. The categories used are:

- Jumps, Calls, Returns and Loops (Real Mode)
- I/O Instructions
- Logic, Arithmetic, Data Transfer, Shift and Rotate Instructions
- Interrupts
- Miscellaneous Instructions
- Protected Mode/Multi-Tasking Instructions

Jumps, Calls, and Loops

In real mode, near calls, jumps, and conditional jumps (transfers within the current code segment) all take the same number of clock cycles to execute on the 80C286 and the 80386. Since the segment sizes are larger on the 80386, the near transfer instructions on the 80386 can transfer a greater distance.

The far calls and jumps (transfers that switch to a new code segment; i.e., a code segment context switch) are faster on the 80C286: four clocks and one clock respectively. The far return instruction executes in three less clock cycles on the 80C286, and the near return takes one extra clock cycle. The protected mode calls, jumps, and returns are all faster

on the 80C286 and are discussed in the section on Protected Mode.

The loop instruction is three clock cycles faster on the 80C286 than the 80386. Thus, the 80C286 would save 300 clock cycles over the 386 if a LOOP instruction were executed 100 times.

INSTRUCTION	ADVANTAGE		
	80C286	NONE	80386
Near JMP and Call		X	
Far CALL, JMP and RET	X		
LOOP	X		

I/O Instructions

The 80C286 has significant advantage with the I/O instructions. The IN instruction is almost 2 1/2 times faster on the 80C286; the 80386 takes 7 extra clock cycles to execute the same instruction. The OUT instruction is over 3 times faster on the 80C286; again the 80386 takes 7 extra clock cycles to execute the same instruction. Executing the I/O instructions on the 80386 is equivalent to executing on the 80C286 with 7 wait states.

The string I/O instructions (INS and OUTS) are also significantly faster on the 80C286. The INS instruction is 10 clock cycles faster on the 80C286, and the OUTS instruction is 9 clock cycles faster. This is particularly important if the string operations are going to be used to input and output a large block of data using the REP prefix. Inputing 100 words of data with the REP INS instruction is 208 clock cycles faster on the 80C286. An even more significant difference can be seen when outputing 100 words with the REP OUTS instruction. In this case, the 80C286 is 800 clock cycles faster than the 80386.

INSTRUCTION	ADVANTAGE		
	80C286	NONE	80386
IN	X		
OUT	X		
INS	X		
OUTS	X		

Logic, Arithmetic, Data Transfer, Shift and Rotate Instructions

Most forms of logic, arithmetic, and data transfer instructions execute in the same number of clock cycles on both processors. Certain operand combinations of these instructions (immediate to register for example) take one extra clock to execute on the 80C286.

In real mode, the segment register transfer instructions execute as fast or faster on the 80C286 than they do on the 80386. For example, using the POP instruction to transfer data into a segment register is 2 clock cycles faster on the 80C286.

Most of the string manipulation instructions execute in the same number of clock cycles on both processors. The MOVS and STOS instructions are faster on the 80C286.

The divide instruction executes in the same number of clock cycles on both processors. The number of clocks to execute the multiply instruction on the 80386 is data dependent; the number of clocks to execute the same instruction on the 80C286 is fixed. On average, the multiply instruction is five clock cycles faster on the 80386, but depending on the data, the 80386 could be as many as 4 clock cycles slower the 80C286.

The rotate and shift instructions are faster on the 80386. Unlike the 80C286, the 80386 rotate and shift instructions do not depend on the number of bits to be shifted or rotated. Thus, the 80386 has the advantage with multi-bit rotate and shift instructions. The 80C286 does, however, execute single bit rotate and shift instructions faster.

INSTRUCTION	ADVANTAGE		
	80C286	NONE	80386
Most Logic and Arithmetic		X	
Certain Operand Combinations of Logic and Arithmetic			X
Divide		X	
Multiply			X
Single Bit Shift or Rotate	X		
Multi-Bit Shift or Rotate			X
String Instructions	X		

Interrupt Instructions

Interrupts are serviced more quickly on the 80C286. The INT instruction, in real mode, executes 14 cycles faster on the 80C286 than it does on the 80386. The INTO, BOUND, and other instructions that can cause an interrupt all benefit from the faster interrupt handling features of the 80C286. The return from interrupt instruction (IRET) is 7 clock cycles faster on the 80C286. The PUSHA and POPA instructions, frequently used by interrupt handling procedures, are both faster on the 80C286. Protected Mode interrupt handling is discussed in the Protected Mode section.

INSTRUCTION	ADVANTAGE		
	80C286	NONE	80386
INTN	X		
INTO	X		
BOUND (If Interrupt)	X		
Break Point Interrupt	X		

Miscellaneous Instructions

The BCD instructions, HLT, and CBW execute from 1 to 5 clock cycles faster on the 80C286. The instructions to set and clear individual flags and the CWD instruction all

execute in the same number of cycles on both processors. The ENTER, LEAVE, and BOUND instructions are from 1 to 3 cycles faster on the 80386. The BOUND instruction is only faster if an interrupt is not caused by the instruction.

INSTRUCTION	ADVANTAGE		
	80C286	NONE	80386
BCD Instructions	X		
Data Conversion (CBW, CWD)	X		
Flag Settling and Clearing		X	
BOUND (If No Interrupt)			X

Protected Mode/Multi-Tasking

When executing 80286 protected mode code, the 80C286 significantly out-performs the 80386. Task switching operations execute 100 to 113 clock cycles faster on the 80C286. The instruction to return from a called task is 63 clock cycles faster on the 80C286. This results in a very significant performance increase for systems utilizing the multi-tasking features.

Inter-segment JMP, CALL and segment loading instructions also operate faster on the 80C286. The 80C286 saves anywhere from 4 to 11 clock cycles depending on the particular inter-segment transfer instruction. In protected mode, the inter-segment return is also faster on the 80C286. The 80C286 is 7 clock cycles faster when executing an inter-segment return to the same privilege level and is 13 cycles faster on inter-segment returns to a different privilege level.

The instructions to initialize and check the protected mode registers execute as fast or faster on the 80C286. The IDTR access instructions are an exception to this in that they take one extra clock cycle to execute on the 80C286. The instruction to switch the processor to protected mode (LMSW) is 7 cycles faster on the 80C286.

Most of the 80286 protected mode access checking instructions operate as fast or faster on the 80C286 than on the 80386. The LAR instruction is one clock cycle faster on the 80C286 and the LSL instruction is 5 clock cycles faster. The VERW instruction executes in the same speed on both processors and the VERR is 5 cycles faster on the 80386. The ARPL instruction used in protected mode procedures for pointer validation is 10 clock cycles faster on the 80C286.

INSTRUCTION	ADVANTAGE		
	80C286	NONE	80386
Task Switching	X		
Segment Register Loading	X		
Inter-Segment Transfer	X		
System Register Instructions		X	
Inter-Segment Transfers	X		
Access Checking Instructions		X	

Subroutine Analysis

This section lists several subroutines and then compares the number of clock cycles each subroutine will take to execute on the 80C286 and on the 80386.

Example 1

This interrupt routine outputs a character to a terminal via a UART. The AL register must contain the character to be output. The routine first checks the status of the UART to determine if it is busy. If it is busy, the routine loops until the UART is free; when the UART is free, the character is output. Following is a listing of the code and the clock cycle analysis for the OUT_CHAR routine.

This sample procedure executes about 25% faster on the 80C286 than on the 386. The advantage is realized through the 80C286's faster interrupt handling and faster I/O instructions.

80C286 CLOCK CYCLES	80386 CLOCK CYCLES	OUT_CHARACTER PROC NEAR		
3	4		PUSHF	; save caller's flags.
3	2		PUSH AX	; save data to be output.
5	12	CK_STATUS:	IN AL, PORT_STATUS	; Input UART status.
6	5		CMP AL, BUSY	; Check If UART Busy.
3/7	3/7		JE CK_STATUS	; If busy go check again.
5	4		POP AX	; If not busy restore AX
3	10		OUT OUT_PORT, AL	; and output data.
5	5		POPF	; Restore Flags
17	22		IRET	; Return.
23	37		INT x	; Instruction to initiate OUTCHAR
				; Interrupt.
73	104	Total cycles if UART not busy.		
18	24	Number of cycles added for each loop while UART is busy.		

EXAMPLE 1.

Example 2

The second example outputs and entire string of characters using the previous interrupt routine (denoted by "INT x" in the code below). The DS:SI registers point to the beginning of the string to be output. The string is variable in length and must be terminated with the "$" character.

To output a string of 20 characters, the 80C286 would take 1,899 clock cycles; using the same routine, the 80386 would take 2,511 cycles. Each time a string of 20 characters is output, the 80C286 will save 612 clock cycles; an 80C286 performance increase of almost 25%. The advantage is realized through the 80C286's faster interrupt handling, faster I/O instructions, faster FAR transfer instructions and faster register saving and restoring instructions.

80C286 CLOCK CYCLES	80386 CLOCK CYCLES	OUT_STRING PROC FAR		
17	18		PUSHA	; save caller's registers.
5	5	NEXT:	LODSB	; Load first char to be output.
3	2		CMP AL, "$"	; Check to see if End of string.
3/7	3/7		JE done	; If end then go to DONE.
73	104		INT x	; If not end output character.
7	7		JMP next	; Go get next char to output.
19	24	DONE:	POPA	; Restore Registers when done.
15	18		RET	; Far Return.
13	17		Call OUT_STRING	; Far Call to initiate.
				; OUT_STRING procedure.
79+91/char	91+121/char	Total number of clocks to start and end routine. +Number of additional clocks to output each character in the output string.		

EXAMPLE 2.

Example 3

This example adds all the values of a source array in memory to the values of a destination array in memory. The result is stored in the destination array. Both arrays are assumed to be in the current data segment. The count (number of words in the array), offset of source array, and offset of destination array are all assumed to be placed on the stack (in that order) by the calling program. The source code for the procedure is listed in the Example 3 Table below.

80C286 CLOCK CYCLES	80386 CLOCK CYCLES	ADD_ARRAY PROC NEAR		
17	18		PUSHA	; save caller's registers.
2	2		MOV BP, SP	; Point BP to current stack
5	4		MOV CX, (bp+22)	; Load array size from stack
				; into CX.
5	4		MOV SI, (bp+20)	; Load offset of source array
				; from stack into SI.
5	4		MOV DI, (bp+18)	; Load offset of destination
				; array from stack into DI.
2	2		CLD	; Clear Direction Flag.
5	5	NEXT:	LODSW	; Load the source word into AX.
7	7		ADD (DI), AX	; Add source to destination.
3	2		ADD DI, 02	; Point DI to next data.
8/4	11		LOOP NEXT	; Continue to ADD all elements
				; in the two arrays.
19	24		POPA	; Restore Registers
11	10		RET 6	; Near return.
		; Following is the code necessary to set up and call the above procedure.		
5	5		PUSH count	; Put count parameter on stack
3	2		PUSH offset S_ARRAY	; Put offset of source array
				; on stack.
3	2		PUSH offset D_ARRAY	; Put offset of destination
				; array on stack.
7	7		CALL ADD_ARRAY	; Near Call to initiate
				; ADD_Array procedure.
84+(23*CX)-4	84+(25*CX)	Total number of clocks to start and end routine. +Number of additional clocks for each item in array to be added.		

EXAMPLE 3.

Both processors take the same number of clock cycles for initialization before the call and closing up after the call (84). The loop that does the adding is faster on the 80C286. To add two 100 word arrays, the 80C286 would take 2,380 clock cycles; the 80386 takes 2,584 (an additional 204 clocks) to execute the same routine. In this example, the LOOP instruction gives the 80C286 the performance over the 80386.

Example 4

This procedure is an example of an operating system procedure developed for a protected mode multi-privilege level system. The procedure INT_SEGMENT is passed a segment selector on the stack and will load that entire segment with zero's. The procedure is designed to execute at privilege level zero will a call gate at privilege level 3; this allows procedures executing at any level to utilize the INIT_SEGMENT procedure. INIT_SEGMENT provides protection checks to ensure that the procedure passing the parameter has valid access to the segment that it is trying to initialize. This prevents a procedure at privilege level three from initializing a segment at privilege level zero.

This example shows that when executing instructions used for privilege verification and privilege level transitions the 80C286 is faster than the 80386. Without taking the LODS instruction into account, the 80C286 is 38 clock cycles faster when executing the same procedure. With the LODS instruction, and assuming a segment size of 100 bytes, the 80C286 would execute this routine 238 clock cycles faster than the 80386.

80C286 CLOCK CYCLES	80386 CLOCK CYCLES	INIT_SEGMENT PROC FAR WC = 1		
17	18		PUSHA	; save caller's registers.
3	2		PUSH ES	;save ES register.
2	2		MOV BP, SP	;Point BP to top of stack.
5	4		MOV AX, (BP+22)	; Load AX with segment selector
				; passed as parameter on stack.
5	4		MOV BX, (BP+20)	; Load BX with return CS to
				; determine caller's CPL.
10	20		ARPL AX, BX	; Adjust the Privilege level of
				; the segment selector according
				; to the caller's CPL.
16	16		VERW AX	; Test for valid write access
3/7	3/7		JNE ERROR	; If no valid access go to error.
17	18		MOV ES, AX	; LOAD ES with segment to be
				; initialized.
14	20		LSL CX, AX	; Load segment size into CX.
2	2		XOR DI, DI	; Load zero into DI.
2	2		XOR AX, AX	; Load zero into AX.
2	2		CLD	; Clear decrement flag.
4+3*cx	5+5*cx		REP STOSB	; Init entire segment to 00.
2	2		CLC	; Clear carry to indicate segment
				; initialized with no errors.
20	21	DONE:	POP ES	; Restore ES register.
19	24		POPA	;Restore Register
55	68		RET 2	; Ret FAR to different privilege
2	2	ERROR:	STC	; SET carry to indicate error.
7	7		JMP DONE	
		; Code to push selector on stack and initiate INIT SEGMENT via call gate.		
3	2		PUSH DATA_SELECTOR	; Place Selector on stack.
82	86		CALL INIT_SEGMENT_GATE	;Instruction to initiate
				; INIT SEGMENT procedure.
253	283	Total clocks if ERROR because segment not accessible.		
283+(3*S)	321+(5*S)	Total number of clocks if segment is initialized to zeros. "S" represents size of segment in bytes.		

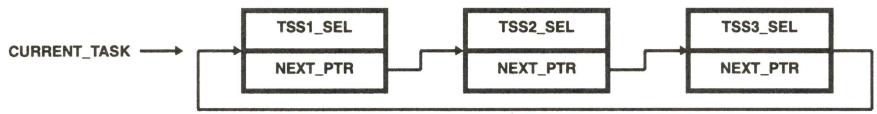
EXAMPLE 4.

Example 5

This Procedure is a task dispatcher that is invoked via an interrupt to cause a task switch to occur. This procedure utilizes a circular linked list of the tasks that need to be executed. A pointer called "CURRENT_TASK" points to the data structure for the current task being executed. The data structure contains the TSS for the task it is describing and a NEXT field that points to the data structure of the next task in the list to be executed. When the Task Dispatcher is invoked it switches the current pointer to the next task in the list and then invokes the new task by jumping to the TSS for that task. The data structure for the linked list is illustrated below.

The task dispatcher is actually a separate task that is invoked via an interrupt that signals that a new task should be initiated. Following is a listing for the simple task dispatcher.

The advantage of the 80C286 in this case is in the faster task switch instruction. The task switch instruction is 101 clock cycles faster on the 80C286 than on the 80386. This performance increase makes the 80C286 the clear choice for multi-tasking applications.



80C286 CLOCK CYCLES	80386 CLOCK CYCLES	TASK_DISPATCH PROC FAR		
5	4	START:	MOV BX, CURRENT TASK + 2	; Load BX with contents of next ; field of current TASK. BX will ; contain the address of the data ; structure for next task to run
3	2		MOV CURRENT TASK, BX	; Update Current Task to point to ; new task to be executed.
178	279		JMP DWORD PTR (BX-2)	; Start new task by jumping to TSS ; for new task.
7	7		JMP START	; JUMP to start for next time the ; TASK dispatcher is invoked.
193	292			

EXAMPLE 5.

Appendix

This appendix contains a table directly comparing the number of clock cycles necessary to execute all the instructions available on both the 80C286 and the 80386. The table includes several addressing modes of each instruction.

The table has five columns. The first column list the instruction being compared. The second column lists the number of clock cycles that the 80C286 needs to execute that instruction. The third column lists the number of clock cycles needed by the 80386 to execute the same instruction. The fourth column divides the number of cycles needed by the 80386 by the number of cycles needed by the 80C286. If this figure is greater than one, (see fifth column) then the 80C286 is faster than the 80386. For example, a 2.0 would indicate the 80C286 executes the same instruction twice as fast as the 80386. A 1.0 indicates that both processors execute the instruction in the same number of cycles. A number less than one indicates the 80386 is faster than the 80C286.

APPENDIX TABLE

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386	80386/ 80C286	80C286 FASTER THAN OR EQUAL TO 80386
AAA	3	4	1.33	√
AAD	14	19	1.36	√
AAM	16	17	1.06	√
AAS	3	4	1.33	√
ADC reg, reg	2	2	1.00	√

APPENDIX TABLE (Continued)

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386	80386/ 80C286	80C286 FASTER THAN OR EQUAL TO 80386
ADC mem, reg	7	7	1.00	√
ADC reg, immed	3	2	0.67	
ADC mem, immed	7	7	1.00	√
ADD reg, reg	2	2	1.00	√
ADD mem, reg	7	7	1.00	√
ADD reg, immed	3	2	0.67	
ADD mem, immed	7	7	1.00	√
AND reg, reg	2	2	1.00	√
AND mem, reg	7	7	1.00	√
AND reg, immed	3	2	0.67	
AND mem, immed	7	7	1.00	√
ARPL reg, reg	10	20	2.00	√
ARPL mem, reg	11	21	1.91	√
BOUND (no interrupt)	13	10	0.77	
CALL immed (near)	7	7	1.00	√
CALL immed (far real mode)	13	17	1.31	√
CALL immed (far PVAM)	26	34	1.31	√
CALL gate (same privilege PVAM)	41	52	1.27	√
CALL gate (different privilege PVAM)	82	86	1.05	√
CALL TSS (Task Switch PVAM)	177	278	1.57	√
CALL task_gate (Task Switch PVAM)	182	287	1.58	√
CBW	2	3	1.50	√
CLC	2	2	1.00	√
CLD	2	2	1.00	√
CLI	3	3	1.00	√
CLTS	2	5	2.50	√
CMC	2	2	1.00	√
CMP reg, reg	2	2	1.00	√
CMP mem, reg	6	5	0.83	
CMP reg, immed	3	2	0.67	
CMP mem, immed	6	5	0.83	
CMPS	8	10	1.25	√
CWD	2	2	1.00	√
DAA	3	4	1.33	√
DAS	3	4	1.33	√
DEC reg	2	2	1.00	√
DEC mem	7	6	0.86	
DIV word, reg	22	22	1.00	√
DIV word, mem	25	25	1.00	√

APPENDIX TABLE (Continued)

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386	80386/ 80C286	80C286 FASTER THAN OR EQUAL TO 80386
ENTER immed1, immed2 (immed 2 = 6)	36	35	0.97	
HLT	2	5	2.50	√
IDIV word, reg	25	27	1.08	√
IMUL word, mem	24	19	0.79	
IN	5	12	2.40	√
INC reg	2	2	1.00	√
INC mem	7	6	0.86	
INS	5	15	3.00	√
INT 3 (real mode)	23	33	1.43	√
INT immed (real mode)	23	37	1.61	√
INT immed (PVAM same privilege)	40	59	1.48	√
INT immed (PVAM different privilege)	78	99	1.27	√
INT TASK_GATE (PVAM Task Switch)	167	280	1.68	√
INTO (No Jump)	3	3	1.00	√
INTO (YES Jump real mode)	24	35	1.46	√
IRET (real mode)	17	22	1.29	√
IRET (PVAM same privilege)	31	38	1.23	√
IRET (PVAM different privilege)	55	82	1.49	√
IRET (PVAM task switch)	169	232	1.37	√
Jcond label (No jump)	3	3	1.00	√
Jcond label (Yes jump)	7	7	1.00	√
JMP near_label	7	7	1.00	√
JMP Far_label (real mode)	11	12	1.09	√
JMP FAR_LABEL (PVAM)	23	27	1.17	√
JMP CALL_GATE (PVAM same privilege)	38	45	1.18	√
JMP TASK_GATE (PVAM task switch)	183	288	1.57	√
JMP TSS (PVAM task switch)	178	279	1.57	√
LAHF	2	2	1.00	√
LAR reg	14	15	1.07	√
LAR mem	16	16	1.00	√
LDS (real mode)	7	7	1.00	√
LDS (PVAM)	21	22	1.05	√
LEA	3	2	0.67	
LEAVE	5	4	0.80	
LGDT	11	11	1.00	√
LIDT	12	11	0.92	
LLDT reg	17	20	1.18	√
LLDT mem	19	20	1.05	√
LMSW reg	3	10	3.33	√

APPENDIX TABLE (Continued)

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386	80386/ 80C286	80C286 FASTER THAN OR EQUAL TO 80386
LMSW mem	6	13	2.17	√
LODS	5	5	1.00	√
LOOP (Jump)	8	11	1.38	√
LOOP (No Jump)	4	11	2.75	√
LSL reg	14	20	1.43	√
LSL mem	16	21	1.31	√
LTR reg	17	23	1.35	√
LTR mem	19	27	1.42	√
MOV reg, reg	2	2	1.00	√
MOV mem, reg	3	2	0.67	
MOV reg, immed	2	2	1.00	√
MOV mem, immed	3	2	0.67	
MOV seg_reg, reg (real mode)	2	2	1.00	√
MOV seg_reg, mem (real mode)	5	5	1.00	√
MOV seg_reg, reg (PVAM)	17	18	1.06	√
MOV seg_reg, mem (PVAM)	19	19	1.00	√
MOVS	5	7	1.40	√
MUL reg	21	15	0.71	
NEG reg	2	2	1.00	√
NEG mem	7	6	0.86	
NOP	3	3	1.00	√
NOT reg	2	2	1.00	√
NOT mem	7	6	0.86	
OR reg, reg	2	2	1.00	√
OR mem, reg	7	6	0.86	
OR reg, immed	3	2	0.67	
OR mem, immed	7	7	1.00	√
OUT	3	10	3.33	√
OUTS	5	14	2.80	√
POP reg	5	4	0.80	
POP mem	5	5	1.00	√
POP seg_reg (real mode)	5	7	1.40	√
POP seg_reg (PVAM)	20	21	1.05	√
POPA	19	24	1.26	√
POPF	5	5	1.00	√
PUSH reg	3	2	0.67	
PUSH mem	5	5	1.00	√
PUSH seg_reg	3	2	0.67	
PUSHA	17	18	1.06	√

APPENDIX TABLE (Continued)

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386	80386/ 80C286	80C286 FASTER THAN OR EQUAL TO 80386
PUSHF	3	4	1.33	√
RCR or RCL reg, 1	2	9	4.50	√
RCR or RCL mem, 1	7	10	1.43	√
RCR or RCL reg, cl (cl = 4)	9	9	1.00	√
RCR or RCL mem, cl (cl = 4)	12	10	0.83	
RCR or RCL reg, 4	9	9	1.00	√
RCR or RCL mem, 4	12	10	0.83	
ROR or ROL reg, 1	2	3	1.50	√
ROR or ROL mem, 1	7	7	1.00	√
ROR or ROL reg, cl (cl = 4)	9	3	0.33	
ROR or ROL mem, cl (cl = 4)	12	7	0.58	
ROR or ROL reg, 4	9	3	0.33	
ROR or ROL mem, 4	12	7	0.58	
REP INS (cx = 100)	405	613	1.51	√
REP MOVS (cx = 100)	405	405	1.00	√
REP OUTS (cx = 100)	405	1205	2.98	√
REP STOS (cx = 100)	304	505	1.66	√
REP CMPS (cx = 100)	905	905	1.00	√
REPE CMPS (N = 100)	905	905	1.00	√
REPE SCAS (N = 100)	802	805	1.00	√
RET (near)	11	10	0.91	
RET (far real mode)	15	18	1.20	√
RET (far PVAM same privilege)	25	32	1.28	√
RET (far PVAM different privilege)	55	68	1.24	√
SAHF	2	3	1.50	√
SHIFT reg, 1 (SHIFT = SAL, SAR, SHR)	2	3	1.50	√
SHIFT mem, 1	7	7	1.00	√
SHIFT reg, cl (cl = 4)	9	3	0.33	
SHIFT mem, cl (cl = 4)	12	7	0.58	
SHIFT reg, 4	9	3	0.33	
SHIFT mem, 4	12	7	0.58	
SBB reg, reg	2	2	1.00	√
SBB mem, reg	7	6	0.86	
SBB reg, immed	3	2	0.67	
SBB mem, immed	7	7	1.00	√
SCAS	7	7	1.00	√
SGDT	11	9	0.82	
SIDT	12	9	0.75	
SLDT reg	2	2	1.00	√
SLDT mem	3	2	0.67	

APPENDIX TABLE (Continued)

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386	80386/ 80C286	80C286 FASTER THAN OR EQUAL TO 80386
SMSW reg	2	2	1.00	√
SMSW mem	3	2	0.67	
STS	2	2	1.00	√
STD	2	2	1.00	√
STI	2	3	1.50	√
STOS	3	4	1.33	√
STR reg	2	23	11.50	√
STR mem	3	27	9.00	√
SUB reg, reg	2	2	1.00	√
SUB mem, reg	7	6	0.86	
SUB reg, immed	3	2	0.67	
SUB mem, immed	7	7	1.00	√
TEST reg, reg	2	2	1.00	√
TEST mem, reg	6	5	0.83	
TEST reg, immed	3	2	0.67	
TEST mem, immed	6	5	0.83	
VERR reg	14	10	0.71	
VERR mem	16	11	0.69	
VERW reg	14	15	1.07	√
VERW mem	16	16	1.00	√
WAIT	3	6	2.00	√
XCHG reg, reg	3	3	1.00	√
XCHG reg, mem	5	5	1.00	√
XLAT	5	5	1.00	√
XOR reg, reg	2	2	1.00	√
XOR mem, reg	7	6	0.86	
XOR reg, immed	3	2	0.67	
XOR mem, immed	7	7	1.00	√
TOTAL number clocks to execute all instructions	6978	9048		
AVERAGE			1.24	
Number of Instructions faster on 80C286		74		
Number of Instructions equal on both processors		66		
Number of Instructions faster on 80386		50		
Total Number of instructions analyzed		190		

APPNOTE

No. AN112.1 March 1997

Harris Digital

80C286/80386 Hardware Comparison

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Introduction

The Harris 80C286 static CMOS microprocessor, available with maximum operating frequencies of 16MHz and 20MHz, offers both performance and design advantages over the 80386 when operating at the same frequency. When both the 80C286 and 80386 are operated on a 16-bit data bus, which fully supports industry standard 8086/80286 code, the 80C286 has better performance, and is significantly simpler to design with than the 80386. The 80C286 also uses significantly lower power than the 80386. The 80C286 also uses significantly lower power than the 80386, leading to less expensive, more reliable overall system design (See Figure 1).

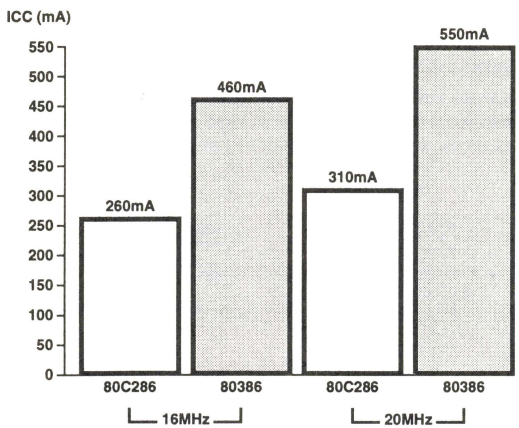


FIGURE 1. 80C286/80386 POWER CONSUMPTION COMPARISON

The following comparison highlights some of the performance advantages that exist on the 80C286:

Summary of 16-Bit Data Bus Performance

80C286

- The 80C286 already has all necessary control lines needed to implement a 16-bit data bus (Ref. section on Control Signals Required to Implement a 16-Bit Data Bus).
- The 80C286 supports a fully pipelined mode of operation for maximum system performance (Ref. section on Pipelined Operation on a 16-Bit Data Bus).
- The 80C286 remains in a pipelined mode of operation even when idle bus cycles occur (Ref. section on Idle Cycles).
- The 80C286 instruction prefetch takes one bus cycle to execute, thereby minimizing the time that the processor Execution Unit must wait should it need the bus (Ref. section on Instruction Prefetching a 16-Bit Data Bus).

80386

- The 80386 requires five additional control lines to be generated by external logic in order to implement a 16-bit data bus (Ref. section on Control Signals Required to Implement 16-Bit Data Bus).
- The 80386 does not support a fully pipelined mode of operation. Some pipelining can be achieved, but to accomplish this, external bus 'monitor' logic must be added to the system (Ref. section on Pipelined Operation on a 16-Bit Data Bus).
- The 80386's pipelining is disrupted by idle bus cycles. A non-pipelined bus cycle, usually with an additional wait state, must be executed before the 80386 can return to pipelined mode. Idle bus cycles occur an average of 9% of the time (Ref. section on Idle Cycles).
- The 80386 instruction prefetch takes two bus cycles to execute, which can cause performance degradation by forcing the Execution Unit of the processor to wait a full bus cycle for use of the bus in order to complete an instruction (Ref. section of Instruction Prefetching on a 16-Bit Data Bus).

16-Bit Data Bus Operation

This section will discuss the control signals required to implement a 16-bit data bus, as well as pipelined operation, idle cycles, and instruction prefetching on a 16-Bit Data Bus.

Control Signals Required to Implement a 16-Bit Data Bus

The 80C286 microprocessor has all the control lines needed to implement a 16-bit data bus resident on chip, no further control lines are required.

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80386 SIGNALS				16-BIT BUS SIGNALS			COMMENTS
BE3#	BE2#	BE1#	BE0#	A1	BHE#	BLE# (A0)	
H*	H*	H*	H*	X	X	X	X -No Active Bytes
H	H	H	L	L	H	L	
H	H	L	H	L	L	H	
H	H	L	L	L	L	L	
H	L	H	H	H	H	L	
H*	L*	H*	L*	X	X	X	X - Not Contiguous Bytes
H	L	L	H	L	L	H	
H	L	L	L	L	L	L	
L*	H*	H*	L*	X	X	X	X - Not Contiguous Bytes
L*	H*	L*	H*	X	X	X	X - Not Contiguous Bytes
L*	H*	L*	L*	X	X	X	X - Not Contiguous Bytes
L	L	H	H	H	L	L	
L*	L*	H*	L*	X	X	X	X - Not Contiguous Bytes
L	L	L	H	L	L	H	
L	L	L	L	L	L	L	

NOTE: BLE# Asserted when D0-D7 of 16-Bit Bus is Active.
BHE# Asserted when D8-D15 of 16-Bit Bus is Active.
A1 Low for All Even Words; A1 High for All Odd Words.

Key: X = Don't Care
H = High Voltage Level
L = Low Voltage Level
* = A Non-Occurring Pattern of Byte Enables; Either None are Asserted, or the Pattern has Byte Enables Asserted for Non-Contiguous Bytes.

FIGURE 2. A1, BLE#, AND BHE# SIGNAL GENERATION TABLE

In order to implement a 16-bit data bus with the 80386 microprocessor, it is necessary to create at least the following five additional control signals: Address Line 1 (A1), Bus Low Enable (BLE#), Bus High Enable (BHE#), Bus Size 16-Bits (BS16#), and Next Address (NA#).

The first of these signals, A1, is an additional address line required to convert the granularity of the 80386's address space from double-word size entities (32-bit) to word size entities (16-bit). The second two signals, BLE# and BHE#, primarily serve as chip selects which enable the appropriate byte or bytes onto the 16-bit data bus. These three signals are generated from the four 80386 byte enables (BE0# - BE3#) as shown in Figure 2. The logic to implement these signals is shown in Figure 3.

In addition, to these three control signals generated from 80386 signals as outputs, two input control signals to the 80386 must be generated to external logic (BS16# and NA#)

BS16# is used to inform the 80386, on a cycle-by-cycle basis that a 16-bit bus size is to be used for data transfer. NA# is used to request that the 80386 put the next cycle address on the bus early, thereby pipelining that cycle.

The 80386, therefore, requires five additional control lines, three outputs and two inputs, in order to implement a 16-bit data bus. The generation of these control lines, in turn, requires additional 'glue' logic (which also introduces additional signal propagation delay, thereby reducing address access time available to the system), and finally, there is additional bus cycle 'monitor' logic necessary if the 16-bit data bus is to be pipelined for higher performance.

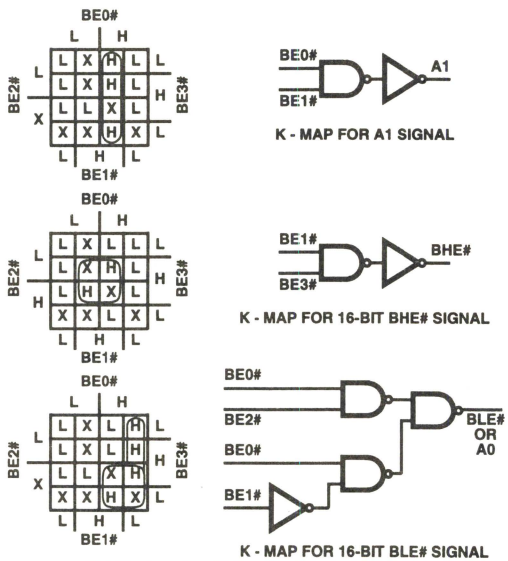


FIGURE 3. A1, BLE#, AND BHE# LOGIC

Pipelined Operation on a 16-Bit Data Bus

At a given clock frequency, pipelined address operation increases a system's performance, while simultaneously allowing relatively slower memories and I/O devices to be used. Pipelined address operation provides the system increased address access time, and increased address decoding time.

The 80C286 is optimized for, and directly supports, fully pipelined bus operations on a 16-bit data bus. In other words, the 80C286 performs all bus operations in a fully pipelined mode.

The 80386 does not support fully pipelined operation on a 16-bit data bus. In order to pipeline a bus cycle on the 80386, the Next Address (NA#) signal must be asserted to the processor. If the Next Address (NA#) signal and the Bus Size 16-Bit (BS16#) signal are both asserted in the same bus cycle, the NA# signal will not be recognized. Since, the BS16# signal must be asserted to the 80386 for many patterns of 16-bit and 8-bit transfers to take place correctly, the pipelining of transfers over a 16-bit bus is limited.

To allow pipelining of 16-bit data, external logic must be implemented to monitor the type of bus cycle taking place, decide if the cycle can be pipelined, and, if so, negate the BS16# signal to the 80386 and assert the NA# signal. Pipelining is possible only if the bus cycle is one of the following three types:

(1) A read operand cycle using only the lower half of the data bus.

(2) A write operand cycle using only the lower half of the data bus.

(3) A write operand cycle using only the upper half of the data bus.

The 80386 will not allow 16-bit pipelining of read or write cycles that have byte alignments that do not conform to one of the previously mentioned three types.

The 80C286, then, fully supports address pipelining, yielding the highest possible system performance, while using relatively lower performance (and therefore cheaper) memories and peripherals. The 80386, however, does not support fully pipelined 16-bit bus operation, and, to support even partial pipelining, requires external bus 'monitor' logic.

Idle Cycles

Another factor to consider when evaluating 80C286 and 80386 performance is the effect of idle cycles on pipelined operation. Calculations have shown that, on average, bus idle cycles occur in the system approximately 9% of the time. The effect of idle cycles on pipelining is quite different on the 80C286 that on the 80386.

The 80C286 pipelined operation is not affected by idle cycles. When an idle cycle or cycles occur in a stream of pipelined bus cycles, the 80C286 returns to pipelining bus cycles immediately after the last idle cycle. In this way, each device on the bus (e.g. memory, peripheral) maintains a fixed timing associated with that device, and therefore always uses the minimum number of wait states required for that device.

On the other hand, the 80386 pipelined operation is disrupted by idle cycles. With the 80386, an idle cycle or cycles occurring in a pipelined stream of bus cycles breaks the pipelining operation. Once an idle cycle has occurred, a non-pipelined bus cycle must always be executed prior to resuming pipelining. Since a non-pipelined bus cycle will have different timing than pipelined bus cycle (even to the same device), an additional wait state must be added to this bus cycle. This not only degrades performance, but requires additional external logic to differentiate between a pipelined bus cycle access, and a non-pipelined bus cycle access, event to the same device with the same address.

From the preceding, it can be seen that **when executing 16-bit code, the 80C286 has a 9% performance increase over the 80386, due to the manner in which each processor handles idle cycles alone.** Note, that with the 80386, a pipelined stream of bus cycles will always be disrupted when an idle cycle occurs, whether using a 16-bit data bus or a 32-bit data bus. In either case, a non-pipelined bus cycle must be executed prior to resuming pipelined operation.

Instruction Prefetching on a 16-Bit Data Bus

One final factor needs to be considered in the evaluation of 80C286 and 80386 performance on a 16-bit data bus; the effect that prefetching instructions has on instruction execution time. Prefetching of instructions is done by the processor Bus Unit on both the 80C286 and 80386. The prefetch is done when the bus would otherwise be idle for the upcoming cycle, and the prefetch queue is not full.

The 80C286 does word size (16-bit) prefetching of instructions, and therefore completes it's prefetch activities in one bus cycle. This minimizes the waiting period to gain access to the bus by other processor entities, such as the Execution Unit.

The 80386 does doubleword (32-bit) prefetching of instructions, even on a 16-bit bus. This means that once a prefetch has begun execution, two bus cycles are required to complete the prefetch. If, for instance, the processor, Execution Unit requires the bus for a data fetch or write in order to complete an executing instruction, it must wait for the two bus cycles of prefetch to complete before it can access the bus. This can substantially degrade instruction execution time.

32-Bit Data Bus Operation

This section discusses operating the 80386 on a 32-bit bus in order to overcome some of the handicaps it suffers on a 16-bit bus. In addition, several advantages and disadvantages associated with the 80386 on a 32-bit bus are considered.

Hardware Advantages of the 80386 on a 32-Bit Data Bus

There are several advantages to operating the 80386 on a 32-bit data bus as opposed to a 16-bit data bus. Some of the control lines that were required for a 16-bit data bus are

eliminated (A1, BLE#, BHE#, and BS16#). It is possible to come closer to a fully pipelined mode of operation, although idle cycles will still disrupt the pipelining 9% of the time. Finally, prefetching on a 32-bit bus executes in one bus cycle instead of two. Offsetting these advantages, however are several major disadvantages.

Hardware Disadvantages of the 80386 on a 32-bit Data Bus

When using a full 32-bit data bus, the chip complexity of a 80386 based system is increased over a 16-bit system. Twice as many transceivers (four instead of two) are required. In addition, in order to accommodate the additional 16 data lines of the 32-bit bus, twice as many memory devices are typically required with the 32-bit system as compared to a 16-bit system. This amounts to an increase in DRAM, alone, of from 18 devices in a typical 16-bit system to 36 devices in a typical 32-bit system.

The 16 additional data lines of the 32-bit bus increase the EMI problems inherent in the system. The additional coupling and crosstalk between data lines must be taken into consideration when laying out the system PC board.

There is significant increase in the amount of board space used as result of the additional chips required to implement a 32-bit bus, as well as the 16 additional data lines. This results in a larger, more complex (and more expensive) PC board that with a 16-bit system, often requiring an increase in the number of board layers.

Reference

[1] "80386 Hardware Reference Manual", Intel Corporation, 1987.

Harris Semiconductor

APPNOTE

No. AN120.1 March 1997

Harris Digital

Interfacing the 80C286-16 with the 80287-10

Author: Ted Schaufelberger

Introduction

An important requirement in many systems is the ability to off-load numeric data processing. In an 80C286 system, this can be accomplished with an 80287 numeric co-processor. However, as processor speeds increase, it may become necessary to interface a high speed 80C286 processor with a lower speed 80287. This Document will briefly describe the interface between a 16MHz 80C286 (80C286-16) and a 10MHz 80287 (80287-10).

Interfacing the 80C286 with an 80287 can be broken down into three main areas:

(1) Bus control lines and data lines which coordinate and implement the flow of data between the two processors (i.e. the data lines, chip select lines, and read/write lines).

(2) The clock line(s), which drive the two processors.

(3) The four status lines through which the 80C286 and 80287 directly communicate status information to one another - comprised of the $\overline{\text{BUSY}}$, $\overline{\text{ERROR}}$, Peripheral Request (PEREQ), and Peripheral Acknowledge ($\overline{\text{PEACK}}$) lines.

Bus Control Lines

The various bus control and data lines in most systems would be coordinated by either a bus controller (such as the 82C288), or a bus controller subsection of an 80C286 oriented chip set. All requisite bus control timing between a 16MHz 80C286, and a 10MHz 80287 would then be handled by these devices (typically with one wait-state inserted to allow for the slower 80287-10).

Clock Lines

A system using a 16MHz 80C286 with a 10MHz 80287 requires separate clock lines for the two processors. The 32MHz system clock used by the 80C286-16 is too fast for the 80287 ±10, necessitating a dedicated clock driver for the 80287. This clock driver should supply a 10MHz clock to the 80287 with a 1/3 duty cycle to allow the 80287-10 to run at it's full 10MHz capability. One solution for providing this clock is the 82C84A-1, which meets this specification with either a 30MHz crystal at it's crystal inputs, or a 30MHz external frequency input to it's EFI pin. In either case, a 10MHz 1/3 duty cycle clock is output to the 80287. Note that when using a dedicated clock driver such as this, the CKM pin of the 80287 must be pulled up.

Status Lines

The 80C286 and 80287 communicate status information with one another through four signals; the $\overline{\text{BUSY}}$ line, the $\overline{\text{ERROR}}$ line, the peripheral request line (PEREQ), and the $\overline{\text{PEACK}}$ line.

The $\overline{\text{BUSY}}$ and $\overline{\text{ERROR}}$ lines can be connected from the 80287 to a 80C286-oriented chipset, or from the 80287 directly to a 80C286. In the case of the chipset interface, the signal timing between the 80287 and 80C286 is coordinated by the chipset. In the case of the direct 80287 to 80C286 interface, the signal timing is handled by the 80C286, and, since the signal flow direction is from the 80287 to the 80C286 (i.e. from the slower device to the faster device), no additional hardware is required to achieve proper timing.

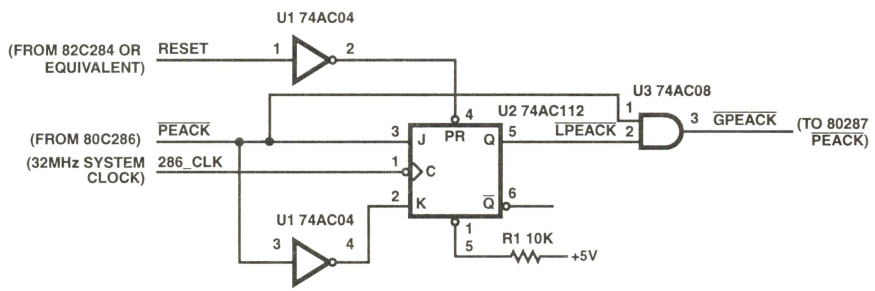


FIGURE 1. PEAK STRETCH CIRCUIT

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The peripheral request (PEREQ) line should be connected directly from the 80287 to the 80C286, and again, since the signal flow direction is from the 80287 to the 80C286, no additional hardware is required.

The peripheral acknowledge ($\overline{PEACK}$) line is normally connected directly from the 80C286 to the 80287. In this case the signal flow direction is from the 80C286 to the 80287 (i.e. faster device to slower device), and the $\overline{PEACK}$ active time is not guaranteed to meet the requirements of the slower 80287-10. Worst case timing for the 80C286-16 reveals that $\overline{PEACK}$ output could be as short as 45.5ns (i.e. $\overline{PEACK}$ (min) = 45.5ns). The 80287-10 input requirement is $\overline{PEACK}$ (min) = 60ns.

The proper $\overline{PEACK}$ timing can be achieved using the circuit shown in Figure 1 comprised of a 74AC04, 74AC08, and a 74AC112. Referring to the timing diagram shown in Figure 2, it can be seen that this circuit effectively "stretches" the 80C286's $\overline{PEACK}$ output (in the form of $\overline{GPEACK}$) to 72.7ns, which satisfies the 80287-10 requirement.

The operation of the circuit shown in Figure 1 is as follows:

(1) The RESET signal (which is also applied to the 80C286) is used to initialize the 'AC112 to a known inactive state (Q = 1).

(2) When the 80C286 asserts the $\overline{PEACK}$ signal, the gated version of this signal ($\overline{GPEACK}$) is asserted with minimal delay (7.9ns through the 'AC08).

(3) On the falling edge of the 80C286 CLK at the beginning of Phase 2 of the T_S cycle, the low state of $\overline{PEACK}$ is clocked into the 'AC112. This effectively holds $\overline{GPEACK}$ low for an additional clock cycle longer than standard $\overline{PEACK}$ timing.

(4) On the falling edge of the 80C286 CLK at the beginning of phase 2 of the first T_C cycle, the high state of $\overline{PEACK}$ is clocked into the 'AC112, which then causes $\overline{GPEACK}$ to go inactive.

The net effect of this circuit operation is to extend the 80C286's Peripheral Acknowledge signal to the 80287-10 sufficiently to meet it's requirements.

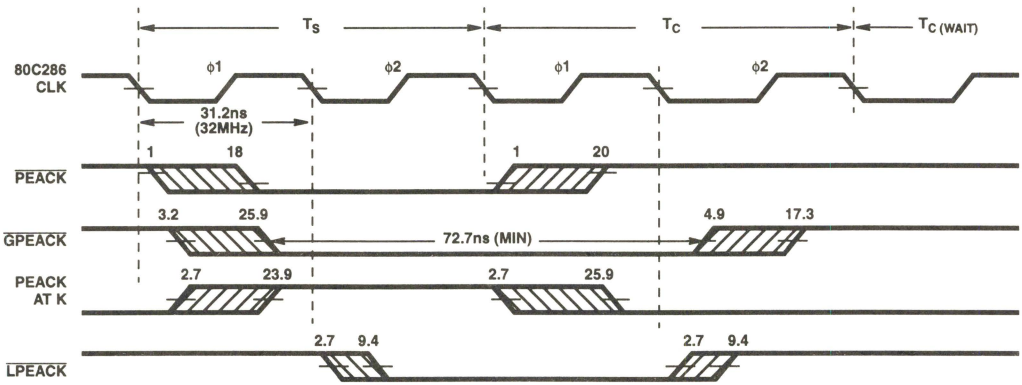


FIGURE 2. PEACK CYCLE TIMING

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APPNOTE

No. AN121.1 March 1997

Harris Digital

Harris 80C286 Performance Advantages Over the 80386SX

Author: Ted Dimbero

Introduction

The Harris 80C286, operating at the same frequency as the 80386SX, can outperform the 80386SX when executing software written for the 80286 and 8086, including all MS-DOS™, PC-DOS™ and OS/2™ -based programs. This performance advantage comes from the 80C286 requirement of fewer clock cycles to execute the same instructions as the 80386SX.

Industry standard 16-bit 8086/80286 code can execute 15-25% more efficiently on the 80C286 than on the 80386SX. There is no performance advantage gained by simply moving a system design from an 80C286 to an 80386SX. The 80C286 is the processor best suited for executing 16-bit 8086/80286 code.

The difference in clock cycle requirements is summarized in Figure 1. Of the 182 common instructions, the 80C286 executes 79 instructions faster than the 80386SX. Another 64 instructions execute in the same number of clock cycles on both processors.

Overall, 143 instructions (78% of all common instructions) execute as fast or faster on the 80C286 than on the 80386SX.

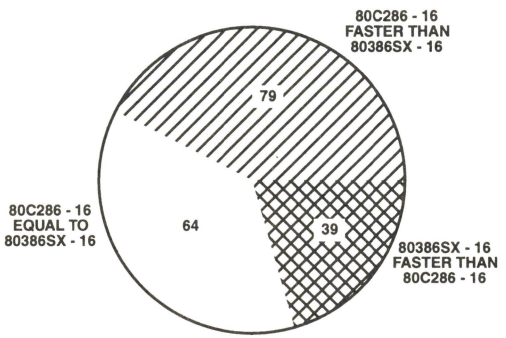


FIGURE 1. EXECUTION SPEED COMPARISON (NUMBER OF INSTRUCTIONS)

Taking this comparison one step further and looking at the performance contribution of each subset of instructions, those instructions that execute faster on the 80386SX are executed an average of 1.6 clock cycles faster. However, the instructions which execute faster on the 80C286 execute in an average of 23.1 clock cycles less than on the 80386SX.

Operating Speeds

The Harris 80C286 is available with operating frequencies of 12.5, 16, 20 and 25MHz. The 80386SX maximum operating frequency is limited to 16MHz. The instruction comparisons in Figure 1 (and throughout this document) evaluate the number of clock cycles required to execute the same instructions on both the 80386SX and the 80C286. Therefore, it illustrates the performance differences when the two processors are running at the same speed.

As this analysis shows, the 80C286 has the performance advantage when the two processors are running at the same speed. This 80C286 advantage is significantly greater when speed differences are taken into consideration.

The 80C286-25, for example, can execute 100% of the instructions available on both processors faster than a 16MHz 80386SX. In some cases, a 2X performance increase can be seen with the 80C286-25 compared to the 80386SX-16 (see Table 1).

This is not a benchmark number that can be credited to differences in system design; it illustrates a one-to-one comparison of the length of time it takes to execute the same instruction on the two processors. That is, given two equivalent systems (both having the same disk access speed, same number of wait states, similar cache controllers, etc), the 80C286-25 system would outperform the 80386SX system on any benchmark.

Table 1 illustrates a performance comparison of the 80386SX-16, 80C286-16, 80C286-20 and 80C286-25. The table lists the number of clock cycles needed to execute five different subroutines (see examples 1-5 in Subroutine Analysis section) and the total execution times for each subroutine for the two processors at varying operating frequencies.

In each of these examples, the results show that the 80C286 outperforms the 80386SX. In addition, the 80C286-25 shows performance increases of 170%-250% over the 80386SX-16. The 80C286 not only outperforms the 80386SX at similar operating frequencies, it also provides a path to increased performance by offering operating frequencies up to 25MHz which are not available with the 80386SX.

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TABLE 1.

SUB-ROUTINES (PGS 6-9)	80386SX # CLOCK CYCLES	80C286 # CLOCK CYCLES	80386SX-16 EXECUTION TIME (μs)	80C286-16		80C286-20		80C286-25	
				EXECUTION TIME (μs)	PER-FORMANCE INCREASE OVER 80386SX-16	EXECUTION TIME (μs)	PER-FORMANCE INCREASE OVER 80386SX-16	EXECUTION TIME (μs)	PER-FORMANCE INCREASE OVER 80386SX-16
Example 1	104	73	6.5	4.6	141%	3.6	180%	2.92	223%
Example 2	2511	1899	156.9	118.7	132%	94.9	165%	75.9	132%
Example 3	2584	2380	161.5	148.7	108%	119.0	135%	95.2	170%
Example 4	837	583	52.3	36.4	143%	29.1	179%	23.3	224%
Example 5	307	193	19.2	12.1	158%	9.65	198%	7.7	249%

Architecture Background

The 80C286 static CMOS microprocessor combines low operating and standby power with high performance and operating frequencies up to 25MHz.

The 80C286 evolved from the industry standard 80C86 microprocessor and has vast architectural enhancements over its predecessor that allow the 80C286 to execute the same code with a significant performance increase.

Disregarding the clock speed increase, when upgrading from an 80C86 to an 80C286, the 80C286 can execute the same code with an increase in throughput of up to 4 times that of the 80C86. This increase is solely due to the architectural enhancements.

It is a common belief that replacing an 80C286 with the 80386SX microprocessor will yield similar performance increases. This is not the case. The new architecture gives the 80386SX 32-bit internal capability but it does not significantly increase the throughput of 16-bit 8086 or 80286 code.

When executing industry standard 8086 or 80286 code, replacing the 80C286 with an 80386SX does not result in a significant performance increase. In many cases, such a replacement will actually cause a performance degradation. This is evident in the following areas:

(1) Input/Output Handling

(2) Interrupt Handling

(3) Control Transfer (Loop, Jump, Call)

(4) 80286 Protected Mode Systems

(5) Multi-Tasking and Task Switching Operations.

The performance advantage of the 80C286 is especially evident in areas such as:

- Protected Mode Operating System - such as OS/2 and Xenix™
- Multi-Tasking Systems.
- Control Applications — utilizing interrupt and I/O instructions.
- Structured Software — utilizing many Control transfer instructions.
- Operating Systems that rely on interrupts to perform functions - such as MS-DOS, PC-DOS and OS/2.
- Upgrading 16-bit 80C86 applications for increased performance.

Figure 2 illustrates a comparison of the number of clock cycles needed to execute several instructions available on all three microprocessors (80C86, 80C286, and 80386SX). This illustrates the dramatic effect of 80C286 architectural enhancements on performance when compared to the 80C86 and the lack of similar performance improvement when executing 8086/80286 code on the 80386SX.

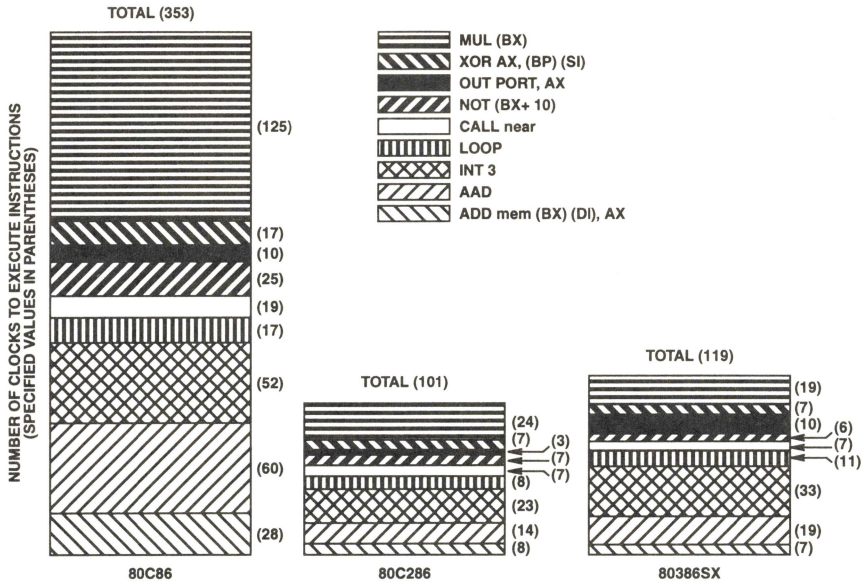


FIGURE 2. ARCHITECTURAL COMPARISON

Hardware System Comparison

Pipelined Operation on a 16-Bit Data Bus

At a given clock frequency, pipelined address operation increases a system's performance, while simultaneously allowing relatively slower memories and I/O devices to be used. Pipelined address operation provides the system increased address access time, and increased address decoding time.

80C286

The 80C286 supports a fully pipelined mode of operation for maximum system performance.

The 80C286 remains in a pipelined mode of operation even when idle bus cycles occur.

80386SX

The 80386SX does not support a fully pipelined mode of operation. Some pipelining can be achieved, but to accomplish this, external bus 'monitor' logic must be added to the system.

The 80386SX's pipelining is disrupted by idle bus cycles. A non-pipelined bus cycle, usually with an additional wait state, must be executed before the 80386SX can return to pipelined mode. Idle bus cycles occur an average of 9% of the time.

Idle Cycles

Another factor to consider when evaluating 80C286 and 80386SX performance is the effect of idle cycles on pipelined operation. Calculations have shown that, on average, bus idle cycles occur in the system approximately 9% of the time. The effect of idle cycles on pipelining is quite different on the 80C286 than on the 80386SX.

The 80C286 pipelined operation is not affected by idle cycles. When an idle cycle or cycles occur in a stream of pipelined bus cycles, the 80C286 returns to pipelining bus cycles immediately after the last idle cycle. In this way, each device on the bus (e.g. memory, peripheral) maintains a fixed timing associated with that device, and therefore always uses the minimum number of wait states required for that device.

On the other hand, the 80386SX pipelined operation is disrupted by idle cycles. With the 80386SX, an idle cycle or cycles occurring in a pipelined stream of bus cycles breaks the pipelining operation. Once an idle cycle has occurred, a non-pipelined bus cycle must always be executed prior to resuming pipelining. Since a non-pipelined bus cycle will have different timing than a pipelined bus cycle (even to the same device), an additional wait state must be added to this bus cycle. This not only degrades performance, but requires additional external logic to differentiate between a pipelined bus cycle access, and a non-pipelined bus cycle access, even to the same device with the same address.

From the preceding, it can be seen that when executing 16-bit code, the 80C286 has a 9% performance increase over the 80386SX, due to the manner in which each processor handles idle cycles alone.

Instruction Comparison

The Appendix in this document illustrates a direct comparison of the number of clock cycles needed to execute the same instructions on the 80C286 and the 80386SX. The table includes examples of instruction timing for all instructions available on both processors. Several addressing modes of each instruction type are included.

Of the 182 instruction examples analyzed, 79 of the instructions execute faster on the 80C286 than on the 80386SX; 64 of the instructions analyzed execute in the same number of clock cycles on both processors. This leaves only 39 instructions with improved performance on the 80386SX (See Figure 2). Over 78% of the instructions analyzed execute as fast or faster on the 80C286 than on the 80386SX.

This is vastly different than the previous 8086-to-80286 upgrade. With that upgrade, the 80C286 exhibits equal or better performance than the 80C86 with 100% of the instructions.

This clearly indicates that the 80C286 is the processor best suited for executing industry standard 8086 and 80286 code.

The following discussion groups each of the instructions into one of several categories to analyze which applications will benefit from utilizing the 80C286. The categories used are:

- Jumps, Calls, Returns and Loops (Real Mode).
- I/O Instructions.
- Logic, Arithmetic, Data Transfer, Shift and Rotate Instructions.
- Interrupts.
- Miscellaneous Instructions.
- Protected Mode/Multi-Tasking Instructions.

Jumps, Calls and Loops

In real mode, near calls, jumps, and conditional jumps (transfers within the current code segment) all take the same number of clock cycles to execute on the 80C286 and the 80386SX. Since the segment sizes are larger on the 80386SX, the near transfer instructions on the 80386SX can transfer a greater distance.

The far calls and jumps (transfers that switch to a new code segment; i.e., a code segment context switch) are faster on the 80C286: four clocks and one clock respectively. The far return instruction executes in three less clock cycles on the 80C286, and the near return takes one extra clock cycle. The protected mode calls, jumps, and returns are all faster on the 80C286 and are discussed in the section on Protected Mode.

The loop instruction is three clock cycles faster on the 80C286 than the 80386SX. Thus, the 80C286 would save 300 clock cycles over the 80386SX if a LOOP instruction were executed 100 times.

INSTRUCTION	ADVANTAGE		
	80C286	NONE	80386SX
Near JMP and Call		X	
Far CALL, JMP and RET	X		
LOOP	X		

I/O Instructions

The 80C286 has a significant advantage with the I/O instructions. The IN instruction is almost 2 1/2 times faster on the 80C286; the 80386SX takes 7 extra clock cycles to execute the same instruction. The OUT instruction is over 3 times faster on the 80C286; again the 80386SX takes 7 extra clock cycles to execute the same instruction. Executing the I/O instructions on the 80386SX is equivalent to executing on the 80C286 with 7 wait states.

The string I/O instructions (INS and OUTS) are also significantly faster on the 80C286. The INS instruction is 10 clock cycles faster on the 80C286, and the OUTS instruction is 9 clock cycles faster. This is particularly important if the string operations are going to be used to input or output a large block of data using the REP prefix. Inputting 100 words of data with the REP INS instruction is 208 clock cycles faster on the 80C286. An even more significant difference can be seen when outputting 100 words with the REP OUTS instruction. In this case, the 80C286 is 800 clock cycles faster than the 80386SX.

INSTRUCTION	ADVANTAGE		
	80C286	NONE	80386SX
IN	X		
OUT	X		
INS	X		
OUTS	X		

Logic, Arithmetic, Data Transfer, Shift and Rotate Instructions

Most forms of the logic, arithmetic, and data transfer instructions execute in the same number of clock cycles on both processors. Certain operand combinations of these instructions (immediate to register for example) take one extra clock cycle to execute on the 80C286.

In real mode, the segment register transfer instructions execute as fast or faster on the 80C286 than they do on the 80386SX. For example, using the POP instruction to transfer data into a segment register is 2 clock cycles faster on the 80C286.

Most of the string manipulation instructions execute in the same number of clock cycles on both processors. The MOVS and STOS instructions are faster on the 80C286.

The divide instruction executes in the same number of clock cycles on both processors. The number of clocks to execute the multiply instruction on the 80386SX is data dependent;

the number of clocks to execute the same instruction on the 80C286 is fixed. On average, the multiply instruction is five clock cycles faster on the 80386SX, but independing on the data, the 80386SX could be as many as 4 clock cycles slower than the 80C286.

The rotate and shift instructions are faster on the 80386SX. Unlike the 80C286, the 80386SX rotate and shift instructions do not depend on the number of bits to be shifted or rotated. Thus, the 80386SX has the advantage with multi-bit rotate and shift instructions. The 80C286 does, however, execute single bit rotate and shift instructions faster.

INSTRUCTION	ADVANTAGE		
	80C286	NONE	80386SX
Most Logic and Arithmetic		X	
Certain Operand Combinations of Logic and Arithmetic			X
Divide		X	
Multiply			X
Single Bit Shift or Rotate	X		
Multi-Bit Shift or Rotate			X
String Instructions	X		

Interrupt Instructions

Interrupts are serviced more quickly on the 80C286. The INT instruction, in real mode, executes 14 cycles faster on the 80C286 than it does on the 80386SX. The INTO, BOUND, and other instructions that can cause an interrupt all benefit from the faster interrupt handling features of the 80C286. The return from interrupt instruction (IRET) is 7 clock cycles faster on the 80C286. The PUSHA and POPA instructions, frequently used by interrupt handling procedures, are both faster on the 80C286. Protected Mode interrupt handling is discussed in the Protected Mode section.

INSTRUCTION	ADVANTAGE		
	80C286	NONE	80386SX
INT n	X		
INTO	X		
BOUND (If Interrupt)	X		
Break Point Interrupt	X		

Miscellaneous Instructions

The BCD instructions, HLT, and CBW execute from 1 to 5 clock cycles faster on the 80C286. The instructions to set and clear individual flags and the CWD instruction all execute in the same number of cycles on both processors. The ENTER, LEAVE, and BOUND instructions are from 1 to 3 cycles faster on the 80386SX. The BOUND instruction is only faster if an interrupt is not caused by the instruction.

INSTRUCTION	ADVANTAGE		
	80C286	NONE	80386SX
BCD Instructions	X		
Data Conversion (CBW, CWD)	X		
Flag Settling and Clearing		X	
BOUND (If No Interrupt)			X

Protected Mode/Multi-Tasking

When executing 80286 protected mode code, the 80C286 significantly out-performs the 80386SX. Task switching operations execute 100 to 271 clock cycles faster on the 80C286. The instruction to return from a called task is 63 clock cycles faster on the 80C286. This results in a very significant performance increase for systems utilizing the multi-tasking features. The 80C286 is clearly better suited than the 80386SX for running protected mode operating systems such as OS/2 and Xenix.

Inter-segment JMP, CALL and segment loading instructions also operate faster on the 80C286. The 80C286 saves anywhere from 4 to 11 clock cycles depending on the particular inter-segment transfer instruction. In protected mode, the inter-segment return is also faster on the 80C286. The 80C286 is 11 clock cycles faster when executing an inter-segment return to the same privilege level and is 17 cycles faster on inter-segment returns to a different privilege level.

The instructions to initialize and check the protected mode registers execute as fast or faster on the 80C286. The IDTR access instructions are an exception to this in that they take one extra clock cycle to execute on the 80C286. The instruction to switch the processor to protected mode (LMSW) is 7 cycles faster on the 80C286.

Most of the 80286 protected mode access checking instructions operate as fast or faster on the 80C286 than on the 80386SX. The LAR instruction is one clock cycle faster on the 80C286 and the LSL instruction is 5 clock cycles faster. The VERW instruction executes in the same speed on both processors and the VERR is 5 cycles faster on the 80386SX. The ARPL instruction used in protected mode procedures for pointer validation is 10 clock cycles faster on the 80C286.

INSTRUCTION	ADVANTAGE		
	80C286	NONE	80386SX
Task Switching	X		
Segment Register Loading	X		
Inter-Segment Transfer	X		
System Register Instructions		X	
Inter-Segment Transfers	X		
Access Checking Instructions		X	

Subroutine Analysis

This section lists several subroutines and then compares the number of clock cycles each subroutine will take to execute on the 80C286 and on the 80386SX.

EXAMPLE 1

This interrupt routine outputs a character to a terminal via a UART. The AL register must contain the character to be output. The routine first checks the status of the UART to determine if it is busy. If it is busy, the routine loops until the UART is free; when the UART is free, the character is output. Following is a listing of the code and the clock clyde analysis for the OUT_CHAR routine.

This sample procedure executes about 25% faster on the 80C286 than on the 80386SX. The advantage is realized through the 80C286's faster interrupt handling and faster I/O instructions.

80C286 CLOCK CYCLES	80386SX CLOCK CYCLES	OUT_CHARACTER PROC NEAR		
3	4		PUSHF	; save caller's flags.
3	2		PUSH AX	; save data to be output.
5	12	CK_STATUS:	IN AL, PORT_STATUS	; Input UART status.
6	5		CMP AL, BUSY	; Check If UART Busy.
3/7	3/7		JE CK_STATUS	; If busy go check again.
5	4		POP AX	; If not busy restore AX
3	10		OUT OUT_PORT, AL	; and output data.
5	5		POPF	; Restore Flags
17	22		IRET	; Return.
23	37		INT x	; Instruction to initiate OUTCHAR
				; Interrupt.
73	104	Total cycles if UART not busy.		
18	24	Number of cycles added for each loop while UART is busy.		

EXAMPLE 1.

EXAMPLE 2

The second example outputs an entire string of characters using the previous interrupt routine (denoted by "INT x" in the code below). The DS:SI registers point to the beginning of the string to be output. The string is variable in length and must be terminated with the "$" character.

80C286 CLOCK CYCLES	80386SX CLOCK CYCLES	OUT_STRING PROC FAR		
17	18		PUSHA	; save caller's registers.
5	5	NEXT:	LODSB	; Load first char to be output.
3	2		CMP AL, "$"	; Check to see if End of string.
3/7	3/7		JE done	; If end then go to DONE.
73	104		INT x	; If not end output character.
7	7		JMP next	; Go get next char to output.
19	24	DONE:	POPA	; Restore Registers when done.
15	18		RET	; Far Return.
13	17		Call OUT_STRING	; Far Call to initiate.
				; OUT_STRING procedure.
79+91/char	91+121/char	Total number of clocks to start and end routine. +Number of additional clocks to output each character in the output string.		

EXAMPLE 2.

To output a string of 20 characters, the 80C286 would take 1,899 clock cycles; using the same routine, the 80386SX would take 2,511 cycles. Each time a string of 20 characters is output, the 80C286 will save 612 clock cycles; an 80C286 performance increase of almost 25%. The advantage is realized through the 80C286's faster interrupt handling, faster I/O instructions, faster FAR transfer instructions, and faster register saving and restoring instructions.

EXAMPLE 3

This example adds all the values of a source array in memory to the values of a destination array in memory. The result is stored in the destination array. Both arrays are assumed to be in the current data segment. The count (number of words in the array), offset of source array, and offset of destination array are all assumed to be placed on the stack (in that order) by the calling program. The source code for the procedure is listed below:

80C286 CLOCK CYCLES	80386SX CLOCK CYCLES	ADD_ARRAY PROC NEAR		
17	18		PUSHA	; save caller's registers.
2	2		MOV BP, SP	; Point BP to current stack
5	4		MOV CX, (bp+22)	; Load array size from stack
				; into CX.
5	4		MOV SI, (bp+20)	; Load offset of source array
				; from stack into SI.
5	4		MOV DI, (bp+18)	; Load offset of destination
				; array from stack into DI.
2	2		CLD	; Clear Direction Flag.
5	5	NEXT:	LODSW	; Load the source word into AX.
7	7		ADD (DI), AX	; Add source to destination.
3	2		ADD DI, 02	; Point DI to next data.
8/4	11		LOOP NEXT	; Continue to ADD all elements
				; in the two arrays.
19	24		POPA	; Restore Registers
11	10		RET 6	; Near return.
		; Following is the code necessary to set up and call the above procedure.		
5	5		PUSH count	; Put count parameter on stack
3	2		PUSH offset S_ARRAY	; Put offset of source array
				; on stack.
3	2		PUSH offset D_ARRAY	; Put offset of destination
				; array on stack.
7	7		CALL ADD_ARRAY	; Near Call to initiate
				; ADD_Array procedure.
84+(23*CX)-4	84+(25*CX)	Total number of clocks to start and end routine. +Number of additional clocks for each item in array to be added.		

EXAMPLE 3.

Both processors take the same number of clock cycles for initialization before the call and closing up after the call (84). The loop that does the adding is faster on the 80C286. To add two 100 word arrays, the 80C286 would take 2,380 clock cycles; the 80386SX takes 2,584 (an additional 204 clocks) to execute the same routine. In this example, the LOOP instruction gives the 80C286 the performance advantage over the 80386SX.

EXAMPLE 4

This procedure is an example of an operating system procedure developed for a protected mode multi-privilege level system. The procedure INIT_SEGMENT is passed a segment selector on the stack and will load that entire segment with zero's. The procedure is designed to execute at privilege level zero with a call gate at privilege level 3; this allows procedures executing at any level to utilize the INIT_SEGMENT procedure. INIT_SEGMENT provides protection checks to ensure that the procedure passing the parameter has valid access to the segment that it is trying to initialize. This prevents a procedure at privilege level three from initializing a segment at privilege level zero.

80C286 CLOCK CYCLES	80386SX CLOCK CYCLES	INIT_SEGMENT PROC FAR WC = 1		
17	18		PUSHA	; save caller's registers.
3	2		PUSH ES	; save ES register.
2	2		MOV BP, SP	; Point BP to top of stack.
5	4		MOV AX, (BP+22)	; Load AX with segment selector
				; passed as parameter on stack.
5	4		MOV BX, (BP+20)	; Load BX with return CS to
				; determine caller's CPL.
10	20		ARPL AX, BX	; Adjust the Privilege level of
				; the segment selector according
				; to the caller's CPL.
16	16		VERW AX	; Test for valid write access
3/7	3/7		JNE ERROR	; If no valid access go to error.
17	18		MOV ES, AX	; LOAD ES with segment to be
				; initialized.
14	20		LSL CX, AX	; Load segment size into CX.
2	2		XOR DI, DI	; Load zero into DI.
2	2		XOR AX, AX	; Load zero into AX.
2	2		CLD	; Clear decrement flag.
4+3*cx	5+5*cx		REP STOSB	; Init entire segment to 00.
2	2		CLC	; Clear carry to indicate segment
				; initialized with no errors.
20	21	DONE:	POP ES	; Restore ES register.
19	24		POPA	; Restore Register
55	72		RET 2	; Ret FAR to different privilege
2	2	ERROR:	STC	; SET carry to indicate error.
7	7		JMP DONE	
		; Code to push selector on stack and initiate INIT SEGMENT via call gate.		
3	2		PUSH DATA_SELECTOR	; Place Selector on stack.
82	98		CALL INIT_SEGMENT_GATE	; Instruction to initiate
				; INIT SEGMENT procedure.
253	299	Total clocks if ERROR because segment not accessible.		
283+(3*S)	377+(5*S)	Total number of clocks if segment is initialized to zeros. "S" represents size of segment in bytes.		

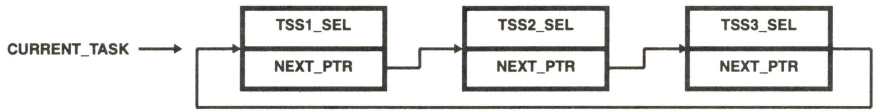
EXAMPLE 4.

This example shows that when executing instructions used for privilege verification and privilege level transitions the 80C286 is faster than the 80386SX. Without taking the LODS instruction into account, the 80C286 is 54 clock cycles faster when executing the same procedure. With the LODS instruction, and assuming a segment size of 100 bytes, the 80C286 would execute this routine 254 clock cycles faster than the 80386SX.

EXAMPLE 5

This Procedure is a task dispatcher that is invoked via an interrupt to cause a task switch to occur. This procedure utilizes a circular linked list of the tasks that need to be executed. A pointer called "CURRENT_TASK" points to the data structure for the current task being executed. The data structure contains the TSS for the task it is describing and a NEXT field that points to the data structure of the next task in the list to be executed. When the Task Dispatcher is invoked it switches the current pointer to the next task in the list and then invokes the new task by jumping to the TSS for that task. The data structure for the linked list is illustrated below.

The task dispatcher is actually a separate task that is invoked via an interrupt that signals that a new task should be initiated. Following is a listing for the simple task dispatcher.



80C286 CLOCK CYCLES	80386SX CLOCK CYCLES	TASK_DISPATCH PROC FAR		
5	4	START:	MOV BX, CURRENT TASK + 2	; Load BX with contents of next
				; field of current TASK. BX will
				; contain the address of the data
				; structure for next task to run
3	2		MOV CURRENT TASK, BX	; Update Current Task to point to
				; new task to be executed.
178	294		JMP DWORD PTR (BX-2)	; Start new task by jumping to TSS
7	7		JMP START	; JUMP to start for next time the
				; TASK dispatcher is invoked.
193	307			

EXAMPLE 5.

The advantage of the 80C286 in this case is in the faster task switch instruction. The task switch instruction is 116 clock cycles faster on the 80C286 than on the 80386SX. This performance increase makes the 80C286 the clear choice for multi-tasking applications.

Appendix

This appendix contains a table directly comparing the number of clock cycles necessary to execute all the instructions available on both the 80C286 and the 80386SX. The table includes several addressing modes of each instruction.

The table has five columns. The first column list the instruction being compared. The second column lists the number of clock cycles that the 80C286 needs to execute that instruction. The third column lists the number of clock cycles needed by the 80386SX to execute the same instruction. The fourth column divides the number of cycles needed by the 80386SX by the number of cycles needed by the 80C286. If this figure is greater than one, (see fifth column) then the 80C286 is faster than the 80386SX. For example, a 2.0 would indicate the 80C286 executes the same instruction twice as fast as the 80386SX. A 1.0 indicates that both processors execute the instruction in the same number of cycles. A number less than one indicates the 80386SX is faster than the 80C286.

APPENDIX TABLE

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386SX	80386SX/ 80C286	80C286-16 FASTER THAN OR EQUAL TO 80386SX-16
AAA	3	4	1.33	√
AAD	14	19	1.36	√
AAM	16	17	1.06	√
AAS	3	4	1.33	√
ADC reg, reg	2	2	1.00	√
ADC mem, reg	7	7	1.00	√
ADC reg, immed	3	2	0.67	
ADC mem, immed	7	7	1.00	√
ADD reg, reg	2	2	1.00	√
ADD mem, reg	7	7	1.00	√
ADD reg, immed	3	2	0.67	
ADD mem, immed	7	7	1.00	√
AND reg, reg	2	2	1.00	√
AND mem, reg	7	7	1.00	√
AND reg, immed	3	2	0.67	
AND mem, immed	7	7	1.00	√
ARPL reg, reg	10	20	2.00	√
ARPL mem, reg	11	21	1.91	√
BOUND (no interrupt)	13	10	0.77	
CALL immed (near)	7	7	1.00	√
CALL immed (far real mode)	13	17	1.31	√
CALL immed (far PVAM)	26	42	1.61	√
CALL gate (same privilege PVAM)	41	64	1.56	√
CALL gate (different privilege PVAM)	82	98	1.19	√
CALL TSS (Task Switch PVAM)	177	285	1.61	√
CALL task_gate (Task Switch PVAM)	182	297	1.63	√
CBW	2	3	1.50	√
CLC	2	2	1.00	√
CLD	2	2	1.00	√
CLI	3	8	2.67	√
CLTS	2	5	2.50	√
CMC	2	2	1.00	√
CMP reg, reg	2	2	1.00	√
CMP mem, reg	6	5	0.83	

APPENDIX TABLE (Continued)

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386SX	80386SX/ 80C286	80C286-16 FASTER THAN OR EQUAL TO 80386SX-16
CMP reg, immed	3	2	0.67	
CMP mem, immed	6	5	0.83	
CMPS	8	10	1.25	√
CWD	2	2	1.00	√
DAA	3	4	1.33	√
DAS	3	4	1.33	√
DEC reg	2	2	1.00	√
DEC mem	7	6	0.86	
DIV word, reg	22	22	1.00	√
DIV word, mem	25	25	1.00	√
ENTER immed1, immed2 (immed 2 = 6)	36	57	1.58	√
HLT	2	5	2.50	√
IDIV word, reg	25	27	1.08	√
IMUL word, mem	24	19	0.79	
IN	5	12	2.40	√
INC reg	2	2	1.00	√
INC mem	7	6	0.86	
INS	5	15	3.00	√
INT 3 (real mode)	23	33	1.43	√
INT immed (real mode)	23	37	1.61	√
INT immed (PVAM same privilege)	40	71	1.77	√
INT immed (PVAM different privilege)	78	111	1.42	√
INT TASK_GATE (PVAM Task Switch)	167	438	2.62	√
INTO (No Jump)	3	3	1.00	√
INTO (YES Jump real mode)	24	35	1.46	√
IRET (real mode)	17	24	1.41	√
IRET (PVAM same privilege)	31	42	1.35	√
IRET (PVAM different privilege)	55	86	1.56	√
IRET (PVAM task switch)	169	285	1.68	√
Jcond label (No jump)	3	3	1.00	√
Jcond label (Yes jump)	7	7	1.00	√
JMP near_label	7	7	1.00	√
JMP Far_label (real mode)	11	12	1.09	√
JMP FAR_LABEL (PVAM)	23	31	1.34	√
JMP CALL_GATE (PVAM same privilege)	38	53	1.35	√
JMP TASK_GATE (PVAM task switch)	183	298	1.63	√
JMP TSS (PVAM task switch)	178	289	1.62	√
LAHF	2	2	1.00	√
LAR reg	14	15	1.07	√
LAR mem	16	16	1.00	√
LDS (real mode)	7	7	1.00	√
LDS (PVAM)	21	23	1.33	√
LEA	3	2	0.67	
LEAVE	5	4	0.80	

APPENDIX TABLE (Continued)

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386SX	80386SX/ 80C286	80C286-16 FASTER THAN OR EQUAL TO 80386SX-16
LGDT	11	11	1.00	√
LIDT	12	11	0.92	
LLDT reg	17	20	1.18	√
LLDT mem	19	24	1.26	√
LMSW reg	3	10	3.33	√
LMSW mem	6	13	2.17	√
LODS	5	5	1.00	√
LOOP (Jump)	8	11	1.38	√
LOOP (No Jump)	4	11	2.75	√
LSL reg	14	20	1.43	√
LSL mem	16	21	1.31	√
LTR reg	17	23	1.35	√
LTR mem	19	27	1.42	√
MOV reg, reg	2	2	1.00	√
MOV mem, reg	3	2	0.67	
MOV reg, immed	2	2	1.00	√
MOV mem, immed	3	2	0.67	
MOV seg_reg, reg (real mode)	2	2	1.00	√
MOV seg_reg, mem (real mode)	5	5	1.00	√
MOV seg_reg, reg (PVAM)	17	22	1.29	√
MOV seg_reg, mem (PVAM)	19	23	1.21	√
MOVS	5	7	1.40	√
MUL reg	21	15	0.71	
NEG reg	2	2	1.00	√
NEG mem	7	6	0.86	
NOP	3	3	1.00	√
NOT reg	2	2	1.00	√
NOT mem	7	6	0.86	
OR reg, reg	2	2	1.00	√
OR mem, reg	7	6	0.86	
OR reg, immed	3	2	0.67	
OR mem, immed	7	7	1.00	√
OUT	3	10	3.33	√
OUTS	5	14	2.80	√
POP reg	5	5	1.00	√
POP mem	5	7	1.40	√
POP seg_reg (real mode)	5	7	1.40	√
POP seg_reg (PVAM)	20	25	1.25	√
POPA	19	24	1.26	√
POPF	5	5	1.00	√
PUSH reg	3	2	0.67	
PUSH mem	5	7	1.40	√
PUSH seg_reg	3	2	0.67	
PUSHA	17	18	1.06	√

APPENDIX TABLE (Continued)

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386SX	80386SX/ 80C286	80C286-16 FASTER THAN OR EQUAL TO 80386SX-16
PUSHF	3	4	1.33	√
RCR or RCL reg, 1	2	9	4.50	√
RCR or RCL mem, 1	7	10	1.43	√
RCR or RCL reg, cl (cl = 4)	9	9	1.00	√
RCR or RCL mem, cl (cl = 4)	12	10	0.83	
RCR or RCL reg, 4	9	9	1.00	√
RCR or RCL mem, 4	12	10	0.83	
ROR or ROL reg, 1	2	3	1.50	√
ROR or ROL mem, 1	7	7	1.00	√
REP INS (cx = 100)	405	613	1.51	√
REP MOVS (cx = 100)	405	407	1.00	√
REP OUTS (cx = 100)	405	512	1.26	√
REP STOS (cx = 100)	304	505	1.66	√
REP CMPS (cx = 100)	905	905	1.00	√
REPE CMPS (N = 100)	905	905	1.00	√
REPE SCAS (N = 100)	805	805	1.00	√
RET (near)	11	12	1.09	√
RET (far real mode)	15	20	1.33	√
RET (far PVAM same privilege)	25	36	1.44	√
RET (far PVAM different privilege)	55	72	1.31	√
SAHF	2	3	1.50	√
SHIFT reg, 1 (SHIFT = SAL, SAR, SHR)	2	3	1.50	√
SHIFT mem, 1	7	7	1.00	√
SBB reg, reg	2	2	1.00	√
SBB mem, reg	7	6	0.86	
SBB reg, immed	3	2	0.67	
SBB mem, immed	7	7	1.00	√
SCAS	7	7	1.00	√
SGDT	11	9	0.82	
SIDT	12	9	0.75	
SLDT reg	2	2	1.00	√
SLDT mem	3	2	0.67	
SMSW reg	2	2	1.00	√
SMSW mem	3	2	0.67	
STC	2	2	1.00	√
STD	2	2	1.00	√
STI	2	3	1.50	√
STOS	3	4	1.33	√
STR reg	2	22	1.00	√
STR mem	3	2	0.67	
SUB reg, reg	2	2	1.00	√
SUB mem, reg	7	7	1.00	√
SUB reg, immed	3	2	0.67	
SUB mem, immed	7	7	1.00	√

APPENDIX TABLE (Continued)

80C286 INSTRUCTION	NUMBER CLOCKS TO EXECUTE ON 80C286	NUMBER CLOCKS TO EXECUTE ON 80386SX	80386SX/ 80C286	80C286-16 FASTER THAN OR EQUAL TO 80386SX-16
TEST reg, reg	2	2	1.00	√
TEST mem, reg	6	5	0.83	
TEST reg, immed	3	2	0.67	
TEST mem, immed	6	5	0.83	
VERR reg	14	10	0.71	
VERR mem	16	11	0.69	
VERW reg	14	15	1.07	√
VERW mem	16	16	1.00	√
WAIT	3	6	2.00	√
XCHG reg, reg	3	3	1.00	√
XCHG reg, mem	5	5	1.00	√
XLAT	5	5	1.00	√
XOR reg, reg	2	2	1.00	√
XOR mem, reg	7	6	0.86	
XOR reg, immed	3	2	0.67	
XOR mem, immed	7	7	1.00	√
TOTAL number clocks to execute all instructions	6894	8664		
AVERAGE			1.25	
Number of Instructions faster on 80C286		79		
Number of Instructions equal on both processors		64		
Number of Instructions faster on 80386		39		
Total Number of instructions analyzed		182		

Harris Semiconductor

APPNOTE

No. AN400.1 March 1997

Harris Digital

Using the HS-3282 ARINC Bus Interface Circuit

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Introduction

The Harris HS-3282 is a high performance CMOS programmable bus interface circuit that was designed to meet the requirements of ARINC Specification 429, and similarly encoded, time multiplexed serial data protocols. Its simple but efficient design allows the HS-3282 to be used without major complications in a variety of applications. By setting an internal control register, the HS-3282 can be programmed to operate at different data rates and with different word lengths, and to transmit either even or odd parity. The device can also be programmed to operate with or without a unique address (SDI — source/destination identifier), and with or without its self test mode implemented. Although the HS-3282 was designed to transmit and receive high-speed data rates (100K BPS or 12.5K BPS), standard baud rates of 9600 or 1200 BPS can be implemented by reducing the input clock frequency. The timing requirements of the HS-3282 make it compatible with 8086 microprocessor or other similarly based systems operating at 5MHz or less. Designed to meet the critical needs of today's advanced aircraft, the HS-3282 is a cornerstone of reliability for systems that cannot tolerate a wide margin of error.

Functional Operation of the HS-3282

In order to clarify and expand on the basic details given in the data sheet, the following information has been provided to point out some of the particularities of the HS-3282.

Clock Frequencies

The two receiver output signals, $\overline{D/R1}$ and $\overline{D/R2}$, have a minimum pulse width of one clock period. Because of this, when using a slower clock rate than 1MHz to drive the HS-3282, these outputs may remain in a low state for a few microseconds after the data in the receivers is fetched. This could cause the same data to be fetched more than once if these outputs are used to drive state sensitive interrupt requests; therefore, it is necessary to use edge sensitive interrupt requests, as mentioned in the typical application of the HS-3282 below.

Bi-Directional Data Bus

Data transfer to and from the host is accomplished via a 16-bit bidirectional, three-stated bus. The control of this bus is completely internal to the HS-3282. When data is written to the transmitter or the control word register, the bus is automatically enabled as an input; when data is read from the receivers, the bus is automatically enabled as an output; at all other times, the bus is in a high impedance state and will not interfere with external operations.

Setting Up the Control Word Register

When a low to high transition occurs on the $\overline{CWSTR}$ pin, the data on the eleven most significant bits of the bidirectional bus is latched into the control word register. The location and function of each of these bits is shown in the data sheet.

Receiver Operation

Incoming data from the line receiver (or from the self test circuit) is shifted into the data shift register by the word gap timer on an edge sensitive basis. This results in a high data rate tolerance; although ARINC specification 429 requires at least a ±1% tolerance, the HS-3282 has at least a ±10% tolerance at all data rates. In order to prevent reception errors, the word gap timer is designed to disable and reset the receiver upon reception of two consecutive null times (or two consecutive data times), and re-enable the receiver after four additional null times. If a word of the proper length (and SDI) has been received by this time, the word will be latched and the $\overline{D/R}$ flag of the corresponding receiver will go low to signal the host that a valid word is ready to be fetched. (For the most efficient operation, the $\overline{D/R}$ flags should be used to generate interrupt requests to the host system.) It should be noted that the parity bit that is stored in the receiver latch may be different than the parity bit of the word that was received. This is because the parity bit that is stored in the receiver latch is actually a parity flag, indicating by its status the parity of the word that was received: if the parity of the word received was odd, the parity flag will be a logic "0"; if the parity of the word received was even, the parity flag will be a logic "1".

Once a word is ready to be fetched, it may be read by the host system in two 16-bit parts over the bi-directional bus by strobing the appropriate $\overline{EN}$ line low twice, once with the SEL line low to read "word 1" and once with the SEL line high to read "word 2". (If preferred, "word 2" may be read before "word 1", or the $\overline{EN}$ line may be held low for one long pulse while the SEL input is toggled to select first one word and then the other.) The actual ARINC contents of these two 16-bit "words" (or the contents of the 25-bit word length) is shown in the data sheet. It should be noted that the $\overline{D/R}$ flag will not be reset unless both words are read.

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Transmitter Operation

As mentioned in the data sheet, the transmitter has a FIFO that can hold up to eight data words. Although the HS-3282 has two inputs, $\overline{PL1}$ and $\overline{PL2}$, used to write data into the FIFO, the data is not actually entered into the FIFO until the second input ($\overline{PL2}$) is pulsed low. Therefore, the first half of each data word must be written to the HS-3282 first. Then, when the $\overline{PL2}$ input is pulsed low to write the second half of the word, the proper data will be transferred into the FIFO.

The HS-3282 transmitter is designed to transmit data in sets containing from one to eight 32 or 25-bit words. It is of primary importance that the transmitter FIFO not be disturbed while this transmission is taking place; therefore, systems should be designed to disallow writing to the FIFO while transmission is taking place. The only exception to this rule is that words can be written into the FIFO while the first word (only) is being transmitted; if transmission of a second word is started before the TX/R has returned to a high state, the FIFO must remain undisturbed until the entire transmission sequence is completed and the TX/R flag goes high. The TX/R flag becomes useful here as an interrupt request output to the host system, signaling that the FIFO is ready for another set of data words.

It is also of primary importance that the ENTX input remain high for the duration of the transmission sequence or the integrity of the data in the FIFO will be broken. This can best be accomplished by feeding the TX/R flag through an inverter and back into the ENTX input. This application will enable the transmitter as soon as the first word is written into the FIFO, and keep it enabled until the transmission sequence is completed; since most host systems operate at much greater speeds than the transmitter, an additional seven words could easily be written into the FIFO while the first word is still being transmitted.

The value of the parity bit as written into the FIFO makes no difference since the transmitter sets the parity bit at transmission time according to the type of parity that it has been programmed to transmit.

Lightning Protection

Although the bus driver has been protected by a 100mW fuse capable of sinking up to 1A for short periods of time (100ms) and internal zener diodes which saturate at about 8.7V, the bus interface circuit has no such protection for its receiver inputs. Because of the possibility of a lighting strike to aircraft, additional protection should be used to protect both the HS-3282 and the bus driver from high voltage spikes. External avalanche diodes with high power ratings (five or ten watts) should be used to clamp the bus at about ±6.8V. This will prevent the fuse and the zeners in the driver from being burned out by current surges, and it will keep the voltage level on the inputs of the receiver within acceptable limits.

A Typical Application of the HS-3282

The following example shows one possible way to interface the HS-3282 with a host system. Although different applications may require different approaches, most systems will have requirements similar to those that have been met here.

Logical Control

As shown in Figure 1, the support circuitry necessary to integrate the HS-3282 into a system primarily involves a logic circuit to drive the control inputs. In most cases, this can be achieved using microprocessor $\overline{RD}$ and $\overline{WR}$ bus control signals and two address lines in conjunction with a decoded chip select line and a DEN (data enable) line. During READ operations, the particular function ($\overline{EN1}$ or $\overline{EN2}$) is selected when the proper address is present while the $\overline{RD}$ line is low; note that the second LSB of the address bus is used to select either word 1 or word 2. The DEN line is used to signal the BIU to place its data on the bus.

Therefore, for read operations, the only timing requirement the host system must meet is a minimum DEN pulse of 200ns plus the propagation delay of the enable gates. During write operations, the $\overline{WR}$ line is inverted and used instead of the DEN line to enable the particular function ($\overline{CWSTR}$, $\overline{PL1}$, or $\overline{PL2}$) previously selected by the address bus. Since the minimum data hold time of the HS-3282 is 0ns, the timing requirement for write operations, besides the minimum 200ns $\overline{WR}$ pulse, is a minimum data disenable delay equal to the total propagation delay caused by the function enable gates.

Address Decoding

In the system shown, the transmitter FIFO is decoded as addresses F8 (first word) and FA (second word), and the control word register is at FC; writing to these addresses will load the corresponding registers of the HS-3282. Receiver latch #1 is at addresses F8 (first word) and FA (second word), and Receiver latch #2 is at addresses FC (first word) and FE (second word); reading these addresses will load the data from the corresponding receiver latch of the HS-3282. Note that an address line can be connected directly to the SEL input of the HS-3282 to perform the receiver latch word select function. Since it is impossible to write to the receiver latches or to read the transmitter FIFO and the control word register, the addresses of the read functions can overlap the addresses of the write functions without presenting a problem. See Table 1.

TABLE 1. TYPICAL HS-3282 FUNCTIONAL DECODING

		ADDRESS			
$\overline{RD}$	$\overline{WR}$	F8	FA	FC	FE
1	0	$\overline{PL1}$	$\overline{PL2}$	CWSTR	CWSTR
0	1	$\overline{EN1}$ (1st Word)	$\overline{EN1}$ (2nd Word)	EN2 (1st Word)	EN2 (2nd Word)

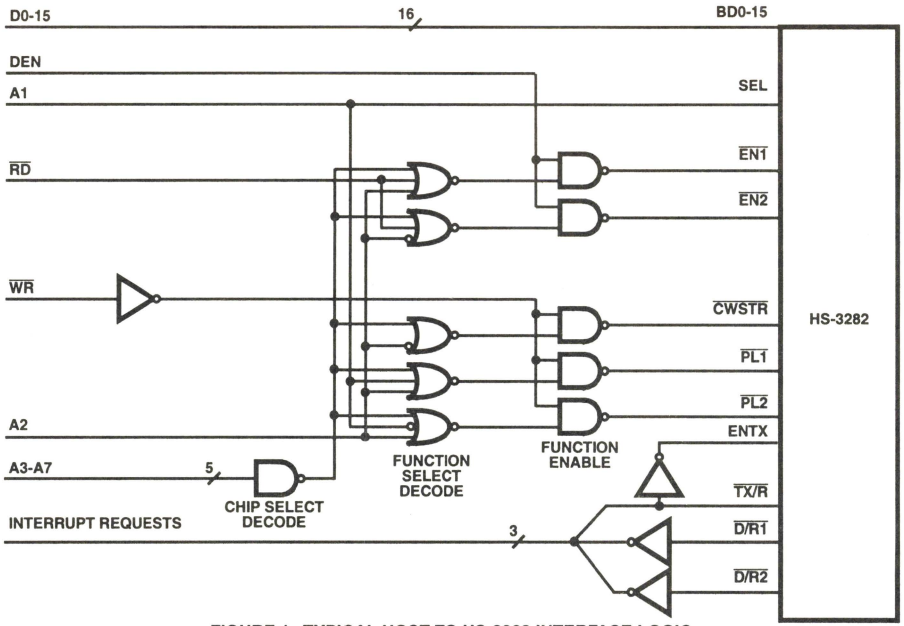


FIGURE 1. TYPICAL HOST TO HS-3282 INTERFACE LOGIC

Interrupts

For the most efficient operation, any system incorporating the HS-3282 should provide conditions by which the device can generate interrupt requests to the host system. If both receivers are being used, then a minimum of three interrupt vectors are needed: one (TX/R) to signal the end of a data set transmission, and one for each of the receivers ($\overline{D/R}$) to signal the presence of a valid word ready to be fetched. Since the TX/R signal can remain high for indeterminate periods of time while the transmitter is inactive, the requests should be received by the host on an edge sensitive basis.

Software Requirements

A flowchart of a simple algorithm that the host system could use to exercise and monitor the functions of the HS-3282 is shown in Figure 2. In order to begin, the HS-3282 must be initialized with a control word, then the host should set some flag in system memory to indicate that the transmitter is available. If data is ready to be transmitted, the host should store the data in a temporary buffer until the transmitter becomes available. At this time, the data is taken from the buffer and loaded into the transmitter FIFO (eight 32-bit words maximum). After loading the FIFO, the host should reset the flag in system memory mentioned previously to indicate that the transmitter is no longer available. Unless an interrupt is received by this time, the host can move on to other tasks or continue storing data in the temporary buffer (as shown by the broken arrow). If a $\overline{D/R}$ interrupt is received, data can be read from the receiver latch and any corresponding action taken. If a TX/R interrupt is received, the transmitter available flag should be set once again, and any ready data in the buffer could be written into the FIFO.

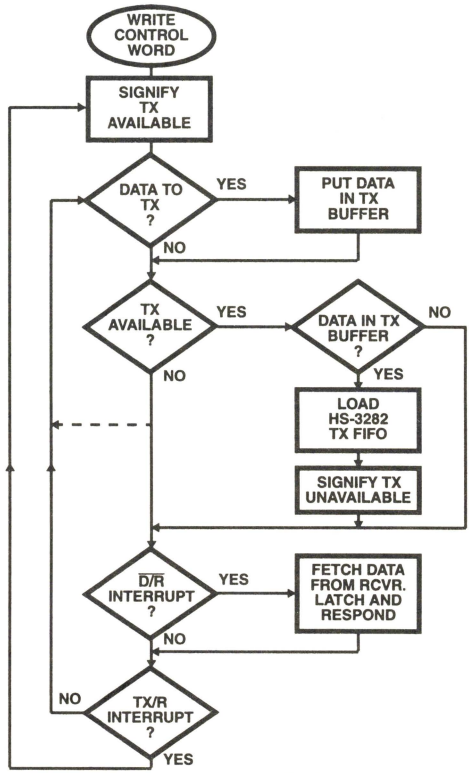


FIGURE 2. SIMPLE HS-3282 DRIVER ALGORITHM

Adapting the HS-3282 to an 8-Bit Data Bus

Although designed for a 16-bit data bus, the HS-3282 can be used in systems with an 8-bit data bus by adding a few external components. The following example shows how this can be done.

Logical Control

Figure 3 shows the circuitry necessary to integrate the HS-3282 into a system that utilizes an 8-bit data bus. The circuit is very similar to the one in Figure 1, the primary difference being the addition of the logic circuitry necessary to drive two input/output latches. The primary purpose of this additional circuitry is to latch the high order byte of data so that the host system can accomplish each 16-bit data transfer with the HS-3282 by using two separate 8-bit operations. Each of the two latches serves a specific purpose: the output latch provides the HS-3282 with the high order byte during write operations ($\overline{PL1}$, $\overline{PL2}$, and $\overline{CWSTR}$), and the input latch receives the high order byte during read operations ($\overline{EN1}$ and $\overline{EN2}$). The outputs on these latches should be three-stated to avoid bus contention. The least significant bit of the address bus is used to activate the latches onto the host system data bus whenever the host system is performing high order byte operations, and this same address bit is inverted and added as an input to each of the function enable gates to prevent the HS-3282 from being activated at the same time. During low order byte operations, the outputs of the function enable gates are used to activate the latches onto the high order byte of the bidirectional bus of the HS-3282, allowing the BIU to instantaneously transfer a full 16-bit word. Since the latches are automatically activated in unison with the BIU during low order byte operations, the high order byte must be handled first during write operations so that the proper data will be present in the output latch when the lower byte is written to the BIU. Conversely, the low order byte must be handled first during read operations since the high order byte is automatically strobed into the input latch when the low order byte is read. Timing requirements are increased by the additional logic gates; read operations now require a minimum DEN pulse equal to 200ns plus the propagation delays of two logic gates, a one-shot, and the input latch; write operations now require a minimum delay from address valid to $\overline{WR}$ enable equal to the propagation delays of two gates and a minimum $\overline{WR}$ pulse of 200ns plus the propagation delays of two gates and the output latch.

Note that one shots are used to drive the strobes on the latches. This is necessary so that the falling edge of the strobe occurs while the data is still active on the bus; otherwise, the propagation delays of the additional gates would cause the latches to close after the data had been disenabled.

Address Decoding

The system in Figure 3 will have the same functional addresses as the system in Figure 1 except that in this case each particular byte of each register has its own address. Therefore, the FIFO is still located at addresses F8 (first word, low byte) and FA (second word, low byte); however, the high bytes must be addressed as F9 (first word) and FB (second word). The receivers are addressed in the same way as shown in Table 2.

TABLE 2. TYPICAL HS-3282 FUNCTIONAL DECODING USING AN 8-BIT DATA BUS

$\overline{RD}$	$\overline{WR}$	ADDRESS							
		F8	F9	FA	FB	FC	FD	FE	FF
1	0	$\overline{PL1}$ Low Byte	$\overline{PL1}$ High Byte	$\overline{PL2}$ Low Byte	$\overline{PL2}$ High Byte	$\overline{CWSTR}$ Low Byte	$\overline{CWSTR}$ High Byte	$\overline{CWSTR}$ Low Byte	$\overline{CWSTR}$ High Byte
0	1	$\overline{EN1}$ Low Byte 1st Word	$\overline{EN1}$ High Byte 1st Word	$\overline{EN1}$ Low Byte 2nd Word	$\overline{EN1}$ High Byte 2nd Word	$\overline{EN2}$ Low Byte 1st Word	$\overline{EN2}$ High Byte 1st Word	$\overline{EN2}$ Low Byte 2nd Word	$\overline{EN2}$ High Byte 2nd Word

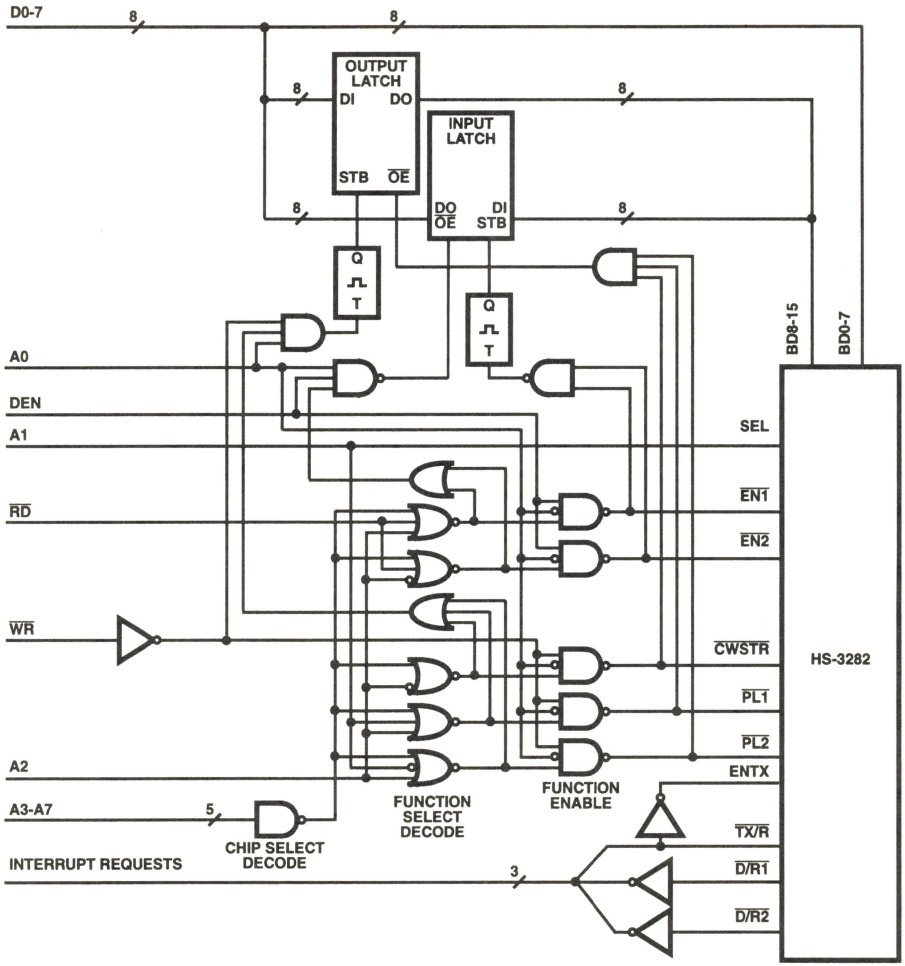


FIGURE 3. TYPICAL HOST TO HS-3282 INTERFACE LOGIC USING AN 8-BIT DATA BUS

Conclusion

Although it was designed for ARINC applications, the HS-3282 bus interface circuit is a very versatile device, capable of serving any type of communications purpose. Its high speed capability and its high reliability make it especially useful in scientific and real time operations where large volume data gathering and time critical transmission of control signals is required. These qualities, in combination with the simplicity with which the device may be incorporated into a system, make the HS-3282 a wise choice for a wide spectrum of applications.

ARINC Specification 429 A Brief Overview

ARINC Specification 429, otherwise known as the Mark 33 Digital Information Transfer System (DITS), is a definition of standards used extensively by the air transport industry for the transfer of digital data between avionics systems elements. Systems utilizing this standard have been installed in a wide range of aircraft including the Boeing 737, 747, 757, and 767; the European Airbus; Bell Helicopter; and a large number of small aircraft. Replacing the earlier ARINC Specification 419 which had standardized the various forms of serial transmission developed during the emergent period of digital avionics technology, Specification 429 eliminates much of the previous confusion by defining the standard for a single form of serial transmission.

According to Specification 429, digital data is transmitted via a differential signal over a uni-directional bus composed of two twisted and shielded wires. The data is sent in 32-bit words, each word containing a parity bit and an eight-bit label that defines the flight function to which the remaining data pertains. This data, encoded in either numeric (binary or BCD) or alphabetic (ISO No. 5) format, is further divided into various fields according to label type. In order to completely standardize communication and prevent conflicts, all flight functions have been assigned a particular label and data format.

The ARINC Specification 429, by defining a single standard for the transfer of digital information, eliminates the need for complex interfaces between avionics systems produced by different manufacturers. This provides those avionics components that conform to this standard with a virtual "plug-in" capability, and gives such components a certain measure of universality. For more information about this specification, contact Aeronautical Radio, Inc., 2551 Riva Road, Annapolis, Maryland 21401.

Harris Semiconductor

APPNOTE

No. AN6565.1 March 1997

Harris Microprocessor

Design of Clock Generators for Use with COSMAC Microprocessor CDP1802

Author: D. Hillman

Introduction

Clock signal generation for the CDP1802 COSMAC Microprocessor is simple and straightforward. The CDP1802 features of static operation, single-phase clock input, and the on-chip oscillator amplifier make practical the use of a low-cost, highly stable, crystal-controlled oscillator as its clock generator. The design of external oscillators for this purpose, crystal or RC controlled, is equally straightforward and they require only minimal circuitry. In addition to the oscillator amplifier, the CDP1802 incorporates all necessary start/stop logic on-chip. This application note describes clock generator designs suitable for various applications.

Crystal Oscillator Design

The basic oscillator circuit for the CDP1802 consists of the on-chip amplifier and an external feedback network as illustrated in Figure 1. For oscillation to occur, the gain of the amplifier (α) times the attenuation (β) of the feedback network must be greater than or equal to one. In addition, the total phase shift through the amplifier and feedback network must be equal to N times 360 degrees, where N is an integer. Oscillations occur in any system in which the amplified signal is returned in phase to the amplifier after being attuned less than it was originally amplified.

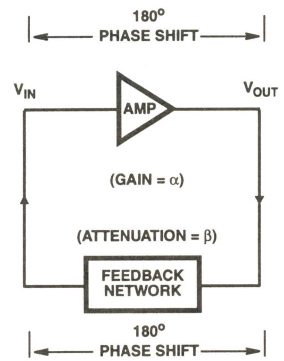


FIGURE 1. BASIC OSCILLATOR CIRCUIT

The frequency stability of an oscillator is primarily dependent upon the phase-changing properties of the feedback network. Because of their high Q and inherent frequency stability, quartz crystals are commonly used in the feedback network.

A parallel resonant oscillator circuit is shown in Figure 2. The phase angle for the type of feedback network shown in this figure is extremely sensitive to a change in frequency, a condition necessary for stable oscillation. If the equivalent resistance of the crystal is in fact zero (infinite Q), a change in phase angle of the feedback circuit would not cause any change in oscillator frequency. Therefore, for an oscillator of highest stability, the Q of the crystal should be as high as possible. In general, Q increases with increasing frequency.

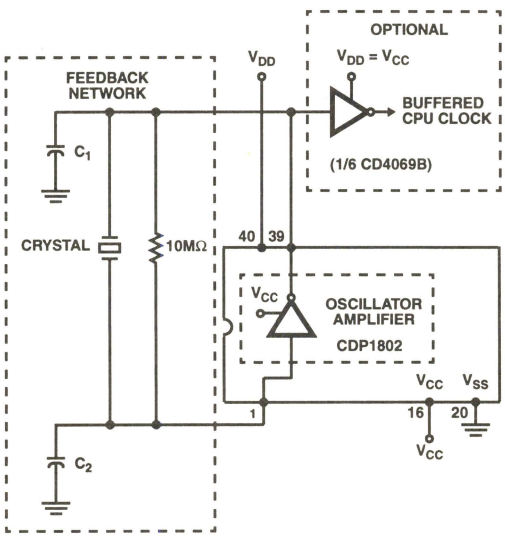


FIGURE 2. PARALLEL RESONANT OSCILLATOR CIRCUIT

The crystal load capacitance, C_L, is defined as the series sum of C_1 and C_2. Higher values of crystal load capacitance generally improve frequency stability, but also increase power consumption. The choice of equivalent load capacitance (usually specified to the crystal suppliers) only fixes

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the series sum of the two capacitors C_1 and C_2. The value of the amplifier output capacitance C_1 should not be fixed. A trimmer should be connected in parallel with, or used in place of, a fixed output capacitor to permit compensation for variation in stray capacitance and circuit component values.

The required capacitance range for the oscillator trimmer capacitor is determined by the variation in oscillation frequency with load capacitance. The total trimming range is mainly a function of the crystal characteristics. For a more detailed analysis, see Reference 4.

Practical Oscillator Circuits

The amplifier, feedback network, and crystal considerations discussed in the preceding paragraphs can be combined for the design of a crystal-controlled oscillator for the CDP1802. The majority of microprocessor applications do not require the frequency of oscillation to be so exact as to require oscillator trimming. An "untrimmed" crystal oscillator will be within 1% of its specified crystal frequency. For most microprocessor applications the following simple guidelines can be used.

1. The crystal should be connected between terminals 1 and 39 of the CDP1802.
2. For crystal frequencies between 100KHz and 6.4MHz, a 10MΩ to 22MΩ feedback resistor should be used in parallel with the crystal.
3. Capacitors C_1 and C_2 are not required but a value of between 20pF and 30pF for each is recommended to improve stability.

It should be noted that the on-chip oscillator and timing generator are capable of operating at frequencies higher than the microprocessor maximum operating frequency. For reliable operation, the crystal frequency must always be less than or equal to the maximum operating frequency specified in the CDP1802 data sheet.

A practical example, the CDP18S020 Evaluation Kit oscillator, consists of a 10MΩ feedback resistor and a 2MHz AT cut crystal, both connected in parallel across terminals 1 and 39 of the CDP1802. (Crystal: Part No. X023303; C_L=15pF; Series M1; holder, series HC330; made by Turotel, Inc., 13402 S. 71 Highway, Grandview, Missouri 68030.) Provisions for oscillator capacitors are made in the Evaluation Kit, but their use is not required. The increase in oscillator stability with respect to supply voltage that can be obtained by adding the capacitors is shown in Figure 3.

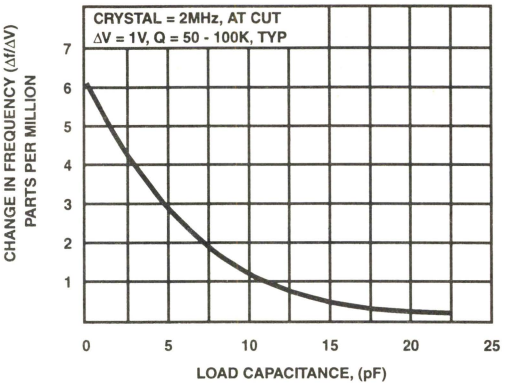


FIGURE 3. STABILITY OF CDP1802 CRYSTAL OSCILLATOR AS A FUNCTION OF LOAD CAPACITANCE VALUE

The amplifier stability also depends upon the value of the resistor in the feedback network. Figure 4 shows the relationship between the feedback resistor value and oscillator stability. The curve indicates that 10MΩ is an adequate value for the feedback resistor.

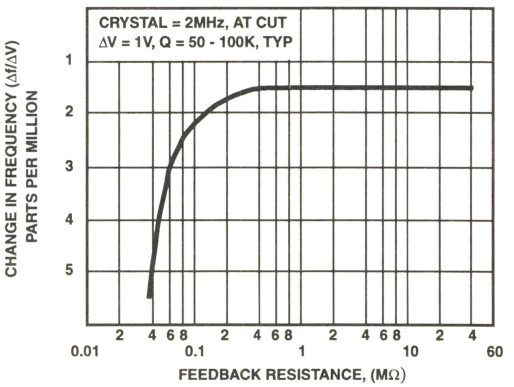
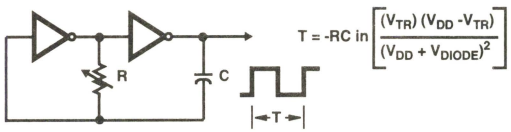


FIGURE 4. STABILITY OF CDP1802 CRYSTAL OSCILLATOR AS A FUNCTION OF FEEDBACK RESISTANCE VALUE

External Clock Generators

For low-frequency applications (less than 500kHz) a cost-effective approach may be to use external RC-controlled oscillators. Three simple RC-controlled oscillators that may be used to clock the CDP1802 are shown in Figure 5. When an external clock is used in high-noise environments, a 20pF to 30pF capacitor between terminal 39 (XTAL) of the CDP1802 and ground may be used to increase the microprocessor noise immunity.



(1/3 CD4069B)

FIGURE 5A. INVERTER TYPE OSCILLATOR (SEE REFERENCES 5 AND 6)

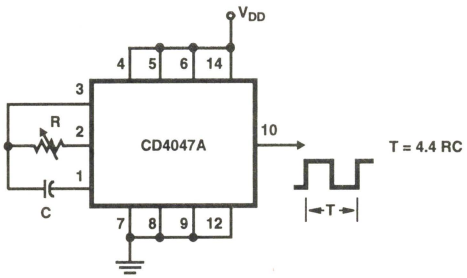
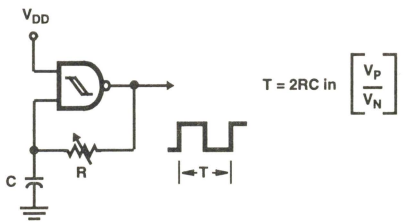


FIGURE 5B. RC OSCILLATOR USING DIGITAL IC CD4047A (SEE REFERENCES 5 AND 6)



(1/4 CD4093B)

FIGURE 5C. SCHMITT-TRIGGER-TYPE RC OSCILLATOR (SEE CD4093B DATA SHEET)

FIGURE 5. THREE SIMPLE RC-CONTROLLED OSCILLATOR CIRCUITS SUITABLE FOR USE AS EXTERNAL CLOCK FOR CDP1802 MICROPROCESSOR (OUTPUT CONNECTED TO PIN 1 THROUGH EVALUATION KIT P2-W)

The selection of the R and C should be compatible with system requirements. The capacitor should be non-polarized and have low leakage. There is no upper limit for either R or C values to maintain oscillation. However, C should be larger than the inherent stray capacitance. R must be larger than the output impedance of the COS/MOS device, which is typically hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted. Based on these considerations recommended values for these components are:

C - greater than 100pF, up to any practical value

R - greater than 10kΩ, but less than 1MΩ

With large values of R and C, the circuit in Figure 5(c) can be used. This circuit, because of its hysteresis, eliminates multiple output pulses caused by noise on the input RC waveform. For a more detailed analysis, see References 5 and 6.

Clock Buffering

In some applications it may be desirable to supply the CPU clock signal to other system components. In such cases the loading on the oscillator circuit should be minimized by buffering the clock through a COS/MOS inverter, as shown in Figure 2. The loading presented by the inverter will be mainly capacitive, about 5pF, and can usually be neglected in non-critical designs. The buffer should be located close to the crystal in order to minimize stray capacitance.

When the crystal oscillator is being trimmed to its desired frequency, the buffered clock technique should also be used to prevent the oscillator from being loaded by the frequency counter.

References

For Harris documents available on the web, see
http://www.semi.harris.com/
Harris AnswerFAX (407) 724-7800.

[1] *CDP1802 Data Sheet*, Harris Semiconductor, AnswerFAX Doc. No. 1305.

[2] *CD4047A Data Sheet*, Harris Semiconductor, AnswerFAX Doc. No. 623.

[3] *CD4093B Data Sheet*, Harris Semiconductor, AnswerFAX Doc. No. 836.

[4] *AN6086 Application Note*, Harris Semiconductor, "Timekeeping Advances Through COS/MOS Technology", AnswerFAX Doc. No. 96086.

[5] *AN6230 Application Note*, Harris Semiconductor, "Timekeeping Advances Through COS/MOS Technology", AnswerFAX Doc. No. 96230.

[6] *AN6267 Application Note*, Harris Semiconductor, "Astable and Monostable Oscillators Using Harris COS/MOS Digital Integrated Circuits", AnswerFAX Doc. No. 96267.

[7] MPM-201 Harris Semiconductor, "User Manual for the Harris CDP1802 COSMAC Microprocessor".

Harris Semiconductor

APPNOTE

No. AN7275.1 March 1997

Harris Digital

User's Guide to the CDP1879 and CDP1879C1 CMOS Real-Time Clocks

Author: D. Derkach

Introduction

The CDP1879 and CDP1879C1 Real-Time Clocks [1] are 24 pin devices, each consisting essentially of a long string of counters that supply standard clock time and date information in BCD format, Figure 1. In addition, the CDP1879 features an alarm circuit that activates the interrupt output pin and a separate clock output pin that provides a programmable square-wave output signal. Both the internal-alarm and clock-out signals can trigger the interrupt output pin, so that a status register is available to indicate the interrupt source. Users can supply a signal to the power-down pin that allows the interrupt-output pin level to control external power-down and wake-up circuits. Software generally required by other real-time clocks to prevent clock rollover is eliminated by a transparent "freeze" circuit that assures data integrity when accessing the clock. The clock's counters, plus a control register that regulates operation, are individually selectable using three address lines. Internal control signals governing read and write operations are selected through the IO/$\overline{\text{MEM}}$ pin, which places the device in a memory-mapped or I/O-mapped mode of operation.

The real time clocks were designed using Harris PaCMOS standard-cell approach and are manufactured under a silicon-gate CMOS process. Both the CDP1879 and CDP1879C1 have guaranteed dc and dynamic parameters that allow operation at temperatures of -40°C to +85°C in a plastic package. In addition, both versions can operate in a ceramic package from -55°C to 125°C (see data sheet [1] for complete static and dynamic values).

The CDP1879 operates from a supply of 4V to 10.5V. It accepts a parallel resonant crystal or will keep time with an external clock source. Crystal frequencies are 1.048576MHz, 2.097152MHz, and 4.194304MHz. The CDP1879C1 is the lower voltage version with an operating voltage range of 4V to 6.5V. Like the CDP1879, it also operates with either an external clock source or at the same crystal frequencies. It can also run with a 32,768Hz crystal.

Interfacing - Hardware Considerations

I/O-Control and Device-Enable Pins

The real-time clocks, shown in block diagram form in Figure 1, are designed to interface directly to Harris CDP1800-series processors (described briefly below). Therefore, pin labels on the clocks, Figure 2, match the pin names of these processors. Figure 3 indicates clock I/O control and direction pins; the functions of these pins are explained immediately below. Figure 4 is an I/O control and device-enabled schematic. Table 1 shows I/O pin connections.

TPA (Timing Pulse A) - TPA refers to a timing signal from the CDP1800-series processors that occurs early in the machine cycle, and that is used to latch the processor's multiplexed high-order address. In the real-time clock, this pin carries a strobe input used to latch the value of the CS pin. In memory-mapped operation, the pin may be tied high, requiring that CS be held for the duration of each read or write cycle. When the I/O-mapping mode is selected, this pin must be pulsed when the CS input is high.

CS (Chip Select) - The chip-select pin is an active high input that is used to enable the clock.

IO/$\overline{\text{MEM}}$ (I/O or Memory-Mode Select) - This pin is tied low to place the clock in the memory-mapped mode, and high when I/O operation is desired. Most processors will use the memory-mapped mode of operation.

$\overline{\text{RD}}$ (Read) - When the clock is in the memory-mapped mode, $\overline{\text{RD}}$ is an active low signal that enables data from the counters or status register to be placed on the data bus for the processor to read. When the clock is in the I/O mode, the read operation occurs when $\overline{\text{RD}}$ is high; a write operation occurs when $\overline{\text{RD}}$ is low and TPB/$\overline{\text{WR}}$ is high.

TPB/$\overline{\text{WR}}$ (Timing Pulse B/Write) - TPB refers to a timing signal from the CDP1800-series processors that appears late in each machine cycle and that is used to write data into accessed peripherals. When the clock is in the memory-mapped mode, TPB/$\overline{\text{WR}}$ is an active low signal used to write data into the clock's counters or control register. During I/O-mapping, a high level on this pin allows data latched on the trailing edge of the signal to be written into the counters or register.

CD1800-Series Interface

The clocks interface to CDP1800-series processors that use memory-mapping and I/O-mapping techniques to communicate with peripherals and memory. Memory-mapping implies address-line decoding to select memory locations and chip selects. With this technique, the real-time

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clock's counters and registers are treated as memory locations. Read and write signals are active low. The CDP1800-series processors include three separate N-lines that are active during the 14 I/O instructions. These instructions are memory referenced so that data traveling in either direction is transferred between the peripherals and memory.

When I/O instructions are executed, the memory location is the reference for data transfer. Therefore, when an output instruction is performed (write cycle) the processor's $\overline{RD}$ line is activated and puts the data in memory onto the data bus. Late in the same cycle, the TPB from the processor is used to write data into the peripheral. An input instruction (read cycle) allows external data to be placed in memory. The processor's $\overline{WR}$ line is activated, and the data is written in.

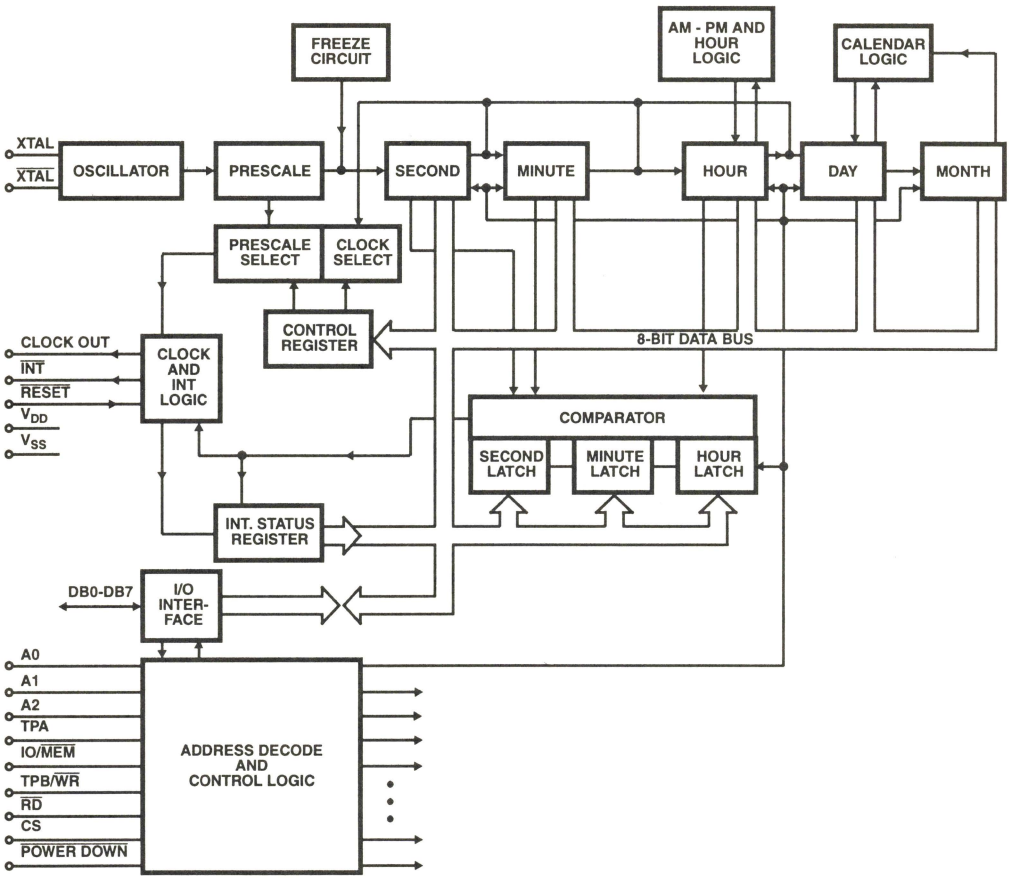


FIGURE 1. BLOCK DIAGRAM OF REAL-TIME CLOCK

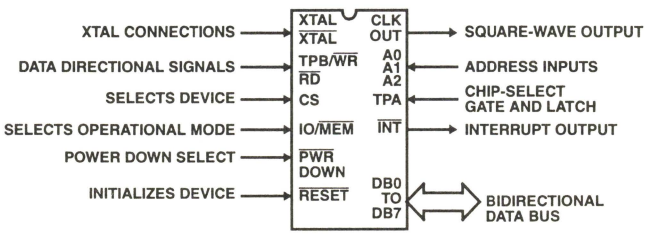


FIGURE 2. REAL-TIME-CLOCK PIN FUNCTIONS

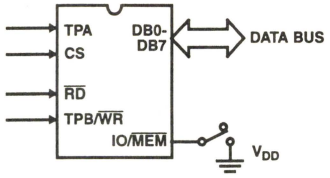


FIGURE 3. I/O CONTROL AND DIRECTION PINS

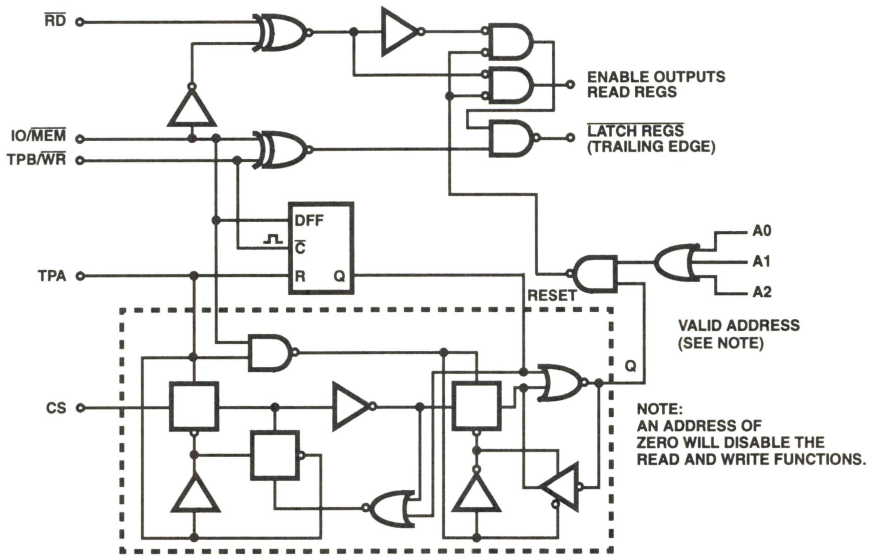


FIGURE 4. I/O CONTROL AND DEVICE ENABLE SCHEMATIC

TABLE 1. I/O PIN CONNECTIONS

PROCESSOR	CDP1879 PIN					
	TPA	CS	$\overline{RD}$	TPB/$\overline{WR}$	IO/$\overline{MEM}$	A0-A2
Harris CDP1800-Series (Memory-Mapped)	TPA (Note 1)	Hi or Decoded Address	$\overline{MRD}$	$\overline{MWR}$	V_{SS}	MA0, MA1, MA2
Harris CDP1800-Series (I/O mapped)	TPA	N or Decoded N Lines	$\overline{MRD}$	TPB	V_{DD}	N0, N1, N2
CDP6805	AS	Hi or Decoded Address	R/$\overline{W}$	DS	V_{DD}	B0 (Note 2), B1, B2
Zilog Corp. Z-80™	V_{DD}	Hi or Decoded Address	$\overline{RD}$	$\overline{WR}$	V_{SS}	A0, A1, A2
8085/NSC800	ALE (Note 1)	Hi or Decoded Address	$\overline{RD}$	$\overline{WR}$	V_{SS}	AD0 (Note 2), AD1, AD2

NOTES:

1. May be connected to V_{DD} when CS is externally latched.
2. Latch externally.

Z-80™ is a Trademark of Zilog Corporation.

Figure 5 shows a typical memory-mapped interface utilizing the CDP1802. This interface places the clock and counter-timer in selectable 4k memory blocks. Figure 6 shows the interface of the clock to an 8085 processor, Figure 7 the interface to a CDP6805, and Figure 8 the interface to a Zilog Corporation Z-80.

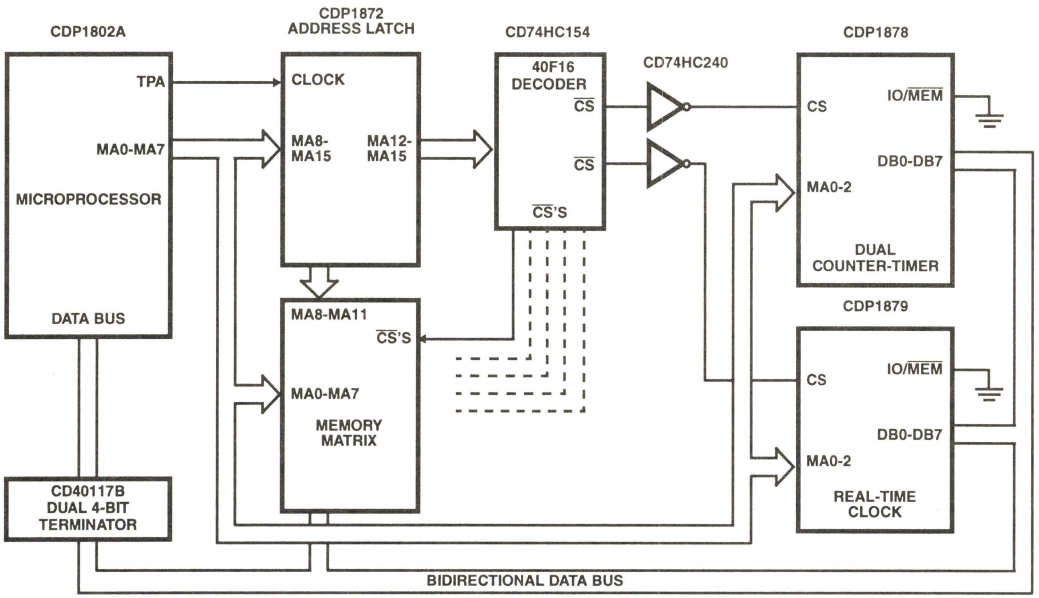


FIGURE 5. REAL-TIME CLOCK AND COUNTER-TIMER IN MEMORY-MAPPED INTERFACE

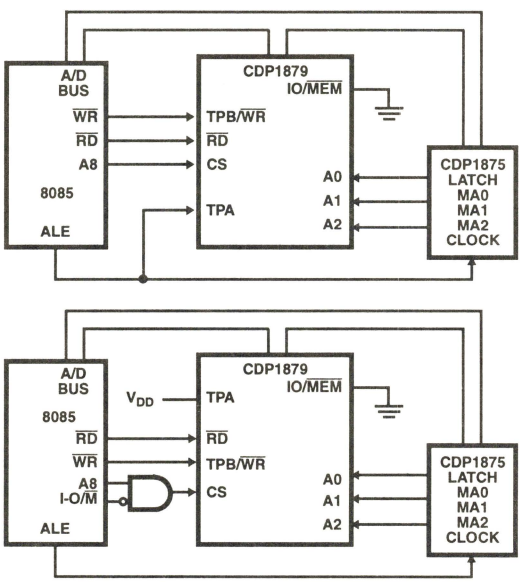


FIGURE 6A. MEMORY-MAPPED INTERFACE

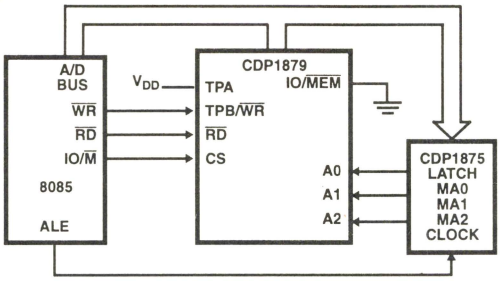


FIGURE 6B. I/O-MAPPED INTERFACE

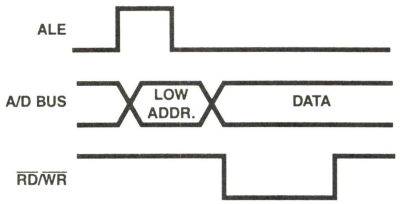


FIGURE 6C. TIMING CYCLES

FIGURE 6. 8085 INTERFACE AND TIMING

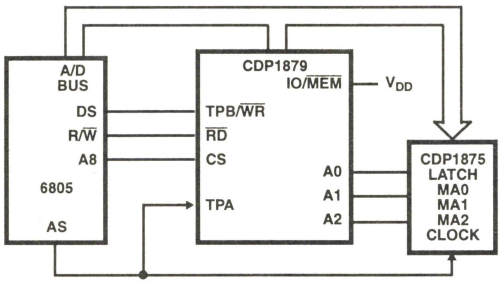


FIGURE 7A. CDP6805 I/O-MAPPED INTERFACE

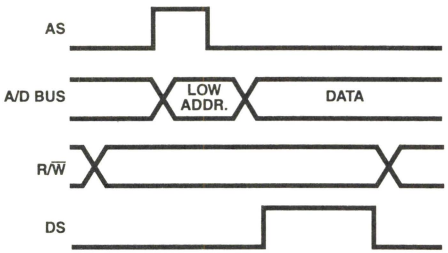


FIGURE 7B. TIMING DIAGRAM

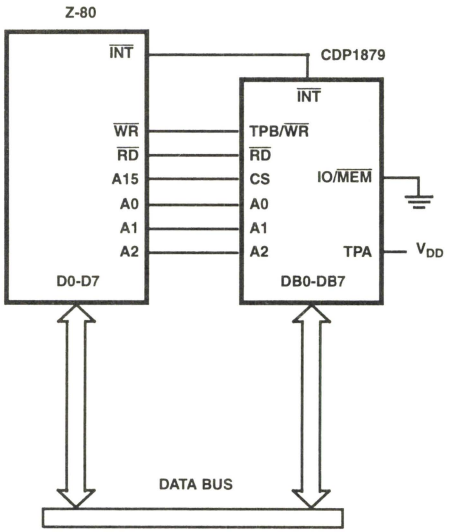


FIGURE 8. ZILOG CORPORATION Z-80 INTERFACE TO THE CDP1879

Timing Considerations

Figures 9 and 10 show read and write-cycle timing wave forms, respectively. The read and write limits shown must be observed to successfully access the clock. Three of the characteristics, hold after read and write, and read access time, may represent critical limit values when the clock is interfaced to processors operating at their maximum frequency limit.

TABLE 2. READ-CYCLE TIMING CHARACTERISTICS

READ CYCLE TIMES (NOTE 1)		LIMITS (ns)	
		MINIMUM (NOTE 2)	MAXIMUM
Data Access from Address	t_{DA}	-	400
Read Pulse Width	t_{RD}	270	-
Data Access from Read	t_{DR}	-	375
Address Hold After Read	t_{RH}	0	-
Output Hold After Read	t_{DH}	50	230
Chip Select Setup to TPA	t_{CS}	50	-

NOTES:
1. Characteristics at T_A = -40°C to +85°C; V_{DD} = 5V ±5%; Input t_R, t_F = 10ns; C_L = 50pF and 1 TTL load.
2. Time required by a limit device to allow for the indicated function.

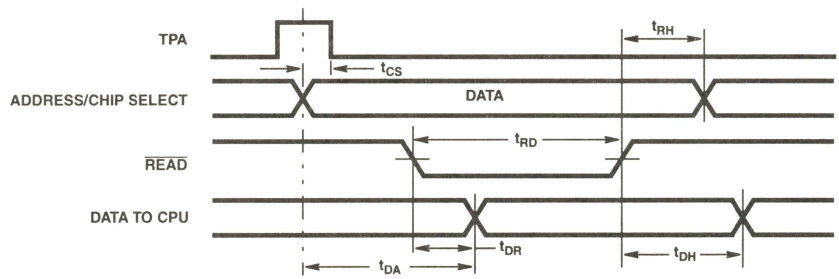


FIGURE 9. READ-CYCLE TIMING WAVEFORMS

TABLE 3. WRITE-CYCLE TIMING CHARACTERISTICS

WRITE CYCLE TIMES (NOTE 1)		LIMITS (ns)	
		MINIMUM (NOTE 2)	MAXIMUM
Address Setup to Write	t_{AS}	225	-
Write Pulse Width	t_{WR}	150	-
Data Setup to Write	t_{DS}	65	-
Address Hold After Write	t_{AH}	0	-
Data Hold After Write	t_{WH}	150	-
Chip Select Setup to TPA	t_{CS}	50	-

NOTES:
1. Characteristics at T_A = -40°C to +85°C; V_{DD} = 5V ±5%; Input t_R, t_F = 10ns; C_L = 50pF and 1 TTL load.
2. Time required by a limit device to allow for the indicated function.

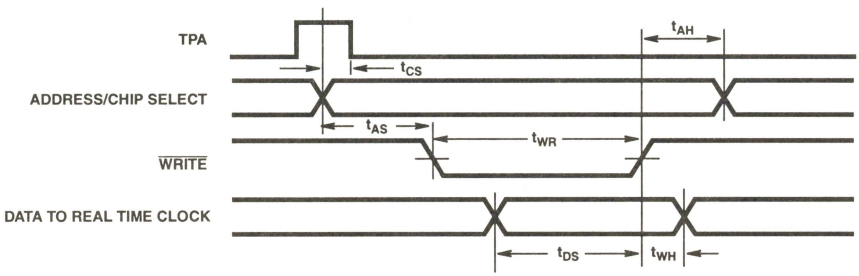


FIGURE 10. WRITE-CYCLE TIMING WAVEFORMS

Output Hold After Read (t_{DH})

When multiplexed bus processors, in which address and data share the same pins, are interfaced to the clock, the output-hold-after-read parameter (230ns) may cause bus contention. As an example, at 5MHz, the CDP6805 requires data to be off the bus within 160ns after data strobe. The 8085A operating with a 6MHz crystal requires 150ns after read. Since the clock may hold data for 230ns, bus contention may occur if these processors are interfaced to the clock at their maximum operating frequencies.

Data Hold After Write (t_{WH})

The real-time clocks require that data be held after the trailing edge of the write pulse for 150ns. Neither the 8085/NSC800, Z-80, nor CDP6805 meet this requirement at their maximum operating frequencies.

Data Access From Read (t_{DR})

The clock will supply data a maximum of 375ns from the leading edge of the read pulse. The data setup requirements for processors operating at their maximum frequencies may require faster access.

Hold and Access-Time Solutions

All of the above parameters are frequency dependent. Often, simply lowering the frequency when accessing the clock will solve any timing problems. Access times can be extended by inserting wait states. Write and read-hold-time problems are more difficult to correct; glue parts, such as latches and buffers, are required to meet the requirements of these timing parameters.

Interfacing - Software Considerations

Programming Model

Figure 11 illustrates the counters, alarm latches, and registers that must be accessed to write in and read out time and date information. The functions are selected through internal decoding of three address lines. Table 4 contains the register access codes for different combinations of address inputs. Figure 12, a programming model of the same registers, shows their read and/or write availability. These address lines and data lines, in conjunction with the I/O control pins, constitute the interface to the clock.

When the clock is configured for memory-mapped operation, it can be considered as six memory locations that reside in an area of memory determined by the definitive decoding of the upper address bits. The clock's I/O-mapped mode utilizes the N-lines (I/O lines) and I/O instructions of the CDP1800-series processor. The processor's N-lines are decoded for use as a chip select, and in a two-level scheme, are also used as the address input signals.

When other processors are interfaced to the clock, the clock will generally be placed in its memory-mapped mode. An exception is interface with the CDP6805, where the clock is usually wired for I/O operation.

Writing to and reading from the clock is as straightforward as accessing memory. Software considerations regarding clock rollover (when the one-second clock may pulse the counters during read or write cycles) are eliminated by utilizing the freeze circuit (described below), which requires only one additional instruction. Use of the freeze circuit eliminates the software burden of looking for a signal or register bit that guarantees valid data. A write cycle with address 1 and don't -care data before any series of counter accesses (read or write cycles) assures that the one-second clock has been held and will not interfere with accesses for 250ms.

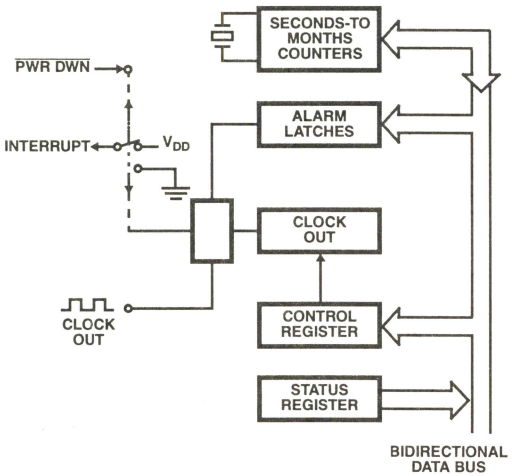


FIGURE 11. FUNCTIONS THAT MUST BE ACCESSED TO WRITE IN AND READ OUT TIME AND DATE INFORMATION

Freeze Circuit

The freeze circuit is designed to allow the user easy access to the real-time clock without the fear that clock rollover will cause erroneous time data. Clock rollover problems occur during counter reads while the asynchronous one-second clock input to the counter-divider chain is rippling through the counters.

As an example in Figure 13A, the one-second clock is about to set the time to 0 seconds, 0 minutes and 3 hours. A read is performed, and the hours counter indicates 2 hours. But before the second and minute counters are read, the one-second clock ripples through them, with the result that the counters hold the time shown in Figure 13B. When the seconds and minutes counters are read (Figure 13B), their values are correct, but the hours time, read before the ripple, is 1 hour off. It is apparent that this type of error can be a substantial problem, particularly if the date and month counters are involved.

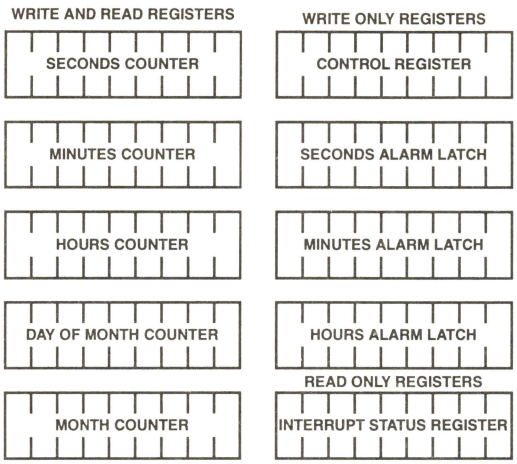


FIGURE 12. PROGRAMMER'S MODEL OF THE REGISTERS OF FIGURE 11

Operation

The counter-series string is clocked by the negative transition of the one-second clock. This clock transition must pass through the freeze circuit before toggling the counter-series string, as shown in Figure 14. The freeze circuit creates a "window" 250ms wide shown as time (A) in Figure 15. If the counter reads or writes (for addresses other than address 7) are performed during this window, the clock transition is held and is not allowed through the freeze circuit until time (C) Figure 15, when the transition is inserted into the counter series string. If counter accesses are initiated just before the one-second-clock transition, the clock would toggle the counters 250ms later. Therefore, a requirement when using the real-time clocks is to finish operations within 250ms of the initial access.

If the clock is accessed during time (A), Figure 15, and then accessed again at time (C), when the counter is allowed to toggle, ripple problems would occur. To preclude this problem, a second window is created by the freeze circuit during time (B). This window will allow a write to address 1 to immediately reset the freeze circuit and clock the counters. Subsequent accesses to the real-time clock will occur well after the clock has rippled through the counters.

If read or write operations are performed during time periods other than (A) or (B), the freeze circuit is not functional.

Figure 16 shows a simplified freeze circuit (a), and the sequence of freeze-circuit operation (b).

TABLE 4. REGISTER TRUTH TABLE

ADDRESS			ACTIVE SIGNAL		BIT 3 CONTROL REGISTER	REGISTER OPERATION
A2	A1	A0	TPB/$\overline{WR}$	RD		
0	1	0	X		0	Write Seconds Counter
0	1	0		X	0	Read Seconds Counter
0	1	1	X		0	Write Minutes Counter
0	1	1		X	0	Read Minutes Counter
1	0	0	X		0	Write Hours Counter
1	0	0		X	0	Read Hours Counter
1	0	1	X		0	Write Date Counter
1	0	1		X	0	Read Date Counter
1	1	0	X		0	Write Month Counter
1	1	0		X	0	Read Month Counter
0	1	0	X		1	Write Seconds Alarm Latch
0	1	1	X		1	Write Minutes Alarm Latch
1	0	0	X		1	Write Hours Alarm Latch
1	1	1	X			Write Control Register
1	1	1		X		Read Int. Status Register

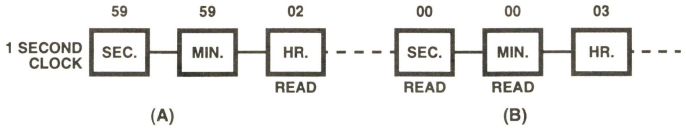


FIGURE 13. FREEZE-CIRCUIT READ EXAMPLE

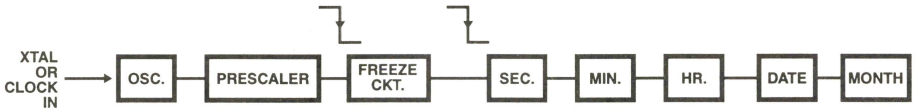


FIGURE 14. COUNTER SERIES STRING

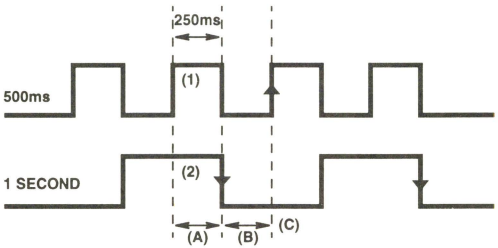


FIGURE 15. FREEZE-CIRCUIT TIMING WAVEFORMS

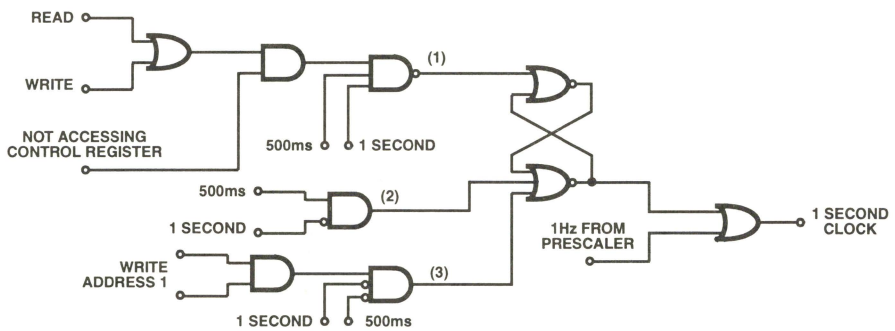


FIGURE 16. (A) SIMPLIFIED FREEZE CIRCUIT, AND (B) FREEZE-CIRCUIT OPERATION

NOTES:

1. Set freeze during time period A, (one second clock is held high)
2. Reset freeze at time period C,
3. or during time period B if address 1 is present during a write cycle.

Restrictions on Accuracy

The data sheet for the real-time clock states that when the seconds counter is written to, the last 7 stages of the prescaler are reset, resulting in a 10ms accuracy. Normally, the seconds counter will be clocked 1 second from the time of the write to the seconds counter. However, if the freeze circuit has been activated, this sequence may not occur, therefore, to assure the 10ms accuracy, the following procedure should be used:

1. Write to seconds counter - don't care data - address 2
2. Dummy write - don't care data - address 1
3. Write to seconds counter - valid data - address 2

The mild restrictions on accesses to the real-time clock require no additional software or hardware considerations to assure data integrity. In all other known clocks, software solutions to clock rollover problems range from reading and comparing the time data twice to sampling register values. Hardware solutions vary between stopping any internal clock updates to monitoring output-pin transitions. The addition of an address 1 write operation preceding accesses to the CDP1879 real-time clock in conjunction with the requirements to finish accesses in 250ms will guarantee stable and accurate time data.

Register Descriptions

The real-time clock contains a control register to configure its operation, and a status register to identify interrupts, five registers or counters to hold the time from seconds to months, and three additional registers that are referred to as alarm latches, which hold the alarm time.

Control Register

The control register is a write-only register that shares the same address as the status register, address 7. A brief explanation of the functions of the eight bits in the control register are shown in Figure 17; more detail is given in the paragraphs that follow.

Bits 0 and 1 - Frequency Select - The logic levels in bits 0 and 1 are decoded and used to select the appropriate input to the last 14 stages of the prescaler chain, Figure 18. Their selection must match the crystal or external clock source used to drive the oscillator selection of the real-time clock.

Bit 2 - Start/Stop - As shown in Figure 18, a 1 in bit 2 enables the input to last through 14 stages of the prescaler chain. A zero in this position inhibits counting.

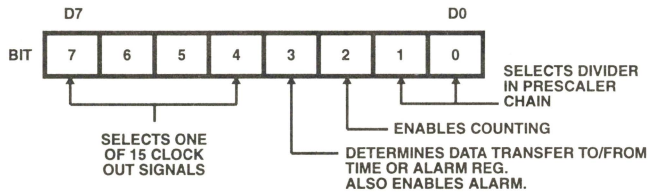
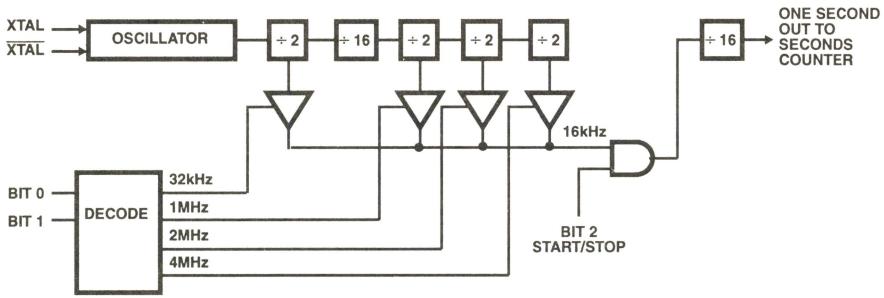


FIGURE 17. CONTROL REGISTER



BIT 0	BIT 1		BIT 2	
0	0	32,768Hz	0	Stop Counter
1	0	1.048576MHz	1	Start Counter
0	1	2.097152MHz		
1	1	4.194304MHz		

FIGURE 18. FREQUENCY-SELECT OPERATION

Bit 3 - Counter/Latch Control - Figure 19 is a simplified diagram of the counter/alarm latch access. Bit 3 has two functions. First, if set to zero, it directs written data to the time counters. If set to 1, data is written into the alarm latches. This bit function is necessary because the time counters and their comparable alarm latches have the same addresses. The second function of bit 3 is to enable the alarm-out signal. An alarm signal (interrupt output low and bit 7 set in the status register) will only appear if this bit (bit 3) is a logic 1.

Bits 4, 5, 6 and 7 - Clock Select - Figure 20 is a block diagram of the clock-out select function; Figure 21 is a table of clock-out selections. Bits 4, 5, 6, and 7 are decoded, and enable the required prescaler or time counter output to toggle the clock-out pin.

Status Register

The status register, Figure 22, is used to indicate the interrupt source. Bits 0 through 5 are held low. Bit 6 high indicates that a programmed negative clock-out transition has occurred, and bit 7 high identifies the alarm circuit as the interrupt source. These bits are reset by an external reset or by writing to the control register. Note, in Figure 23, the delay of approximately 30ms before the alarm signal sets bit 7.

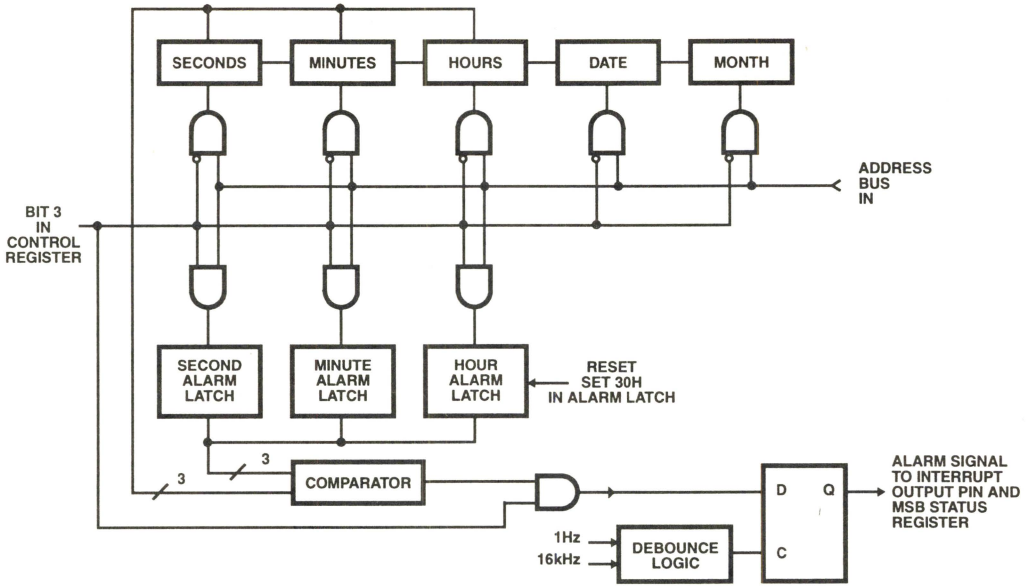


FIGURE 19. SIMPLIFIED DIAGRAM OF COUNTER/ALARM LATCH ACCESS

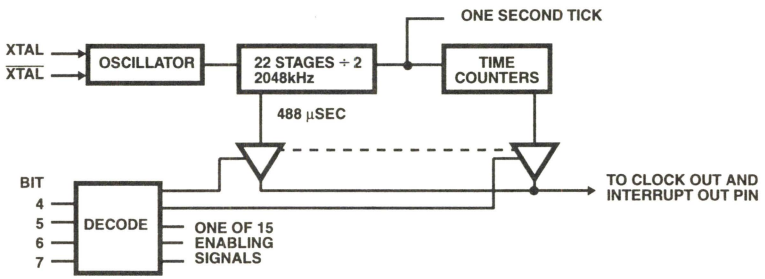
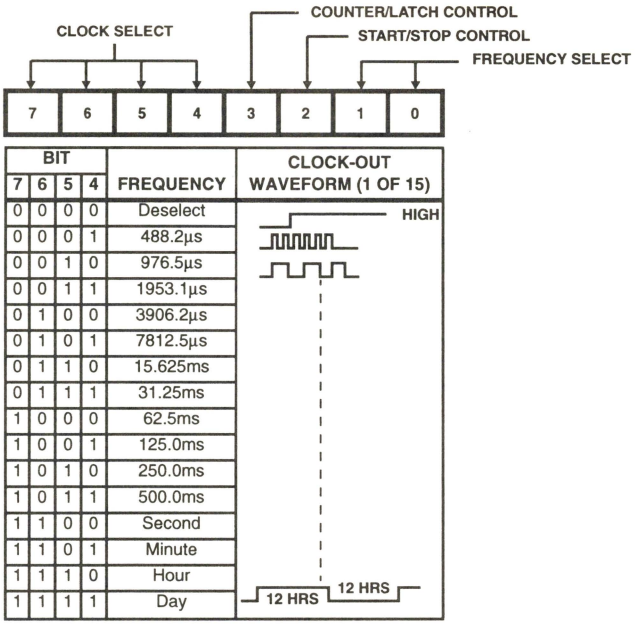


FIGURE 20. BLOCK DIAGRAM, CLOCK-OUT SELECT



BIT 7	6	5	4	FREQUENCY	CLOCK-OUT WAVEFORM (1 OF 15)
0	0	0	0	Deselect	
0	0	0	1	488.2µs	
0	0	1	0	976.5µs	
0	0	1	1	1953.1µs	
0	1	0	0	3906.2µs	
0	1	0	1	7812.5µs	
0	1	1	0	15.625ms	
0	1	1	1	31.25ms	
1	0	0	0	62.5ms	
1	0	0	1	125.0ms	
1	0	1	0	250.0ms	
1	0	1	1	500.0ms	
1	1	0	0	Second	
1	1	0	1	Minute	
1	1	1	0	Hour	
1	1	1	1	Day	

FIGURE 21. CLOCK-OUT SELECTIONS

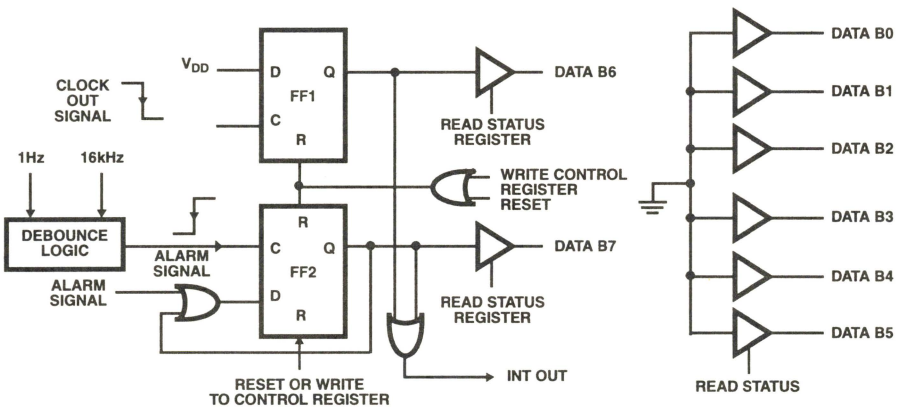


FIGURE 22. STATUS REGISTER

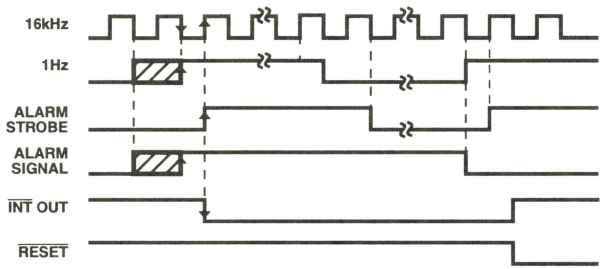


FIGURE 23. DEBOUNCE WAVEFORMS

Operating Sequence

Although accessing of the clock is similar to accessing of memory, certain procedures should be followed when writing the data to assure correct operation.

The control register is accessed first to set the operating characteristics and to direct subsequent accesses to the counters or alarm latches. The upper nibble of the control-register byte selects one of 15 square-wave output signals that appear at the clock-out pin. If a clock-out is selected before the time counters are accessed and loaded, an inadvertent interrupt may be generated. To preclude this occurrence when the interrupt signal is utilized, the upper nibble of the control register byte is set to zero during the initial control-register write cycle. The time counters and/or alarm latches are then loaded. The control register is then written to again, and the value in the upper nibble selects the required clock.

Data Format Required (BCD)

1. Seconds and Minutes counters and alarm latches 00 to 59
2. Hours counter: 01 to 12 for AM/PM
   00 to 23 for 24-hour time

   Bit 7: 0 = AM, 1 = PM

   Bit 6: 0 = 24 hour, 1 = 12 hour

   Hour alarm latch: 01 to 12 for AM/PM, 00 to 23 for 24 hour.

   12 hour (AM/PM): Bit 7: 0 = AM, 1 = PM

   If the time counter is set for 24-hour time, bit 7 is don't care.
3. Day-of-month counter: 01 to 28, 29, 30 or 31.
4. Month counter: Jan. = 1, Dec. = 12

   Bit 7: 0 = No leap year, 1 = leap year

Setting the Time

The time counters, from seconds to months, are accessed and written into using the procedure described below. Data entered is in BCD format. For example, 12 seconds in the seconds counter would be represented as 00010010. The hours counter, however, utilizes its upper bits for AM/PM designation and 12/24-hour selection. Moreover, bit 7 in the months counter is set by the user to indicate leap year. All of these bits must be set as required in addition to the BCD hour and month information. For example, if 4 PM is written to the hours counter, a BCD code of 00000100 for the hours plus a 1 in bits 6 and 7 to enable PM and 12-hour operation would require a data byte of 11000100 (Hex C4).

Procedure to Set the Time

1. Chip selected and address 7 present on the address lines to access the control register.
2. Write to control register with the required data byte. Bit 3 must be set to zero.
3. Use addresses 2 to 6 to access seconds-to-months counters, in any order, and load appropriate data byte. (BCD data plus bits 6 and 7 in hours counter and bit 7 in month counter.)
4. Writing to the seconds counter resets the last 7 stages of the prescaler, thereby setting an accuracy of 10ms.

Setting the Alarm

Figure 24 shows the alarm logic. As previously described, bit 3 in the control register must be a 1 to direct subsequent data to the alarm latches. A comparator circuit compares the time and alarm latch seconds, minutes, and hour outputs. When this comparison is true and bit 3 in the control register is set to 1, an alarm is generated that activates the interrupt-out pin and sets bit 7 in the status register to a high logic level. The two most significant bits in the hours time counter are used for an AM/PM indication (User set for AM or PM with subsequent toggling every 12 hours) and to set 12/24-hour operation.

If bit 6, the 12/24-hour control bit, is set to zero (24-hours), a match of bit 7 (AM/PM) between the hours time counter and alarm latch is not required to generate a true comparison.

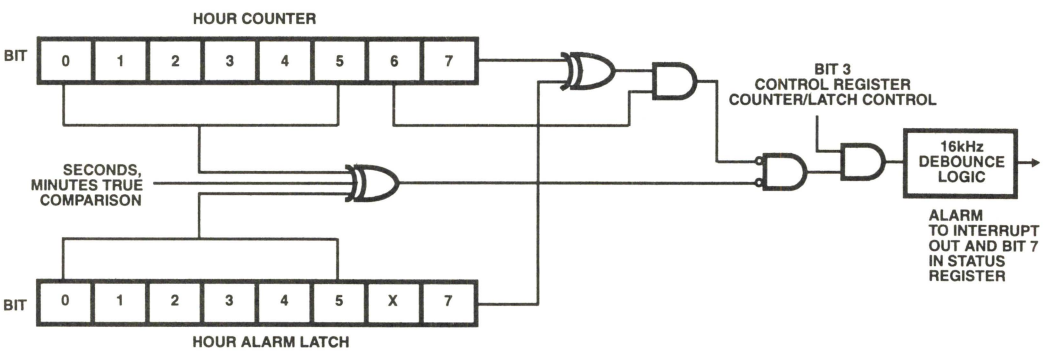


FIGURE 24. ALARM LOGIC

When an alarm occurs, there is a delay of 30µs before the alarm bit is set in the status register. The interrupt-out pin signal is also delayed for this period. Additionally, if a clock out was selected that also activates the interrupt-out in coincidence with the alarm-out signal (for example, clock-out set for one second and any alarm-time set), the status register will indicate a clock-out transition (bit 6 = 1) 30µs before bit 7 is set to 1 in the status register.

Resetting the Interrupt-Out Signal and Status Register

There are two methods of resetting the interrupt-out signal and status register once an alarm or clock-out transition has occurred.

Reset Pin (Schmitt Input)

A low on the reset pin will accomplish the following:

1. Set the interrupt-out pin high.
2. Clear the status register.
3. Place 30 Hex in the hour alarm latch. This entry will prevent an inadvertent interrupt when programming the time.

Control Register Write

Writing to the control register sets the interrupt-out high and clears the status register.

Power-Down Operation

Figure 25 shows power-down input-control logic. A low on the power-down pin (Schmitt input) activates the real-time-clock's power-down function. This function is enabled at the trailing edge of a read or write signal and, therefore, power down will not occur until the read or write cycle is concluded.

When power down is activated, the following events occur:

1. Read and write control signals are disabled.
2. The data bus is placed in an input condition and logic transitions are ignored. (Therefore, the bus must be terminated.)
3. The clock-out signal is set low.
4. The interrupt-out pin is three-stated.

The clock continues to keep time and there is no appreciable change in operating power. The interrupt output will go low if an alarm or clock transition (internal clock transition) occurs after power down has been initiated. An application using the power-down feature to control a microprocessor's clock signal is illustrated in Figure 26. This application is especially appealing in a CMOS circuit design where only quiescent current will be drawn when the processor's clock input is disabled.

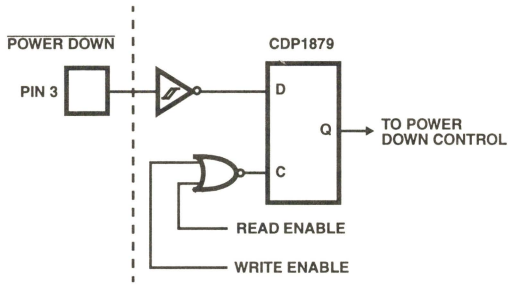


FIGURE 25. POWER-DOWN INPUT-CONTROL LOGIC

In an operational sequence utilizing the circuitry of Figure 26, the serial Q output of the CPU is activated after the clock is configured with an alarm time. The oscillator then stops and the device enters the power-down mode. When the alarm activates and the $\overline{INT}$ output is set low, the CPU resets and polls the $\overline{EF1}$ flag to determine whether a cold or warm start routine is in order. The control register is then written to, an event that resets the interrupt requests.

Any general-purpose microprocessor can utilize the low operating power of the real-time clock. Typical operating current with a crystal-controlled oscillator at 32kHz and 5V is 100µA, and at 4MHz, 600µA. The trade-off between high frequency and accuracy and low-frequency operation with lower power consumption must be resolved by the user. The ease of programming and the features offered by the real-time clock aid the designer and lower the level of programmed support required.

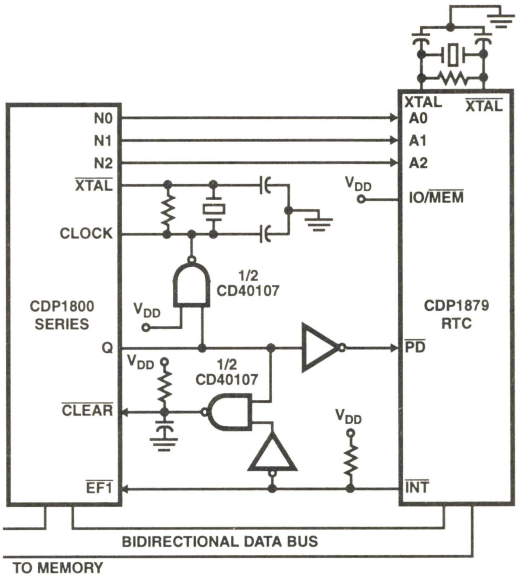


FIGURE 26. APPLICATION OF REAL-TIME CLOCK THAT USES POWER-DOWN FEATURE TO CONTROL A MICROPROCESSOR'S CLOCK SIGNAL

Power Considerations

The CDP1879 power requirements are shown in Table 5. The values listed are maximum limits with a V_{DD} of ±5% and a temperature range of -40°C to 85°C.

Table 6 shows output drive capabilities under the same conditions. All inputs must meet CMOS requirements with a minimum high of 3.5V and a maximum low of 1.5V at a V_{DD} of 5V.

Standby Operation (Low Voltage)

When utilizing an external crystal with its on-board oscillator as the frequency source, the CDP1879 and CDP1879C1 can operate at a supply voltage no lower than 4 volts. However, if a 32kHz external frequency source is provided at the XTAL input pin, the clock can operate in a standby mode down to 2.5V at 0 to 70°C, and 3V at -40°C to +85°C. Figure 27 shows the typical minimum standby voltage. Figure 28 shows that the real-time clock must be disabled by CS (chip-select signal) a minimum of 2µs before reaching the standby voltage level, and enabled again after the same period of time when the voltage is raised again.

When the clock is in the standby mode, it functions only as a timekeeping device; all read/write data accesses are disallowed.

TABLE 5. POWER REQUIREMENTS OF THE REAL-TIME CLOCK

MODE	INPUT FREQUENCY	POWER-SUPPLY VOLTAGE		UNITS
		5V	10V	
Operating Current with Crystal Oscillator	(NOTE 1) 32kHz	0.25	-	mA
	1MHz	0.5	3.0	mA
	2MHz	0.6	3.5	mA
	4MHz	0.8	5.0	mA
Operating Current with External Clock Source	32kHz	0.15	0.25	mA
	1MHz	1.0	2.0	mA
	2MHz	1.5	3.0	mA
	4MHz	2.0	4.5	mA

NOTE:

1. CDP1879C1 Only

TABLE 6. OUTPUT DRIVE CAPABILITIES

POWER-SUPPLY VOLTAGE	5V	10V	UNITS
Data-Bus and Interrupt-Out Drive (Sink)	1.8	3.6	mA
Data-Bus and Interrupt-Out Drive (Source)	-1.10	-2.6	mA
Clock Out (Sink)	0.6	1.2	mA
Clock Out (Source)	-1.1	-2.6	mA

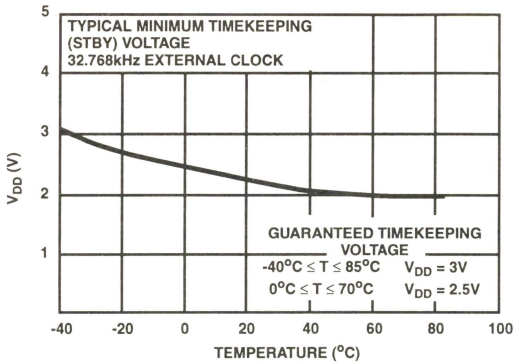


FIGURE 27. TYPICAL MINIMUM STANDBY VOLTAGE

Oscillator Operation

The CDP1879 operates with a crystal connected to its XTAL and $\overline{XTAL}$ inputs, or accepts an external clock source at its XTAL input that has a rise and fall time of less that 10µs. Typical oscillator parameters are listed in Table 8; suggested circuits are described in Figures 29 through 32.

TABLE 7. STANDBY-VOLTAGE CHARACTERISTICS

PARAMETER	V_{DD}	V (STBY)	CDP1879		CDP1879C1		UNITS
			MIN	MAX	MIN	MAX	
Chip Deselect to Stby Voltage Time, $t_{C(STBY)}$	5	2.5, 3	2	-	2	-	µs
	10	2.5, 3	1	-	-	-	µs
Recovery to Normal Operation Time, t_{RC}	5	2.5, 3	2	-	2	-	µs
	10	2.5, 3	1	-	-	-	µs

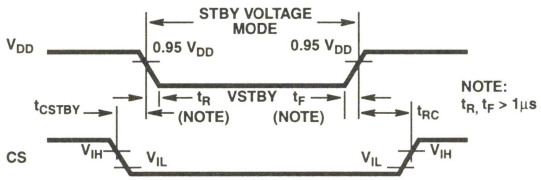


FIGURE 28. WAVEFORMS AND TIMING DIAGRAM

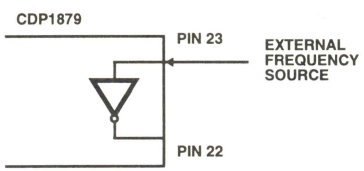


FIGURE 29. CONNECTIONS FOR CDP1879 WHEN AN EXTERNAL FREQUENCY SIGNAL IS SUPPLIED

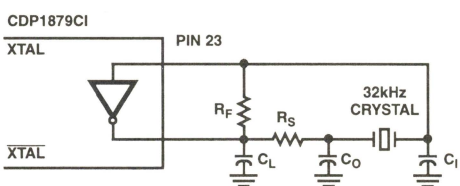


FIGURE 30. SUGGESTED OSCILLATOR CIRCUIT FOR 32kHz CRYSTAL OPERATION

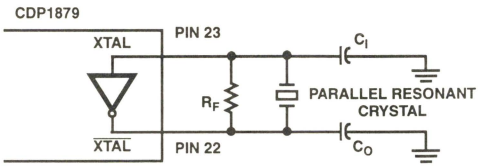


FIGURE 31. SUGGESTED OSCILLATOR CIRCUIT FOR 1, 2, OR 4MHz OPERATION

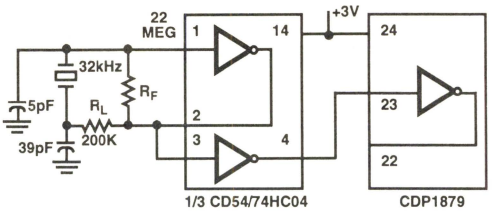


FIGURE 32. TYPICAL EXTERNAL-CLOCK-SOURCE DIAGRAM

Design Considerations for a Stable Crystal Oscillator

1. Stray capacitance should be minimized for best oscillator performance. Circuit-board traces connected to the oscillator pins should be kept to a maximum of 1 inch, and there should be no parallel traces.
2. A signal or power-source line must not cross or approach the oscillator-circuit line.
3. It is advisable to put a nonelectrolytic 0.1µF capacitor between V_{DD} and V_{SS} of the CDP1879.

Real-Time-Clock System

Figure 33 illustrates a working system in which the CDP1879 is configured for I/O operation to display time in minutes and hours. Figure 34 shows the real-time-clock flowchart. A CDP1802 processor outputs instructions and data in a two-level device-selection scheme. An output instruction of OUT 1 (Hex 61) activates the processors N lines, and is decoded by the CDP1873C to provide a chip-select signal to the CDP1875C output port. The data present on the data bus during the output instruction is latched in the CDP1875C and provides the chip-select signal for the clock or the CD22105A LCD driver.

If no other OUT 1 instruction with different bus data is issued by the processor, the device will remain selected. Subsequent output and input instructions will then address the clock, if it is selected, to read or write to its registers. When the LCD driver is selected, the processor's OUT 2 instructions load the driver with the display information.

The backplane signal from the LCD driver is input to one of the processor's flag lines, and is sampled to flash the colon by placing the colon input, via the processor's Q line, in or out of phase with the backplane signal. The CDP1879's clock-out signal is set for one second, and drives the processor's interrupt to turn the display colon off. A routine in the main program turns the colon on when the interrupt is not present.

A sample program that illustrates the CDP1879's clock-out signal and alarm capability is listed in Figure 35. The alarm routine is written to flash eights when the alarm activates. The clock will continue to keep time and will display it along with the alarm display.

Reference

For Harris documents available on the web, see
http://www.semi.harris.com/
Harris AnswerFAX (407) 724-7800

[1] *CDP1879, CDP1879C-1 Data sheet,* Harris Semiconductor, AnswerFAX Doc No. 1360

TABLE 8. TYPICAL OSCILLATOR-CIRCUIT PARAMETERS FOR SUGGESTED OSCILLATOR CIRCUITS

PARAMETER	OSCILLATOR FREQUENCY				UNITS
	4.197MHz	2.097MHz	1.049MHz	(NOTE 1) 32768Hz	
R_F	22	22	22	22	MΩ
C_O	39	39	39	39	pF
C_I	5	5	5	5	pF
R_S	-	-	-	200	kΩ
C_L	-	-	-	91	pF
Crystal Impedance	73	200	200	50K (max)	Ω

NOTE:

1. CDP1879C1 Only

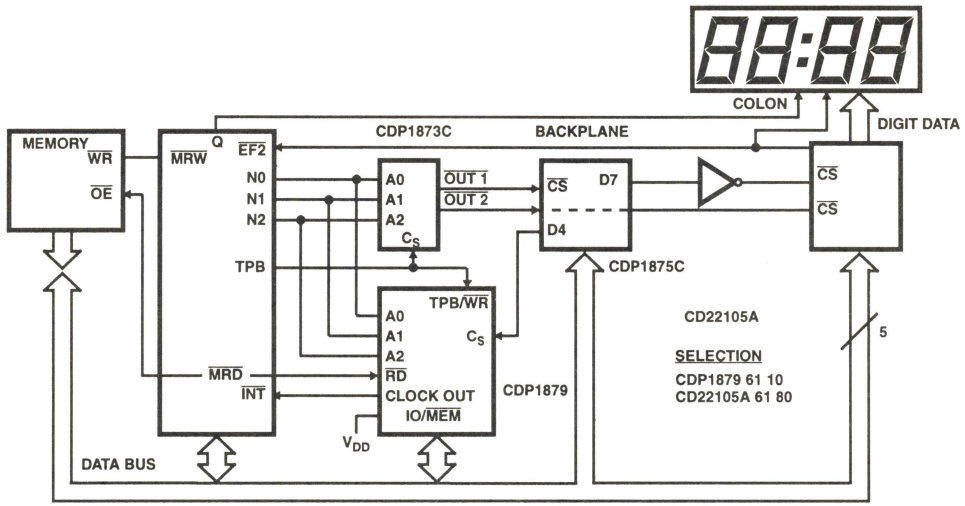


FIGURE 33. REAL-TIME CLOCK SYSTEM

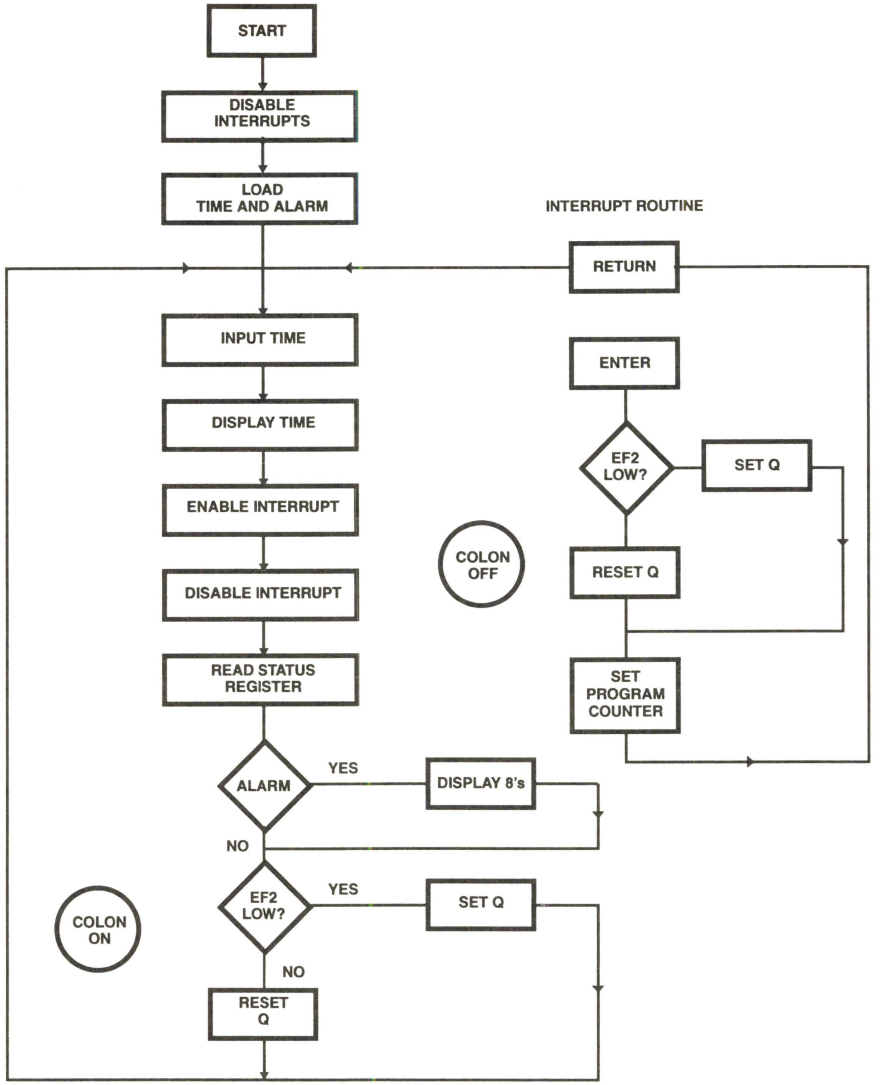


FIGURE 34. REAL-TIME-CLOCK FLOWCHART

```
        ... PROGRAM DISPLAYS 8:30 A.M. AND FLASHES
        ... 8'S AND TIME WHEN ALARM ACTIVATES
        ... AT 8:31:10.
        ... INTERRUPT ON PROCESSOR CONNECTS TO 1 SEC.
        ... CLOCK OUT ON CDP1879. EF2 CONNECTS TO
        ... BACKPLANE SIGNAL ON LCD DRIVER.
        ... INTERRUPT ROUTINE IS USED TO TURN COLON OFF
        ... BY SAMPLING EF2 AND TOGGLING Q.
        ... TWO LEVEL I/O IS USED FOR SELECTION
        ... CLOCK IS SELECTED WITH 61 10.
        ... LCD DRIVER IS SELECTED WITH 61 80.
        ... AND 62 INSTRUCTIONS LOAD DRIVER AFTER SELECTION.
        DIS; DC00H
        LDI A.1 (ENTER); PHI R1          ... SET INTERRUPT POINTER
        LDI A.0 (ENTER); PLO R1
        OUT 1; DC 010H                   ... SELECT CLOCK
        OUT 7; DC 003H                   ... LOAD C.R.
        OUT 2; DC 000H                   ... ZERO SECONDS
        OUT 3; DC 030H                   ... 30 MINUTES
        OUT 4; DC 048H                   ... 8 A.M.
        OUT 7; DC 00BH                   ... SELECT ALARM LATCH
        OUT 2; DC 010H                   ... 10 SEC. ALARM
        OUT 3; DC 031H                   ... 31 MIN. ALARM
        OUT 4; DC 048H                   ... 8 A.M. ALARM
        OUT 7; DC 0CFH                   ... ONE SEC. CLOCK
                                         ... ALARM ACTIVATES 1 MIN.
                                         ... 10 SEC. AFTER START
INPUT   SEX 0; OUT1; DC 010H             ... SELECT CLOCK
        LDI A.1 (MIN); PHI R8
        LDI A.0 (MIN); PLO R8
        SEX 8
        INP 3; PLO R7                    ... INP MINUTES
        ANI 0FH                          ... MASK UPPER
        STXD; GLO R7                     ... STR LOW MIN.
        ANI 0F0H                         ... MASK LOWER
        SHR; SHR; SHR; SHR
        ADI 010H; STXD                   ... ADD CHAR. POS.
        INP 4; PLO R7                    ... INPUT HOURS
        ANI 0FH                          ... MASK UPPER
        ADI 020H; STXD                   ... ADD CHAR. POS
        GLO R7; ANI 030H                 ... MASK 6 BITS
        BNZ HR                           ... CHECK FOR 0 HRS
        LDI 03FH; STR R8                 ... STR BLANK HRS
        BR OUT

HR      SHR; SHR; SHR; SHR
        ADI 030H                         ... ADD CHAR. POS.
        STR R8
OUT     SEX 0
        OUT 1; DC 080H                   ... SELECT LCD DRIVER
        SEX 8
        OUT 2; OUT 2; OUT 2; OUT 2       ... LOAD DRIVER
        SEX 0
        RET; DC 00H                      ... ENABLE INT TO SAMPLE CLOCK OUT
        DIS; DC 00H                      ... DISABLE INT
        OUT 1; DC 010H
        SEX 8
        INP 7; XRI 0C0H                  ... READ STATUS REG
        BX ALARM                         ... FOR ALARM
CHK     B2 ON                            ... COLON ON
        REQ; BR INPUT
ON      SEQ
        BR INPUT                         ... REPEAT
ALARM   LDI A.1 (MIN); PHI R8
        LDI A.0 (MIN); PLO R8
        LDI 008H; STXD                   ... LEAD 8'S INTO
        LDI 018H; STXD                   ... LCD DRIVER
        LDI 028H; STXD
        LDI 038H; STR R8
        SEX 0; OUT 1; DE 080H; SEX 8
        OUT 2; OUT 2; OUT 2; OUT 2
        BR CHK
BACK    SEP R0                           ... RETURN MAIN
ENTER   B2 OFF                           ... ENTER POINT FOR
        SEQ                              ... INTERRUPT ROUTINE
        BR SET                           ... COLON OFF
OFF     REQ
SET     LDI A.1 (INPUT); PHI R0          ... RESET P.C.
        LDI A.0 (INPUT); PLO R0
        BR BACK
HOURS   DS 3
MIN     DS 1
```

FIGURE 35. REAL-TIME-CLOCK PROGRAM

Harris Semiconductor

APPNOTE

No. AN7374.2 March 1997

Harris Digital

The CDP1871A Keyboard Encoder

Author: D. Derkach

Introduction

The CDP1871A Keyboard Encoder [1] interfaces directly between a CDP1800-series (or other) processor and a mechanical keyboard array. It services up to 53 ASCII-coded keys and up to 32 Hex-coded keys. This note describes the encoder's operation, explains its dynamic electrical characteristics, and features those factors that will affect device operation when the encoder is used with a non-1800-series processor.

Operation

The CDP1871A is made up of two major sections: the counter/scan-selection logic and the control logic. Figure 1 shows a block diagram of the device, Figure 2 the terminal diagram, and Figure 3 the control schematic; the Appendix contains operational information as well as recommended operating conditions and electrical characteristics.

The counter and scan-selection logic scans the keyboard array using the drive lines (D1 - D11) and the sense lines (S1 - S8). The outputs of the internal five stage scan counter are conditionally encoded by the ALPHA, SHIFT, and CONTROL inputs, Appendix Table A-1, and are used to drive the D1 - D11 output lines high, one at a time. Each D1 - D11 output may drive up to eight keys, which are sampled by the sense-line inputs (S1 - S8). The S1 - S8 inputs are enabled by the internal three stage scan counter.

The control logic interfaces with the CDP1800-series I/O and timing signals to establish timing and status conditions for the CDP1871A.

The TPB input clocks the scan counters, and is also used to reset the data available output ($\overline{DA}$). When a valid keydown condition is detected on a sense line, the control logic inhibits the clock to the scan counters on the next low-to-high transition of TPB, and the $\overline{DA}$ output is set low. The scan-counter outputs (C1 - C8) represent the ASCII and HEX key codes (Appendix Table A-2), and are used to drive the BUS 0 - BUS 7 outputs, which interface directly to the CDP1800-series data bus.

The BUS 0 - BUS 7 outputs, which are normally three-stated, are enabled by decoding the CS inputs during a CPU input instruction. The low-to-high transition of TPB during the input instruction resets the $\overline{DA}$ output high. Once the $\overline{DA}$ output has been reset, it cannot go low again until the present key is released and a new keydown condition is detected. (This arrangement prevents unwanted repeated keycode outputs, which may be caused by fast software routines.)

After the depressed key is released and the debounce delay (determined by R_X, C_X) has occurred, the scan clock inhibit is removed, allowing the scan counters to advance on the following high-to-low transitions of TPB. This condition provides an N-key lockout feature, which prevents the entry of erroneous codes when two or more keys are pressed simultaneously. The first key pressed in the scanning order is recognized, while all other keys pressed are ignored until the first key is released and read by the CPU, at which time the next key pressed in the scanning order is detected.

If the first key remains closed after the CPU reads the data and resets the $\overline{DA}$ output (on the low-to-high transition of the TPB), an auxiliary signal ($\overline{RPT}$) is generated. This signal is available to the CPU, and indicates an auto-repeat condition. The $\overline{RPT}$ output is reset high at the end of the debounce delay after the depressed key is released.

The debounce input (pin 36) provides a terminal connection for an external user-selected RC circuit designed to eliminate detection of a keydown condition caused by keyboard noise. The operation of the debounce circuit is explained below with the aid of Figures 1 and 3.

When a valid keydown is detected, the on chip active-resistor device (R_N) is enabled, and the external capacitor (C_X) is discharged, providing a key closure debounce time of approximately R_NC_X. The discharge of C_X is sensed by the Schmitt trigger inverter, which clocks the $\overline{DA}$ flip-flop (latching the $\overline{DA}$ output low and inhibiting the scan clock). (The $\overline{DA}$ flip-flop is reset by the low-to-high transition of TPB when the CS inputs are enabled.)

When a valid key release is detected, R_N is disabled and C_X begins charging through the external resistor (R_X), providing a key release debounce time of approximately R_XC_X. The change in charge is, again, sensed by the Schmitt trigger inverter, enabling the scan clock to continue on the next high-to-low transitions of TPB, after the current keycode data is read by the CPU.

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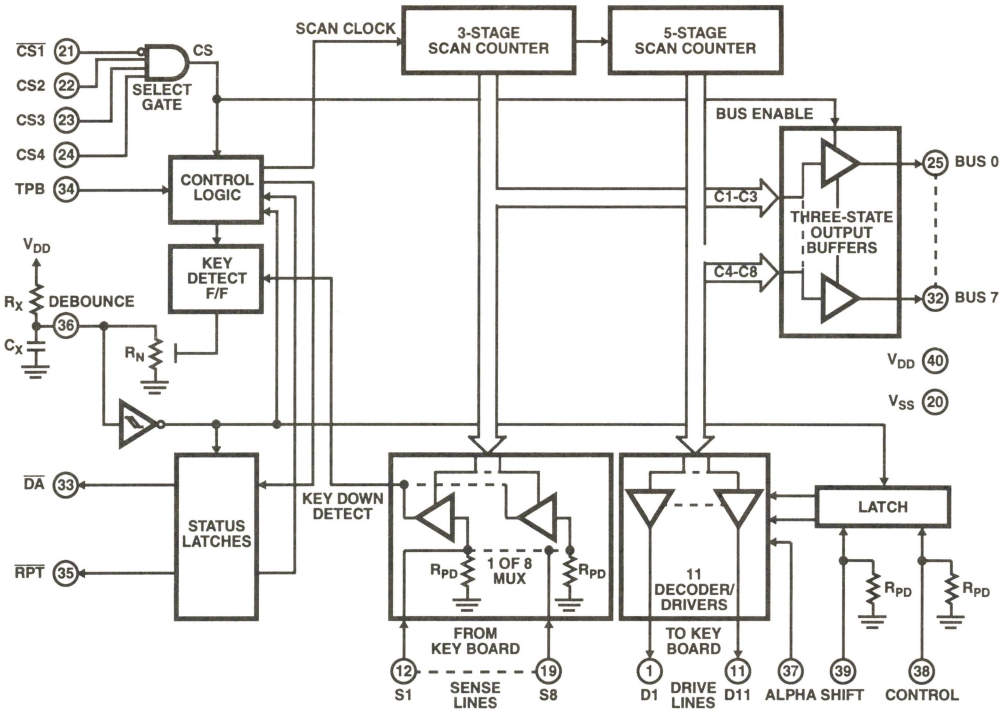


FIGURE 1. BLOCK DIAGRAM OF THE CDP1871A KEYBOARD ENCODER

40 LEAD DIP
TOP VIEW

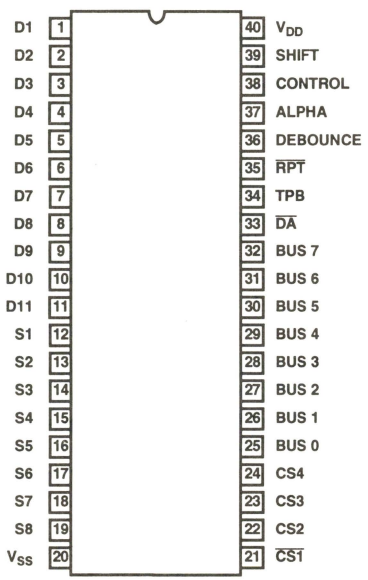


FIGURE 2. TERMINAL DIAGRAM

Functions of Terminals

D1 - D11 (Outputs)

Drive lines for the 11 x 8 keyboard switch matrix. These outputs are connected through the external switch matrix to the sense lines (S1 - S8).

S1 - S8 (Inputs)

Sense lines for the 11 x 8 keyboard matrix. These inputs have internal pull-down resistors, and are driven high by the drive line when a keyboard switch is closed.

$\overline{CS1}$, CS2, CS3, CS4 (Inputs)

Chip-select inputs, which are used to enable the tristate data bus outputs (BUS 0 - BUS 7), and to enable the resetting of the status flag ($\overline{DA}$) on the low-to-high transition of TPB. These four inputs are normally connected to the N-lines (N0 - N2) and $\overline{MRD}$ output of the CDP1800-series microprocessor.

BUS 0 - BUS 7 (Outputs)

Tristate data bus outputs that provide the ASCII and HEX codes of the detected keys. The outputs are normally connected to the BUS 0 - BUS 7 terminals of the CDP1800-series microprocessor.

$\overline{DA}$ (Output)

The data available output flag, which is set low when a valid key closure is detected. It is reset high by the low-to-high transition of TPB when data is read from the CDP1871A. This output is normally connected to a flag input ($\overline{EF1}$ - $\overline{EF4}$) of the CDP1800-series microprocessor.

TPB (Input)

The input clock used to drive the scan generator and reset the status flag ($\overline{DA}$). This input is normally connected to the TPB output of the CDP1800-series microprocessor.

RPT (Output)

The repeat-output flag used to indicate that a key is still closed after data has been read from the CDP1871A ($\overline{DA}$ high). It remains low as long as the key is closed, and is used for an autorepeat function, under CPU control. This output is normally connected to a flag input (EF1 - EF4) of the CDP1800-series microprocessor.

Debounce (Input)

This input is connected to the junction of an external resistor to V_{DD} and an external capacitor to V_{SS}. It provides a debounce time delay (t = RC) after the release of a key. The external pull-up resistor is required under all circumstances.

Alpha, Shift, Control (Inputs)

A high on the shift or control input will be internally latched (after the debounce time), and the drive and sense line decoding will be modified as shown in Appendix Table A-1. These inputs are normally connected to the keyboard, but produce no code by themselves. The shift and control inputs have internal pull-down resistors to simplify use with momentary-contact switches. The alpha input is not latched and is designed to provide an alpha-lock function when used with a standard SPDT switch. When alpha = 1, the drive and sense line decoding will be modified as shown in Appendix Table A-1.

V_{DD}, V_{SS}

V_{DD} is the positive supply voltage input. V_{SS} is the most negative supply voltage terminal, and is normally connected to ground. All outputs swing from V_{SS} to V_{DD}. The recommended input-voltage swing is also from V_{SS} to V_{DD}.

Figure 4 shows a CDP1800-series processor operating in its I/O mapped mode with the keyboard encoder. CDP1800-series processors have fourteen I/O instructions and three dedicated output lines (N0 - N2) that are used for I/O functions. The N lines are toggled when the I/O instructions are used; otherwise, they remain at a low level.

Unlike memory-mapping, when the processor outputs and inputs data, the memory is the source of the system data when the input or output instructions are executed.

For example, an input instruction writes data to the memory and the processor; therefore, the read line remains high while the write line goes low. An output instruction outputs data from the memory. In this case, the read line goes low and the write line remains high.

An important input to the encoder is the TPB signal. This timing signal occurs at the end of the machine cycle of a CDP1800-series processor and is used to clock the encoder's scan counter. It also resets the data available signal when the encoder is selected. It is synchronous in that it must not toggle when the chip is selected and data is being read from the encoder.

The TPB signal is used to strobe data into a peripheral. Note in Figure 4 that the read line is used in addition to the N lines to select the encode; therefore, the only time the encoder will drive the data bus is when the proper input instruction is executed. The encoder is not selected until the N lines are at the required levels and the read line is high. When a key closure is detected by the CDP1871A, the data available signal is activated; the processor is alerted by sensing its EF flag input. The processor then performs an input instruction to capture the key data.

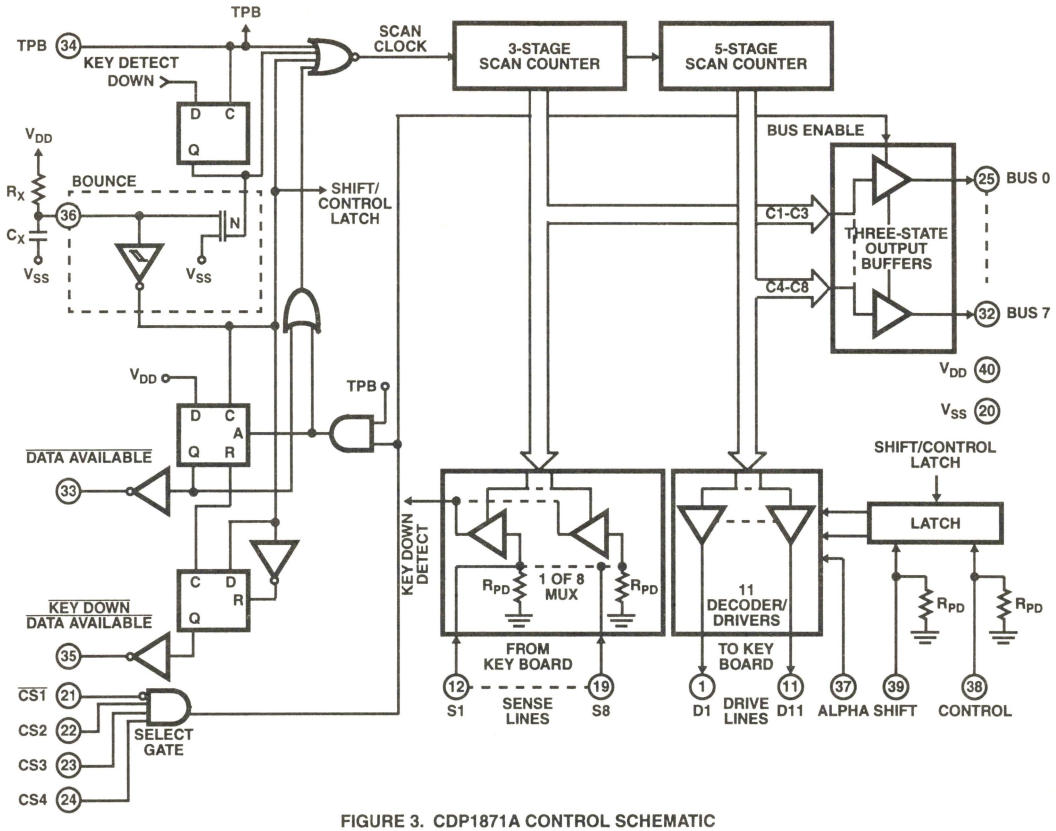


FIGURE 3. CDP1871A CONTROL SCHEMATIC

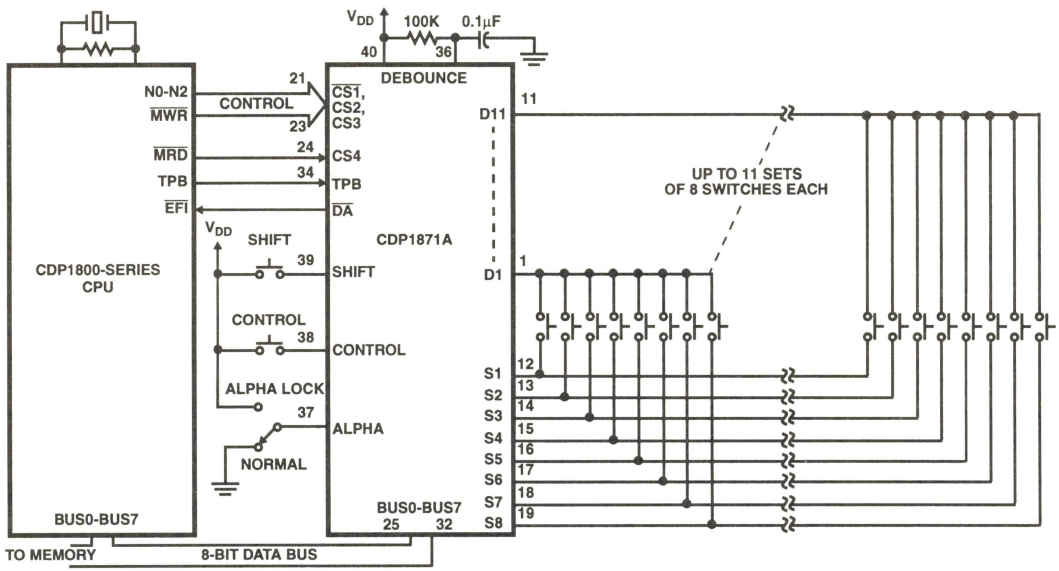


FIGURE 4. TYPICAL CDP1800-SERIES MICROPROCESSOR SYSTEM USING THE CDP1871A

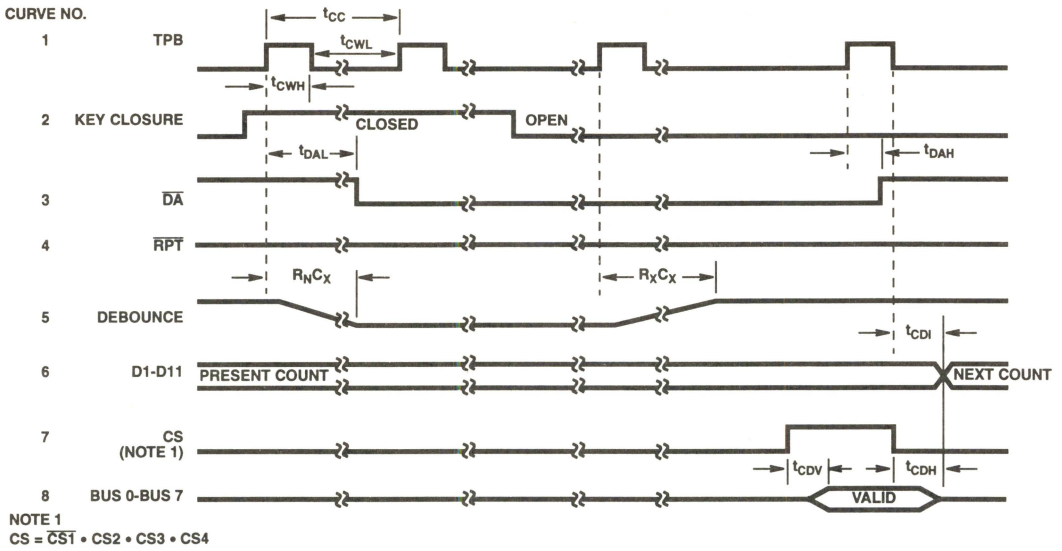


FIGURE 5. CDP1871A DYNAMIC TIMING DIAGRAM (NON-REPEAT)

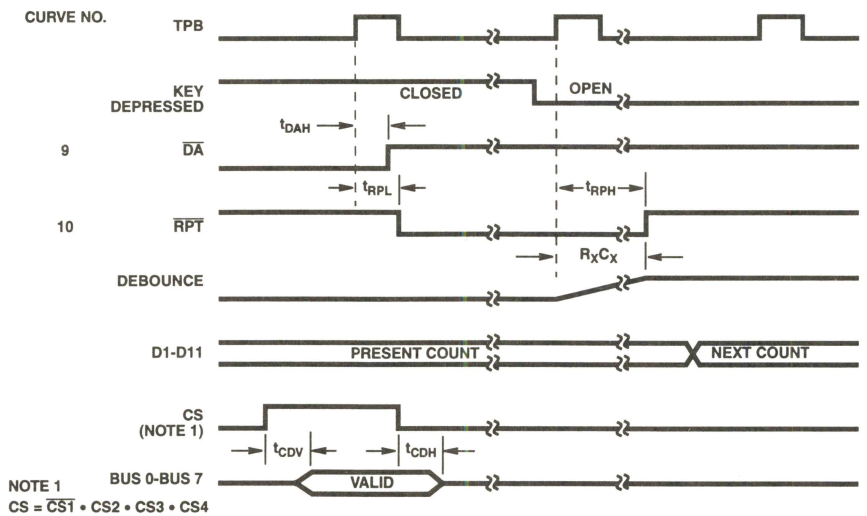


FIGURE 6. CDP1871A DYNAMIC TIMING DIAGRAM (REPEAT)

Dynamic Electrical Characteristics

The dynamic electrical characteristics of the CDP1871A are shown in Table 1, and the timing diagrams in Figure 5. The clock cycle time, the first entry, A, Table 1, and curve 1 in the timing diagram of Figure 5, TPB, define the high and low limits of the clock cycle as $t_{CC} + t_{CWH} + t_{CWL}$. TPB must remain high for at least 100ns (B). The low portion of the clock cycle (t_{CWL}) consists of t_{CD} [1] (E) and the keyboard capacitance. This parameter is selected to allow the TPB clock pulse time to ripple through the scan counters. The maximum frequency of TPB is 400kHz at 5V V_{DD} and 800kHz at 10V V_{DD}.

Table parameters C and D and curve 3 define the data available valid and invalid (reset) delays. The delays are measured from the leading edge of the TPB signal. The valid delay signal is activated on the first TPB signal after the leading edge debounce time when a key closure is detected, and returns high when the encoder is selected on the low-to-high transition of TPB. The valid data out delay and hold times from chip select are shown in table entries F, G and curve 8. The final parameters, H and J, refer to the repeat signal set and reset level delays measured from the leading edge of the TPB; curve 10, Figure 6.

Note in Figure 5 that the action starts when a key closure is sensed by the encoder; curve 2. On the next low-to-high transition of TPB, the debounce time of R_NC_X occurs as C_X discharges through the transistor and the Schmitt trigger clocks the data available flip-flop; curve 3. The R_N value of the transistor is about 200Ω, so that, with an external capacitor of 0.1µF, a 20µs delay can be expected. The key release trailing edge debounce time is calculated from the values of the external capacitor and resistor (R_X, C_X). With a 0.1µF capacitor and a 100kΩ resistor, the debounce time will be 10ms.

Once the data available signal has been reset (chip selected and TPB high), the scan counter operates again on the next trailing edge of TPB, curve 6, and table parameter E. Note in Figure 6 that the repeat signal is activated when the data available signal is reset high while the key is still closed; curves 9 and 10. The repeat signal is reset after the debounce time on the next leading edge of the TPB signal when the key is no longer closed.

TABLE 1. DYNAMIC ELECTRICAL CHARACTERISTICS OF THE CD1871A

PARAMETER			V_{DD} (V)	LIMITS						UNITS
				CDP1871AD CDP1871AE			CDP1871ACD CDP1871ACE			
				MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Clock Cycle Time	A	t_{CC}	5	-	-	-	-	-	-	Note 2
			10	-	-	-	-	-	-	
Clock Pulse Width High	B	t_{CWH}	5	100	40	-	100	40	-	ns
			10	50	20	-	-	-	-	
Data Available Valid Delay	C	t_{DAL}	5	-	260	500	-	260	500	ns
			10	-	130	250	-	-	-	
Data Available Invalid Delay	D	t_{DAH}	5	-	70	150	-	70	150	ns
			10	-	35	75	-	-	-	
Scan Count Delay (Non-Repeat)	E	t_{CD1}	5	-	850	1900	-	850	1900	ns
			10	-	425	950	-	-	-	
Data Out Valid Delay	F	t_{CDV}	5	-	120	250	-	120	250	ns
			10	-	60	125	-	-	-	
Data Out Hold Time	G	t_{CDH}	5	-	100	200	-	100	200	ns
			10	-	50	100	-	-	-	
Repeat Valid Delay	H	t_{RPL}	5	-	150	400	-	150	400	ns
			10	-	75	200	-	-	-	
Repeat Invalid Delay	J	t_{RPM}	5	-	350	700	-	350	700	ns
			10	-	170	350	-	-	-	

NOTES:

1. Typical Values are for T_A = +25°C and Nominal V_{DD}.
2. $t_{CC} = t_{CWH} + t_{CWL}$, $t_{CWL} = t_{CD1} + K$, k = 0.9 per pF of keyboard capacitance.

Use with Other Processors

Although the keyboard encoder has been designed to operate with CDP1800-series processors, it can be used with other processors if certain precautions are followed.

The encoder is designed as an I/O port; it is not intended to operate with its chip selects active at all times. If this feature is desired, connect an external Schmitt trigger to the debounce pin and place a tristate latch on the data bus.

The most likely use of the CDP1871A will be as an I/O port, and the concern here is the synchronization of the TPB input. The TPB must be held high when the chip selects are active to reset the data available signal. If the TPB is allowed to toggle with the chip selected before it is read, it can hold the data available flip-flop in reset continuously, and can clock the scan counter.

Figure 7 shows the encoder connected to a CDP6805 processor. It can interface directly in this arrangement since the DS output from the CDP6805 is similar to the timing of the TPB timing signal of the CDP1800. However, in a 5MHz system, DS occurs every microsecond, too fast for the encoder's requirement of a TPB input less than 400kHz at 5V. If a divider is used to lower the TPB input, synchronization will be lost. A way around this problem is to use a NAND gate in front of the TPB input and to have one of its inputs tied to the active-low chip select; Figure 8. Then, when the CDP1871A is selected, the TPB input will be forced high and TPB will only toggle again after the encoder is read and the chip select signal is again false.

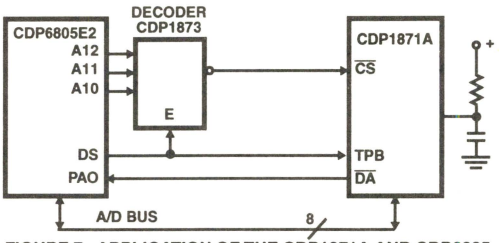


FIGURE 7. APPLICATION OF THE CDP1871A AND CDP6805 PROCESSOR

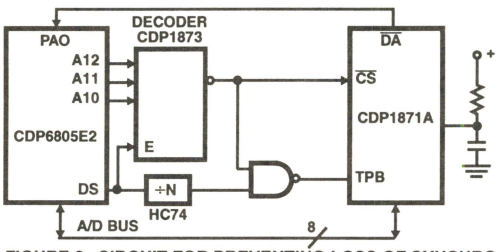


FIGURE 8. CIRCUIT FOR PREVENTING LOSS OF SYNCHRONIZATION IN CDP1871A/CDP6805 INTERFACE

Note that DS enables the decoder, so that during the time that the processor is placing its low address on the data bus, the CDP1871A is disabled. If an asynchronous clock is used for the TPB input, as shown in Figure 9, the NAND gate can be used to assure that TPB remains high during the CDP1871A select times.

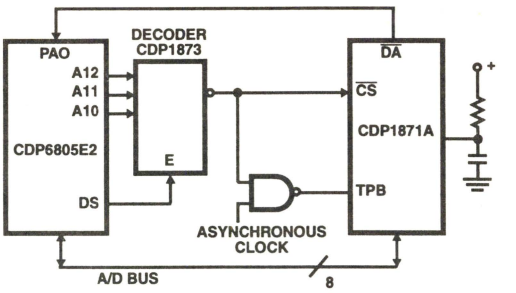


FIGURE 9. METHOD OF ASSURING THAT TPB REMAINS HIGH DURING CDP1871A SELECT TIMES

The keyboard encoder can be used to advantage with another popular processor, the 8085. Figure 10 shows a circuit that interfaces the two devices with an OR gate and a NAND gate. In this circuit, the only time the encoder can drive the data bus is when it is selected and the read signal is active. Since there is no DS equivalent in the 8085 processor, the additional device shown in the figure is needed.

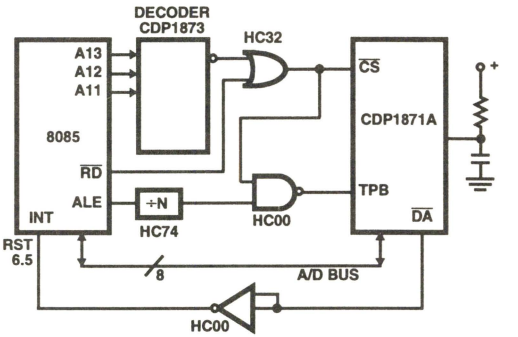


FIGURE 10. A CDP1871A/8085 INTERFACE EMPLOYING AN OR AND A NAND GATE

Figure 11 shows the encoder connected to the 6502 processor. The timing for this part is similar to that for the CDP6805, and the same concerns apply.

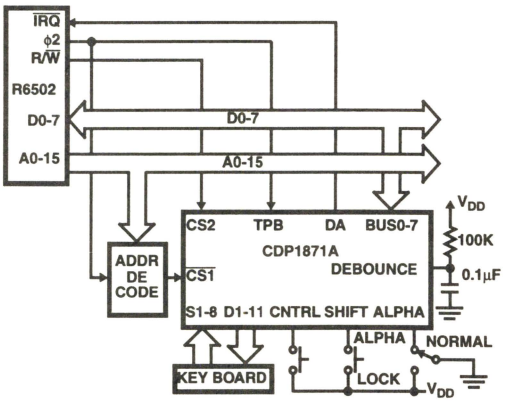


FIGURE 11. A CDP1871A/R6502 INTERFACE

Reference

[1] CMOS Keyboard Encoder, CD1871A," Harris Semiconductor File No. 1374. (The CDP1871A comes in two versions: CDP1871A and CDP1871AC. The two are identical except for recommended operating voltage range: 4V to 10.5V for the A version, and 4V to 6.5V for the AC version.)

Appendix

TABLE A-1. DRIVE AND SENSE LINE KEYBOARD CONNECTIONS (NOTE 1)

SENSE LINES	DRIVE LINES															
	D1		D2		D3		D4		D5		D6		D7	(NOTE 2) D8	(NOTE 2) D9	(NOTE 2) D10	(NOTE 2) D11
S1	SP	0	(	8	‘	@	H	H	P	P	X	X	Space	80_{16}	88_{16}	90_{16}	98_{16}
	0		8		@	NUL	h	BS	p	DLE	x	CAN					
S2	!	1	)	9	A	A	I	I	Q	Q	Y	Y		81_{16}	89_{16}	91_{16}	99_{16}
	1		9		a	SOH	i	HT	q	DC1	y	EM					
S3	“	2	*	:	B	B	J	J	R	R	Z	Z	Line Feed	82_{16}	$8A_{16}$	92_{16}	$9A_{16}$
	2		:		b	STX	j	LF	r	DC2	z	SUB					
S4	#	3	+	;	C	C	K	K	S	S	{	[	Escape	83_{16}	$8B_{16}$	93_{16}	$9B_{16}$
	3		;		c	ETX	k	VT	s	DC3	[	ESC					
S5	$	4	<	,	D	D	L	L	T	T	¦	\		84_{16}	$8C_{16}$	94_{16}	$9C_{16}$
	4		,		d	EOT	l	FF	t	DC4	\	FS					
S6	%	5	=	-	E	E	M	M	U	U	}	]	Carriage Return	85_{16}	$8D_{16}$	95_{16}	$9D_{16}$
	5		-		e	ENQ	m	CR	u	NAK	]	GS					
S7	&	6	>	.	F	F	N	N	V	V	~	↑		86_{16}	$8E_{16}$	96_{16}	$9E_{16}$
	6		.		f	ACK	n	SO	v	SYN	↑	RS					
S8	‘	7	?	/	G	G	O	O	W	W	DEL	–	Delete	87_{16}	$8F_{16}$	97_{16}	$9F_{16}$
	7		/		g	BEL	o	SI	w	ETB	–	US					

KEY:

SHIFT*	ALPHA*
NORMAL	CONTROL*

* CONTROL Overrides SHIFT and ALPHA

= No Response

NOTES:

1. Showing ASCII outputs for all combinations with and without SHIFT, ALPHA LOCK and CONTROL.
2. Drive lines 8, 9, 10 and 11 generate non-ASCII hex values which can be used for special codes.

TABLE A-2. HEXADECIMAL VALUES OF ASCII CHARACTERS

	BITS				b7 → b6 → b5 →	MSD							
						0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	b4	b3	b2	b1	HEX ↓	0	1	2	3	4	5	6	7
LSD	0	0	0	0	0	NUL	DLE	SP	0	@	P	\	p
	0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
	0	0	1	0	2	STX	DC2	"	2	B	R	b	r
	0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
	0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
	0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
	0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
	0	1	1	1	7	BEL	ETB	/	7	G	W	g	w
	1	0	0	0	8	BS	CAN	(	8	H	X	h	x
	1	0	0	1	9	HT	EM	)	9	I	Y	i	y
	1	0	1	0	A	LF	SUB	*	:	J	Z	j	z
	1	0	1	1	B	VT	ESC	+	;	K	[	k	{
	1	1	0	0	C	FF	FS	,	<	L	\	l	¦
	1	1	0	1	D	CR	GS	-	=	M	]	m	}
	1	1	1	0	E	SO	RS	.	>	N	↑	n	~
	1	1	1	1	F	SI	US	/	?	O	–	o	DEL

TABLE A-3. RECOMMENDED OPERATING CONDITIONS AT T_A = -40°C TO +85°C

For Maximum Reliability, Operating Conditions should be selected so that operation is always within the following ranges:

PARAMETER		V_{DD} (V)	LIMITS				UNITS
			CDP1871AD CDP1871AE		(NOTE 1) CDP1871ACD CDP1871ACE		
			MIN	MAX	MIN	MAX	
Supply Voltage Range		-	4	10.5	4	6.5	V
Recommended Input Voltage Range		-	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Clock Input Frequency, TPB (Keyboard Capacitance = 200pF)	f_{CL}	5	DC	0.4	DC	0.4	MHz
		10	DC	0.8	-	-	

NOTE:

1. D in suffix indicates ceramic package; E indicates plastic package.

TABLE A-4. STATIC ELECTRICAL CHARACTERISTICS at T_A = -40°C to +85°C, Except as Noted

PARAMETER	SYMBOL	CONDITIONS			LIMITS						UNITS
					CDP1871AD CDP1871AE			CDP1871ACD CDP1871ACE			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	0.1	50	-	1	200	µA
		-	0, 10	10	-	1	200	-	-	-	
Output Low Drive (Sink) Current (except debounce and D1 - D11)	I_{OL}	0.4	0, 5	5	0.5	1	-	0.5	1	-	mA
		0.5	0, 10	10	1	2	-	-	-	-	
Debounce	I_{OL}	0.4	0, 5	5	0.75	1.5	-	0.75	1.5	-	
		0.5	0, 10	10	1	2	-	-	-	-	
D1 - D11	I_{OL}	0.4	0, 5	5	.05	0.1	-	.05	0.1	-	
		0.5	0, 10	10	0.1	0.2	-	-	-	-	
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-0.3	-0.6	-	-0.3	-0.6	-	
		9.5	0, 10	10	-0.75	-1.5	-	-	-	-	
Input Low Voltage (Except Debounce)	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		1, 9	-	10	-	-	3	-	-	-	
Input High Voltage (Except Debounce)	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	
		1, 9	-	10	7	-	-	-	-	-	
Debounce Schmitt Trigger Input Voltage											
Positive Trigger Voltage	V_D	0.4	-	5	2.0	3.3	4.0	2.0	3.3	4.0	
		0.5	-	10	4.0	6.3	8.0	-	-	-	
Negative Trigger Voltage	V_N	0.4	-	5	0.8	1.8	3.0	0.8	1.8	3.0	
		0.5	-	10	1.9	4.0	6.0	-	-	-	
Hysteresis	V_H	0.4	0, 5	5	0.3	1.6	2.6	0.3	1.6	2.6	
		0.5	0, 10	10	0.7	2.3	4.7	-	-	-	
Output Voltage Low Level	V_{OL}	-	0, 5	5	-	0	0.05	-	0	0.05	
		-	0, 10	10	-	0	0.05	-	-	-	
Output Voltage High Level	V_{OH}	-	0, 5	5	4.95	5	-	4.95	5	-	
		-	0, 10	10	9.95	10	-	-	-	-	
Input Leakage Current (Except S1 - S8, Shift, Control)	I_{IN}	-	0, 5	5	-	0.01	1	-	0.01	1	µA
		-	0, 10	10	-	0.01	1	-	-	-	
Three-State Output Leakage Current	I_{OUT}	0.5	0, 5	5	-	0.01	1	-	0.02	2	
		0, 10	0, 10	10	-	0.02	2	-	-	-	
Pull-Down Resistor Value (S1 - S8, Shift, Control)	R_{PD}	-	-	-	7	14	24	7	14	24	kΩ
Operating Current (All outputs unloaded)	I_{OPER}	0.5, 4.5	0, 5	5	-	0.6	-	-	0.6	-	mA
f_{CL} = 0.4MHz											
f_{CL} = 0.8MHz		1, 9	0, 10	10	-	2.7	-	-	-	-	

NOTE:

1. Typical values are for T_A = +25°C and nominal V_{DD}.

MICROPROCESSOR PRODUCTS 8

HARRIS QUALITY AND RELIABILITY

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Harris Quality

Introduction

Success in the integrated circuit industry means more than simply meeting or exceeding the demands of today's market. It also includes anticipating and accepting the challenges of the future. It results from a process of continuing improvement and evolution, with perfection as the constant goal.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force – from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of the Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. In addition to facilitating the development of SPC and DOX, Quality professionals support other continuous improvement tools such as control charts, measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs – with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress.

The Improvement Process

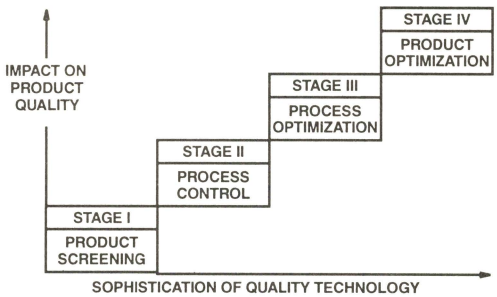


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage III to Stage IV, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

ISO 9000 Certification

The manufacturing operations of Harris Semiconductor have all received ISO certification. The ISO 9000 series of standards were very consistent with our goals to build an even stronger quality system foundation.

Qualified Manufacturing List (QML)

Harris Semiconductor has supplied military grade integrated circuits for over 20 years. The government's certifying body had audited and granted approval to ship JAN, 883 compliant, and Source Military Drawing parts used in ground and space applications. The discipline required to manufacture high reliability components has been beneficial to the commercial product lines. Harris has now taken the next evolutionary step by transitioning into QML as defined in MIL-PRF-38535. These guidelines incorporate the best commercial practices for semiconductor manufacturing.

Designing for Manufacturability

Assuring quality and reliability in integrated circuits begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS

AREA	CONTROLS/MONITORS
Wafer Fab	• Internal Audits • Environmental - Room/Hood Particulates - Temperature/Humidity - Water Quality • Product - Junction Depth - Sheet Resistivities - Defect Density - Critical Dimensions - Visual Inspection - Lot Acceptance • Process - Film Thickness - Implant Dosages - Capacitance Voltage Changes - Conformance to Specification • Equipment - Repeatability - Profiles - Calibration - Preventive Maintenance
Assembly	• Internal Audits • Environmental - Room/Hood Particulates - Temperature/Humidity - Water Quality • Product - Documentation Check - Dice Inspection - Wire Bond Pull Strength/Controls - Ball Bond Shear/Controls - Die Shear Controls - Post-Bond/Pre-Seal Visual - Fine/Gross Leak - PIND Test - Lead Finish Visuals, Thickness - Solderability • Process - Operator Quality Performance - Saw Controls - Die Attach Temperatures - Seal Parameters - Seal Temperature Profile - Sta-Bake Profile - Temp Cycle Chamber Temperature - ESD Protection - Plating Bath Controls - Mold Parameters

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS (Continued)

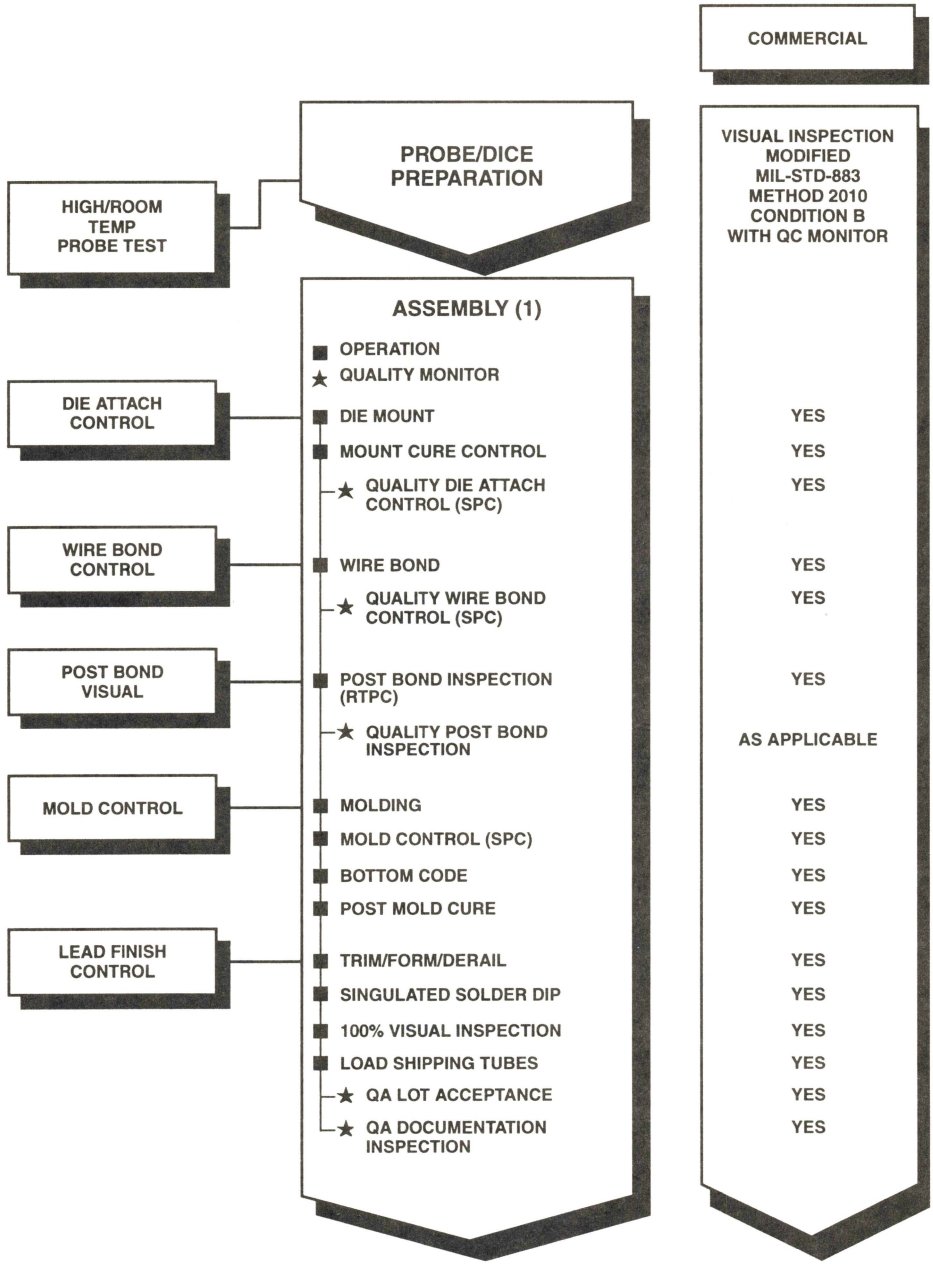
AREA	CONTROLS/MONITORS
Test	• Internal Audits • Temperature/Humidity • ESD Controls • Temperature Test Calibration • Test System Calibration • Test Procedures • Control Unit Compliance • Lot Acceptance Conformance • Group A Lot Acceptance
Probe	• Internal Audits • Wafer Repeat Correlation • Visual Requirements • Documentation • Process Performance
Burn-In	• Internal Audits • Functionality Board Check • Oven Temperature Controls • Procedural Conformance
Brand	• Internal Audits • ESD Controls • Brand Permanency • Temperature/Humidity • Procedural Conformance
QCI Inspection	• Internal Audits • Group B Conformance • Group C and D Conformance

Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

The validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment

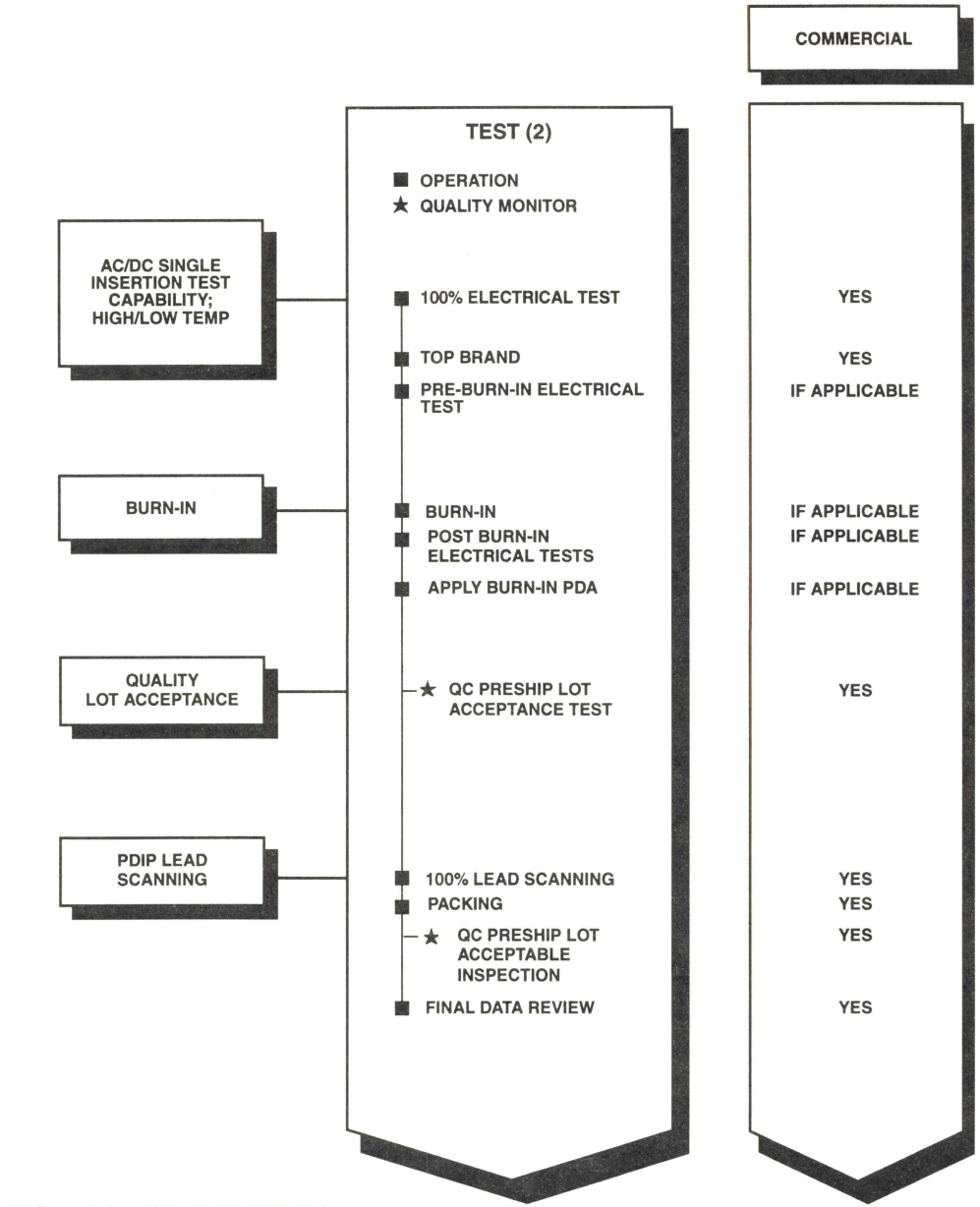
Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs (see Table 2).



(1) Example for a PDIP Package Part

FIGURE 2.

Harris Semiconductor Standard Processing Flow



(2) Example for a Linear Part in PDIP Package

FIGURE 3.

TABLE 2. SUMMARIZING CONTROL APPLICATIONS

FAB			
• Diffusion - Junction Depth - Sheet Resistivities - Oxide Thickness - Implant Dose Calibration - Uniformity	• Thin Film - Film Thickness - Uniformity - Refractive Index - Film Composition - Particles Added	• Photo Resist - Critical Dimension - Resist Thickness - Etch Rates - Energy Monitor (E_O)	• Measurement Equipment - Critical Dimension - Film Thickness - Resistivity
ASSEMBLY			
• Pre-Seal - Die Prep Visuals - Yields - Die Attach Heater Block - Die Shear - Wire Pull - Ball Bond Shear - Saw Blade Wear - Pre-Cap Visuals	• Post-Seal - Internal Package Moisture - Tin Plate Thickness - PIND Defect Rate - Solder Thickness - Leak Tests - Module Rm. Solder Pot Temp. - Seal - Temperature Cycle	• Measurement - XRF - Radiation Counter - Thermocouples - GM-Force Measurement	
TEST			
	- Handlers/Test System - Defect Pareto Charts - Lot % Defective - ESD Failures per Month	- Monitor Failures - Lead Strengthening Quality - After Burn-In PDA	
OTHER			
• IQC - Vendor Performance - Material Criteria - Quality Levels	• Environment - Water Quality - Clean Room Control - Temperature - Humidity	• IQC Measurement/Analysis - XRF - ADE - 4 Point Probe - Chemical Analysis Equipment	

Special Testing

Harris Semiconductor offers several standard screen flows to support a customer's need for additional testing and reliability assurance. These flows include environmental stress testing, burn-in, and electrical testing at temperatures other than +25°C. The flow shown in Figure 2 and Figure 3 indicates the Harris standard processing flow for a commercial linear part in a PDIP package. In addition, Harris can supply products tested to customer specifications both for electrical requirements and for nonstandard environmental stress screening. Consult your field sales representative for details.

TABLE 3. HARRIS I.C. DESIGN TOOLS

DESIGN STEP	PRODUCTS	
	ANALOG	DIGITAL
Functional Simulation	Cds Spice	Cds Spice Verilog
Parametric Simulation	Cds Spice Monte Carlo	Cds Spice
Schematic Capture	Cadence	Cadence
Functional Checking	Cadence	Cadence
Rules Checking	Cadence	Cadence
Parasitic Extraction	Cadence	Cadence

Controlling and Improving the Manufacturing Process - SPC/DOX

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use control charts to determine the normal variabilities in processes, materials, and products. Critical process variables and performance characteristics are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that an operation is outside the process control limits or indicates a nonrandom pattern inside the limits. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. Table 3 lists some typical manufacturing applications of control charts at Harris Semiconductor.

SPC is important, but still considered only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost (see Table 4).

TABLE 4. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

STAGE		APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at upgrading process performance by studying the key variables controlling the process, and optimizing the procedures or design to yield the best result. This approach is a more time-consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in ANSI/ASQC Z1.4, MIL-STD-883 and MIL-PRF-38535 are used by our quality inspectors.

The focus on this quality parameter has resulted in a continuous improvement to less than 100 PPM, and the goal is to continue improvement toward 0 PPM.

Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of Harris statisticians, private consultants, and internally developed programs, training of engineers, facilitators, and operators/technicians has been an ongoing activity in Harris Semiconductor.

Over the past years, Harris has also deployed a comprehensive training program for hourly operators and facilitators in job requirements and functional skills. All hourly manufacturing employees participate (see Table 5).

Incoming Materials

Improving the quality and reducing the variability of critical incoming materials is essential to product quality enhancement, yield improvement, and cost control. With the use of statistical techniques, the influence of silicon, chemicals, gases and other materials on manufacturing is highly measurable. Current measurements indicate that results are best achieved when materials feeding a statistically controlled manufacturing line have also been produced by statistically controlled vendor processes.

To assure optimum quality of all incoming materials, Harris has initiated an aggressive program, linking key suppliers with our manufacturing lines. This user-supplier network is the Harris Vendor Certification process by which strategic vendors, who have performance histories of the highest quality, participate with Harris in a lined network; the vendor's factory acts as if it were a beginning of the Harris production line.

SPC seminars, development of open working relationships, understanding of Harris's manufacturing needs and vendor capabilities, and continual improvement programs are all part of the certification process. The sole use of engineering limits no longer is the only quantitative requirement of incoming materials. Specified requirements include centered means, statistical control limits, and the requirement that vendors deliver their products from their own statistically evaluated, in-control manufacturing processes.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors who must meet rigorous incoming inspection criteria (see Table 6).

TABLE 5. SUMMARY OF TRAINING PROGRAMS

COURSE	AUDIENCE	TOPICS COVERED
SPC, Basic	Manufacturing Operators, Non-Manufacturing Personnel	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts
SPC, Intermediate	Manufacturing Supervisors, Technicians	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Introduction to Capability
SPC, Advanced	Manufacturing Engineers, Manufacturing Managers	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Advanced Control Charts, Variance Component Analysis, Capability Analysis
Design of Experiments (DOX)	Engineers, Managers	Factorial and Fractional Designs, Blocking Designs, Nested Models, Analysis of Variance, Normal Probability Plots, Statistical Intervals, Variance Component Analysis, Multiple Comparison Procedures, Hypothesis Testing, Model Assumptions/Diagnostics
Regression	Engineers, Managers	Simple Linear Regression, Multiple Regression, Coefficient Interval Estimation, Diagnostic Tools, Variable Selection Techniques
Response Surface Methods (RSM)	Engineers, Managers	Steepest Ascent Methods, Second Order Models, Central Composite Designs, Contour Plots, Box-Behnken Designs
Capability Studies	Techs, Facilitators, Engineers	Capability Indices (C_P and C_{PK}), Variance Components, Nested Models, Fixed and Random Effects

TABLE 6. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

MATERIAL	INCOMING INSPECTIONS	VENDOR DATA REQUIREMENTS
Silicon	• Resistivity • Crystal Orientation • Dimensions • Edge Conditions • Taper • Thickness • Total Thickness Variation • Backside Criteria • Oxygen • Carbon	• Equipment Capability Control Charts - Oxygen - Resistivity • Control Charts Related to - Enhanced Gettering - Total Thickness Variation - Total Indicated Reading - Particulates • Certificate of Analysis for all Critical Parameters • Control Charts from On-Line Processing • Certificate of Conformance
Chemicals/Photoresists/ Gases	• Chemicals - Assay - Major Contaminants • Molding Compounds - Spiral Flow - Thermal Characteristics • Gases - Impurities • Photoresists - Viscosity - Film Thickness - Solids - Pinholes	• Certificate of Analysis on all Critical Parameters • Certificate of Conformance • Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Water - Selected Parameters • Control Charts - Assay - Contaminants • Control Charts on - Photospeed - Thickness - UV Absorbency - Filterability - Water - Contaminants
Thin Film Materials	• Assay • Selected Contaminants	• Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Dimensional Characteristics • Certificate of Analysis for all Critical Parameters • Certificate of Conformance
Assembly Materials	• Visual Inspection • Physical Dimension Checks • Glass Composition • Bondability • Intermetallic Layer Adhesion • Ionic Contaminants • Thermal Characteristics • Lead Coplanarity • Plating Thickness • Hermeticity	• Certificate of Analysis • Certificate of Conformance • Process Control Charts on Outgoing Product Checks and In-Line Process Controls

Calibration Laboratory

Another important resource in the product assurance system is a calibration lab in each Harris Semiconductor operation site. These labs are responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both production and engineering areas. The accuracy of instruments used at Harris is traceable to a national standards. Each lab maintains a system which conforms to the current revision of ANSI/NCSL Z540-1.

Each instrument requiring calibration is assigned a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Manufacturing Science - CAM, JIT, TPM

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened - in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

Just In Time (JIT)

The major focus of JIT is cycle time reduction and linear production. Significant improvements in these areas result in large benefits to the customer. JIT is a part of the Total Quality Management philosophy at Harris and includes Employee Involvement, Total Quality Control, and the total elimination of waste.

Some key JIT methods used for improvement are sequence of events analysis for the elimination of non-value added activities, demand/pull to improve production flow, TQC check points and Employee Involvement Teams using root cause analysis for problem solving.

JIT implementations at Harris Semiconductor have resulted in significant improvements in cycle time and linearity. The benefits from these improvements are better on time delivery, improved yield, and a more cost effective operation.

JIT, SPC, and TPM are complementary methodologies and used in conjunction with each other create a very powerful force for manufacturing improvement.

Total Productive Maintenance (TPM)

TPM or Total Productive Maintenance is a specific methodology which utilizes a definite set of principles and tools focusing on the improvement of equipment utilization. It focuses on the total elimination of the six major losses which are equipment failures, setup and adjustment, idling and minor stoppages, reduced speed, process defects, and reduced yield. A key measure of progress within TPM is the overall equipment effectiveness which indicates what percentage of the time is a particular equipment producing good parts. The basic TPM principles focus on maximum equipment utilization, autonomous maintenance, cross functional team involvement, and zero defects. There are some key tools within the TPM technical set which have proven to be very powerful to solve long standing problems. They are initial clean, P-M analysis, condition based maintenance, and quality maintenance.

Utilization of TPM has shown significant increases in utilization on many tools across the Sector and is rapidly becoming widespread and recognized as a very valuable tool to improve manufacturing competitiveness.

The major benefits of TPM are capital avoidance, reduced costs, increased capability, and increased quality. It is also very compatible with SPC techniques since SPC is a good stepping stone to TPM implementation and it is in turn a good stepping stone to JIT because a high overall equipment effectiveness guarantees the equipment to be available and operational at the right time as demanded by JIT.

Harris Reliability

Introduction

At Harris Semiconductor, reliability is built into every product by emphasizing quality throughout manufacturing. This starts by ensuring the excellence of the design, layout, and manufacturing processes. The quality of the raw materials and workmanship is monitored using statistical process control (SPC) to preserve the reliability of the product. The primary and ultimate goal of these efforts is to provide full performance to the product specification throughout its useful life.

Reliability Engineering

The Reliability Engineering department is responsible for all aspects of reliability assurance at Harris Semiconductor:

- Charter
  - To ensure that Harris is recognized by our customers and competitors as a company that consistently delivers products with high reliability.

- Mission
  - To develop systems for assessing, enhancing, and assuring that quality and reliability are integrated into all aspects of our business.

- Vision
  - To establish excellence and integrity through all design and manufacturing processes as it relates to quality and reliability.

Values

- To be considered responsive and service oriented by our customers.
- To be acknowledged by Harris as a highly qualified resource for reliability assurance, product analysis, and electronic materials characterization.
- To successfully utilize the organization's talents through trained, empowered employees/employee team participation.
- To maintain an attitude of integrity, dignity and respect for all.

Strategy

- To provide quantitative assessments of product reliability focusing on the identification and timely elimination of design and processing deficiencies that degrade product performance and operating life expectancy.
- To provide systems for continuous improvement of reliability and quality through the assessment of existing processes, products, and packages.
- To perform product analysis as a means of problem solving and feedback to our customers, both internal and external.
- To exercise full authority over the internal qualifications of new products, processes, and packages.

The reliability organization is comprised of a team that possesses a broad cross section of expertise in these areas:

- Custom Military (Radiation Hardened)
- Automotive ASICs
- Harsh Environment Plastic Packaging
- Advanced Methods for Design for Reliability (DFR)
- Strength in Power Semiconductor
- Chemical/Surface Analysis Capabilities
- Failure Analysis Capabilities

The reliability focus is customer satisfaction (external and internal) and is accomplished through the development of standards, performance metrics, and service systems. These major systems are summarized below:

- A process and product development system known as ACT PTM (Applying Concurrent Teams to Product-To-Market) has been established. The ACT PTM philosophy is one of new product development through a team that pursues customer involvement. The team has the authority, responsibility, and training necessary to successfully bring the product to market. This not only includes product definition and design, but also all manufacturing capabilities as well.
- Standard test vehicles (over 100) have been developed for process characterization of wear-out failure mechanisms. These vehicles are used for conventional stresses (for modeling failure rates) and for wafer level reliability characterization during development.
- Common qualification standards have been established for all sites.
- A reliability monitoring system (also known as the Matrix monitoring system) is utilized for products in production to ensure ongoing reliability and verification of continuous improvement.
- The field return system is designed to handle a variety of customer issues in a timely manner. Product issues are often handled by routing the product into the PFAST (Product Failure Analysis Solution Team) system. Return authorizations (RAs) are issued where an entire lot of product needs to be returned to Harris. The Customer Return Services (CRS) group is responsible for the administration of this system (see Customer Return Services.)
- The PFAST system has been established to expedite failure analysis, failure root cause determination, and corrective actions for field returns. PFAST is a team effort involving many functional areas at all Harris sites. The purpose of this system is to enable Harris's Field Sales and Quality operations to properly route, track, and respond to our customer's needs as they relate to product analysis.

Design for Reliability (Wear-Out Characterization)

The concept of "Design for Reliability" focuses on moving reliability assessment away from tests on sample product to a point much earlier in the design cycle. Effort is directed at building in and verifying the reliability of a new process well before manufacture of the first shippable product that uses that technology. This gives these first new products a higher probability of success and achieves reduced product-to-market cycle times.

In practice, a set of standardized test vehicles containing special test structures are transferred to the new process using the layout ground rules specified for that process. Each test structure is designed for a specific wear-out failure mechanism. Highly accelerated stress tests are performed on these structures and the results can be extrapolated to customer use conditions. Generally, log-normal statistics are used to define wear-out distributions for the life prediction models. The results are used to establish reliability design ground rules and critical node lists for each process. These ground rules and critical nodes ensure that wear-out failures do not occur during the customer's projected use of the product.

Process/Product/Package Qualifications

Once the new process has successfully completed wear-out characterization, the final qualification consists of more conventional testing (e.g. biased life, storage life, temp cycle etc.). These tests are performed on the first new product designs (sampled across multiple wafer production lots). Successful completion of the final qualification tests concurrently qualifies the new process and the new products that were used in the qualification. Subsequent products designed within the now-established ground rules are qualified individually prior to introduction. New package configurations are also qualified individually prior to being available for use with new products.

Harris's qualification procedures are specified via controlled documentation and the same standard is used at Harris's sites worldwide. Figure 4 gives more information on the new process/product development and life cycle.

Product/Package Reliability Monitors

Many of the accelerated stress-tests used during initial reliability qualification are also employed during the routine monitoring of standard product. Harris's continuing reliability monitoring program consists of three groups of stress tests, labeled Matrix I, II and III. Table 6 outlines the Matrix tests used to monitor plastic packaged ICs in Harris's off-shore assembly plants, where each wafer fab technology is sampled. Matrix I consists of highly accelerated, short duration (typically 48 hours) tests, sampled biweekly, which provide real-time feedback on product reliability. Matrix II consists of the more conventional, longer term stress-tests, sampled monthly, which are similar to those used for product qualification. Finally, Matrix III, performed monthly on each package style, monitors the mechanical reliability aspects of the package. Any failures occurring on the Matrix monitors are fully analyzed and the failure mechanisms identified, with containment and corrective actions obtained from Manufacturing and Engineering. This information along with all of the test results are routinely transmitted to a central data base in Reliability Engineering, where failure rate trends are analyzed and tracked on an ongoing basis. These data are used to drive product improvements, to ensure that failure rates are continuously being reduced over time.

Reliability data, including the Matrix Monitor results, can be obtained by contacting your local Harris sales office.

TABLE 7. PLASTIC PACKAGED IC MONITORING TESTS

MATRIX I

TEST	CONDITIONS	DURATION	SAMPLE/ LTPD
Autoclave	+121°C, 100%RH, 15PSIG	96 Hours	45/5
Biased Life	+175°C	48 Hours	45/5
Biased Life	+125°C	48 Hours	45/5
HAST	+135°C, 85% RH	48 Hours	45/5
Thermal Shock	-65°C to +150°C	200 Cycles	45/5

MATRIX II

TEST	CONDITIONS	DURATION	SAMPLE/ LTPD
Autoclave	+121°C, 100%RH, 15PSIG	192 Hours	45/5
Biased Humidity	+85°C, 85% RH	1000 Hours	45/5
Biased Life	+125°C	1000 Hours	45/5
Dynamic Life	+125°C	1000 Hours	45/5
Storage Life	+150°C	1000 Hours	45/5
Temp. Cycle	-65°C to +150°C	1000 Cycles	45/5

MATRIX III

TEST	CONDITIONS	SAMPLE/LTPD
Brand Adhesion	MIL-STD-883/2015	15/15
Flammability	(UL-94 Vertical Burn)	11/20
Lead Fatigue	MIL-STD-883/2004	15/15
Physical Dimensions	MIL-STD-883/2016	11/20
Solderability	MIL-STD-883/2003	45/15

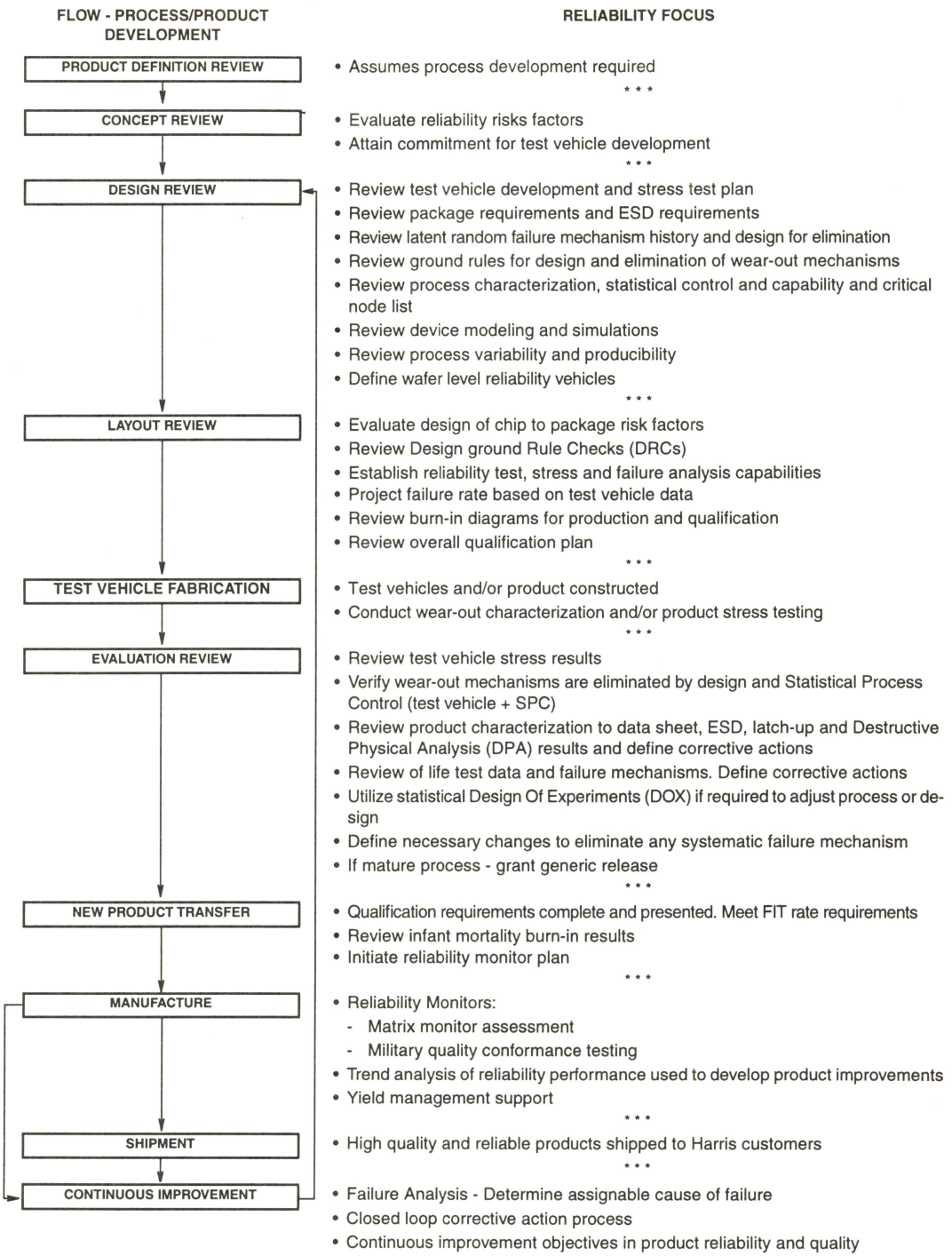


FIGURE 4. NEW PROCESS/PRODUCT DEVELOPMENT AND LIFE CYCLE

Customer Return Services

Harris places a high priority on resolving customer return issues. The Customer Return Services (CRS) department is responsible for determining the best manner to handle a return issue as illustrated in Figure 5.

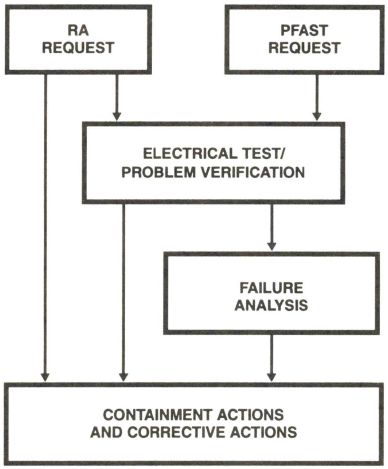


FIGURE 5. GENERAL RETURN FLOW

The diversity of return reasons requires that many different organizations be involved to test, analyze, and correct field return issues. The CRS group coordinates the responses from the supporting organizations to drive closure of issues within the customer response time requirements, see Table 7. The results from the work performed on customer returns are used to initiate corrective actions and continuous improvements within the factories.

The two methods used to return devices are by a RA (Return Authorization) request or by a PFAST (Product Failure Analysis Solution Team) request. The main difference between RA and PFAST is that the PFAST requests often require extensive analysis and a more formal response to the customer. All returns follow the same general procedure from the customer's perspective as seen in steps one to four of the customer return procedure.

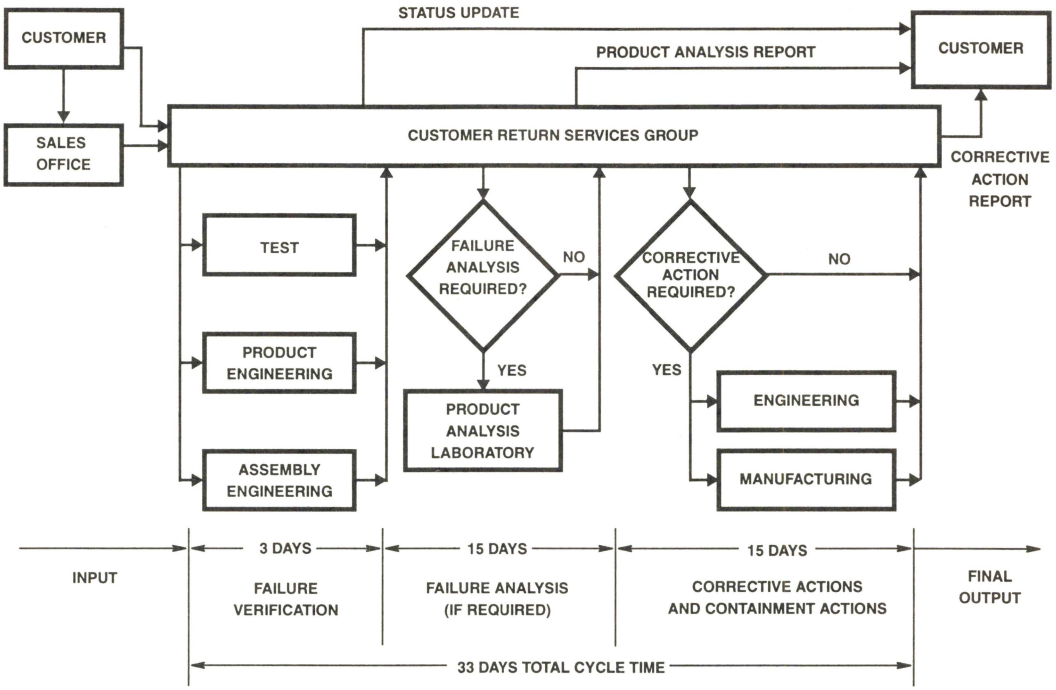
- **Step 1** - Customer or Sales office contacts the Customer Return Services department. If a return is to be routed into the PFAST system, then a PFAST Action Request (see the PFAST form in this section) needs to be completed to understand the customer's issue and direct the analysis efforts.
  - **Phone Number: (407)-724-7400**
  - **FAX Number: (407)-724-7658**
  - **Internet: creturn@huey.mis.semi.harris.com**
  - **PROFS: CRETURN**
- **Step 2** - The Customer Return Services department notifies all affected sales, factory, and engineering organizations of the issue.
- **Step 3** - When product is received, the issue is verified and any required analysis is performed. Where applicable, a preliminary analysis report is sent to the customer.
- **Step 4** - A determination of the root cause of failure initiates the corrective actions to address the source of the problem. A final corrective action report is sent to the customer if requested.

The RA request is used to return and replace an entire lot of product. The lot is returned to Harris for replacement or credit. Once the product is received various tests and evaluations will be performed to determine the appropriate actions that should be taken to resolve any problems or issues.

A PFAST request is used to return a small sample for analysis of a problem. The ultimate outcome of both types of requests is to determine corrective actions that would preclude the same problem occurring in the future. Where appropriate, a containment plan is also implemented to prevent a re-occurrence of the problem in the field. The customer return flow diagram (Figure 6) provides the typical activities and cycle times for processing a PFAST request.

TABLE 8. CUSTOMER RETURN SERVICES

CHARTER	MISSION	RESPONSIBILITIES
To resolve product quality issues while providing feedback to both external and internal customers to facilitate corrective actions and continuous improvement of the product.	To provide a single point interface between the customer and the factory for resolving technical problems, issues, and field returns.	1. Maintain customer return history. 2. Track returns through the factory. 3. Establish a history library of problems and corrective actions. 4. Ensure closure with customers.



NOTE: The days indicated are the typical number of 'working days' not calendar days. Analysis difficulty and the nature of the corrective actions may either improve or degrade the total cycle time.

FIGURE 6. CUSTOMER RETURN FLOW DIAGRAM

HARRIS SEMICONDUCTOR

PFAST ACTION REQUEST

(Product Failure Analysis Solution Team)

Request # _____

Date: _____

Originator _____	Customer _____
Company/Phone No. _____	Location _____
Device Type/Part No. _____	Customer's Reference No. _____
No. Samples Returned _____	Quantity Received _____

Instructions and requirements are on the back of this form.

Has Field Applications been contacted for assistance? ☐ No ☐ Yes - Who was contacted _____

SOURCE OF PROBLEM

(Enter the sequence of events in the boxes provided)

1. Visual/Mechanical
   - ☐ Describe _____
2. Incoming Test ☐ Not Performed
   - ☐ 100% Tested ☐ Sample Tested
   - No. Tested _____ No. of Rejects _____
   - Are results representative of previous lots?
   - ☐ YES ☐ NO
3. In Process/Manufacturing Failure
   - ☐ Board Test ☐ System Test
   - How many units failed? _____
   - Failed after _____hours of testing
   - Was unit retested at incoming inspection?
   - ☐ YES ☐ NO
   - Are results representative of previous lots?
   - ☐ YES ☐ NO
4. Field Failure
   - Failed after _____hours operation
   - Estimated failure rate_____ % per _____
   - End User_____ Location _____
   - Min. _____°C Ave. _____°C Max. _____°C
5. Other

ACTION REQUESTED BY CUSTOMER

Specific Action Requested (Contact PFAST Coordinator for other options)

- ☐ Test Sample for Correlation Only
- ☐ Test Sample for Product Return >$5k
- ☐ Failure Analysis
- ☐ Other

Impact of Failed Units on Customer's Situation: _____

Customer Contact with Specific Knowledge of Rejects

Name _____

Position _____ Phone_____

REASON FOR ELECTRICAL REJECT

(Where appropriate serialize units and specify for each)

Test Conditions Relating to Failure

Tester Used (Mfgr/Model) _____

Test Temperature _____

Test Time ☐ Continuous (T = _____sec) ☐ One Shot (T = _____sec)

Describe any observed condition to which failure appears sensitive _____

1. ☐ DC Failure
   - ☐ Open ☐ Short ☐ Leakage
   - ☐ Power Drain ☐ Input Level ☐ Output Level
   - Pin Number_____
2. ☐ AC Failure
   - Power Supply Voltages = _____V
   - Input Voltages V_{IH} = _____V V_{IL} = _____V
   - Pin Number_____
   - Failing characteristics _____
3. ☐ RAM and ROM Failures (ROM failures must be returned with a good master unit if failure analysis is requested).
   - Address of Failing Location _____
   - Describe Pattern Used (If not standard patterns, give very complete description including address sequence). _____
   - Include timing diagrams and circuit schematic if available.
   - ROM Programmer Used (If purchased unprogrammed) _____

Conformal Coating (Mfgr/Model) _____

Additional Comments:

FIGURE 7. PFAST ACTION REQUEST

INSTRUCTIONS FOR COMPLETING PFAST ACTION REQUEST FORM

The purpose of this form is to help us provide you with a more accurate, complete, and timely response to failures which may occur. Accurate and complete information is essential to ensure that the appropriate corrective action can be implemented. Due to this need for accurate and complete information, requests without a completed PFAST Action Request form will be returned.

Source of Problem:

This section requests the product flow leading to the failure. Mark an 'X' in the appropriate boxes up to and including the step which detected the failure. Also mark an 'X' in the appropriate box under "ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?" to indicate whether this is a rare failure or a repeated problem.

Example 1. No incoming electrical test was performed; the units were installed onto boards; the boards functioned correctly for two hours and then 1 unit failed. The customer rarely has a failure due to the Harris device.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE _____
2. INCOMING TEST ☒ NOT PERFORMED
   ☐ 100% TESTED ☐ SAMPLE TESTED
   NO. TESTED _____ NO. OF REJECTS _____
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ☒ BOARD TEST ☐ SYSTEM TEST
   HOW MANY UNITS FAILED? 1
   FAILED AFTER 2 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ☒ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ☒ NO
4. FIELD FAILURE
   FAILED AFTER _____ HOURS OPERATION
   ESTIMATED FAILURE RATE _____% PER _____
   END USER _____ LOCATION _____
   MIN. _____°C AVE. _____°C MAX._____°C
5. OTHER _____

Example 2. 100 out of the 500 units shipped were tested at incoming and all passed. The units were installed into boards and the boards passed. The boards were installed into the system and the system failed immediately when turned on. There were 3 system failures due to this part. The customer frequently has failures of this Harris device. The 3 units were not retested at incoming.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE _____
2. INCOMING TEST ☐ NOT PERFORMED
   ☐ 100% TESTED ☒ SAMPLE TESTED
   NO. TESTED 100 NO. OF REJECTS 0
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☒ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ☒ BOARD TEST ☒ SYSTEM TEST
   HOW MANY UNITS FAILED? 3
   FAILED AFTER 0 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ☒ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☒ YES ☐ NO
4. FIELD FAILURE
   FAILED AFTER _____ HOURS OPERATION
   ESTIMATED FAILURE RATE _____% PER _____
   END USER _____ LOCATION _____
   MIN. _____°C AVE. _____°C MAX._____°C
5. OTHER _____

Action Requested by Customer:

This section should be completed with the customer's expectations. This information is essential for an appropriate response.

Reason for Electrical Reject:

This section should be completed if the type of failure could be identified. If this information is contained in attached customer correspondence there is no need to transpose onto the PFAST Action Request form.

PFAST REQUIREMENTS

The value of returning failing products is in the corrective actions that are generated. Failure to meet the following requirements can cause erroneous conclusion and corrective action; therefore, failure to meet these requirements will result in the request being returned. Contact the local PFAST Coordinator if you have any questions.

Units with conformal coating should include the coating manufacturer and model. This is requested since the coating must be removed in order to perform electrical and hermeticity testing.

1. Units must be returned with proper ESD protection (ESD-safe shipping tubes within shielding box/bag or inserted into conductive foam within shielding box/bag). No tape, paper bags, or plastic bags should be used. This requirement ensures that the devices are not damaged during shipment back to Harris.
2. Units must be intact (lid not removed and at least part of each package lead present). This is a requirement since the parts must be intact in order to perform electrical test. Also, opening the package can remove evidence of the cause of failure and lead to an incorrect conclusion.
3. Programmable parts (ROMs, PROMs, UVEPROMs, and EEPROMs) must include a master unit with the same pattern. This requirement is to provide the pattern so all failing locations can be identified. A master unit is required if a failure analysis is requested.

FIGURE 7. PFAST ACTION REQUEST (Continued)

Product Analysis Lab

The Product Analysis Laboratory capabilities and charter encompass the isolation and identification of failure modes and mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. The primary activities of the Product Analysis Lab are electrical verification/characterization of the failure, package inspection/analysis, die inspection/analysis, and circuit isolation/probing. A variety of tools and techniques have been developed to ensure the accuracy and integrity of the product analysis. This section lists some of the tools and techniques that are employed during a typical analysis.

The electrical verification/characterization of devices failing electrical parameters is essential prior to performing an analysis. The information obtained from the electrical verification provides a direction for the analysis efforts. The following electrical verification/characterization equipment may be used to obtain electrical data on a device:

- HP82000M Mixed Signal Tester
- LV500 ASIC verification system
- LTS2020 Analog tester
- Curve Tracer
- Parametric Analyzer

Prior to die level analysis, package inspection and analysis are performed. These steps are performed routinely since valuable data may not be obtainable once the package is opened. The package inspection and analysis may require the use of some of the following lab equipment:

- X-Ray
- C-Mode Scanning Acoustic Microscope (C-SAM)
- Optical inspection microscopes
- Package opening tools and techniques

Once the device has been opened, die inspection and analysis can be performed. Depending on the type of failure, several tools and techniques may be used to identify the failure mechanism. Usually the faster and easier to use operations are performed first in an attempt to expedite the analysis. The list of equipment and techniques for performing die inspection and analysis is as follows:

- Optical microscopes
- Liquid crystal
- Emission microscope
- Scanning electron microscopes - SEM

The final step of circuit isolation is ready to be performed when an area of the circuit has been identified as the source of the problem through one of the previous analysis efforts. Circuit analysis is performed using the following probing and isolation tools:

- Mechanical probing
- Laser cutter and isolation
- E-Beam probing
- Cross sectioning and chemical deprocessing

A typical analysis flow is shown in the Figure 8 below. The exact analysis steps and sequence are determined as the situation dictates. For the analysis to be conclusive, it is essential that the failure mechanism correlates to the initial product failure conditions. Some failure mechanisms require elemental and chemical analysis to identify the root cause within the manufacturing process. Elemental and chemical analysis tasks are sent to the Analytical Services Lab for further evaluation.

The results of each analysis are entered into a computer data base. This data base is used to search for specific types of problems, to identify trends, and to verify that the corrective actions were effective.

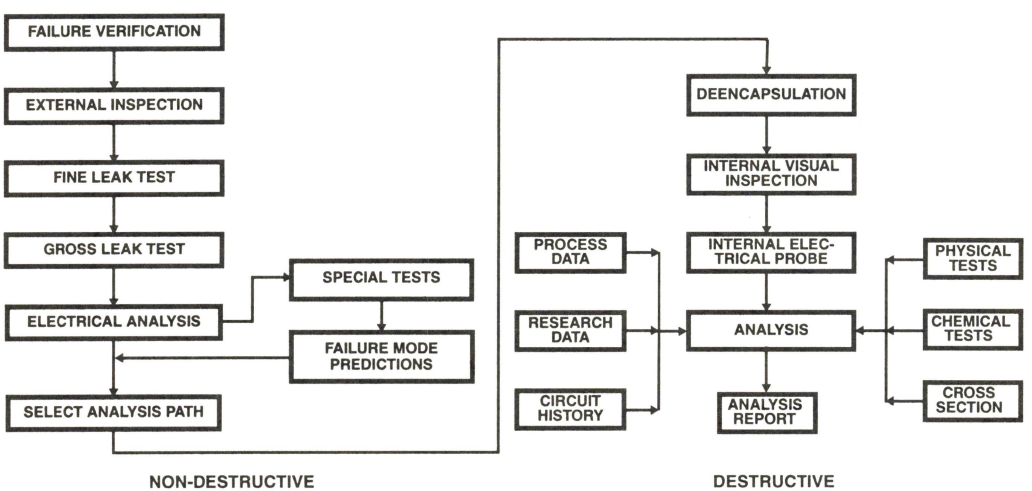


FIGURE 8. ANALYSIS SEQUENCE

Analytical Services Laboratory

Chemical and physical analysis of materials and processes is an integral part of Harris' Total Quality/Continuous Improvement efforts to build reliability into processes and products. Manufacturing operations are supported with real-time analyses to help maintain robust processes. Analyses are run in cooperation with raw material suppliers to help them provide controlled materials in dock-to-stock procurement programs.

Harris facilities, engineering, manufacturing, and product assurance are supported by the Analytical Services Laboratory. Organized into chemical or microbeam analysis methodology, staff and instrumentation from both labs cooperate in fully integrated approaches necessary to complete analytical studies.

The department also maintains ongoing working arrangements with commercial laboratories, universities, and equipment manufacturers to obtain any materials analysis in cases where instrumental capabilities are not available in our own facility. Figure 9 and Figure 10 show the capabilities of each area.

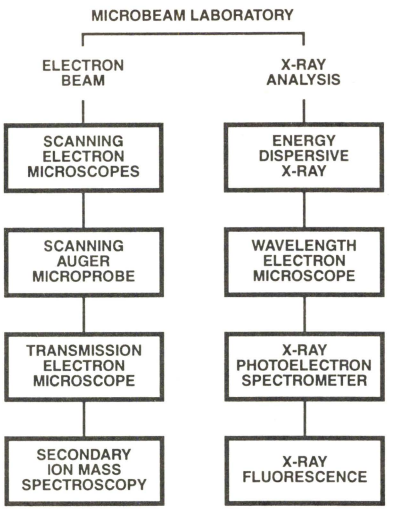


FIGURE 9. MICROBEAM LABORATORY

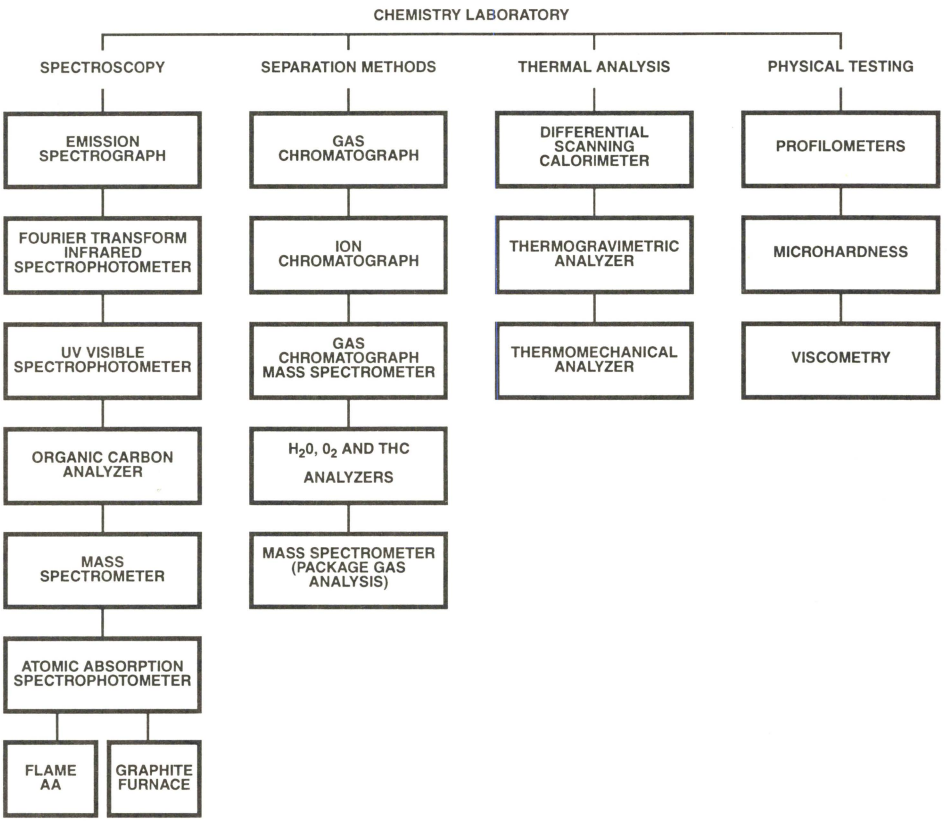


FIGURE 10. CHEMISTRY LABORATORY

Reliability Fundamentals and Calculation of Failure Rate

Table 9 defines some of the more important terminology used in describing the lifetime of integrated circuits. Of prime importance is the concept of "failure rate" and its calculation.

Failure Rate Calculations

Since reliability data can be accumulated from a number of different life tests with several different failure mechanisms, a comprehensive failure rate is desired. The failure rate calculation can be complicated if there are more than one failure mechanism in a life test, since the failure mechanisms are thermally activated at different rates The equation below accounts for these considerations along with a statistical factor to obtain the upper confidence level (UCL) for the resulting failure rate.

$$\lambda = \left[\sum_{i=1}^{\beta} \frac{x_i}{\sum_{j=1}^{k} TDH_j \, AF_{ij}} \right] \times \frac{M \times 10^9}{\sum_{i=1}^{\beta} x_i}$$

where,

λ = failure rate in FITs (Number fails in 10^9 device hours)

β = number of distinct possible failure mechanisms

k = number of life tests being combined

x_i = number of failures for a given failure mechanism $i = 1, 2, \ldots \beta$

TDH_j = Total device hours of test time (unaccelerated) for Life Test $j, j = 1, 2, 3, \ldots k$

AF_{ij} = Acceleration factor for appropriate failure mechanism $i = 1, 2, \ldots k$

$M = X^2_{(\alpha, 2r+2)}/2$
where,
X^2 = chi square factor for $2r + 2$ degrees of freedom
r = total number of failures (Σx_i)
α = risk associated with UCL;
i.e. $\alpha = (100\text{-UCL}(\%))/100$

In the failure rate calculation, Acceleration Factors (AF_{ij}) are used to derate the failure rate from the thermally accelerated life test conditions to a failure rate indicative of actual use temperature. Although no standard exists, a temperature of +55°C has been popular. Harris Semiconductor Reliability Reports will derate to +55°C and will express failure rates at 60% UCL. Other derating temperatures and UCLs are available upon request.

TABLE 9. FAILURE RATE PRIMER

TERMS	DEFINITIONS/DESCRIPTION
Failure Rate λ	Measure of failure per unit of time. The early life failure rate is typically higher, decreases slightly, and then becomes relatively constant over time. The onset of wear-out will show an increasing failure rate, which should occur well beyond useful life. The useful life failure rate is based on the exponential life distribution.
FIT (Failure In Time)	Measure of failure rate in 10^9 device hours; e.g., 1 FIT = 1 failure in 10^9 device hours, 100 FITS = 100 failure in 10^9 device hours, etc.
Device Hours	The summation of the number of units in operation multiplied by the time of operation.
MTTF (Mean Time To Failure)	Mean of the life distribution for the population of devices under operation or expected lifetime of an individual, MTTF = $1/\lambda$, which is the time where 63.2% of the population has failed. Example: For λ = 10 FITS (or 10 E-9/Hr.), MTTF = $1/\lambda$ = 100 million hours.
Confidence Level (or Limit)	Probability level at which population failure rate estimates are derived from sample life test: 10 FITs at 95% UCL means that the population failure rate is estimated to be no more that 10 FITs with 95% certainty. The upper limit of the confidence interval is used.
Acceleration Factor (AF)	A constant derived from experimental data which relates the times to failure at two different stresses. The AF allows extrapolation of failure rates from accelerated test conditions to use conditions.

Acceleration Factors

Acceleration factor is determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and has been found to be an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = EXP\left[\frac{E_a}{k}\left(\frac{1}{T_{USE}} - \frac{1}{T_{STRESS}}\right)\right]$$

where,

AF = Acceleration Factor

E_a = Thermal Activation Energy (See Table 10)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

Both T_{use} and T_{stress} (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature.

Activation Energy

The Activation Energy (E_a) of a failure mechanism is determined by performing at least two tests at different levels of stress (temperature and/or voltage). The stresses will provide the time to failure (t_f) for the two (or more) populations thus allowing the simultaneous solution for the activation energy as follows:

$$\ln (t_{f1}) = C + \frac{E_a}{kT_1} \qquad \ln (t_{f2}) = C + \frac{E_a}{kT_2}$$

By subtracting the two equations and solving for the activation energy, the following equation is obtained:

$$E_a = \frac{k[\ln(t_{f1}) - \ln(t_{f2})]}{(1/T1 - 1/T2)}$$

where,

E_a = Thermal Activation Energy (See Table 10)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

T_1, T_2 = Life test temperatures in degrees Kelvin

TABLE 10. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3eV - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3eV - 0.5eV	HTOL and voltage stress screens.	Vendor statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress testing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5eV - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistical Process Control of assembly processes, proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation.
Mask Defects/ Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles, Statistical Process Control of photoresist/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test and HTOL.	Statistical Process Control of C-V data, oxide/ interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL and oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

MICROPROCESSOR PRODUCTS 9

PACKAGING INFORMATION

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Microprocessor Package Selection Guide

PART NUMBER	PLASTIC PACKAGES					CERAMIC PACKAGES			
	PDIP	SOIC	SSOP	PLCC	MQFP	CERDIP	SBDIP	CPGA	CLCC
CDP1802A	E40.6	-	-	N44.65	-	-	D40.6	-	-
CDP1802AC	E40.6	-	-	N44.65	-	-	D40.6	-	-
CDP1802BC	E40.6	-	-	N44.65	-	-	D40.6	-	-
CDP1802AC/3	-	-	-	-	-	-	D40.6	-	-
CDP1805AC	E40.6	-	-	N44.65	-	-	D40.6	-	-
CDP1806AC	E40.6	-	-	N44.65	-	-	D40.6	-	-
80C286	-	-	-	N68.95	-	-	-	G68.B	-
80C286/883	-	-	-	-	-	-	-	G68.B	-
80C86	E40.6	-	-	N44.65	-	F40.6	-	-	J44.A
80C88	E40.6	-	-	N44.65	-	F40.6	-	-	J44.A
CDP1851	E40.6	-	-	-	-	-	D40.6	-	-
CDP1851C	E40.6	-	-	-	-	-	D40.6	-	-
CDP1852	E24.6	-	-	-	-	-	D24.6	-	-
CDP1852C	E24.6	-	-	-	-	-	D24.6	-	-
CDP1852/3	-	-	-	-	-	-	D24.6	-	-
CDP1852C/3	-	-	-	-	-	-	D24.6	-	-
CDP1853	E16.3	-	-	-	-	-	D16.3	-	-
CDP1853C	E16.3	-	-	-	-	-	D16.3	-	-
CDP1853/3	-	-	-	-	-	-	D16.3	-	-
CDP1853C/3	-	-	-	-	-	-	D16.3	-	-
CDP1855	E28.6	-	-	-	-	-	D28.6	-	-
CDP1855C	E28.6	-	-	-	-	-	D28.6	-	-
CDP1857C	E16.3	-	-	-	-	-	D16.3	-	-
CDP1871A	E40.6	-	-	N44.65	-	-	D40.6	-	-
CDP1871AC	E40.6	-	-	N44.65	-	-	D40.6	-	-
CDP1872C	E22.4	-	-	-	-	-	-	-	-
CDP1874C	E22.4	-	-	-	-	-	-	-	-
CDP1875C	E22.4	-	-	-	-	-	D22.4A	-	-
CDP1877	E28.6	-	-	-	-	-	-	-	-
CDP1877C	E28.6	-	-	-	-	-	-	-	-
CDP1878C	E28.6	-	-	-	-	-	D28.6	-	-
CDP1879	E24.6	-	-	-	-	-	D24.6	-	-
CDP1879C-1	E24.6	-	-	-	-	-	D24.6	-	-
CDP1881C	E20.3	-	-	-	-	-	-	-	-
CDP1882	E18.3	-	-	-	-	-	D18.3	-	-
CDP1882C	E18.3	-	-	-	-	-	D18.3	-	-

Microprocessor Package Selection Guide (Continued)

PART NUMBER	PLASTIC PACKAGES					CERAMIC PACKAGES			
	PDIP	SOIC	SSOP	PLCC	MQFP	CERDIP	SBDIP	CPGA	CLCC
CDP1883	E20.3	-	-	-	-	-	-	-	-
CDP1883C	E20.3	-	-	-	-	-	-	-	-
ICM7170	E24.6	M24.3	-	-	-	-	D24.6	-	-
82C237	E40.6	-	-	N44.65	-	F40.6	-	-	J44.A
82C284	-	-	-	-	-	F18.3	-	-	-
82C284/883	-	-	-	-	-	F18.3	-	-	-
82C37A	E40.6	-	-	N44.65	-	F40.6	-	-	J44.A
82C54	E24.6	-	-	N28.45	-	F24.6	-	-	J28.A
82C55A	E40.6	-	-	N44.65	-	F40.6	-	-	J44.A
82C59A	E28.6	-	-	N28.45	-	F28.6	-	-	J28.A
82C82	E20.3	-	-	N20.35	-	F20.3	-	-	J20.A
82C83H	E20.3	-	-	N20.35	-	F20.3	-	-	J20.A
82C84A	E18.3	-	-	N20.35	-	F18.3	-	-	J20.A
82C85	-	-	-	N28.45	-	F24.3	-	-	J28.A
82C86H	E20.3	-	-	N20.35	-	F20.3	-	-	J20.A
82C87H	E20.3	-	-	N20.35	-	F20.3	-	-	J20.A
82C88	E20.3	-	-	N20.35	-	F20.3	-	-	J20.A
82C89	E20.3	-	-	N20.35	-	F20.3	-	-	J20.A
82C50A	E40.6	-	-	N44.65	-	-	-	-	-
82C52	E28.6	-	-	N28.45	-	F28.6	-	-	J28.A
CDP1854A	E40.6	-	-	N44.65	-	-	D40.6	-	-
CDP1854AC	E40.6	-	-	N44.65	-	-	D40.6	-	-
CDP1854A/3	-	-	-	-	-	-	D40.6	-	-
CDP1854AC/3	-	-	-	-	-	-	D40.6	-	-
CDP6402	E40.6	-	-	-	-	-	D40.6	-	-
CDP6402C	E40.6	-	-	-	-	-	D40.6	-	-
HD-4702	E16.3	-	-	-	-	F16.3	-	-	J18.B
HD-4702/883	-	-	-	-	-	F16.3	-	-	-
HD-6402	E40.6	-	-	-	-	F40.6	-	-	-
HD-6402/883	-	-	-	-	-	F40.6	-	-	-
HD-6408	E24.6	-	-	-	-	F24.6	-	-	-
HD-6409	E20.3	M20.3	-	-	-	F20.3	-	-	J20.A
HD-6409/883	-	-	-	-	-	F20.3	-	-	J20.A
HD-15530	-	-	-	-	-	F24.6	-	-	J28.A
HD-15531	E40.6	-	-	-	-	F40.6	-	-	-
HD-15531/883	-	-	-	-	-	F40.6	-	-	-

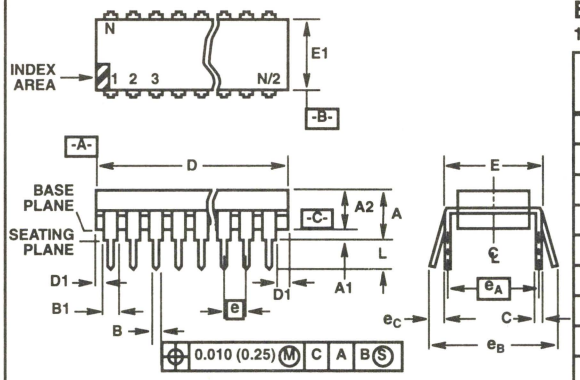
Microprocessor Package Selection Guide (Continued)

PART NUMBER	PLASTIC PACKAGES					CERAMIC PACKAGES			
	PDIP	SOIC	SSOP	PLCC	MQFP	CERDIP	SBDIP	CPGA	CLCC
HS-3182	-	-	-	-	-	-	D16.3	-	J28.A
HS-3282	-	-	-	-	-	F40.6	-	-	J44.A
ICL232	E16.3	M16.3	-	-	-	F16.3	-	-	-
HIN200	-	M20.3	-	-	-	-	-	-	-
HIN201	-	M16.3	-	-	-	-	-	-	-
HIN202	E16.3	M16.3 M16.15	M16.209	-	-	-	-	-	-
HIN204	-	M16.3	-	-	-	-	-	-	-
HIN206	E24.3	M24.3	M24.209	-	-	-	-	-	-
HIN207	E24.3	M24.3	M24.209	-	-	-	-	-	-
HIN208	E24.3	M24.3	M24.209	-	-	-	-	-	-
HIN209	E24.3	M24.3	-	-	-	-	-	-	-
HIN211	-	M28.3	M28.209	-	-	-	-	-	-
HIN213	-	M28.3	M28.209	-	-	-	-	-	-
HIN230	-	M20.3	-	-	-	-	-	-	-
HIN231	-	M16.3	-	-	-	-	-	-	-
HIN232	E16.3	M16.3	-	-	-	F16.3	-	-	-
HIN234	-	M16.3	-	-	-	-	-	-	-
HIN236	E24.3	M24.3	-	-	-	-	-	-	-
HIN237	E24.3	M24.3	-	-	-	-	-	-	-
HIN238	E24.3	M24.3	-	-	-	-	-	-	-
HIN239	-	M24.3	-	-	-	-	-	-	-
HIN240	-	-	-	-	Q44.10X10	-	-	-	-
HIN241	-	M28.3	M28.209	-	-	-	-	-	-
CDP1821C/3	-	-	-	-	-	-	D16.3	-	-
CDP1822	E22.4	-	-	-	-	-	D22.4A	-	-
CDP1822C	E22.4	-	-	-	-	-	D22.4A	-	-
CDP1822C/3	-	-	-	-	-	-	D22.4A		
CDP1823	E24.6	-	-	-	-	-	D24.6	-	-
CDP1823C	E24.6	-	-	-	-	-	D24.6	-	-
CDP1823C/3	-	-	-	-	-	-	D24.6		
CDP1824	E18.3	-	-	-	-	-	D18.3	-	-
CDP1824C	E18.3	-	-	-	-	-	D18.3	-	-
CDP1824/3	-	-	-	-	-	-	D18.3	-	-
CDP1824C/3	-	-	-	-	-	-	D18.3	-	-
CDP1826C	E22.4	-	-	-	-	-	-	-	-

Microprocessor Package Selection Guide (Continued)

PART NUMBER	PLASTIC PACKAGES					CERAMIC PACKAGES			
	PDIP	SOIC	SSOP	PLCC	MQFP	CERDIP	SBDIP	CPGA	CLCC
MWS5101	E22.4	-	-	-	-	-	D22.4A	-	-
MWS5101A	E22.4	-	-	-	-	-	D22.4A	-	-
HM-6508	E16.3	-	-	-	-	F16.3	-	-	-
HM-6508/883	-	-	-	-	-	F16.3	-	-	-
HM-6518	E18.3	-	-	-	-	F18.3	-	-	-
HM-6518/883	-	-	-	-	-	F18.3	-	-	-
HM-6551	E22.4	-	-	-	-	F22.4	-	-	-
HM-6551/883	-	-	-	-	-	F22.4	-	-	-
HM-6561	E18.3	-	-	-	-	F18.3	-	-	-
HM-6561/883	-	-	-	-	-	F18.3	-	-	-
HM-6504	E18.3	-	-	-	-	F18.3	-	-	J18.B
HM-6504/883	-	-	-	-	-	F18.3	-	-	-
HM-6514	E18.3	-	-	-	-	F18.3	-	-	J18.B
HM-6514/883	-	-	-	-	-	F18.3	-	-	-
MWS5114	E18.3	-	-	-	-	-	D18.3	-	-
HM-6516	E24.6	-	-	-	-	F24.6	-	-	J32.A
HM-6516/883	-	-	-	-	-	F24.6	-	-	J32.A
HM-65162	E24.6	-	-	-	-	F24.6	-	-	J32.A
HM-65162/883	-	-	-	-	-	F24.6	-	-	J32.A
HM-65262	-	-	-	-	-	F20.3	-	-	J20.C
HM-65262/883	-	-	-	-	-	F20.3	-	-	J20.C
HM-65642	-	-	-	-	-	F28.6	-	-	-
HM-65642/883	-	-	-	-	-	F28.6	-	-	J32.A
HM-6642	-	-	-	-	-	-	D24.3 D24.6	-	J28.A
HM-6642/883	-	-	-	-	-	-	D24.3 D24.6	-	J28.A
HM-6617	-	-	-	-	-	-	D24.3 D24.6	-	J32.A
HM-6617/883	-	-	-	-	-	-	D24.3 D24.6	-	J32.A

Dual-In-Line Plastic Packages (PDIP)



E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

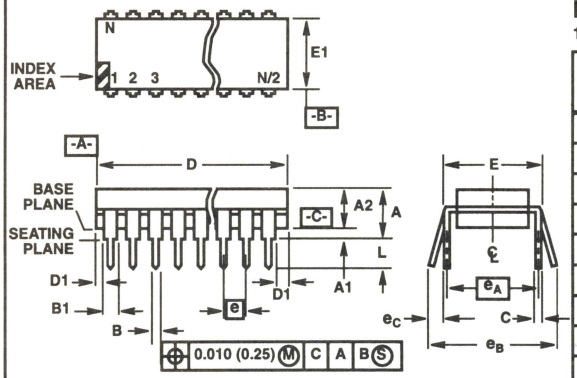
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E18.3 (JEDEC MS-001-BC ISSUE D)
18 LEAD DUAL-IN-LINE PLASTIC PACKAGE

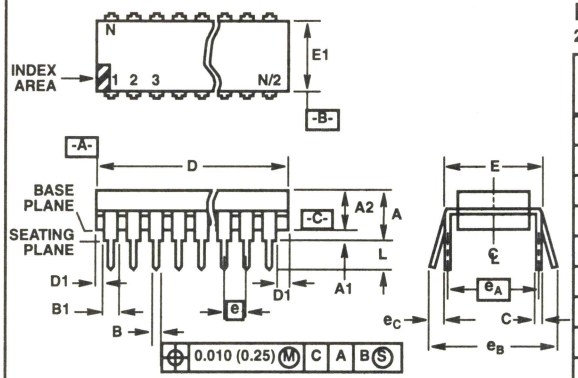
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.845	0.880	21.47	22.35	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	18		18		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

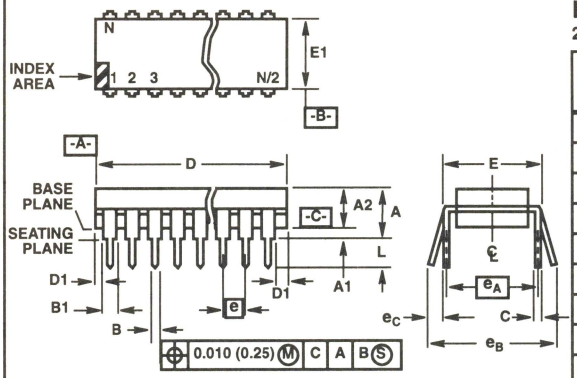
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E22.4 (JEDEC MS-010-AA ISSUE C)
22 LEAD DUAL-IN-LINE PLASTIC PACKAGE

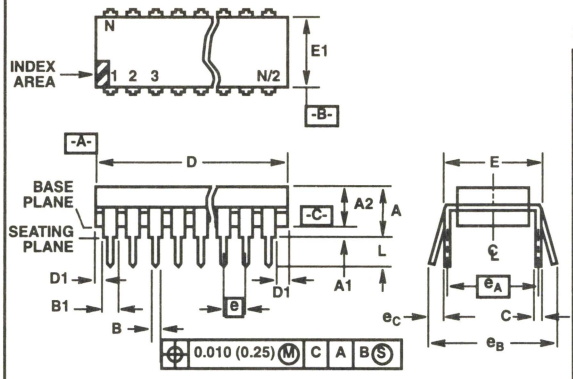
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.065	1.15	1.65	8
C	0.009	0.015	0.229	0.381	-
D	1.065	1.120	27.06	28.44	5
D1	0.005	-	0.13	-	5
E	0.390	0.425	9.91	10.79	6
E1	0.330	0.390	8.39	9.90	5
e	0.100 BSC		2.54 BSC		-
e_A	0.400 BSC		10.16 BSC		6
e_B	-	0.500	-	12.70	7
L	0.115	0.160	2.93	4.06	4
N	22		22		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



NOTES:

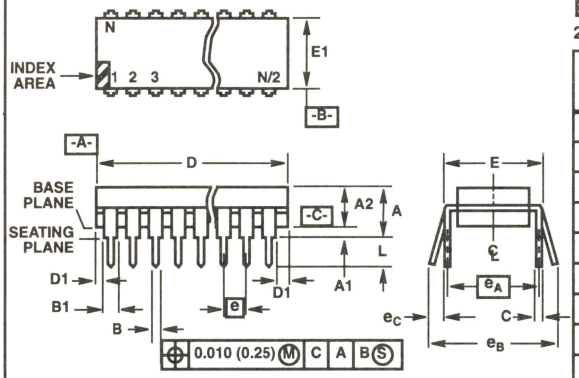
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E24.6 (JEDEC MS-011-AA ISSUE B)
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.150	1.290	29.3	32.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	24		24		9

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Dual-In-Line Plastic Packages (PDIP)



NOTES:

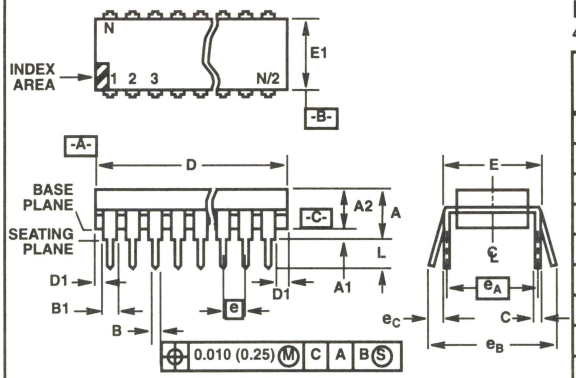
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-011-AB ISSUE B)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

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Dual-In-Line Plastic Packages (PDIP)



E40.6 (JEDEC MS-011-AC ISSUE B)
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

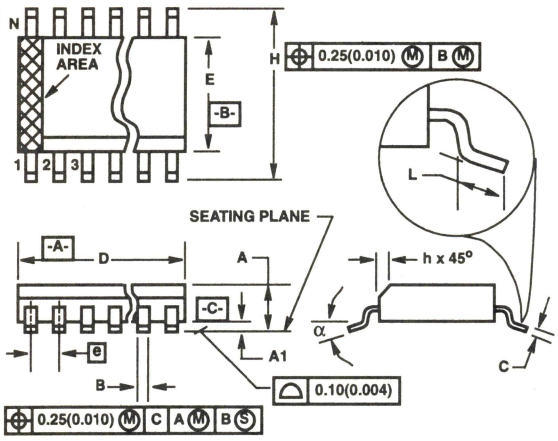
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Small Outline Plastic Packages (SOIC)



M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

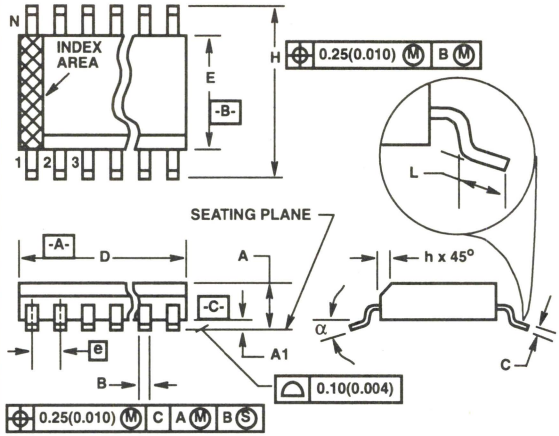
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

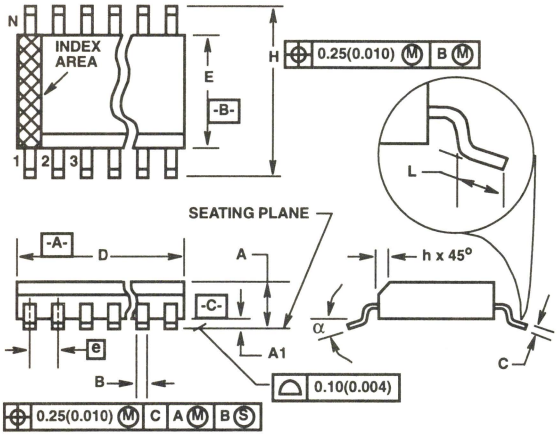
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

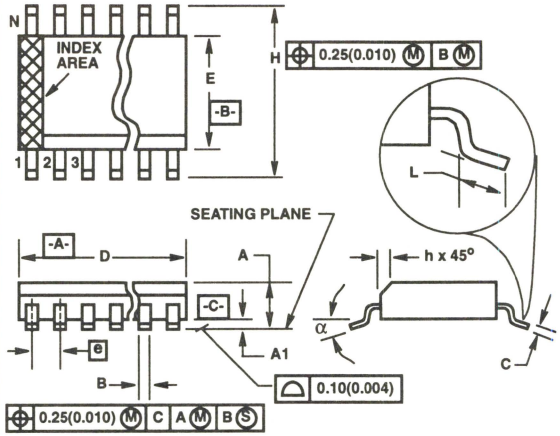
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

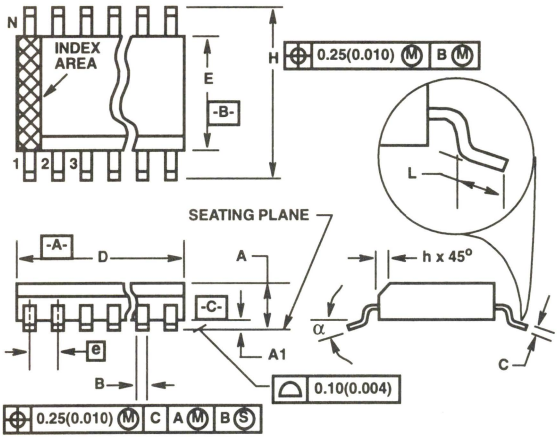
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

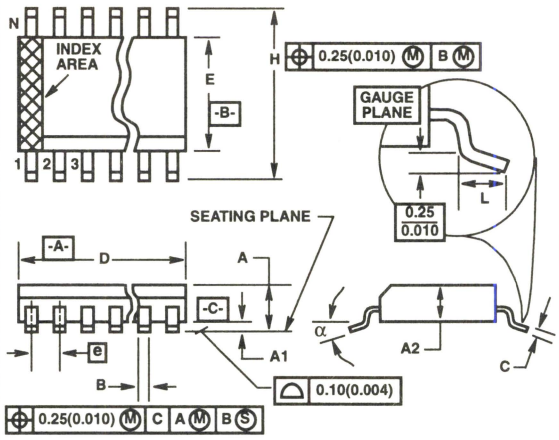
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP)



M16.209 (JEDEC MO-150-AC ISSUE B)
16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

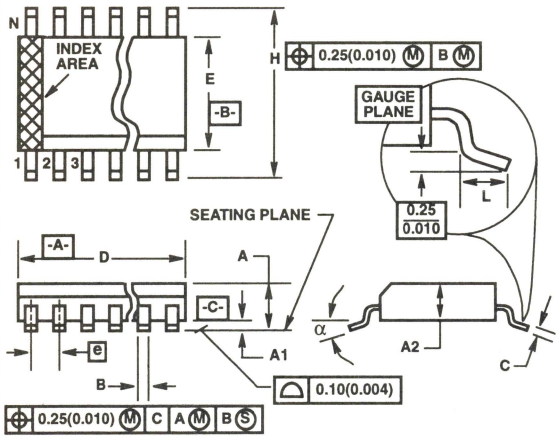
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.233	0.255	5.90	6.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 2 3/95

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP)



M24.209 (JEDEC MO-150-AG ISSUE B)
24 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

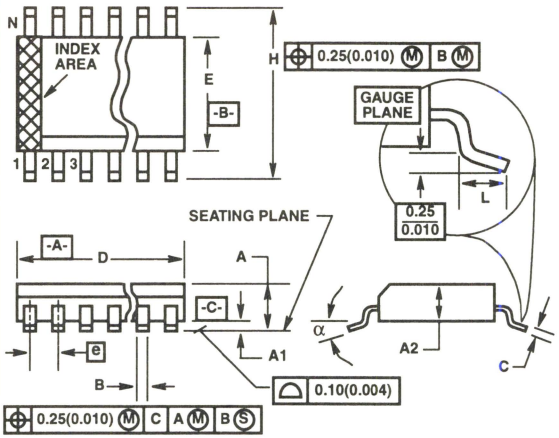
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.312	0.334	7.90	8.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	24		24		7
α	0°	8°	0°	8°	-

Rev. 1 3/95

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP)



M28.209 (JEDEC MO-150-AH ISSUE B)
28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

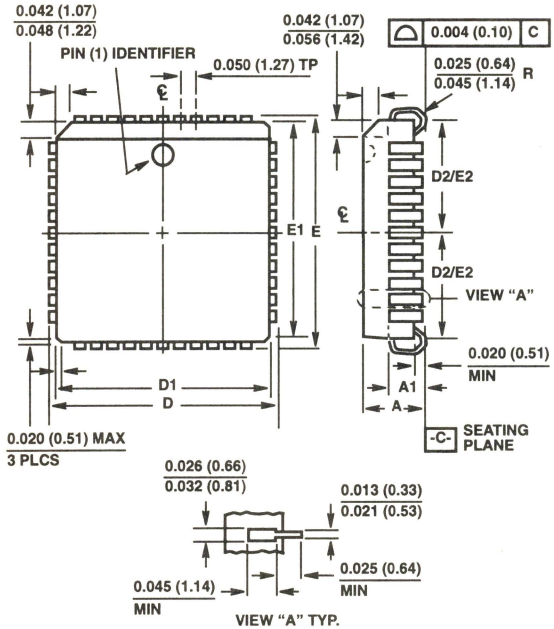
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.390	0.413	9.90	10.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 1 3/95

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Plastic Leaded Chip Carrier Packages (PLCC)



N20.35 (JEDEC MS-018AA ISSUE A)
20 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

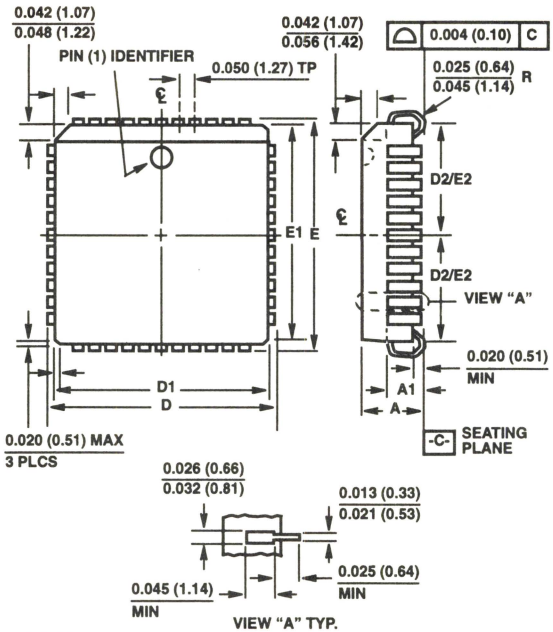
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.385	0.395	9.78	10.03	-
D1	0.350	0.356	8.89	9.04	3
D2	0.141	0.169	3.59	4.29	4, 5
E	0.385	0.395	9.78	10.03	-
E1	0.350	0.356	8.89	9.04	3
E2	0.141	0.169	3.59	4.29	4, 5
N	20		20		6

Rev. 1 3/95

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

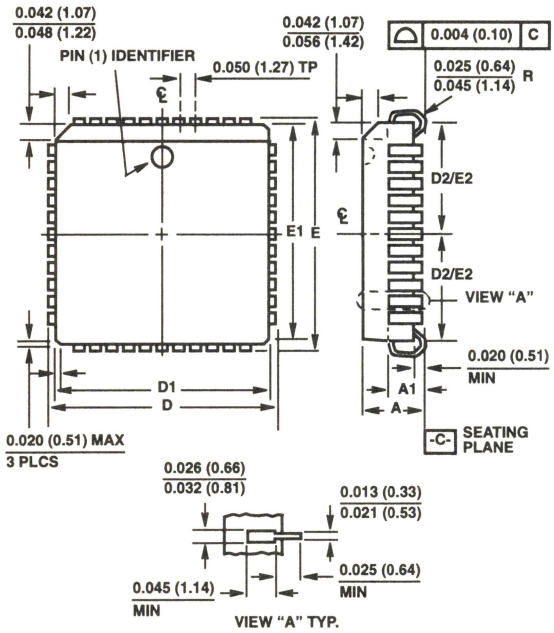
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

Rev. 1 3/95

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Plastic Leaded Chip Carrier Packages (PLCC)



N44.65 (JEDEC MS-018AC ISSUE A)
44 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

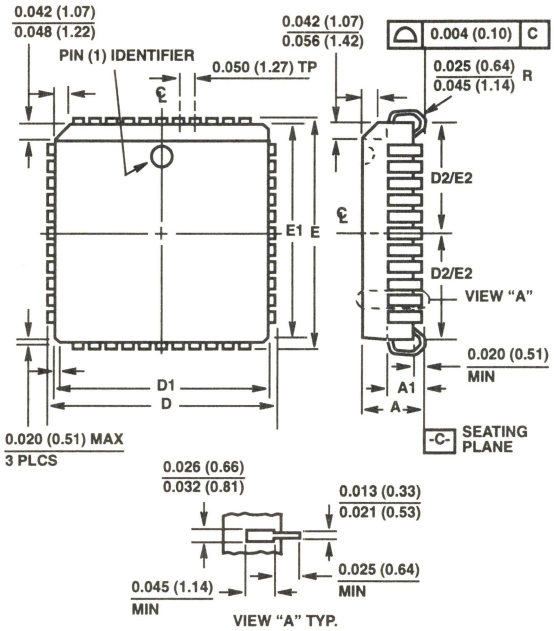
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.685	0.695	17.40	17.65	-
D1	0.650	0.656	16.51	16.66	3
D2	0.291	0.319	7.40	8.10	4, 5
E	0.685	0.695	17.40	17.65	-
E1	0.650	0.656	16.51	16.66	3
E2	0.291	0.319	7.40	8.10	4, 5
N	44		44		6

Rev. 1 3/95

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Plastic Leaded Chip Carrier Packages (PLCC)



N68.95 (JEDEC MS-018AE ISSUE A)
68 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

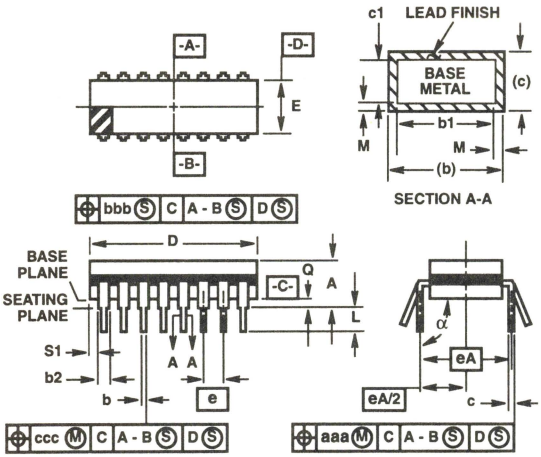
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.985	0.995	25.02	25.27	-
D1	0.950	0.958	24.13	24.33	3
D2	0.441	0.469	11.21	11.91	4, 5
E	0.985	0.995	25.02	25.27	-
E1	0.950	0.958	24.13	24.33	3
E2	0.441	0.469	11.21	11.91	4, 5
N	68		68		6

Rev. 1 3/95

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

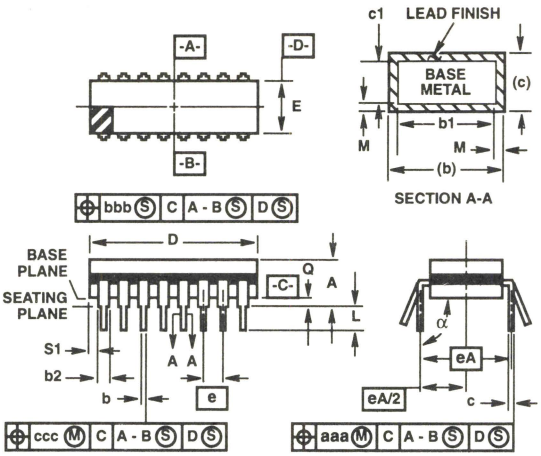
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F18.3 MIL-STD-1835 GDIP1-T18 (D-6, CONFIGURATION A)
18 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

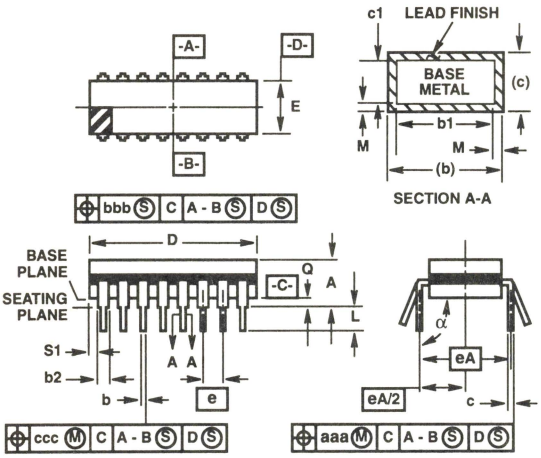
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.960	-	24.38	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	18		18		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F20.3 MIL-STD-1835 GDIP1-T20 (D-8, CONFIGURATION A)
20 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

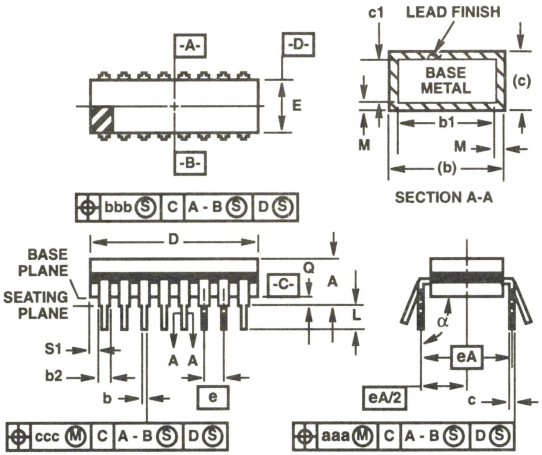
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.060	-	26.92	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	20		20		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F22.4 MIL-STD-1835 GDIP1-T22 (D-7, CONFIGURATION A)
22 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

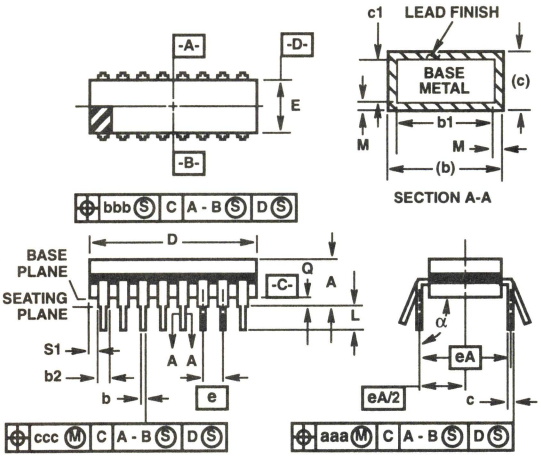
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.111	-	28.22	5
E	0.350	0.410	8.89	10.41	5
e	0.100 BSC		2.54 BSC		-
eA	0.400 BSC		10.16 BSC		-
eA/2	0.200 BSC		5.08 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	22		22		8

Rev. 0 6/13/95

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F24.3 MIL-STD-1835 GDIP3-T24 (D-9, CONFIGURATION A)
24 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

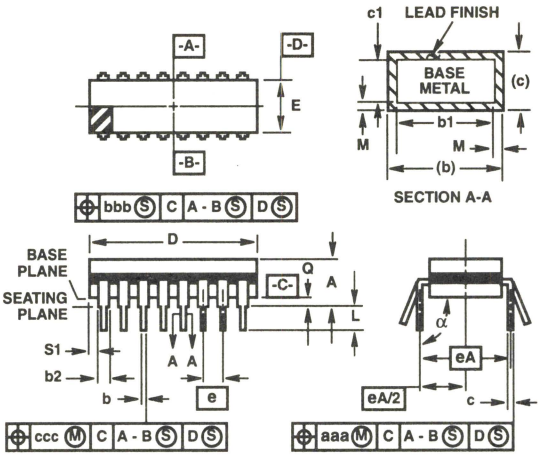
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.220	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.280	-	32.51	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	24		24		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F24.6 MIL-STD-1835 GDIP1-T24 (D-3, CONFIGURATION A)
24 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

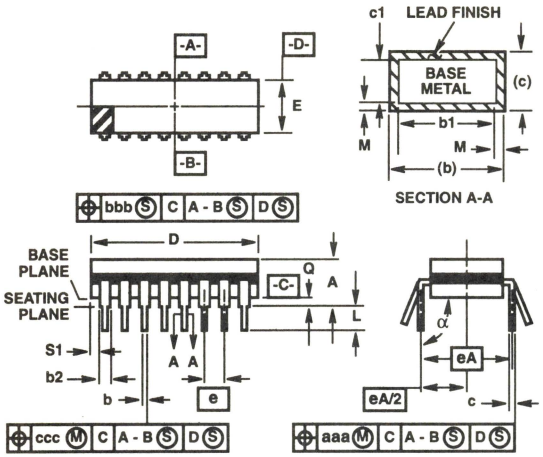
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290	-	32.77	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.120	0.200	3.05	5.08	-
Q	0.015	0.075	0.38	1.91	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	24		24		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F28.6 MIL-STD-1835 GDIP1-T28 (D-10, CONFIGURATION A)
28 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

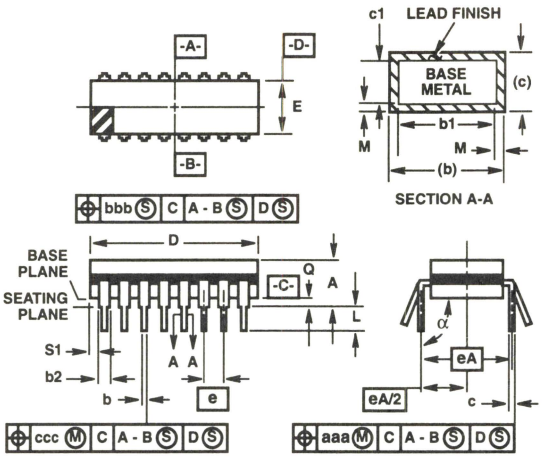
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	28		28		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F40.6 MIL-STD-1835 GDIP1-T40 (D-5, CONFIGURATION A)
40 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

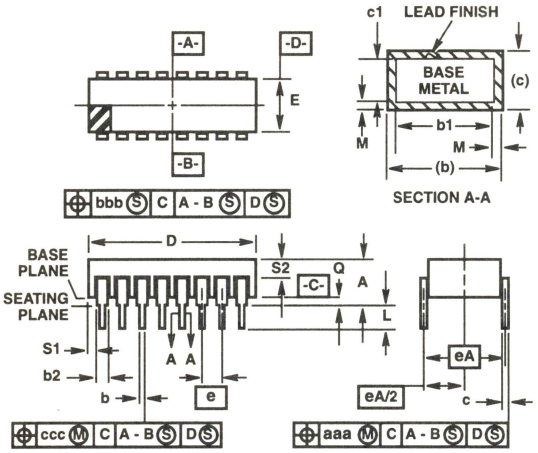
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	2.096	-	53.24	5
E	0.510	0.620	12.95	15.75	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	40		40		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

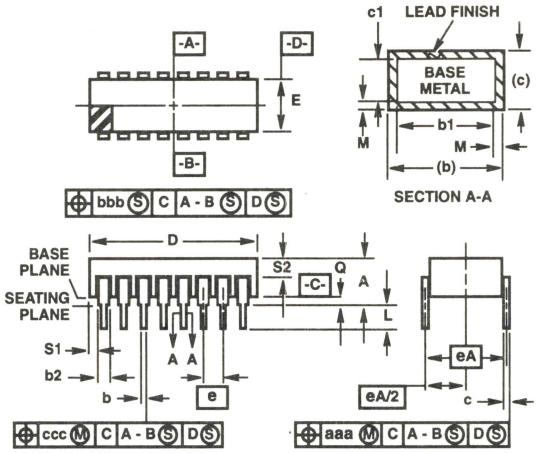
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D18.3 MIL-STD-1835 CDIP2-T18 (D-6, CONFIGURATION C)
18 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

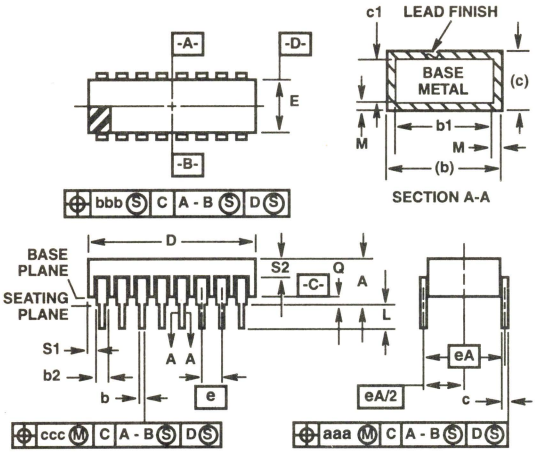
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.960	-	24.38	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	18		18		8

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D22.4A

22 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

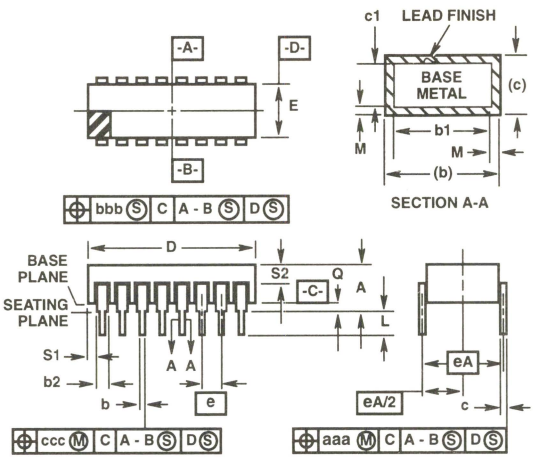
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.111	-	28.22	-
E	0.350	0.410	8.89	10.41	-
e	0.100 BSC		2.54 BSC		-
eA	0.400 BSC		10.16 BSC		-
eA/2	0.200 BSC		5.08 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	5
S1	0.000	-	0.00	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	22		22		8

Rev. 0 6/20/95

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D24.3 MIL-STD-1835 CDIP4-T24 (D-9, CONFIGURATION C)
24 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

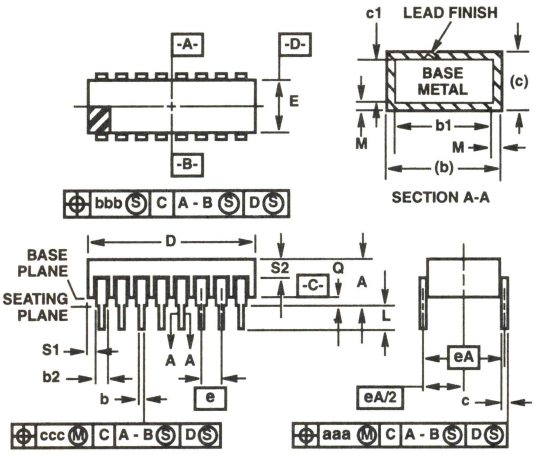
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.280	-	32.51	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	24		24		8

Rev. 0 4/96

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D24.6 MIL-STD-1835 CDIP2-T24 (D-3, CONFIGURATION C)
24 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

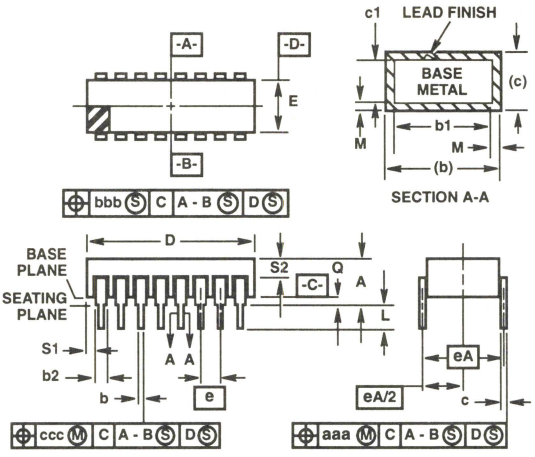
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290	-	32.77	-
E	0.500	0.610	12.70	15.49	-
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.120	0.200	3.05	5.08	-
Q	0.015	0.075	0.38	1.91	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	24		24		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D28.6 MIL-STD-1835 CDIP2-T28 (D-10, CONFIGURATION C)
28 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

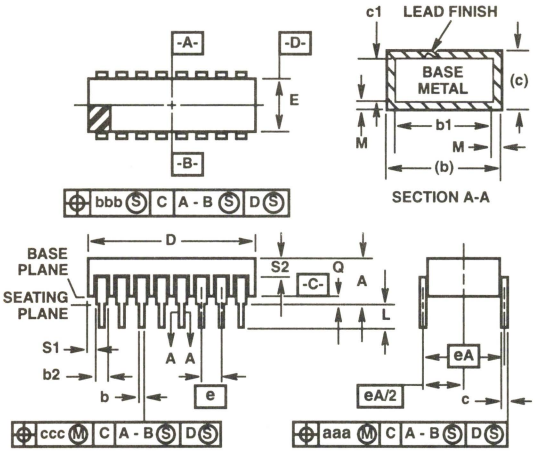
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	-
E	0.500	0.610	12.70	15.49	-
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	28		28		8

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D40.6 MIL-STD-1835 CDIP2-T40 (D-5, CONFIGURATION C)
40 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

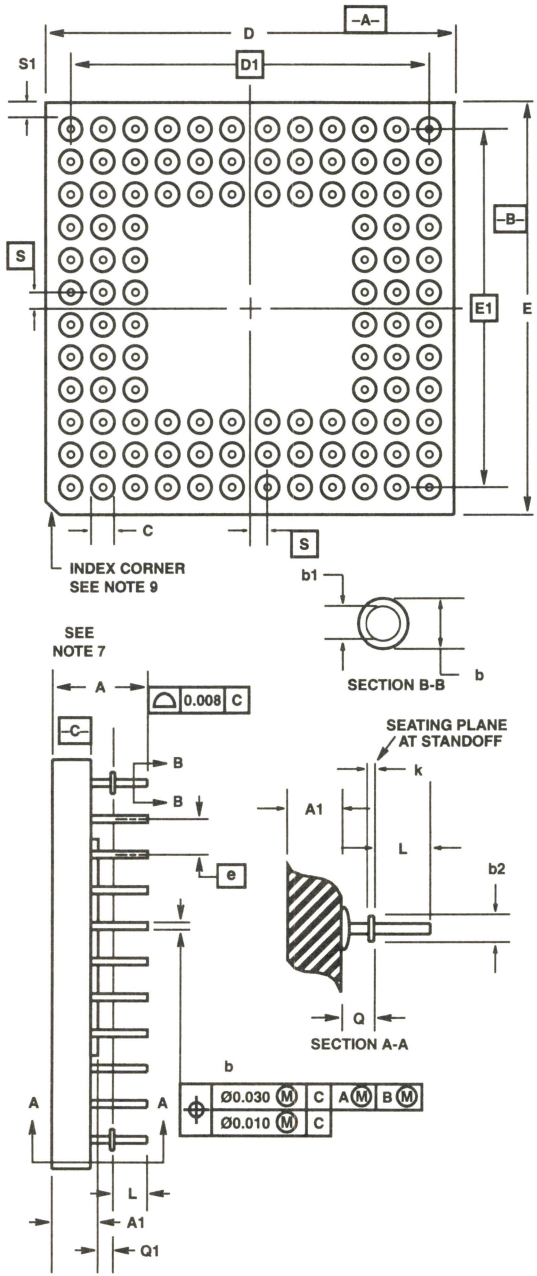
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	2.096	-	53.24	4
E	0.510	0.620	12.95	15.75	4
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	40		40		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Pin Grid Array Packages (CPGA)



G68.B MIL-STD-1835 CMGA3-P68D (P-AC)
68 LEAD CERAMIC PIN GRID ARRAY PACKAGE

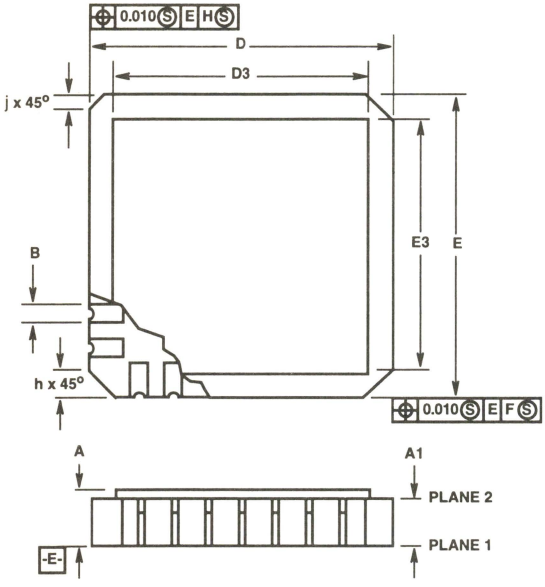
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.215	0.345	5.46	8.76	-
A1	0.070	0.145	1.78	3.68	3
b	0.016	0.0215	0.41	0.55	8
b1	0.016	0.020	0.41	0.51	-
b2	0.042	0.058	1.07	1.47	4
C	-	0.080	-	2.03	-
D	1.140	1.180	28.96	29.97	-
D1	1.000 BSC		25.4 BSC		-
E	1.140	1.180	28.96	29.97	-
E1	1.000 BSC		25.4 BSC		-
e	0.100 BSC		2.54 BSC		6
k	0.008 REF		0.20 REF		-
L	0.120	0.140	3.05	3.56	-
Q1	0.025	0.060	0.64	1.52	5
S	0.000 BSC		0.00 BSC		10
S1	0.003	-	0.08	-	-
M	11		11		1
N	-	121	-	121	2

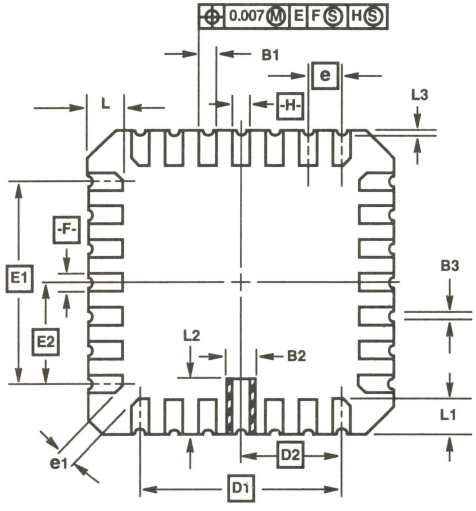
Rev. 0 6/20/95

NOTES:

1. "M" represents the maximum pin matrix size.
2. "N" represents the maximum allowable number of pins. Number of pins and location of pins within the matrix is shown on the pinout listing in this data sheet.
3. Dimension "A1" includes the package body and Lid for both cavity-up and cavity-down configurations. This package is cavity down. Dimension "A1" does not include heatsinks or other attached features.
4. Standoffs are required and shall be located on the pin matrix diagonals. The seating plane is defined by the standoffs at dimension "Q1".
5. Dimension "Q1" applies to cavity-down configurations only.
6. All pins shall be on the 0.100 inch grid.
7. Datum C is the plane of pin to package interface for both cavity up and down configurations.
8. Pin diameter includes solder dip or custom finishes. Pin tips shall have a radius or chamfer.
9. Corner shape (chamfer, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
10. Dimension "S" is measured with respect to datums A and B.
11. Dimensioning and tolerancing per ANSI Y14.5M-1982.
12. Controlling dimension: INCH.

Ceramic Leadless Chip Carrier Packages (CLCC)





J18.B

18 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

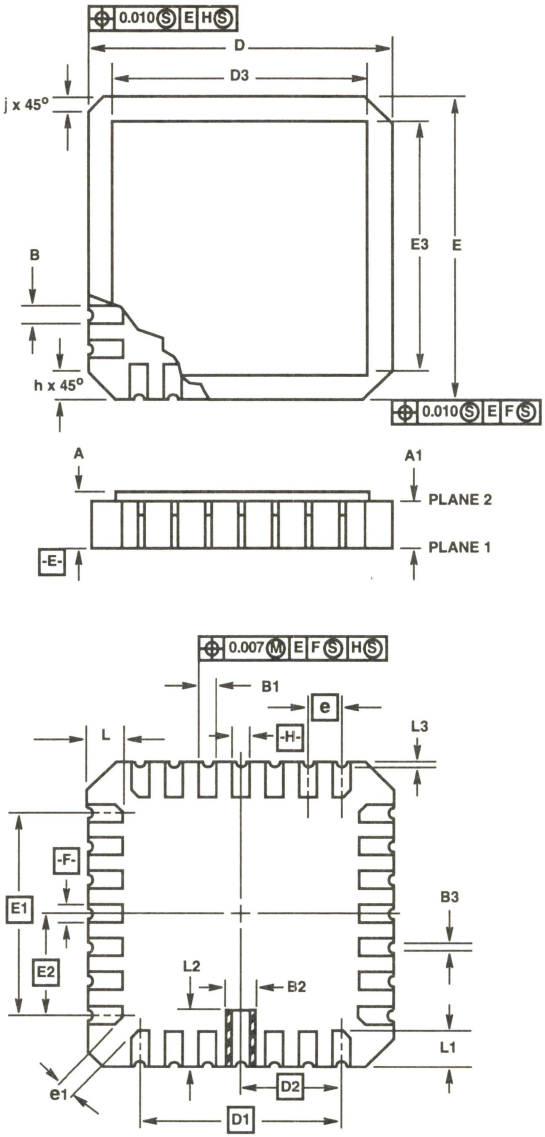
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.054	0.075	1.37	1.91	6, 7
A1	0.044	0.063	1.12	1.60	-
B	-	-	-	-	-
B1	0.020	0.030	0.51	0.76	2, 4
B2	-	-	-	-	-
B3	0.006	0.022	0.15	0.56	-
D	0.280	0.305	7.11	7.75	-
D1	0.150 BSC		3.81 BSC		-
D2	0.075 BSC		1.91 BSC		-
D3	-	0.305	-	7.75	1, 2
E	0.345	0.365	8.76	9.27	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.365	-	9.27	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.012R REF		0.30R REF		5
j	0.012R REF		0.30R REF		5
L	0.040	0.050	1.02	1.27	-
L1	0.040	0.050	1.02	1.27	-
L2	0.090	0.110	2.29	2.79	-
L3	0.003	0.015	0.08	0.38	-
ND	4		4		3
NE	5		5		3
N	18		18		3

Rev. 0 6/20/95

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Ceramic Leadless Chip Carrier Packages (CLCC)



J20.A MIL-STD-1835 CQCC1-N20 (C-2)
20 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

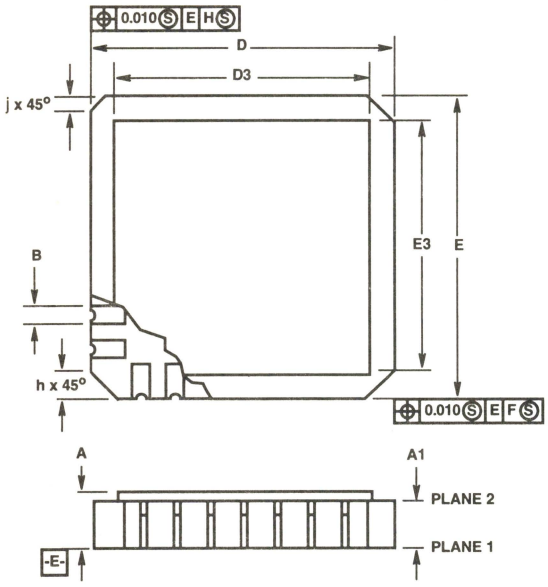
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

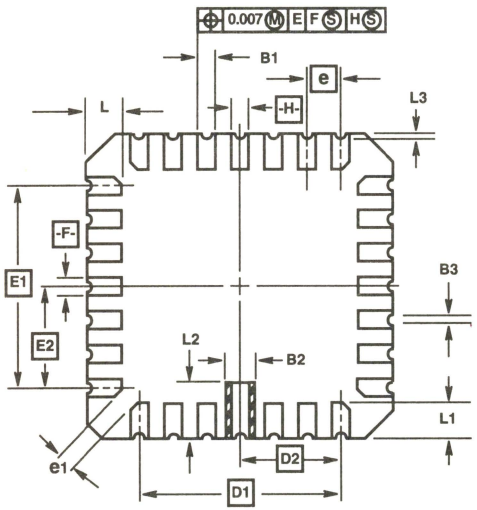
Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Ceramic Leadless Chip Carrier Packages (CLCC)





J20.C MIL-STD-1835 CQCC3-N20 (C-13)
20 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

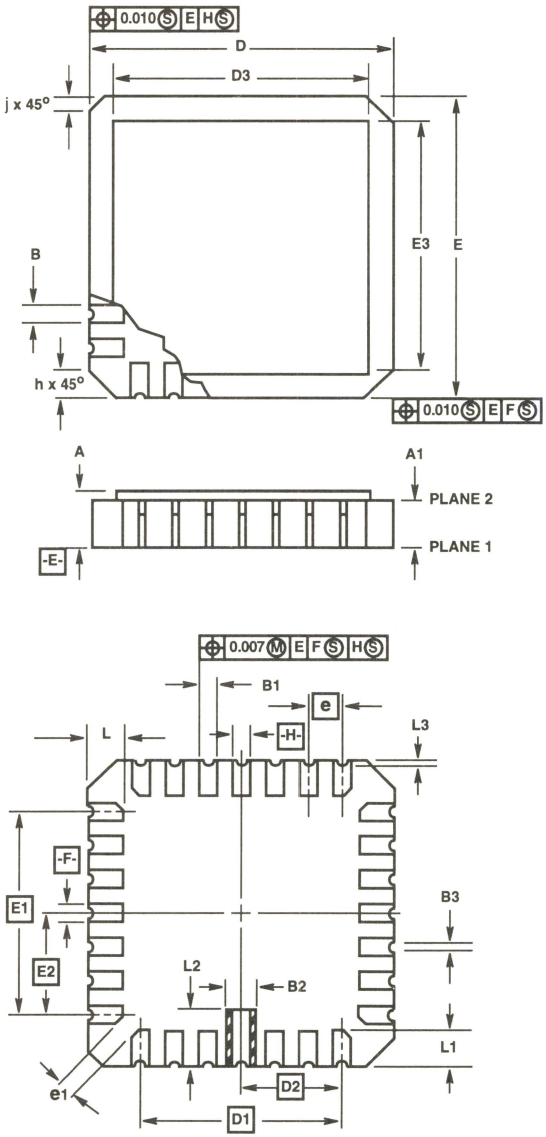
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.120	1.52	3.05	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.280	0.305	7.11	7.75	-
D1	0.150 BSC		3.81 BSC		-
D2	0.075 BSC		1.90 BSC		-
D3	-	0.305	-	7.75	2
E	0.420	0.440	10.67	11.18	-
E1	0.250 BSC		6.35 BSC		-
E2	0.125 BSC		3.17 BSC		-
E3	-	0.440	-	11.18	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	4		4		3
NE	6		6		3
N	20		20		3

Rev. 0 6/13/95

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Ceramic Leadless Chip Carrier Packages (CLCC)



J28.A MIL-STD-1835 CQCC1-N28 (C-4)
28 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

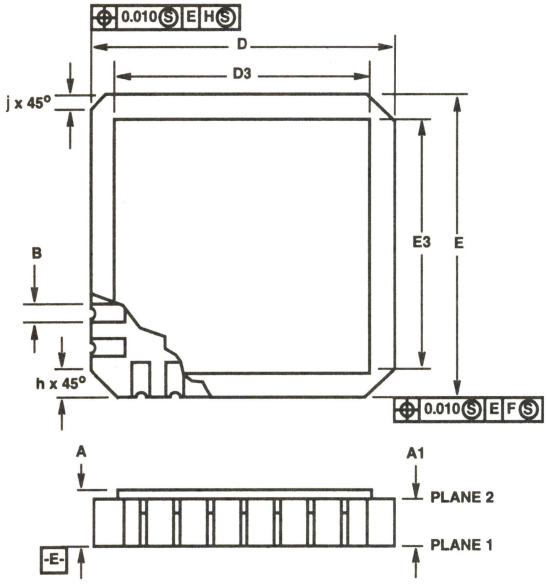
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.442	0.460	11.23	11.68	-
D1	0.300 BSC		7.62 BSC		-
D2	0.150 BSC		3.81 BSC		-
D3	-	0.460	-	11.68	2
E	0.442	0.460	11.23	11.68	-
E1	0.300 BSC		7.62 BSC		-
E2	0.150 BSC		3.81 BSC		-
E3	-	0.460	-	11.68	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.90	2.41	-
L3	0.003	0.015	0.08	0.038	-
ND	7		7		3
NE	7		7		3
N	28		28		3

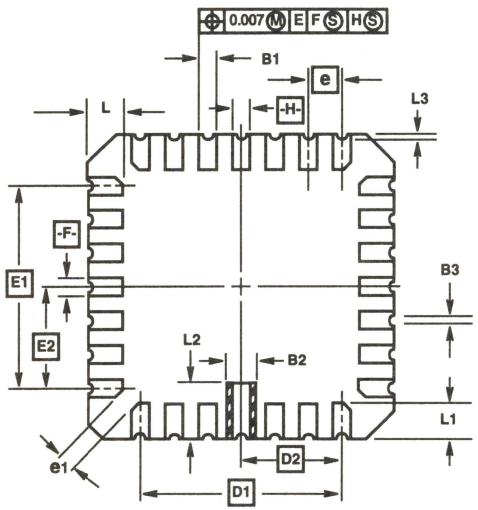
Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Ceramic Leadless Chip Carrier Packages (CLCC)





J32.A MIL-STD-1835 CQCC1-N32 (C-12)
32 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

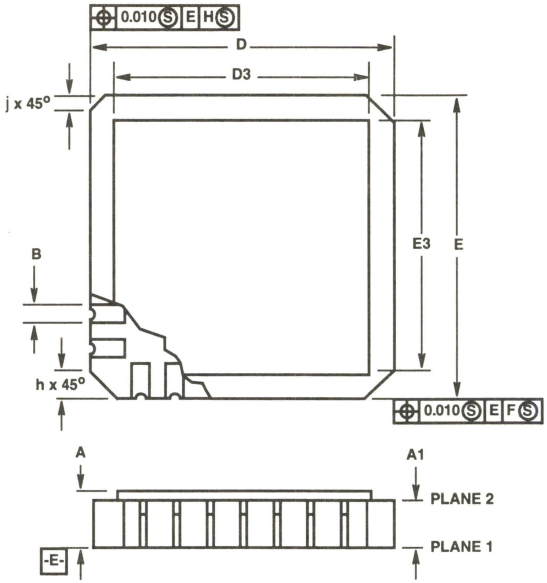
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.120	1.52	3.05	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.442	0.458	11.23	11.63	-
D1	0.300 BSC		7.62 BSC		-
D2	0.150 BSC		3.81 BSC		-
D3	-	0.458	-	11.63	2
E	0.540	0.560	13.72	14.22	-
E1	0.400 BSC		10.16 BSC		-
E2	0.200 BSC		5.08 BSC		-
E3	-	0.558	-	14.17	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.90	2.41	-
L3	0.003	0.015	0.08	0.038	-
ND	7		7		3
NE	9		9		3
N	32		32		3

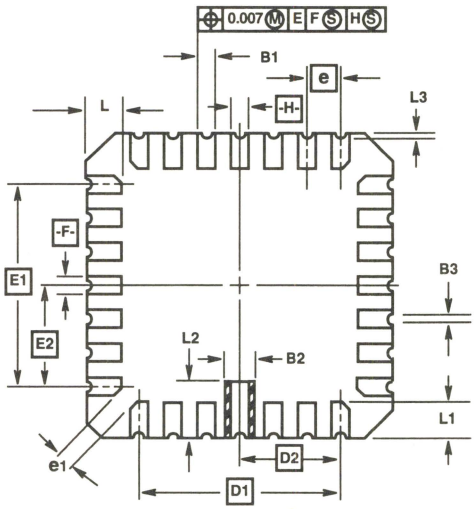
Rev. 0 6/13/95

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Ceramic Leadless Chip Carrier Packages (CLCC)





J44.A MIL-STD-1835 CQCC1-N44 (C-5)
44 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.120	1.63	3.05	6, 7
A1	0.054	0.088	1.37	2.24	-
B	0.033	0.039	0.84	0.99	4
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.640	0.662	16.26	16.81	-
D1	0.500 BSC		12.70 BSC		-
D2	0.250 BSC		6.35 BSC		-
D3	-	0.662	-	16.81	2
E	0.640	0.662	16.26	16.81	-
E1	0.500 BSC		12.70 BSC		-
E2	0.250 BSC		6.35 BSC		-
E3	-	0.662	-	16.81	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.90	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	11		11		3
NE	11		11		3
N	44		44		3

Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

MICROPROCESSOR PRODUCTS 10

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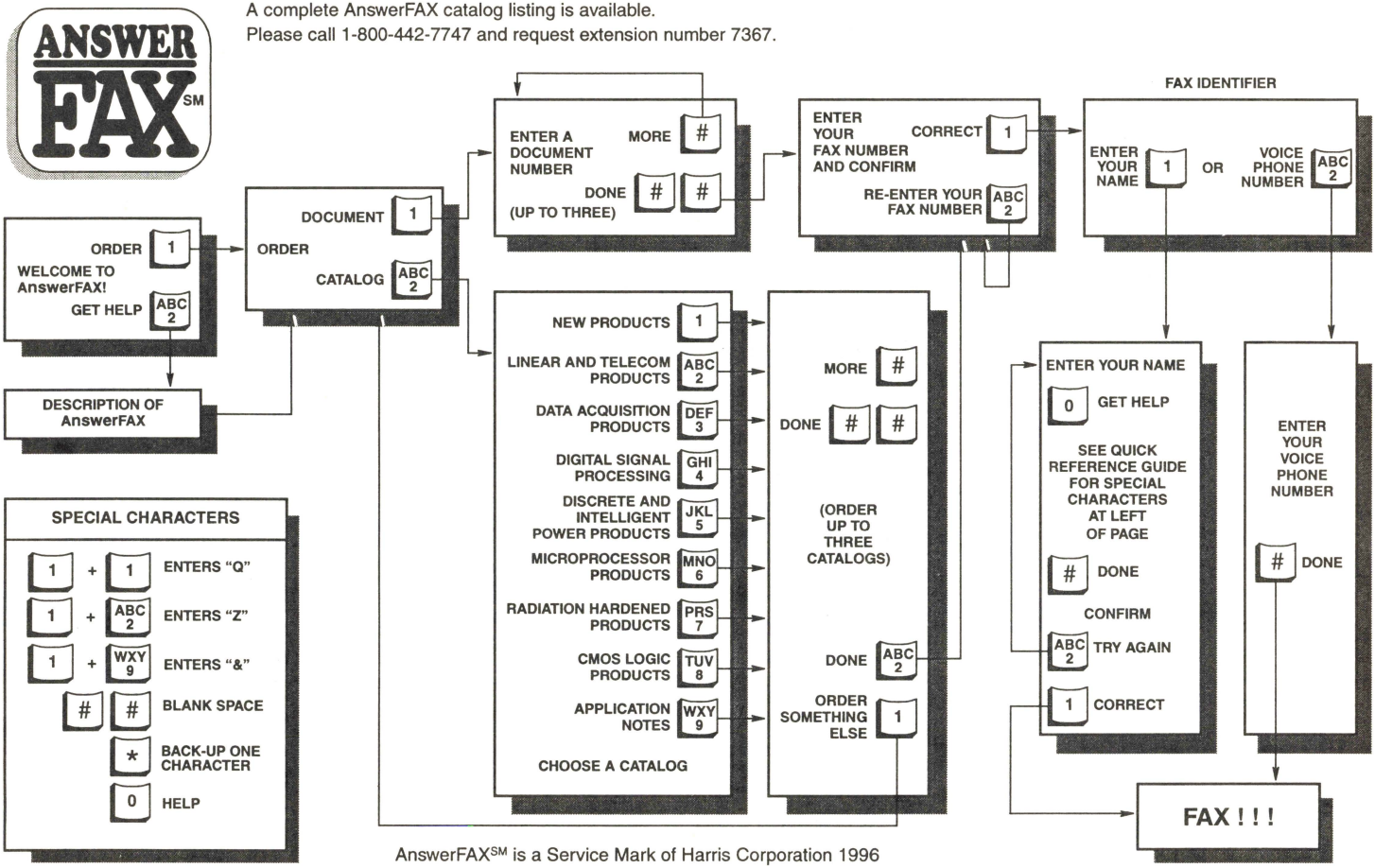
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	DB316	**POWER MOSFET DATA BOOK SUPPLEMENT** (1996: 380pp) This data book contains the data sheets of recently introduced products and also updates some of the data sheets in the Power MOSFET Data Book DB223B. These data sheets contain the detailed specification for these products.
	DB235B	**RADIATION HARDENED** (1993: 2,232pp) The Harris radiation-hardened products include the CD4000, HCS/HCTS and ACS/ACTS logic families, SRAMs, PROMs, op amps, analog multiplexers, the 80C85/80C86 microprocessor family, analog switches, gate arrays, standard cells and custom devices.
	DB260.2	**CDP6805 CMOS MICROCONTROLLERS & PERIPHERALS** (1995: 436pp) This data book represents the full line of Harris Semiconductor CDP6805 products for commercial applications and supersedes previously published CDP6805 data books under the Harris, GE, RCA or Intersil names.
	DB301B	**DATA ACQUISITION** (1994: 1,104pp) Product specifications on A/D converters (display, integrating, successive approximation, flash); D/A converters, switches, multiplexers, and other products.
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	DB303	**MICROPROCESSOR PRODUCTS** (1992: 1,156pp) For commercial and military applications. Product specifications on CMOS microprocessors, peripherals, data communications, and memory ICs.
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	Analog Military	**ANALOG MILITARY** (1989: 1,264pp) This data book describes Harris' military line of Linear, Data Acquisition, and Telecommunications circuits.
	DB312	**ANALOG MILITARY DATA BOOK SUPPLEMENT** (1994: 432pp) The 1994 Military Data Book Supplement, combined with the 1989 Analog Military Product Data Book, contain detailed technical information on the extensive line of Harris Semiconductor Linear and Data Acquisition products for Military (MIL-STD-883, DESC SMD and JAN) applications and supersedes all previously published Linear and Data Acquisition Military data books. For applications requiring Radiation Hardened products, please refer to the 1993 Harris Radiation Hardened Product Data Book (document #DB235B)
	PSG201.23	**PRODUCT SELECTION GUIDE** (1996: 834pp) Key product information on all Harris Semiconductor devices. Sectioned (Linear, Data Acquisition, Digital Signal Processing, Telecom, Intelligent Power, Discrete Power, Digital Microprocessors and Hi-Rel/Military and Rad Hard) for easy use and includes cross references and alphanumeric part number index.
	SG103	**CMOS LOGIC SELECTION GUIDE** (1994: 288pp) This product selection guide contains technical information on Harris Semiconductor High Speed 54/74 CMOS Logic Integrated Circuits for commercial, industrial and military applications. It covers Harris' High Speed CMOS Logic HC/HCT Series, AC/ACT Series, BiCMOS Interface Logic FCT Series and CMOS Logic CD4000B Series.
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March 13, 1997

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27007	BR-007	Complete Listing of Harris Sales Offices, Representatives and Authorized Distributors World Wide (10 pages)
27027	BR-027	Ordering Nomenclature Guide (20 pages) BR-027.1
MICROPROCESSOR INFORMATION		
7019	DB303, Section 9	Microprocessor Packaging Information (10 pages)
7024	DB260.2, Section 7	Operating and Handling Considerations (5 pages)
7025	DB260.2, Section 7	CDP6805 Package Selection (13 pages)
7026	DB260.2, Section 4	CDP6805/CDP68HC05 Instruction Set (10 pages)
7027	DB260.2, Section 8	Package and Ordering Information (8 pages)
MICROPROCESSOR DATA SHEETS		
2957	80C86	CMOS 16 Bit Microprocessor (32 pages)
2949	80C88	CMOS 8/16-Bit Microprocessor (32 pages) FN2949.1
2947	80C286	High Performance Microprocessor with Memory Management and Protection (60 pages) FN2947.2
2948	80C286/883	High Performance Microprocessor With Memory Management and Protection (12 pages)
2967	82C37A	CMOS High Performance Programmable DMA Controller (22 pages)
2958	82C50A	CMOS Asynchronous Communications Element (21 pages) FN2958.1
2950	82C52	CMOS Serial Controller Interface (18 pages) FN2950.1
2970	82C54	CMOS Programmable Interval Timer (17 pages) FN2970.1
2969	82C55A	CMOS Programmable Peripheral Interface (22 pages) FN2969.1
2784	82C59A	CMOS Priority Interrupt Controller (20 pages) FN2784.2
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2971	82C83H	CMOS Octal Latching Inverting Bus Driver (6 pages) FN2971.1
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2746	CDP6805E2, CDP6805E2C, CDP6805E3, CDP6805E3C	CMOS 8-Bit Microprocessor (28 pages)
1369	CDP6805F2, CDP6805F2C	CMOS High Performance Silicon Gate 8-Bit Microcontroller (16 pages)
1364	CDP6805G2, CDP6805G2C	CMOS High Performance Silicon Gate 8-Bit Microcontroller (16 pages)
4058	CDP68HC05J4	8-Bit Microcontroller Series (27 pages) FN4058

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1375	CDP6818	CMOS Real-Time Clock with RAM (19 pages)
2041	CDP6818A	CMOS Real-Time Clock with RAM (19 pages)
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2748	CDP68HC05C4, CDP68HC05C8, CDP68HCL05C4, CDP68HCL05C8, CDP68HSC05C4, CDP68HSC05C8	8-Bit Microcontroller Series (51 pages) or call Harris Semiconductor (407) 724-7237 and request by mail. FN2748.3
1557	CDP68HC05D2	8-Bit Microcontroller (40 pages)
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4248	CDP68HC05J4B, CDP68HCL05J4B, CDP68HSC05J4B	8-Bit Enhanced Microcontroller Series (39 pages) FN4248
1963	CDP68HC68A2	CMOS Serial 10-Bit A/D Converter (17 pages)
1858	CDP68HC68P1	CMOS Serial 8-Bit Input/Output Port (8 pages)
1544	CDP68HC68R1, CDP68HC68R2	CMOS 128 Word (CDP68HC68R1) and 256 Word (CDP68HC68R2) by 8-Bit Static RAMs (6 pages)
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